HMC862LP3E

v03.1210

0.1 - 15 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1, 2, 4, 8)

Typical Applications

The HMC862LP3E is ideal for:

- Satellite Communication Systems
- Point-to-Point & Point-to-Multi-Point Radios
- Military Applications
- Test Equipment

Features

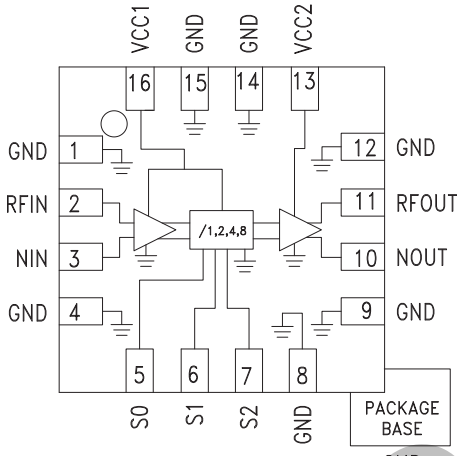
Low Noise Floor: -153 dBc/Hz at 100 kHz offset

Programmable Frequency Divider, N = 1, 2, 4, 8

Wide Bandwidth: 100 MHz to 15 GHz

16 Lead 3X3 mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC862LP3E is a low noise programmable frequency divider in a 3x3 mm leadless surface mount package. The divider can be programmed to divide from N=1, 2, 4, 8 in the 100 MHz to 15 GHz input frequency range. The low phase noise, wide frequency range and flexible division ratio make this device ideal for high performance and wide band communication systems.

Electrical Specifications, T_A = +25° C, Vcc1 = Vcc2 = +5V

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Input Characteristics					
Max RF Input Frequency	Sine Wave or Square Wave Input	15			GHz
Min RF Input Frequency	Sine Wave or Square Wave Input [1]			0.1	GHz
RF Input Power Range (N = 1)	Sine Wave or Square Wave Input [1] [2] Fin < 8 GHz	-10		10	dBm
	Sine Wave or Square Wave Input [1] [2] Fin > 8 GHz	-10		0	dBm
RF Input Power Range (N = 2, 4, 8)	Sine Wave or Square Wave Input [1]	-10		10	dBm
Divider Output Characteristics					
Output Power (N = 1)	(see the Pout plot for N = 1) [2]		-2 to +3		dBm
Output Power (N = 2, 4, 8)	(see the Pout plots for each division ratio)		2		dBm
Divider Ratio N			1, 2, 4, 8		
SSB Phase Noise @ 100 kHz Offset	Fin = 6 GHz, Pin = 0 dBm, N = 2		-153		dBc/Hz
Logic Inputs					
VIH Input High Voltage		3		5	V
VIL Input Low Voltage		0		0.4	V
Power Supplies					
Vcc	Analog Supply	4.75	5	5.25	V
Current Consumption					
Icc	N = 1, S0 = L, S1 = L, S2 = L		106		mA
	N = 2, S0 = H, S1 = L, S2 = L		143		mA
	N = 4, S0 = H, S1 = H, S2 = L		153		mA
	N = 8, S0 = H, S1 = H, S2 = H		162		mA
Control Bits			3		Bit

[1] Square wave input waveform is recommended below 400 MHz for best phase noise performance. If sine wave input waveform is used below 400 MHz, it is recommended that power input is > +5 dBm for best operation including phase noise performance.

[2] For N = 1, frequencies > 8 GHz, and input power > 0 dBm, output power will saturate and gradually drop with increasing input power, but part will continue to function.

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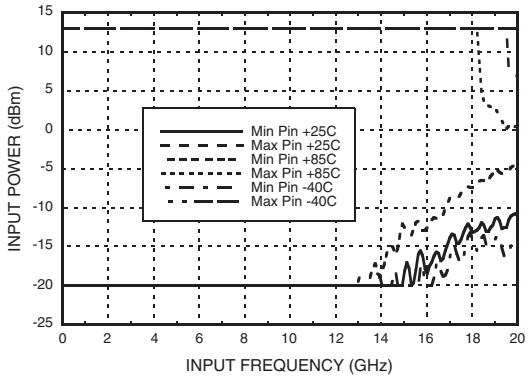
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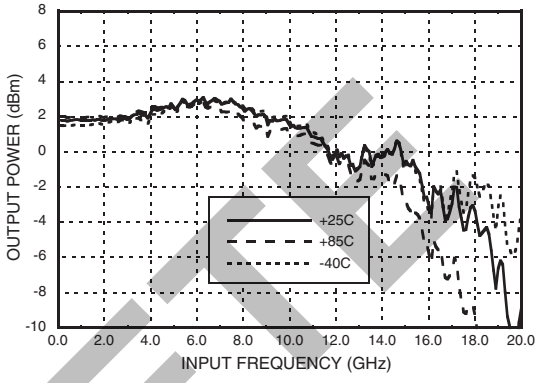
0.1 - 15 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1, 2, 4, 8)

Divide-by-1

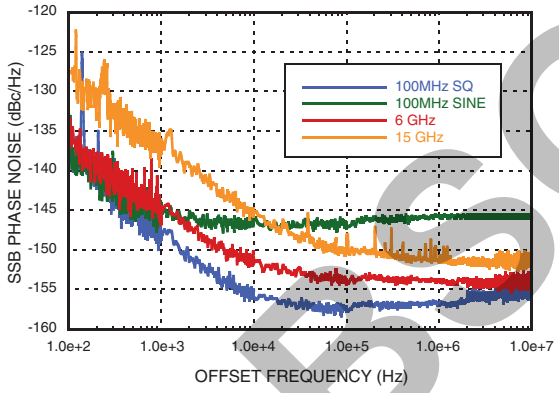
Input Sensitivity vs. Temperature



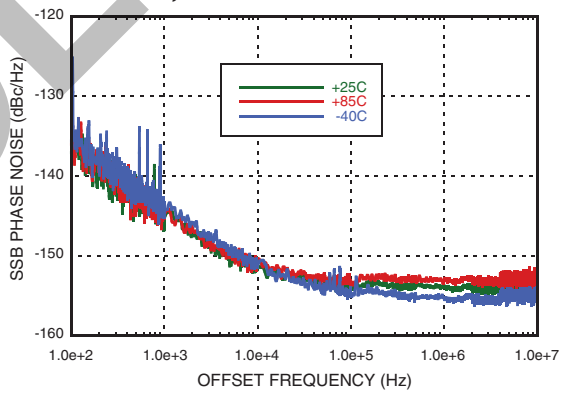
Output Power vs. Temperature, Pin = 0 dBm



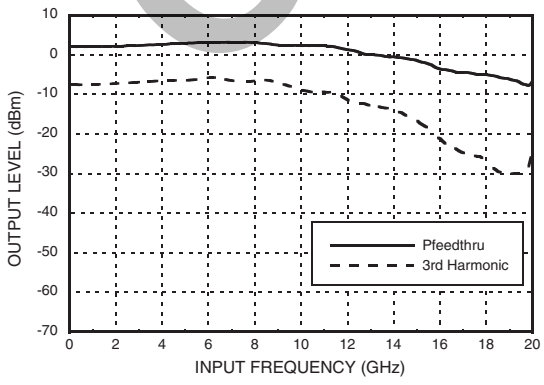
Phase Noise vs. Frequency, Pin = 0 dBm



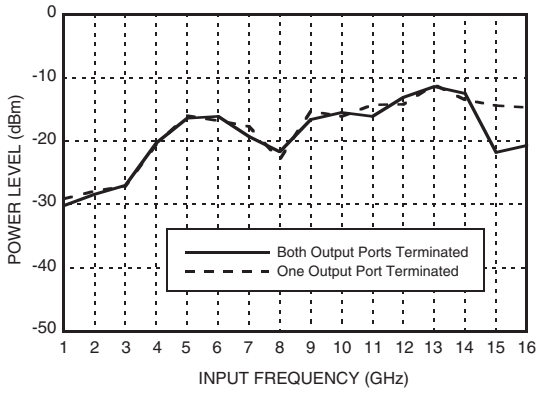
Phase Noise vs. Temperature, Pin = 0 dBm, Fin = 6 GHz



Output Harmonics, Pin = 0 dBm T = 25 °C



Reverse Leakage, Pin = 0 dBm T = 25 °C



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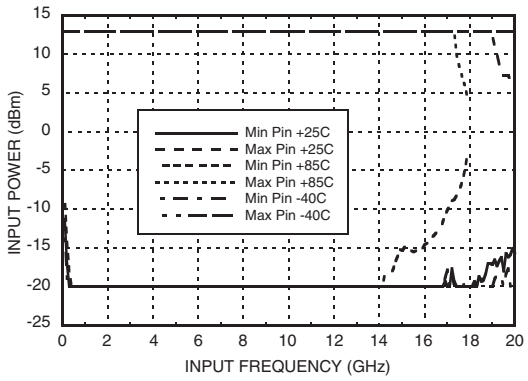
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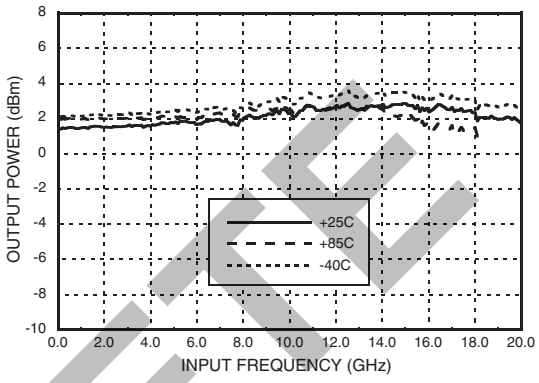
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Divide-by-2

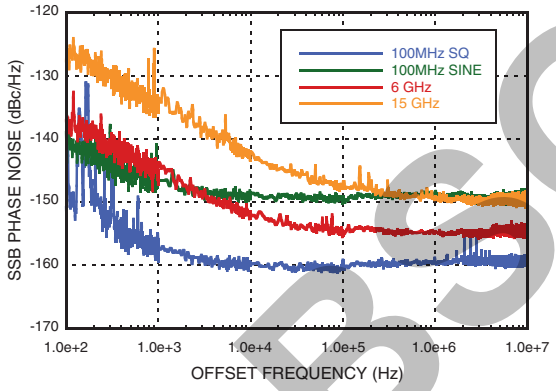
Input Sensitivity vs. Temperature



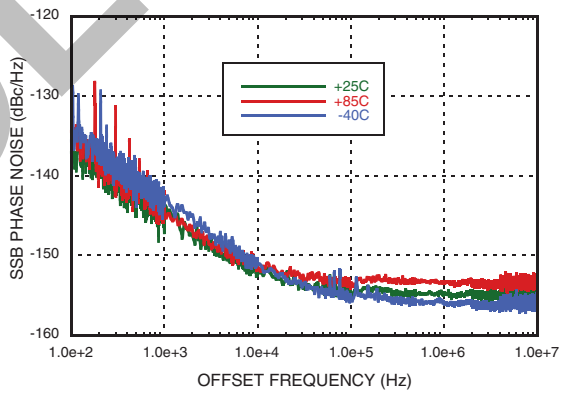
Output Power vs. Temperature, Pin = 0 dBm



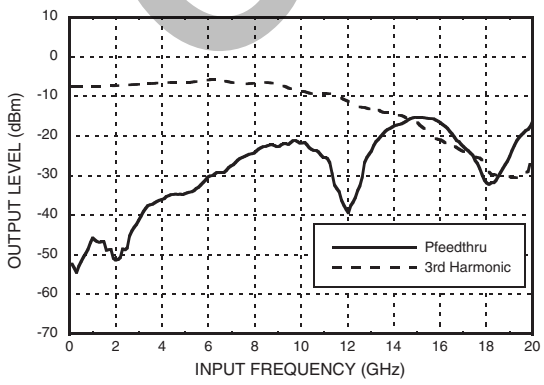
Phase Noise vs. Frequency, Pin = 0 dBm



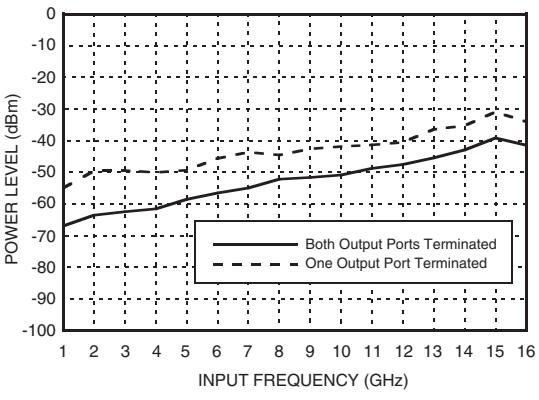
Phase Noise vs. Temperature Pin = 0 dBm, Fin = 6 GHz



Output Harmonics, Pin = 0 dBm T = 25 °C



Reverse Leakage, Pin = 0 dBm T = 25 °C



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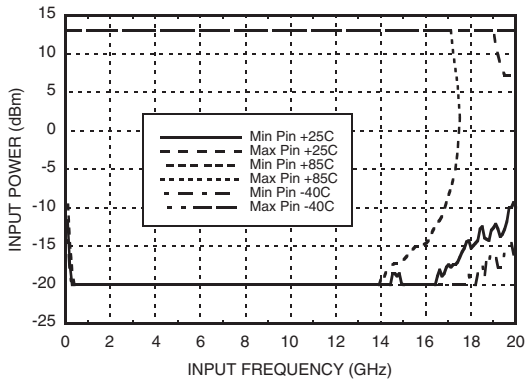
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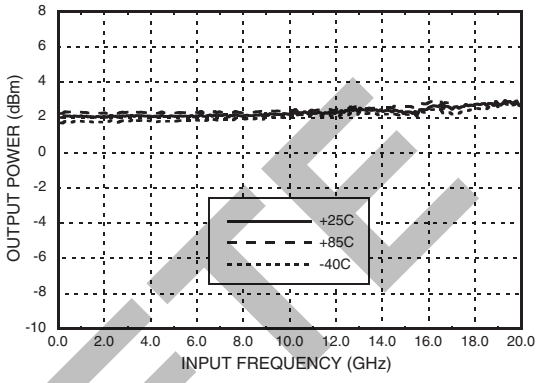
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Divide-by-4

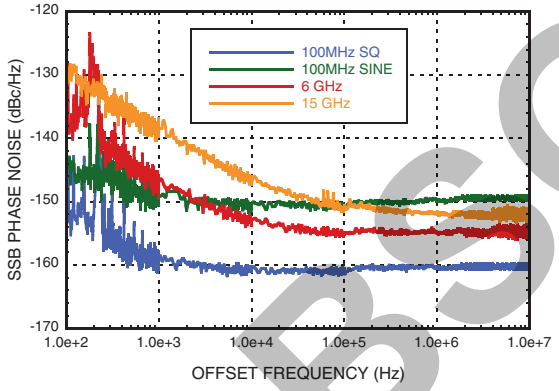
Input Sensitivity vs. Temperature



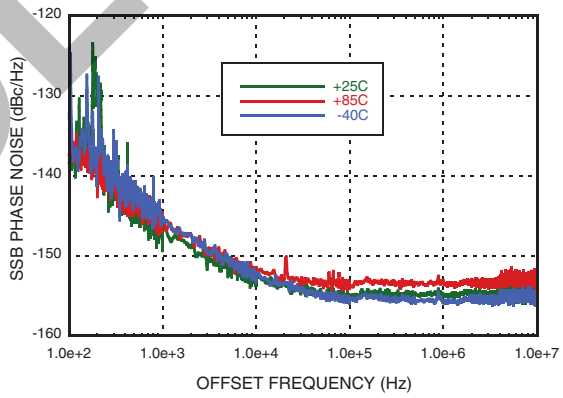
Output Power vs. Temperature, Pin = 0 dBm



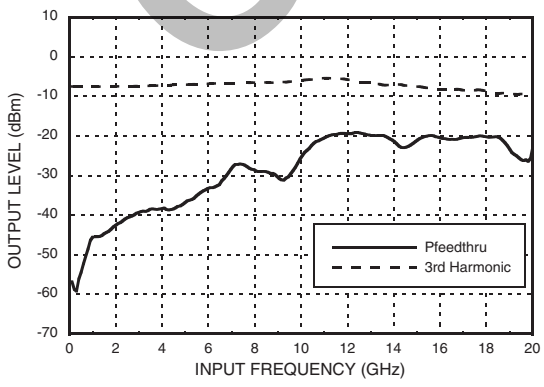
Phase Noise vs. Frequency, Pin = 0 dBm



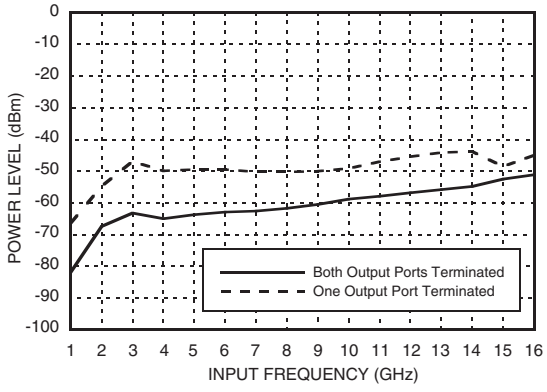
Phase Noise vs. Temperature Pin = 0 dBm, Fin = 6 GHz



Output Harmonics, Pin = 0 dBm T = 25 °C



Reverse Leakage, Pin = 0 dBm T = 25 °C



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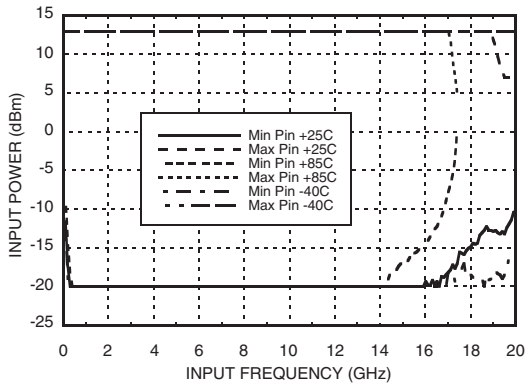
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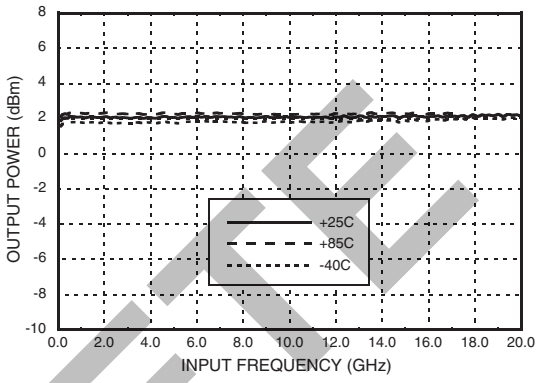
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Divide-by-8

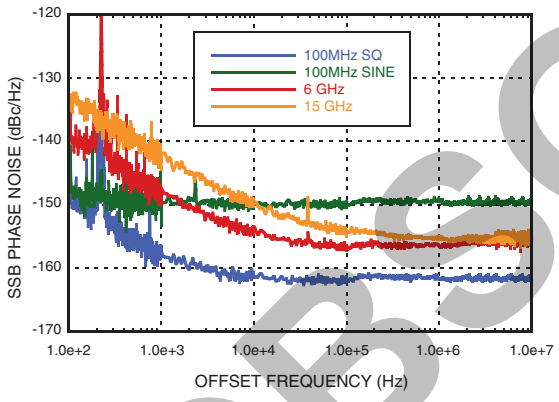
Input Sensitivity vs. Temperature



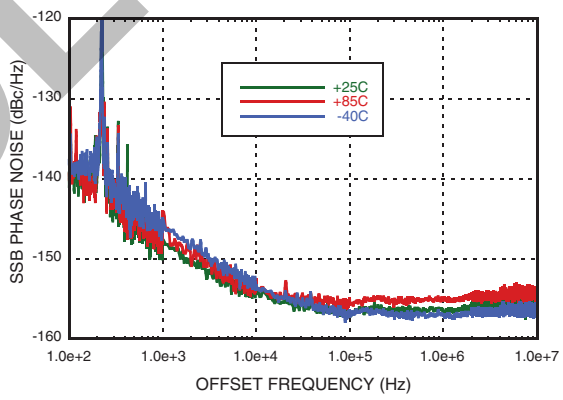
Output Power vs. Temperature, Pin = 0 dBm



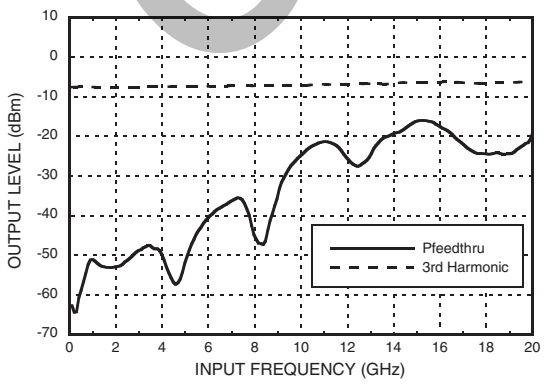
Phase Noise vs. Frequency, Pin = 0 dBm



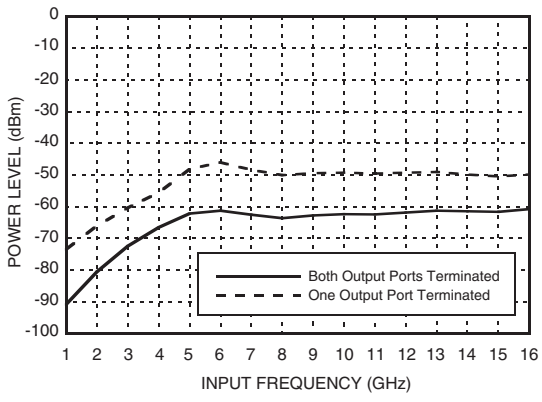
Phase Noise vs. Temperature Pin = 0 dBm, Fin = 6 GHz



Output Harmonics, Pin = 0 dBm T = 25 °C



Reverse Leakage, Pin = 0 dBm T = 25 °C



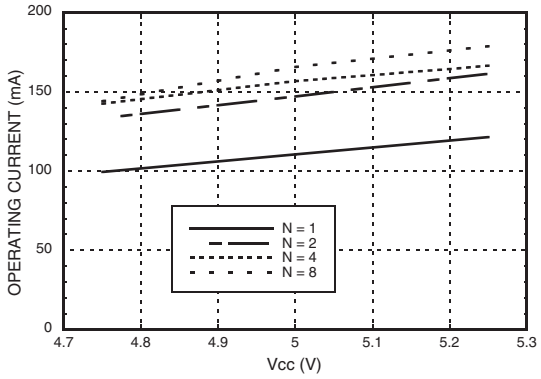
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0.1 - 15 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1, 2, 4, 8)

Icc vs. Vcc



Programming Truth Table for Frequency Division Ratios

S0	S1	S2	Divider Ratio (N)
0	0	0	1
1	0	0	2
1	1	0	4
1	1	1	8

0 = Logic Low 1 = Logic High
Note: Vcc1, Vcc2 must be applied before logic.

Digital Control Input Voltages

State	S0, S1, S2
Low	0 to 0.4V
High	3V to 5V

Absolute Maximum Ratings

RF Input Power	13 dBm
Supply Voltage (Vcc)	5.5V
Logic Inputs (S0, S1, S2)	-0.5V to (0.5V + Vcc)
Storage Temperature	-65 to +125 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Reliability Information

Junction Temperature to Maintain 1 Million Hour MTTF	150 °C
Nominal Junction Temperature (T = 85 °C)	112 °C
Thermal Resistance (Junction to GND Paddle, 5V Supply)	33 °C/W
Operating Temperature	-40 to +85 °C

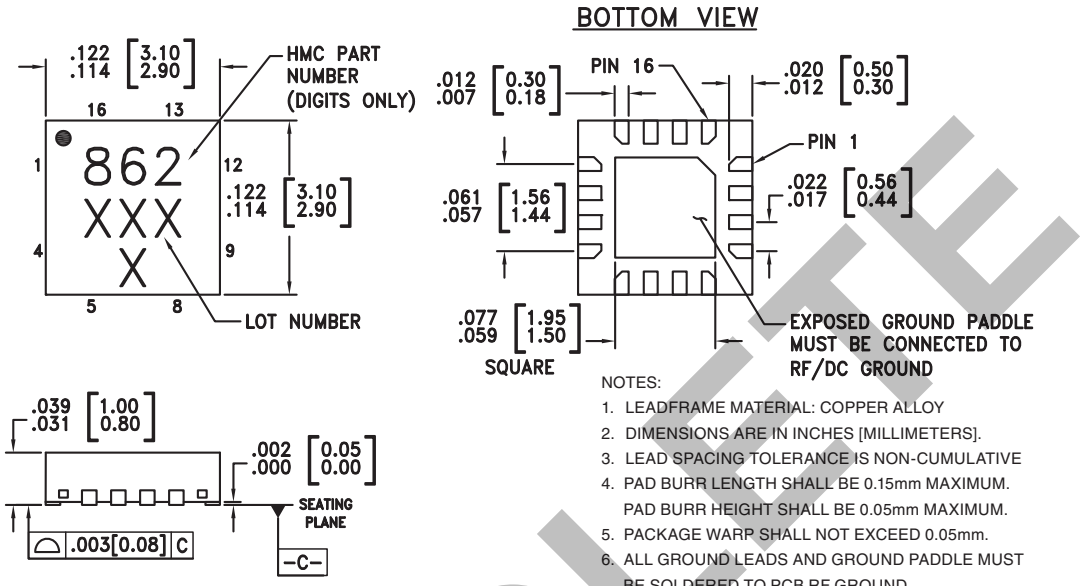
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0.1 - 15 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1, 2, 4, 8)

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC862LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	862 XXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

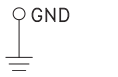
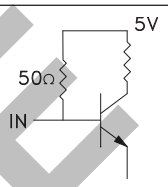
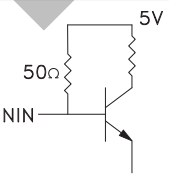
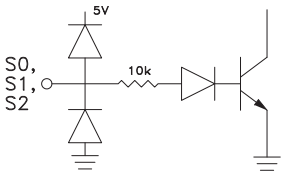
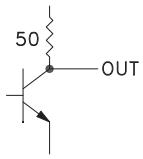
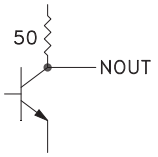
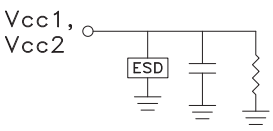
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0.1 - 15 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1, 2, 4, 8)

Pin Description

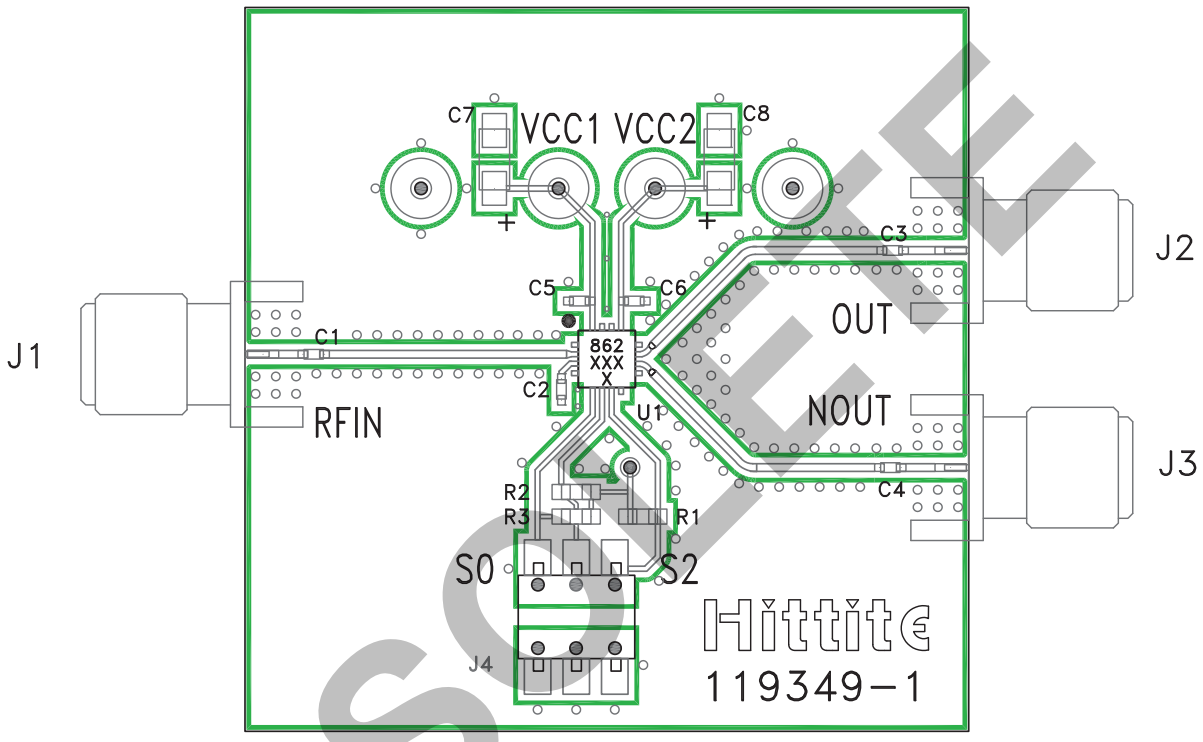
Pin Number	Function	Description	Interface Schematic
1, 4, 8, 9, 12, 14, 15	GND	Ground: Backside of package has exposed metal ground slug which must be connected to RF/DC ground.	
2	IN	RF Input must be DC blocked.	
3	$\overline{\text{NIN}}$	RF Input 180° out of phase with pin 2 for differential operation. AC ground for single ended operation. DC block for differential operation.	
5, 6, 7	S0, S1, S2	CMOS compatible division ratio control bit. See Programming Truth Table	
10	$\overline{\text{NOUT}}$	Divider output 180° out of phase with pin 11. RF output must be DC blocked.	
11	OUT	Divided Output. RF output must be DC blocked.	
13, 16	Vcc1, Vcc2	Supply voltage 5V. Connect both pins to +5V supply.	

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Evaluation PCB



OBSOLETE

List of Materials for Evaluation PCB 119351 [1]

Item	Description
J1 - J3	PCB Mount SMA-F RF Connector
J4	DC Connector Header, Molex 2mm
C1 - C4	ATC530L, 100 nF, 16V, Broadband Capacitor, 0402 Pkg.
C5, C6	1000 pF Capacitor, 0402 Pkg.
C7, C8	4.7 µF Capacitor, Tantalum, 1206 Pkg.
R1 - R3	10 kOhm Resistor, 0402 Pkg.
Vcc1, Vcc2	Mill-Max 0.040" Dia. PC Pin, 3101-2-00-21-00-00-08-0
U1	HMC862LP3E, Programmable Divider
PCB [2]	119349 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

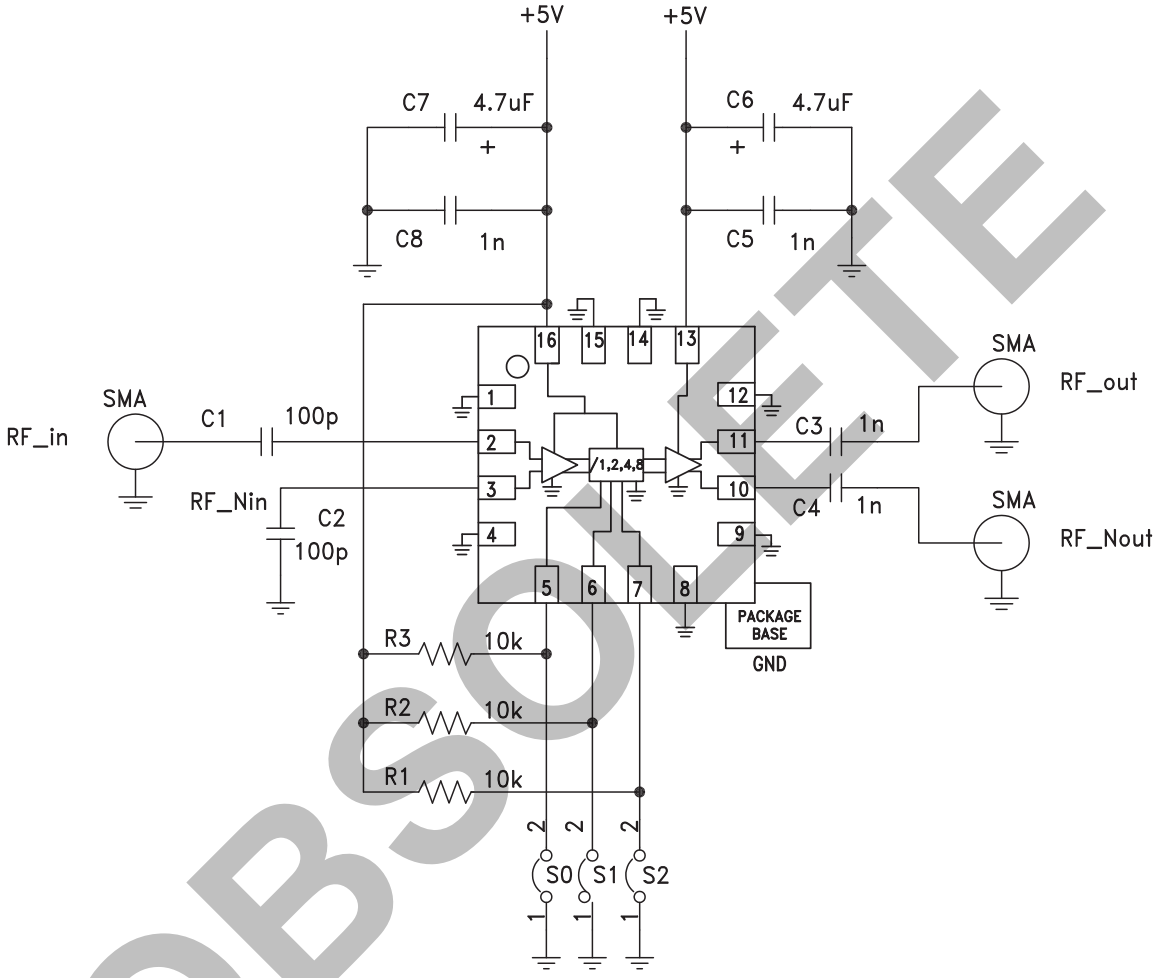
The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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0.1 - 15 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1, 2, 4, 8)

Evaluation PCB Schematic



OBSOLETE

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