DDR2 SDRAM FBDIMM

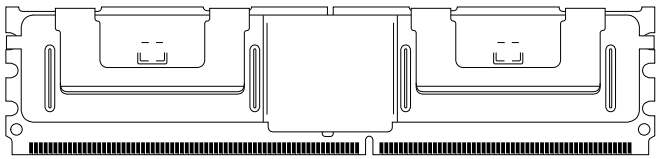
MT18HTF12872FDZ – 1GB
MT18HTF25672FDZ – 2GB

Features

- 240-pin, DDR2 fully buffered dual in-line memory module (FBDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 1GB (128 Meg x 72), 2GB (256 Meg x 72)
- 3.2 Gb/s, 4 Gb/s, or 4.8 Gb/s link transfer rates
- High-speed, 1.5V differential, point-to-point link between the host controller and advanced memory buffer (AMB)
- Fault-tolerant; can work around a bad bit lane in each direction
- High-density scaling with up to eight FBDIMM devices per channel
- SMBus interface to AMB for configuration register access
- In-band and out-of-band command access
- Deterministic protocol
  - Enables memory controller to optimize DRAM accesses for maximum performance
  - Delivers precise control and repeatable memory behavior
- Automatic DDR2 SDRAM bus and channel calibration
- Transmitter de-emphasis to reduce ISI

Figure 1: 240-Pin FBDIMM (MO-256 R/C B)

Module height: 30.35mm (1.19in)



Options	Marking
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 2.5ns @ CL = 5 (DDR2-800)	-80E
– 3.0ns @ CL = 5 (DDR2-667)	-667

Features (Continued)

- MBIST and IBIST test functions
- Transparent mode for DRAM test support
- $V_{DD} = V_{DDQ} = 1.8V$ for DRAM
- $V_{REF} = 0.9V$ SDRAM command and address termination
- $V_{CC} = 1.5V$ for AMB
- $V_{DDSPD} = 3–3.6V$ for AMB and EEPROM
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank
- Supports 95°C operation with 2X refresh

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	800	533	400	12.5	12.5	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55

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Table 2: Addressing

Parameter	1GB	2GB
Refresh count	8K	8K
Device bank address	4 BA[1:0]	8 BA[2:0]
Device page size per bank	1KB	1KB
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Row address	16K A[13:0]	16K A[13:0]
Column address	2K A[9:0]	2K A[9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 1GB

Base device: MT47H64M8,[1] 512Mb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)	Link Transfer Rate
MT18HTF12872FDZ-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5	4.8 GT/s
MT18HTF12872FDZ-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5	4.0 GT/s

Table 4: Part Numbers and Timing Parameters – 2GB

Base device: MT47H128M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)	Link Transfer Rate
MT18HTF25672FDZ-80E__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5	4.8 GT/s
MT18HTF25672FDZ-667__	2GB	256 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5	4.0 GT/s

Notes:
1. Data sheets for the base devices can be found on Micron's Web page.
2. All part numbers end with a four-place code (not shown) that designates component, PCB, and AMB revisions. Consult factory for current revision codes. Example: MT18HTF25672FDZ-667M1D4.

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Pin Assignments and Descriptions

Table 5: Pin Assignments

240-Pin FBDIMM Front								240-Pin FBDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{DD}	31	PN3	61	PN9#	91	PS9#[1]	121	V_{DD}	151	SN3	181	SN9#	211	SS9#[1]
2	V_{DD}	32	PN3#	62	V_{SS}	92	V_{SS}	122	V_{DD}	152	SN3#	182	V_{SS}	212	V_{SS}
3	V_{DD}	33	V_{SS}	63	PN10	93	PS5	123	V_{DD}	153	V_{SS}	183	SN10	213	SS5
4	V_{SS}	34	PN4	64	PN10#	94	PS5#	124	V_{SS}	154	SN4	184	SN10#	214	SS5#
5	V_{DD}	35	PN4#	65	V_{SS}	95	V_{SS}	125	V_{DD}	155	SN4#	185	V_{SS}	215	V_{SS}
6	V_{DD}	36	V_{SS}	66	PN11	96	PS6	126	V_{DD}	156	V_{SS}	186	SN11	216	SS6
7	V_{DD}	37	PN5	67	PN11#	97	PS6#	127	V_{DD}	157	SN5	187	SN11#	217	SS6#
8	V_{SS}	38	PN5#	68	V_{SS}	98	V_{SS}	128	V_{SS}	158	SN5#	188	V_{SS}	218	V_{SS}
9	V_{CC}	39	V_{SS}	69	V_{SS}	99	PS7	129	V_{CC}	159	V_{SS}	189	V_{SS}	219	SS7
10	V_{CC}	40	PN13[1]	70	PS0	100	PS7#	130	V_{CC}	160	SN13[1]	190	SS0	220	SS7#
11	V_{SS}	41	PN13#[1]	71	PS0#	101	V_{SS}	131	V_{SS}	161	SN13#[1]	191	SS0#	221	V_{SS}
12	V_{CC}	42	V_{SS}	72	V_{SS}	102	PS8	132	V_{CC}	162	V_{SS}	192	V_{SS}	222	SS8
13	V_{CC}	43	V_{SS}	73	PS1	103	PS8#	133	V_{CC}	163	V_{SS}	193	SS1	223	SS8#
14	V_{SS}	44	DNU	74	PS1#	104	V_{SS}	134	V_{SS}	164	DNU	194	SS1#	224	V_{SS}
15	V_{TT}	45	DNU	75	V_{SS}	105	DNU	135	V_{TT}	165	DNU	195	V_{SS}	225	DNU
16	DNU	46	V_{SS}	76	PS2	106	DNU	136	DNU	166	V_{SS}	196	SS2	226	DNU
17	RESET#	47	V_{SS}	77	PS2#	107	V_{SS}	137	M_Test (DNU)	167	V_{SS}	197	SS2#	227	V_{SS}
18	V_{SS}	48	PN12[1]	78	V_{SS}	108	V_{DD}	138	V_{SS}	168	SN12[1]	198	V_{SS}	228	SCK
19	DNU	49	PN12#[1]	79	PS3	109	V_{DD}	139	DNU	169	SN12#[1]	199	SS3	229	SCK#
20	DNU	50	V_{SS}	80	PS3#	110	V_{SS}	140	DNU	170	V_{SS}	200	SS3#	230	V_{SS}
21	V_{SS}	51	PN6	81	V_{SS}	111	V_{DD}	141	V_{SS}	171	SN6	201	V_{SS}	231	V_{DD}
22	PN0	52	PN6#	82	PS4	112	V_{DD}	142	SN0	172	SN6#	202	SS4	232	V_{DD}
23	PN0#	53	V_{SS}	83	PS4#	113	V_{DD}	143	SN0#	173	V_{SS}	203	SS4#	233	V_{DD}
24	V_{SS}	54	PN7	84	V_{SS}	114	V_{SS}	144	V_{SS}	174	SN7	204	V_{SS}	234	V_{SS}
25	PN1	55	PN7#	85	V_{SS}	115	V_{DD}	145	SN1	175	SN7#	205	V_{SS}	235	V_{DD}
26	PN1#	56	V_{SS}	86	DNU	116	V_{DD}	146	SN1#	176	V_{SS}	206	DNU	236	V_{DD}
27	V_{SS}	57	PN8	87	DNU	117	V_{TT}	147	V_{SS}	177	SN8	207	DNU	237	V_{TT}
28	PN2	58	PN8#	88	V_{SS}	118	SA2	148	SN2	178	SN8#	208	V_{SS}	238	V_{DDSPD}
29	PN2#	59	V_{SS}	89	V_{SS}	119	SDA	149	SN2#	179	V_{SS}	209	V_{SS}	239	SA0
30	V_{SS}	60	PN9	90	PS9[1]	120	SCL	150	V_{SS}	180	SN9	210	SS9[1]	240	SA1

Note: 1. The following signals are cyclical redundancy code (CRC) bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, SS9/SS9#.

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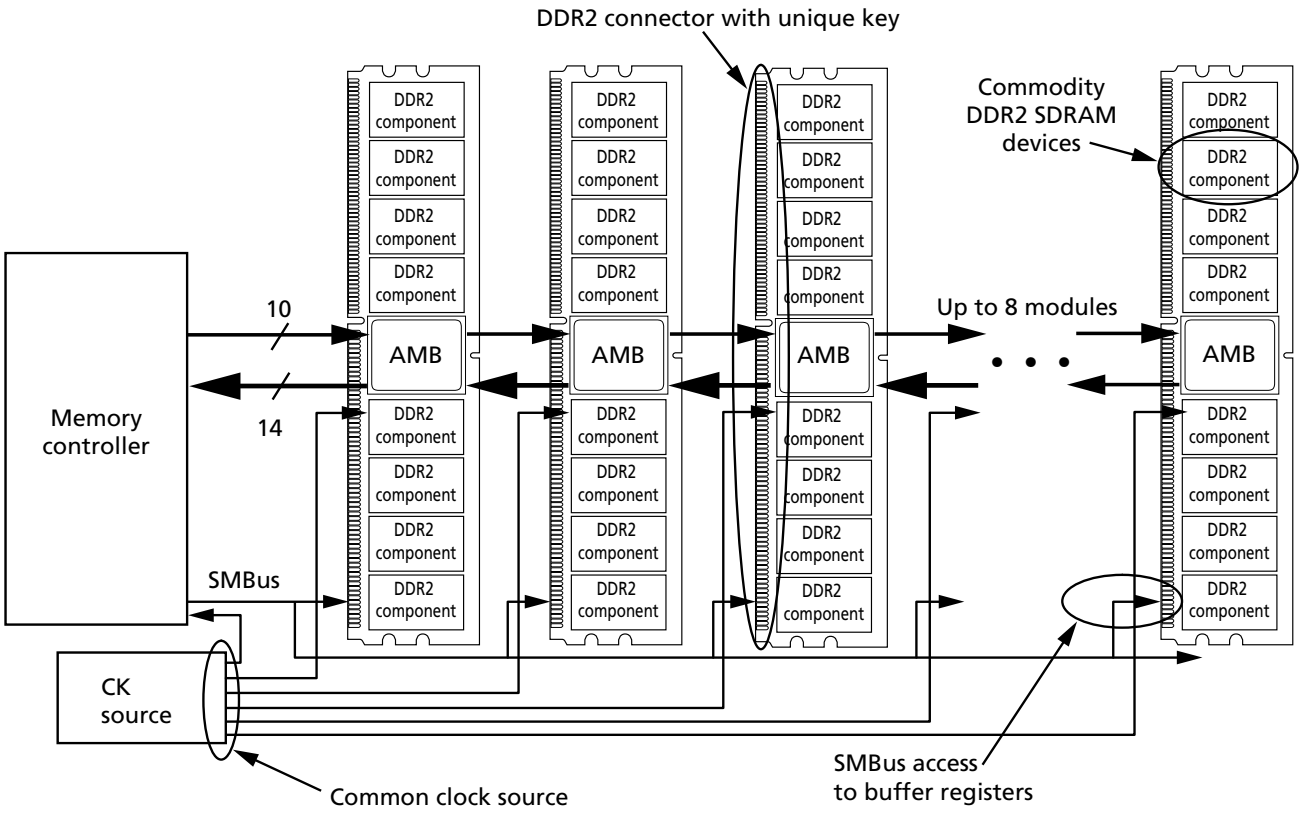
Table 6: Pin Descriptions

Symbol	Type	Description
PS[9:0]	Input	Primary southbound data, positive lines.
PS#[9:0]	Input	Primary southbound data, negative lines.
SCK	Input	System clock input, positive line.
SCK#	Input	System clock Input, negative line.
SCL	Input	Serial presence-detect (SPD) clock input.
SS[9:0]	Input	Secondary southbound data, positive lines.
SS#[9:0]	Input	Secondary southbound data, negative lines.
PN[13:0]	Output	Primary northbound data, positive lines.
PN#[13:0]	Output	Primary northbound data, negative lines.
SN[13:0]	Output	Secondary northbound data, positive lines.
SN#[13:0]	Output	Secondary northbound data, negative lines.
SA[2:0]	I/O	SPD address inputs, also used to select the FBDIMM number in the AMB.
SDA	I/O	SPD data input/output.
RESET#	Supply	AMB reset signal.
V_{CC}	Supply	AMB core power and AMB channel interface power (1.5V).
V_{DD}	Supply	DRAM power and AMB DRAM I/O power (1.8V).
V_{DDSPD}	Supply	SPD/AMB SMBUS power (3.3V).
V_{SS}	Supply	Ground.
V_{TT}	Supply	DRAM address/command/clock termination power (V_{DD}/2).
M_Test	–	The M_Test pin provides an external connection for testing the margin of V_{REF}, which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.
DNU	–	Do not use.

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System Block Diagram

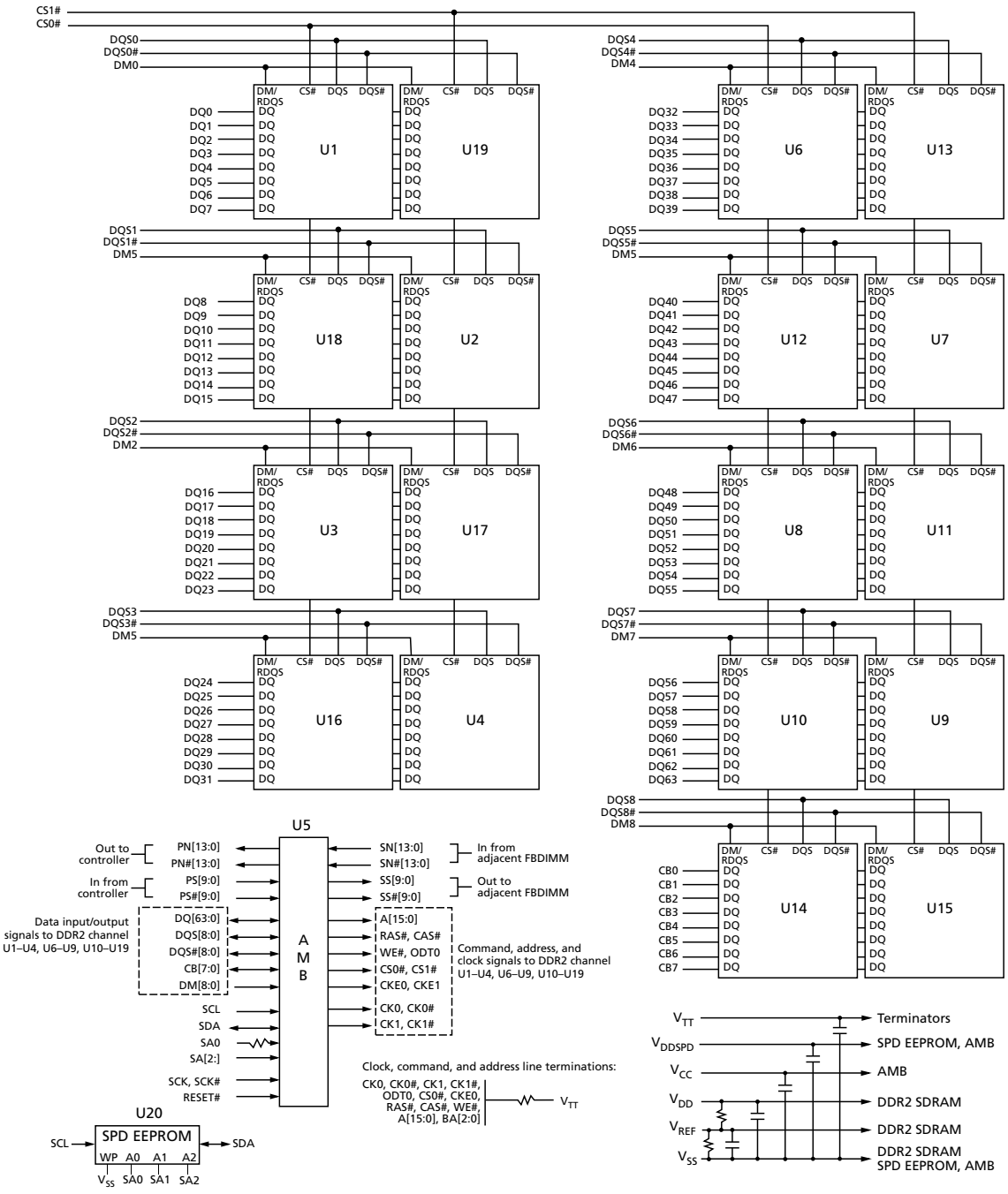
Figure 2: System Block Diagram



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Functional Block Diagram

Figure 3: Functional Block Diagram



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General Description

Micron's FBDIMM devices adhere to the currently proposed industry specifications for FBDIMMs. The following specifications contain detailed information on FBDIMM design, interfaces, and theory of operation and are listed here for the system designers' convenience. Refer to the JEDEC Web site for available specifications.

- FBDIMM Design Specification – pending JEDEC approval
- FBDIMM: Architecture and Protocol – JESD206
- FBDIMM: Advanced Memory Buffer (AMB) – JESD82-20
- Design for Test, Design for Validation (DF*x*) Specification
- Serial Presence-Detect (SPD) for Fully Buffered DIMM – JEDEC Standard No. 21-C, page 4.1.2.7-1

This DDR2 SDRAM module is a high-bandwidth, large-capacity channel solution that has a narrow host interface. FBDIMM devices use DDR2 SDRAM devices isolated from the channel behind an AMB on the FBDIMM. Memory device capacity remains high, and total memory capacity scales with DDR2 SDRAM bit density.

As shown in the System Block Diagram, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel enhances the communication path and significantly increases the reliability and availability of the memory subsystem.

Advanced Memory Buffer

The AMB isolates the DDR2 SDRAM devices from the channel. This single-chip AMB component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged between the host controller and DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential, 1.5V, point-to-point interface. The AMB also enables buffering of memory traffic to support large memory capacities. Refer to the JEDEC JESD82-20 specification for further information.

IDD Conditions and Specifications

Table 7: I_{DD} Conditions

Symbol	Condition
$I_{DD_IDLE_0}$	**Idle current, single, or last DIMM:** L0 state; Idle (0% bandwidth); Primary channel enabled; Secondary channel disabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
$I_{DD_IDLE_1}$	**Idle current, first DIMM:** L0 state; Idle (0% bandwidth); Primary and secondary channels enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
$I_{DD_ACTIVE_1}$	**Active power:** L0 state; 50% DRAM bandwidth; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH
$I_{DD_ACTIVE_2}$	**Active power, data pass through:** L0 state; 50% DRAM bandwidth to downstream DIMM; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH; Command and address lines stable

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Table 7: I_{DD} Conditions (Continued)

Symbol	Condition
$I_{DD_TRAINING}$	**Training:** Primary and secondary channels enabled; 100% toggle on all channel lanes; DRAMs idle; 0% bandwidth; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I_{DD_IBIST}	**IBIST over all IBIST modes:** DRAM idle (0% bandwidth); Primary channel enabled; Secondary channel enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I_{DD_EI}	**Electrical idle:** DRAM idle (0% bandwidth); Primary channel disabled; Secondary channel disabled; CKE LOW; Command and address lines floated; DDR2 SDRAM clock active; ODT and CKE driven LOW

Note: 1. Actual test conditions may vary from published JEDEC test conditions.

Table 8: I_{DD} Specifications – 1GB DDR2-667

Symbol	$I_{DD_IDLE_0}$	$I_{DD_IDLE_1}$	$I_{DD_ACTIVE_1}$	$I_{DD_ACTIVE_2}$	$I_{DD_TRAINING}$	I_{DD_IBIST}	I_{DD_EI}	Units
I_{CC}	2600	3400	3900	3700	4000	4500	2500	A
I_{DD}	1510	1510	2777	1510	1510	1510	326	A
Total power	7.0	8.2	11.4	8.7	9.2	10.0	4.5	W

Table 9: I_{DD} Specifications – 1GB DDR2-800

Symbol	$I_{DD_IDLE_0}$	$I_{DD_IDLE_1}$	$I_{DD_ACTIVE_1}$	$I_{DD_ACTIVE_2}$	$I_{DD_TRAINING}$	I_{DD_IBIST}	I_{DD_EI}	Units
I_{CC}	TBD	TBD	TBD	TBD	TBD	TBD	TBD	A
I_{DD}	TBD	TBD	TBD	TBD	TBD	TBD	TBD	A
Total power	TBD	TBD	TBD	TBD	TBD	TBD	TBD	W

Table 10: I_{DD} Specifications – 2GB DDR2-667 (Die rev H)

Symbol	$I_{DD_IDLE_0}$	$I_{DD_IDLE_1}$	$I_{DD_ACTIVE_1}$	$I_{DD_ACTIVE_2}$	$I_{DD_TRAINING}$	I_{DD_IBIST}	I_{DD_EI}	Units
I_{CC}	2600	3400	3900	3700	4000	4500	2500	A
I_{DD}	1132	1132	2161	1122	1132	1132	326	A
Total power	6.2	7.5	10.2	7.9	8.4	9.2	4.5	W

Table 11: I_{DD} Specifications – 2GB DDR2-667 (Die rev M)

Symbol	$I_{DD_IDLE_0}$	$I_{DD_IDLE_1}$	$I_{DD_ACTIVE_1}$	$I_{DD_ACTIVE_2}$	$I_{DD_TRAINING}$	I_{DD_IBIST}	I_{DD_EI}	Units
I_{CC}	2600	3400	3900	3700	4000	4500	2500	A
I_{DD}	1132	1132	2161	1332	1332	1332	380	A
Total power	6.2	7.5	10.2	7.9	8.4	7.2	4.6	W

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Table 12: I_{DD} Specifications – 2GB DDR2-800 (All Die Revisions)

Symbol	$I_{DD_IDLE_0}$	$I_{DD_IDLE_1}$	$I_{DD_ACTIVE_1}$	$I_{DD_ACTIVE_2}$	$I_{DD_TRAINING}$	I_{DD_IBIST}	I_{DD_EI}	Units
I_{CC}	TBD	TBD	TBD	TBD	TBD	TBD	TBD	A
I_{DD}	TBD	TBD	TBD	TBD	TBD	TBD	TBD	A
Total power	TBD	TBD	TBD	TBD	TBD	TBD	TBD	W

Note: 1. Total power is based on maximum voltage levels, I_{CC} at 1.575V and I_{DD} at 1.9V.

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
EEPROM and AMB supply voltage	V_{DDSPD}	3	3.6	V
Input high voltage: Logic 1; all inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; all inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CCR}	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CCW}	2	3	mA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA and SCL fall time	^{t}F	–	300	ns	2
Data-in hold time	^{t}HD:DAT	0	–	µs	
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Clock HIGH period	^{t}HIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SDA and SCL rise time	^{t}R	–	0.3	µs	2
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	^{t}SU:DAT	100	–	ns	
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Stop condition setup time	^{t}SU:STO	0.6	–	µs	

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Table 14: Serial Presence-Detect EEPROM AC Operating Conditions (Continued)

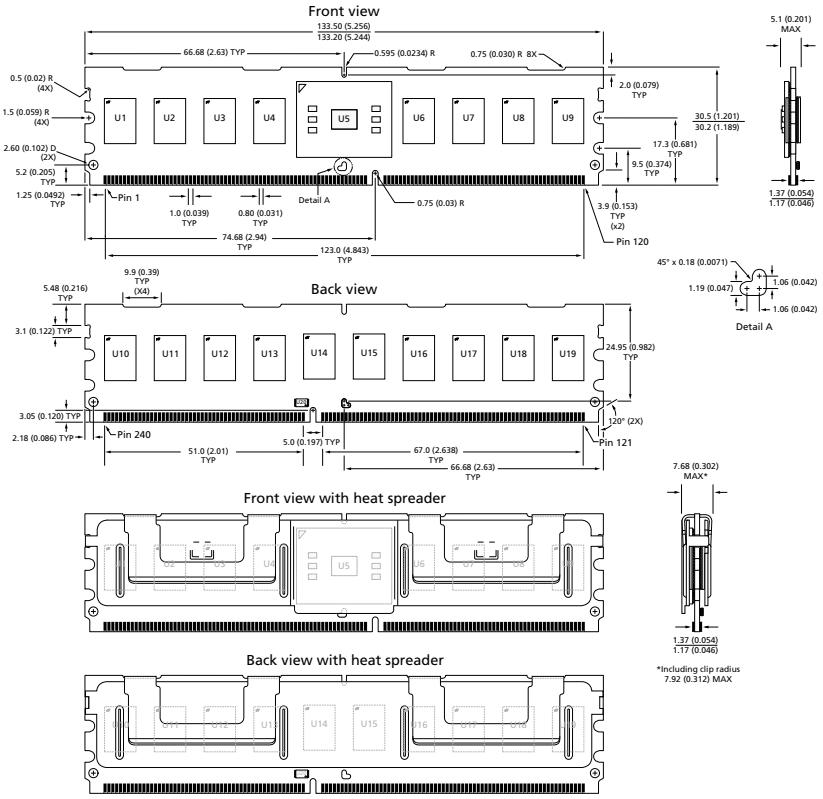
Parameter/Condition	Symbol	Min	Max	Units	Notes
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

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Module Dimensions

Figure 4: 240-Pin DDR2 FBDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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