iW-RainboW-G28M
Zynq-7000 SoC SODIMM SOM
Hardware User Guide



iWave
Embedding Intelligence

Document Revision History

Document Number		iW-PRFOZ-UM-01-R2.0-REL1.3-Hardware
Revision	**Date**	**Description**
1.0	03rd Oct 2018	• Initial Release Version
1.1	24th July 2020	• CPU pin number corrected for SODIMM PIN 39 • SODIMM Pin 148 & 149 signals name is defined
1.2	03rd Sep 2020	• SODIMM Pin 107, 108, 109, 111, 112 & 114 signals name is defined
1.3	23rd Jun 2021	• Updated Block Diagram • Updated PL Block information in SODIMM PCB Edge Interface section • Added Stability information in Table 3: Zynq-7000 SoC SOM Reference Clock • Corrected 2.8.7 FPGA IOs – PL BANK35 section • Corrected L9P signal pad name from K19 to L19 in section 2.7 Wi-Fi & Bluetooth and 2.8.7 FPHA IOs-PL BANK35 "Note" • Added Power input requirement " Important Note"

PROPRIETARY NOTICE: This document contains proprietary material for the sole use of the intended recipient(s). Do not read this document if you are not the intended recipient. Any review, use, distribution or disclosure by others is strictly prohibited. If you are not the intended recipient (or authorized to receive for the recipient), you are hereby notified that any disclosure, copying distribution or use of any of the information contained within this document is STRICTLY PROHIBITED. Thank you. "iWave Systems Tech. Pvt. Ltd."

Disclaimer

iWave Systems reserves the right to change details in this publication including but not limited to any Product specification without notice.

No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by iWave Systems, its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.

CPU and other major components used in this product may have several silicon errata associated with it. Under no circumstances, iWave Systems shall be liable for the silicon errata and associated issues.

Trademarks

All registered trademarks, product names mentioned in this publication are the property of their respective owners and used for identification purposes only.

Certification

iWave Systems Technologies Pvt. Ltd. is an ISO 9001:2015 Certified Company.

Warranty & RMA

Warranty support for Hardware: 1 Year from iWave or iWave's EMS partner.
For warranty terms, go through the below web link,
http://www.iwavesystems.com/support/warranty.html

For Return Merchandise Authorization (RMA), go through the below web link,
http://www.iwavesystems.com/support/rma.html

Technical Support

iWave Systems technical support team is committed to provide the best possible support for our customers so that our Hardware and Software can be easily migrated and used.
For assistance, contact our Technical Support team at,

Email : support.ip@iwavesystems.com
Website : www.iwavesystems.com
Address : iWave Systems Technologies Pvt. Ltd.
7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore, Karnataka,
India – 560076

Table of Contents

1. INTRODUCTION 7

1.1 Purpose 7
1.2 SODIMM SOM Overview 7
1.3 List of Acronyms 7
1.4 Terminlogy Description 9
1.5 References 9

2. ARCHITECTURE AND DESIGN 10

2.1 Zynq-7000 SoC SODIMM SOM Block Diagram 10
2.2 Zynq-7000 SoC SODIMMSOM Features 11
2.3 Zynq-7000 SoC 13
2.4 Zynq-7000 SoC Reference Clock 15
2.5 PMIC 15
2.6 Memory 16
2.6.1 DDR3L SDRAM 16
2.6.2 QSPI Flash 16
2.6.3 eMMC Flash 16
2.6.4 Micro SD Slot (Optional) 17
2.6.5 NAND Flash (Optional) 17
2.7 Wi-Fi & Bluetooth 18
2.8 SODIMM PCB Edge Connector 19
2.8.1 Gigabit Ethernet Interface 23
2.8.2 USB 2.0 OTG Interface 24
2.8.3 Debug UART Interface 24
2.8.4 I2C Interface 25
2.8.5 SD/SDIO interface (Optional) 25
2.8.6 FPGA IOs – PL BANK34 26
2.8.7 FPGA IOs – PL BANK35 32
2.8.8 FPGA IOs – PL BANK13 37
2.8.9 JTAG Interface 40
2.8.10 Power Input 40
2.8.11 Reset Signal 40
2.9 Zynq-7000 SoC PS Pin Multiplexing on SODIMM 41

3. TECHNICAL SPECIFICATION 43

3.1 Electrical Characteristics 43
3.1.1 Power Input Requirement 43
3.1.2 Power Consumption 44
3.2 Environmental Characteristics 45
3.2.1 Environmental Specification 45
3.2.2 Heat Sink 45
3.2.3 RoHS Compliance 46
3.2.4 Electrostatic Discharge 46

3.3 MechanicalCharacteristics 47
3.3.1 SODIMM SOM Mechanical Dimensions 47
3.3.2 Guidelines to insert the SODIMM SOM into Carrier board 48
3.3.1 SODIMM SOM removing procedure from Carrier board 48
4. ORDERING INFORMATION 49
5. APPENDIX 51
5.1 Zynq-7000 SoC SODIMM SOM Development Platform 51

List of Figures

Figure 1:Zynq-7000 SoC SODIMM SOM Block Diagram 10
Figure 2: Zynq-7000 CPU Simplified Block Diagram 13
Figure 3: Zynq-7000 SoC Devices Comparison 14
Figure 4: Zynq-7000 SoC IOs 14
Figure 5: SODIMM PCB Edge Connector 19
Figure 6: Zynq-7000 SoC SODIMM SOM Heat Sink 46
Figure 7: Mechanical dimension of Zynq-7000 SoC SODIMM SOM - Top View 47
Figure 8: Mechanical dimension of Zynq-7000 SoC SODIMM SOM- Side View 47
Figure 9: SODIMM SOM Insertion procedure 48
Figure 10: SODIMM SOM Removing Procedure 48
Figure 11: Zynq-7000 SoC SODIMM SOM Development Platform 51

List of Tables

Table 1: Acronyms & Abbreviations 7
Table 2: Terminology 9
Table 3: Zynq-7000 SoC SOM Reference Clock 15
Table 4: SODIMM PCB Edge Connector Pinout Map 20
Table 5: PS IOMUX on Zynq-7000 SoC SODIMM SOM 41
Table 6: Power Input Requirement 43
Table 7: Power Consumption[1] 44
Table 8: Environmental Specification 45
Table 9: Orderable Product Part Numbers 49

1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Zynq-7000 SODIMM System on Module based on the Xilinx's Zynq-7000 SoC. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Zynq-7000 SODIMM System on Module from a Hardware Systems perspective.

1.2 SODIMM SOM Overview

The Zynq-7000 SODIMM SOM is an extension of Zynq 7000 SoC. Also with the SOM approach one can reduce the cost and time required for the development of customised solution on Zynq-7000 SoC. The Zynq-7000 SODIMM module has a form factor of 67.6mm x 37mm and provides the functional requirements for an embedded application. A single ruggedized SODIMM connector provides the carrier board interface to carry all the I/O signals to and from the SODIMM module.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BSP	Board Support Package
DDR3	Double Data Rate 3
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LCD	Liquid Crystal Display
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PTH	Plated Through hole
PL	Programmable Logic

Acronyms	Abbreviations
PS	Processing System
QSPI	Quad Serial Peripheral Interface
RTC	Real Time Clock
SD	Secure Digital
SoC	System On Chip
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Zynq-7000 SoC Datasheet & Technical Reference Manual
- 200 Pin DDR S.O.DIMM physical Specification

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq-7000 SoC SODIMM SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about SODIMM edge connector pin assignment and usage.

2.1 Zynq-7000 SoC SODIMM SOM Block Diagram

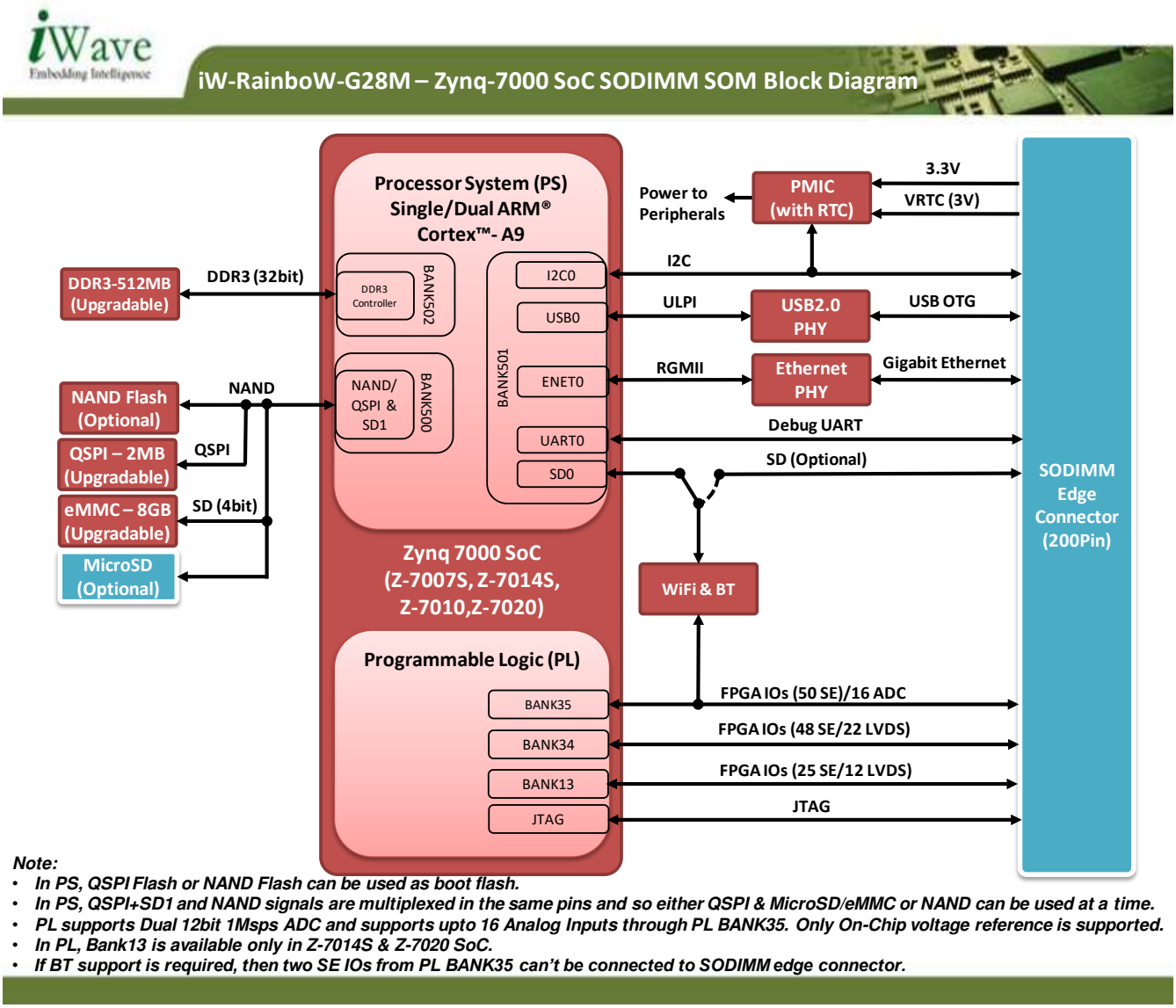


Figure 1:Zynq-7000 SoC SODIMM SOM Block Diagram

2.2 Zynq-7000 SoC SODIMMSOM Features

The Zynq-7000 SoC SODIMM SOM supports the following features.

SoC

- Xilinx Zynq-7000 SoC
  - Compatible Zynq-7000 SoC Family – Z-7007S, Z-7014S, Z-7010, Z-7020

    Integrates a feature-rich dual/single core ARM® Cortex™-A9 MPCore™ based processing system (PS) and Xilinx programmable logic (PL) in a single device.

PMIC

- Dialog's DA9062 PMIC

Memory

- DDR3L SDRAM – 512 MB (Expandable upto 1GB)
- eMMC Flash - 8GB (Expandable) [1, 2]
- QSPI Flash for PS booting - 2MB (Expandable upto 16MB) [2]
- Micro SD slot (Optional) [1, 2]
- NAND Flash (Optional) [2]

Other On-SOM Features

- Wi-Fi & Bluetooth [3, 5]
- Gigabit Ethernet PHY Transceiver
- USB2.0 Transceiver

SODIMM PCB Edge Interfaces

From PS Block

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- USB 2.0 OTG x 1 Port (through On-SOM USB2.0 transceiver)
- Debug UART
- I2C x 1 Port
- SD (4bit) x 1 Port (Optional) [3]
- JTAG Interface

From PL Block

- FPGA IOs – PL Bank34 [4]
  - Upto 22 LVDS IOs/48 Single ended (SE) IOs
    - Upto three Clock Capable LVDS/SE pins
- FPGA IOs – PL Bank35 [5, 6]
  - Upto 50 SE IOs
    - Upto three Clock Capable SE pins
    - Upto 16 1Mbps Analog Input Channels
- FPGA IOs – PL Bank13 [7, 8]
  - Upto 12 LVDS IOs/25 Single ended (SE) IOs
    - Upto four Clock Capable LVDS/SE pins

General Specification

- Power Supply : 3.3V (from SODIMM PCB edge connector)
- Form Factor : 67.6mm x 37mm

[1] *In Zynq-7000 SoC SODIMM SOM, SD1 interface signals are connected to both eMMC Flash and MicroSD connector. So either one feature only can be supported at a time in the SOM and by default, eMMC is supported.*

[2] *In Zynq-7000 SoC PS, QSPI+SD/eMMC and NAND Signals are multiplexed in same pins and so either QSPI + SD/eMMC or NAND Flash can be supported. By default, QSPI + eMMC is supported in Zynq-7000 SoC SODIMM SOM.*

[3] *In Zynq-7000 SoC SODIMM SOM, SD0 interface signals from PS can be connected to either WIFI module or SODIMM Edge connector. By default, SD0 signals are connected to WIFI module.*

[4] *In Zynq-7000 SoC SODIMM SOM, IO voltage of PL BANK34 is connected from PMIC LDO1 and can be set from 1.2V to 3.3V.*

[5] *In Zynq-7000 SoC SODIMM SOM, IO voltage of PL BANK35 is connected from PMIC LDO4 and can be set to from 1.2V to 3.3V. If On-SOM Bluetooth support is required, then BANK35 IO voltage has to be set to 3.3V only and so BANK35 doesn't support 1.8V LVDS IOs at this time.*

[6] *In Zynq-7000 SoC, PL BANK35 IO pins can support upto 16 Analog Inputs through on chip Dual 12bit 1Msps ADC. Note that only On-Chip voltage reference is supported in Zynq-7000 SoC SODIMM SOM.*

[7] *In Zynq-7000 SoC, PL BANK13 is not available in Z-7007S and Z-7010 devices and so BANK13 IOs on SODIMM edge connector is NC in Z-7007S and Z-7010 SoC based SODIMM SOM.*

[8] *In Zynq-7000 SoC SODIMM SOM, IO voltage of PL BANK13 is fixed to 3.3V by default and so this bank IOs can be used as only 3.3V Single Ended IOs. If 1.8V LVDS IOs support is required for BANK13, contact iWave.*

2.3 Zynq-7000 SoC

The Zynq-7000 SoC SODIMM SOM is based on Xilinx Zynq-7000 SoC with CLG400 package and compatible to Z-7007S, Z-7014S, Z-7010 and Z-7020 devices. Xilinx Zynq-7000 family devices integrate a feature-rich dual or single-core ARM® Cortex™-A9 MPCore™ based processing system (PS) and Xilinx programmable logic (PL) in a single device. The Block Diagram of Zynq-7000 SoC from Xilinx website is shown below for reference.

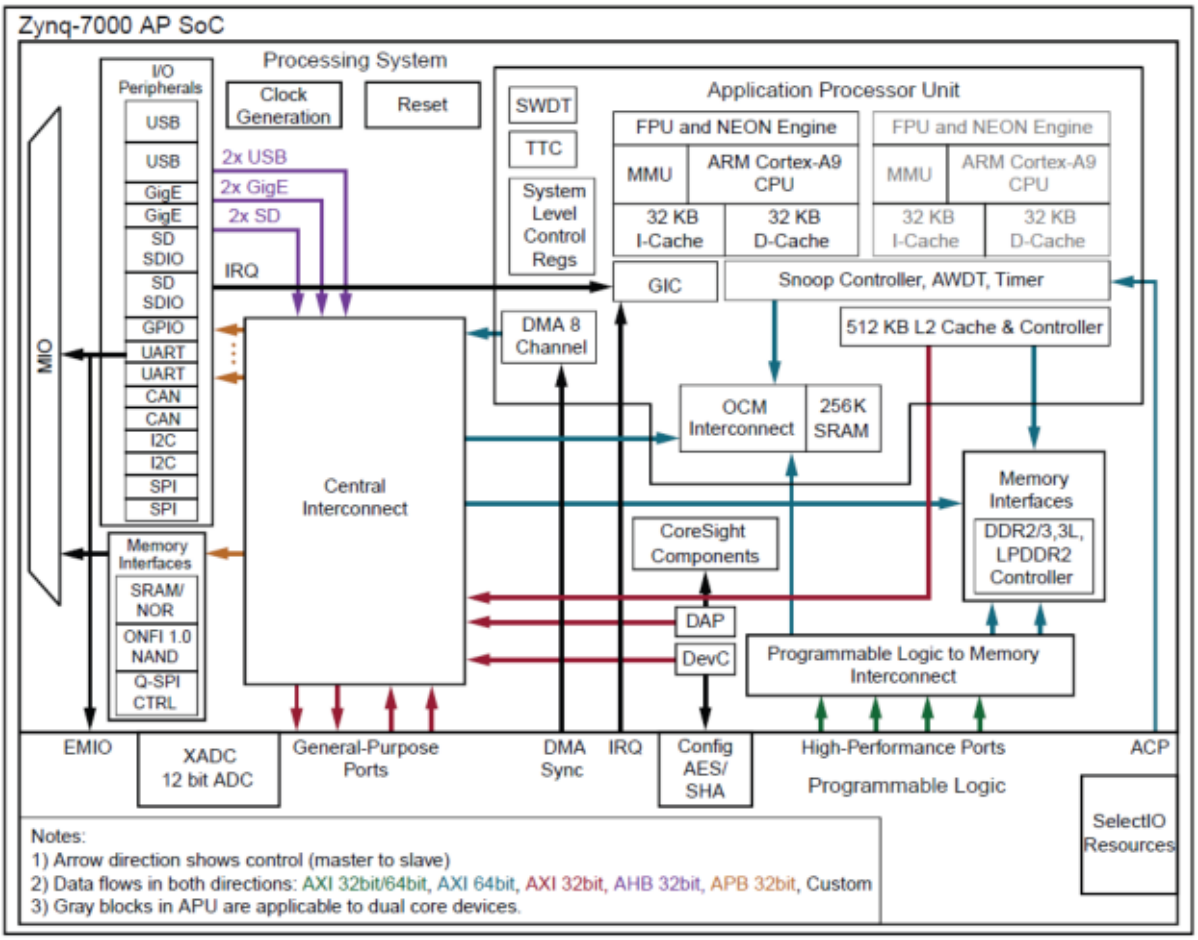


Figure 2: Zynq-7000 CPU Simplified Block Diagram

Note: Please refer the latest Zynq 7000 Datasheet & Reference Manual for more details which may be revised from time to time.

The Zynq-7000 SODIMM SOM is compatible to Z-7007S, Z-7014S, Z-7010 and Z-7020 SoC devices and feature comparison between these SoC devices are shown below.

	Device Name	Z-7007S	Z-7014S	Z-7010	Z-7020
	Part Number	XC7Z007S	XC7Z014S	XC7Z010	XC7Z020
Processing System	Processor Core	Single-core ARM Cortex-A9 MPCore™ with CoreSight™	Dual-core ARM Cortex-A9 MPCore™ with CoreSight™		
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor			
	Maximum Frequency	667 MHz (-1); 766 MHz (-2)	667 MHz (-1); 766 MHz (-2); 866 MHz (-3)		
	L1 Cache	32 KB Instruction, 32 KB data per processor			
	L2 Cache	512 KB			
	On-Chip Memory	256 KB			
	DMA Channels	8 (4 dedicated to Programmable Logic)			
	Security	RSA Authentication, and AES and SHA 256-bit Decryption and Authentication for Secure Boot			
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)		2x AXI 32b Master 2x AXI 32-bit Slave 4x AXI 64-bit/32-bit Memory AXI 64-bit ACP 16 Interrupts			
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA
	Programmable Logic Cells	23K	65K	28K	85K
	Look-Up Tables (LUTs)	14,400	40,600	17,600	53,200
	Flip-Flops	28,800	81,200	35,200	106,400
	Block RAM (# 36 Kb Blocks)	1.8 Mb (50)	3.8 Mb (107)	2.1 Mb (60)	4.9 Mb (140)
	DSP Slices (18x25 MACCs)	66	170	80	220
	Peak DSP Performance (Symmetric FIR)	73 GMACs	187 GMACs	100 GMACs	276 GMACs
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs			
	Security	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication			

Figure 3: Zynq-7000 SoC Devices Comparison

Note: Please refer the latest Zynq 7000 Datasheet & Reference Manual for more details which may be revised from time to time.

The Zynq-7000 SoC has 54 dedicated PS I/O pins called as MIO for the peripheral interfaces of the PS. Since 54 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in Zynq-7000 SoC to route most of the IO peripheral interfaces to PL I/O pins called as EMIO. Zynq-7000 SoC PS Peripheral Pin mapping options between MIO & EMIO is shown below.

Peripheral Interface	MIO	EMIO
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 54 bits	Yes CAN: External PHY GPIO: Up to 64 bits
GigE: 0,1	RGMII v2.0 External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (Tx and Rx)	Full UART (Tx, Rx, DTR, DCD, DSR, RI, RTS and CTS) either require: Two Processing System pins (Rx and Tx) through MIO and six additional Programmable Logic pins, *or* Eight Programmable Logic pins
Processor JTAG	Yes	Yes

Figure 4: Zynq-7000 SoC IOs

2.4 Zynq-7000 SoC Reference Clock

Table 3: Zynq-7000 SoC SOM Reference Clock.

Sl. No	On-SOM Oscillator Frequency	Zynq-7000 Ball Name/ Pin Number	Signal Type/ Termination	Description	Stability
1	33.33MHz	PS_CLK_500/ E7	3.3V, LVCMOS	33.33Mhz single ended reference clock for PS.	±50ppm
2	50MHz*	BANK34_REF_CLK/ N18	3.3V, LVCMOS	50Mhz single ended reference clock for PL.	±50ppm
3	-	BANK35_REF_CLKp & BANK35_REF_CLKn/ H16 & H17	1.8V LVDS/ 3.3V LVCMOS	Optional Single ended or LVDS reference clock for PL. *Note: This is an optional feature and by default not populated.*	-

Important Note: If 50MHz external reference clock has to be used in PL, then IO voltage of PL BANK34 has to be set to 3.3V only through PMIC LDO1.

2.5 PMIC

The Zynq-7000 SoC SODIMM SOM supports Dialog semiconductor DA9062 PMIC for On-SOM power management. The DA9062 PMIC provides all required power to Zynq-7000 SoC and all On SOM peripherals. This PMIC supports up to four buck converters, four linear regulators, RTC supply and coin-cell charger.

The Zynq-7000 SoC's I2C0 interface from PS MIO is connected to PMIC with I2C address 0x58 for configuring the PMIC. The DA9062 PMIC's Linear Regulators LDO1 and LDO4 are connected to PL BANK 34 and BANK 35 respectively. These LDO Outputs from PMIC can be configured from 1.2V to 3.3V through I2C0 in Uboot.

2.6 Memory

2.6.1 DDR3L SDRAM

The Zynq-7000 SoC SODIMM SOM supports 512MB DDR3 RAM memory for Zynq-7000 SoC PS by default. Two 16bit, 256MB DDR3 SDRAM ICs are used to support a total on board RAM memory of 512MB. This device operates at 1.35V voltage level. The RAM size can be expandable up to maximum of 1GB.

2.6.2 QSPI Flash

The Zynq-7000 SoC SODIMM SOM supports 2MB QSPI Flash as default boot device for Zynq-7000 SoC PS. This is connected to QSPI controller of the PS and operates at 3.3 Voltage level. The QSPI Flash size can be expandable up to maximum of 16MB.

Note: In Zynq-7000 SoC PS, QSPI+SD/eMMC and NAND Signals are multiplexed in same pins and so either QSPI + SD/eMMC or NAND Flash can be supported. By default, QSPI + eMMC is supported in Zynq-7000 SoC SODIMM SOM.

2.6.3 eMMC Flash

The Zynq-7000 SoC SODIMM SOM supports eMMC Flash memory for storage Media and also can be used as secondary boot device for Zynq-7000 SoC PS. This eMMC Flash memory is directly connected to the SD1 controller of the PS through MIO pins and operates at 3.3V Voltage level. Since SD1 controller supports only upto four data lines, eMMC Flash supports up to 4bit mode only in Zynq-7000 SoC SODIMM SOM. The Zynq-7000 SoC SD/SDIO controller supports MMC3.31 standard.

Note: In Zynq-7000 SoC PS, QSPI+SD/eMMC and NAND Signals are multiplexed in same pins and so either QSPI + SD/eMMC or NAND Flash can be supported. By default, QSPI + eMMC is supported in Zynq-7000 SoC SODIMM SOM.

Note: In Zynq-7000 SoC SODIMM SOM, SD1 interface signals are connected to both eMMC Flash and MicroSD connector. So either one feature only can be supported at a time in the SOM and by default, eMMC is supported.

2.6.4 Micro SD Slot (Optional)

The Zynq-7000 SoC SODIMM SOM optionally supports Micro SD slot to connect Micro SD card for Storage Media and also can be used as Secondary Boot device for Zynq-7000 SoC PS. Micro SD Card Connector (J2) is directly connected to the SD1 controller of the PS through MIO pins and operates at 3.3V Voltage level. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 2.0 Part A2. Also it supports card detect feature through PS GPIO "PS_MIO9_500". This is the optional feature and will not be populated in default configuration.

Note: In Zynq-7000 SoC PS, QSPI+SD/eMMC and NAND Signals are multiplexed in same pins and so either QSPI + SD/eMMC or NAND Flash can be supported. By default, QSPI + eMMC is supported in Zynq-7000 SoC SODIMM SOM.

Note: In Zynq-7000 SoC SODIMM SOM, SD1 interface signals are connected to both eMMC Flash and MicroSD connector. So either one feature only can be supported at a time in the SOM and by default, eMMC is supported.

2.6.5 NAND Flash (Optional)

The Zynq-7000 SoC SODIMM SOM has the hardware footprint option for NAND Flash memory which can be used as Boot Media Device for Zynq-7000 SoC PS. This NAND Flash is directly connected to the SMC Controller of the Zynq-7000 SoC PS through MIO pins and operates at 3.3V Voltage level. The SMC controller NAND Flash interface supports ONFI Specification 1.0 and can support upto 1GB memory device. This is the optional feature and not populated in default configuration.

Note: In Zynq-7000 SoC PS, QSPI+SD/eMMC and NAND Signals are multiplexed in same pins and so either QSPI + SD/eMMC or NAND Flash can be supported. By default, QSPI + eMMC is supported in Zynq-7000 SoC SODIMM SOM.

2.7 Wi-Fi & Bluetooth

The Zynq-7000 SoC SODIMM SOM supports Microchip's "ATWILC3000" based Wi-Fi & Bluetooth combo module for connectivity. This module is an IEEE 802.11 b/g/n RF/Baseband/MAC link controller and Bluetooth 4.0 Low Energy (BLE) compliant module, optimized for low power mobile applications. The Zynq-7000 SoC SODIMM SOM supports a 32.768 kHz clock oscillator for this module for sleep operation.

The ATWILC3000 Wi-Fi module supports single stream 1x1 IEEE 802.11n mode providing up to 72 Mbps PHY rate. The module features fully integrated Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive switch, Power Management and chip Antenna. This module offers very low power consumption while simultaneously providing high performance. The Zynq-7000 SoC's SD0 SDHC controller through MIO pins are used for Wi-Fi interface which supports 1-bit or 4-bit transfer mode at the clock range of 0-50 MHz. The Zynq-7000 SoC's PS SD0 pins are 1.8V IO level and so level translator is used between the SoC and Wi-Fi Module.

The ATWILC3000 Bluetooth supports Bluetooth 4.0 Basic Rate, Enhanced Rate & BLE. The Zynq-7000 SoC's UART interface through EMIO pins are used for Bluetooth interface. The Zynq-7000 SoC SODIMM SOM supports UART TX and RX though PL BANK35 pins L9P and L9N respectively.

Note: In Zynq-7000 SoC SODIMM SOM, SD0 interface signals from Zynq-7000 SoC can be connected to either ATWILC3000 Wi-Fi module or to SODIMM Edge connector. In Wi-Fi supported Zynq-7000 SoC SODIMM SOM, SD0 interface signals are connected to ATWILC3000 Wi-Fi module. In Non-Wi-Fi supported Zynq-7000 SoC SODIMM SOM, SD0 interface signals are connected to SODIMM Edge connector.

Note: In Zynq-7000 SoC SODIMM SOM, PL BANK35 pins L9P and L9N from Zynq-7000 SoC can be connected to either ATWILC3000 Bluetooth module or to SODIMM Edge connector. In Bluetooth supported Zynq-7000 SoC SODIMM SOM, PL BANK35 L20 and L19 signals are connected to ATWILC3000 Bluetooth module. In Non-Bluetooth supported Zynq-7000 SoC SODIMM SOM, PL BANK35 pins L19 and L20 are connected to SODIMM Edge connector.

Note: In Zynq-7000 SoC SODIMM SOM, IO voltage of PL BANK35 is connected from PMIC LDO4 and can be set to 1.8V or 3.3V to support 3.3V Single Ended IOs respectively. If On-SOM Bluetooth support is required, then BANK35 IO voltage has to be set to 3.3V only.

2.8 SODIMM PCB Edge Connector

The Zynq-7000 SoC SODIMM SOM Supports JEDEC Physical Standard 200pin SODIMM PCB edge connector for interfaces expansion.

The Zynq-7000 SoC SODIMM SOM PCB Edge connector pinout Map is shown in the below ***Table 4*** and the interfaces which are available at SODIMM PCB Edge connector are explained in the following sections.

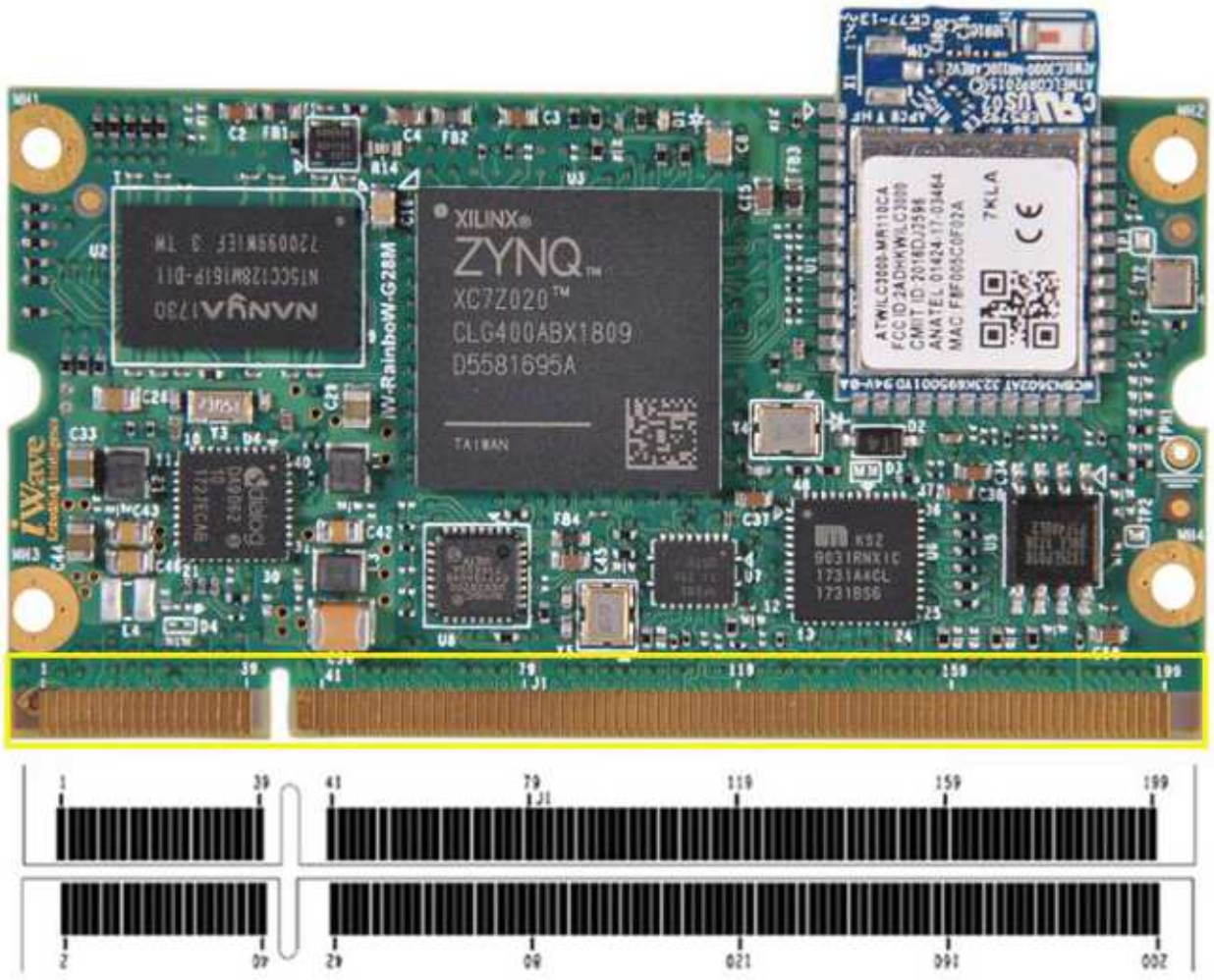


Figure 5: SODIMM PCB Edge Connector

Number of Pins - 200

Connector Part - Not Applicable (On Board PCB Edge connector)

Mating Connector - 1473005-1 from TE Connectivity

Table 4: SODIMM PCB Edge Connector Pinout Map

Signal	SODIMM Pin (Top)	SODIMM Pin (Bottom)	Signal
GND	1	2	GPHY_ATXRXM
NC	3	4	GPHY_ATXRXP
GND	5	6	GPHY_BTXRXM
PL_IO_L19N_T3_VREF_13	7	8	GPHY_BTXRXP
PL_IO_L19P_T3_13	9	10	PL_IO_L6N_T0_VREF_13
GPHY_LINK_LED2	11	12	GPHY_ACTIVITY_LED1
GND	13	14	GPHY_CTXRXM
GPHY_DTXRXM	15	16	GPHY_CTXRXP
GPHY_DTXRXP	17	18	PL_IO_L11N_T1_SRCC_13
PL_IO_L11P_T1_SRCC_13	19	20	VIN_3V3
PL_IO_L22P_T3_13	21	22	PL_IO_L15P_T2_DQS_13
PL_IO_L22N_T3_13	23	24	PL_IO_L15N_T2_DQS_13
NC	25	26	PL_IO_L12P_T1_MRCC_13
GND	27	28	PL_IO_L12N_T1_MRCC_13
PL_IO_L20P_T3_13	29	30	PL_IO_L18P_T2_13
PL_IO_L20N_T3_13	31	32	VIN_3V3
PL_IO_L18N_T2_13	33	34	PL_IO_L1N_T0_34
PL_IO_L2N_T0_34	35	36	PL_IO_L1P_T0_34
PL_IO_L2P_T0_34	37	38	PL_IO_L10N_T1_34
PL_IO_L10P_T1_34	39	40	GND
Key			Key
GND	41	42	PL_IO_L18N_T2_34
PL_IO_L23N_T3_34	43	44	PL_IO_L18P_T2_34
PL_IO_L23P_T3_34	45	46	VIN_3V3
PL_IO_L13N_T2_MRCC_34	47	48	PL_IO_L17N_T2_13
NC	49	50	PL_IO_L17P_T2_13
GND	51	52	PL_IO_L13N_T2_MRCC_13
PL_IO_L14N_T2_SRCC_13	53	54	PL_IO_L13P_T2_MRCC_13
PL_IO_L14P_T2_SRCC_13	55	56	PL_IO_L21N_T3_DQS_13
PL_IO_L16N_T2_13	57	58	PL_IO_L21P_T3_DQS_13
PL_IO_L16P_T2_13	59	60	VIN_3V3
PL_IO_L8N_T1_34	61	62	PL_IO_L4N_T0_34
PL_IO_L8P_T1_34	63	64	PL_IO_L4P_T0_34
GND	65	66	PL_IO_L7N_T1_34
PL_IO_L11N_T1_SRCC_34	67	68	PL_IO_L7P_T1_34
PL_IO_L11P_T1_SRCC_34	69	70	PL_IO_L17P_T2_34
PL_IO_L6N_T0_VREF_34	71	72	VIN_3V3
PL_IO_L6P_T0_34	73	74	PL_IO_L17N_T2_34
PL_IO_0_34	75	76	PL_IO_25_34
USB_OTG_ID	77	78	USB_PWR_EN

Signal	SODIMM Pin (Top)	SODIMM Pin (Bottom)	Signal
GND	79	80	PL_IO_L3P_T0_DQS_PUDC_B_34
USB_OTG_DP	81	82	NC
USB_OTG_DM	83	84	NC
NC	85	86	PL_IO_L9P_T1_DQS_34
NC	87	88	VIN_3V3
PL_IO_L9N_T1_DQS_34	89	90	PL_IO_L12P_T1_MRCC_34
PL_IO_L19P_T3_34	91	92	PL_IO_L12N_T1_MRCC_34
PL_IO_L19N_T3_VREF_34	93	94	PL_IO_L22P_T3_34
GND	95	96	PL_IO_L22N_T3_34
PL_IO_L5P_T0_34	97	98	PL_IO_L21P_T3_DQS_34
PL_IO_L5N_T0_34	99	100	PL_IO_L21N_T3_DQS_34
PL_IO_L20P_T3_34	101	102	PL_IO_L16P_T2_34
PL_IO_L20N_T3_34	103	104	PL_IO_L16N_T2_34
GPIO (PS_MIO48_501)	105	106	VIN_3V3
SD0_DATA0(PS_MIO42_501)[1]	107	108	SD0_CMD(PS_MIO41_501)[1]
SD0_CLK(PS_MIO40_501)[1]	109	110	PL_IO_L24N_T3_34
SD0_DATA1(PS_MIO43_501)[1]	111	112	SD0_DATA2(PS_MIO44_501)[1]
GND	113	114	SD0_DATA3(PS_MIO45_501)[1]
B_I2C0_SDA(PS_MIO47_501)	115	116	B_I2C0_SCL(PS_MIO46_501)
B_UART0_RX(PS_MIO50_501)	117	118	B_UART0_TX(PS_MIO51_501)
PL_IO_L14N_T2_SRCC_34	119	120	PL_IO_L15N_T2_DQS_34
PL_IO_L14P_T2_SRCC_34	121	122	PL_IO_L15P_T2_DQS_34
PL_IO_L3N_T0_DQS_34	123	124	VIN_3V3
PL_IO_L23P_T3_35	125	126	PL_IO_L21P_T3_DQS_AD14P_35
NC	127	128	NC
NC	129	130	NC
GND	131	132	PL_IO_L22N_T3_AD7N_35
PL_IO_L23N_T3_35	133	134	PL_IO_L20P_T3_AD6P_35
NC	135	136	PL_IO_L12P_T1_MRCC_35
NC	137	138	PL_IO_L22P_T3_AD7P_35
PL_IO_L24P_T3_AD15P_35	139	140	PL_IO_L21N_T3_DQS_AD14N_35
NC	141	142	VIN_3V3
PL_IO_L8N_T1_AD10N_35	143	144	PL_IO_L11N_T1_SRCC_35
PL_IO_L8P_T1_AD10P_35	145	146	PL_IO_L7P_T1_AD2P_35
PL_IO_L7N_T1_AD2N_35	147	148	PL_IO_L9P_T1_DQS_AD3P_35[1]
PL_IO_L9N_T1_DQS_AD3N_35[1]	149	150	PL_IO_L11P_T1_SRCC_35
GND	151	152	PL_IO_L14P_T2_AD4P_SRCC_35
PL_IO_L10N_T1_AD11N_35	153	154	PL_IO_L10P_T1_AD11P_35
PL_IO_L6N_T0_VREF_35	155	156	PL_IO_L16P_T2_35
PL_IO_25_35	157	158	PL_IO_L12N_T1_MRCC_35
PL_IO_L14N_T2_AD4N_SRCC_35	159	160	VIN_3V3

Signal	SODIMM Pin (Top)	SODIMM Pin (Bottom)	Signal
PL_IO_L6P_T0_35	161	162	PL_IO_L17P_T2_AD5P_35
PL_IO_L24N_T3_AD15N_35	163	164	PL_IO_L17N_T2_AD5N_35
PL_IO_L18N_T2_AD13N_35	165	166	PL_IO_L20N_T3_AD6N_35
PL_IO_L19P_T3_35	167	168	PL_IO_L16N_T2_35
GND	169	170	PL_IO_L15P_T2_DQS_AD12P_35
PL_IO_L18P_T2_AD13P_35	171	172	PL_IO_L15N_T2_DQS_AD12N_35
PL_IO_L19N_T3_VREF_35	173	174	PL_IO_L1P_T0_AD0P_35
PL_IO_L5P_T0_AD9P_35	175	176	PL_IO_L4P_T0_35
PL_IO_L3N_T0_DQS_AD1N_35	177	178	PL_IO_L4N_T0_35
PL_IO_L5N_T0_AD9N_35	179	180	VIN_3V3
PL_IO_L3P_T0_DQS_AD1P_35	181	182	NC
VRTC_3V0	183	184	NC
GND	185	186	GND
B_PS_SRST_B_501	187	188	NC
PL_IO_L1N_T0_AD0N_35	189	190	PL_IO_L2N_T0_AD8N_35
JTAG_TDO	191	192	VIN_3V3
NC	193	194	PL_IO_0_35
JTAG_TDI	195	196	PL_IO_L2P_T0_AD8P_35
JTAG_TCK	197	198	GND
JTAG_TMS	199	200	VBUS_USB

[1] Note: In Zynq-7000 SoC SODIMM SOM, these signals from Zynq-7000 SoC can be connected to either ATWILC3000 Wi-Fi/Bluetooth module or to SODIMM Edge connector. In Non-Wi-Fi/Bluetooth supported Zynq-7000 SoC SODIMM SOM, these pins can be used as SDIO & PL IOs at SODIMM Edge connector.

2.8.1 Gigabit Ethernet Interface

The Zynq-7000 SoC SODIMM SOM supports one 10/100/1000 Mbps Ethernet interface on SODIMM Edge connector. The MAC is integrated in the Zynq-7000 SoC PS and connected to the external Gigabit Ethernet PHY "KSZ9031RNX" on SOM. This PHY is interfaced with ENET0 interface of Zynq-7000 SoC PS through MIO pins and works at 1.8V IO voltage level. Also this PHY supports Link and Activity indication LED control signals and available on SODIMM Edge. The below table provides details about Ethernet Interface signals on SODIMM Edge connector.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
2	GPHY_ATXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
4	GPHY_ATXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
6	GPHY_BTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
8	GPHY_BTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
11	GPHY_LINK_LED2	NA	O, 1.8V CMOS/ 10K PU	Gigabit Ethernet link status LED.
12	GPHY_ACTIVITY_LED1	NA	O, 1.8V CMOS/ 10K PU	Gigabit Ethernet speed status LED.
14	GPHY_CTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
15	GPHY_DTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
16	GPHY_CTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
17	GPHY_DTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.

Since MAC and PHY are supported on SOM itself, only Magnetics is required on the carrier board. It is recommended that centre tap pins of magnetics should be separated from one another and connected through separate 0.1uF common mode capacitors to ground. Since this PHY doesn't recommend to connect any power source to magnetic centre tap pins, CTREF voltage to SODIMM Edge is not supported on SOM. The below table provides some of the compatible magnetics recommended by the PHY Manufacturer.

Part Description	Part Number	Manufacturer	Temperature
Gigabit Ethernet Discrete Transformer	TG1G-E001NZRL	HALO	-40°C to 85°C
Gigabit Ethernet Discrete Transformer	HX5008NL	Pulse	-40°C to 85°C
RJ45 Magjack with two Green LED	JK0654219NL	Pulse	0°C to 70°C
RJ45 Magjack with two Green LED	0826-1G1T-23-F	Bel Fuse	0°C to 70°C

2.8.2 USB 2.0 OTG Interface

The Zynq-7000 SoC SODIMM SOM supports one USB2.0 OTG interface on SODIMM Edge connector. USB0 OTG controller of Zynq-7000 SoC PS is used for USB2.0 OTG interface. This USB controller is capable of fulfilling a wide range of applications for USB 2.0 implementations as a host, a device, or On-the-Go. Also this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the MIO pins. The Zynq 7000 SoC SODIMM SOM supports "USB3320" ULPI transceiver from Microchip and woks at 1.8V IO voltage level.

The Zynq 7000 SoC SODIMM SOM supports active high power enable signal on SODIMM Edge connector from this USB PHY for external VBUS power control. Also it supports USB ID input and USB VBUS from SODIMM Edge connector and connected to USB PHY for USB Host/Device detection and VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
81	USB_OTG_DP	NA	IO, USB	USB OTG data positive.
83	USB_OTG_DM	NA	IO, USB	USB OTG data negative.
77	USB_OTG_ID	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
78	USB_PWR_EN	NA	O, 3.3V CMOS	USB active high power enable output to control external USB Vbus.
200	VBUS_USB	NA	I, 5V Power	USB VBUS for VBUS monitoring. *Note: Recommending to connect always available 5V to this pin from carrier board to maintain compatibility with iWave's other SODIMM SOMs.*

2.8.3 Debug UART Interface

The Zynq-7000 SoC SODIMM SOM support one UART interfaces on SODIMM Edge connector for Zynq-7000 SoC PS Debug. The UART0 controller of Zynq-7000 SoC PS is used for Debug UART interface through MIO pins. This controller is structured with separate RXD and TXD data path. Each path includes a 64- Byte FIFIO. The UART0 pins of Zynq 7000 SoC PS is 1.8V IO level and so the level translator is used between the SoC & SODIMM Edge connector to support 3.3V IO level.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
117	UART0_RX (PS_MIO50_501)	PS_MIO50_501/ B13	I, 3.3V LVCMOS	Debug UART0 Receive data line.
118	UART0_TX (PS_MIO51_501)	PS_MIO51_501/ B9	O, 3.3V LVCMOS	Debug UART0 Transmit data line.

2.8.4 I2C Interface

The Zynq-7000 SoC SODIMM SOM supports one I2C interface on SODIMM Edge connector. The I2C0 module of Zynq-7000 SoC PS is used for I2C interface through MIO pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes.

The I2C0 pins of Zynq-7000 SoC PS is 1.8V IO level and so the level translator is used between the SoC & SODIMM Edge connector to support 3.3V IO level. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C0 interface is also connected to On-SOM PMIC with I2C address 0x58 in the Zynq-7000 SoC SODIMM SOM.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
115	I2C0_SDA(PS_MIO47_501)	PS_MIO47_501/ B14	IO, 3.3V OD/ 4.7K PU	I2C0 data.
116	I2C0_SCL(PS_MIO46_501)	PS_MIO46_501/ D16	O, 3.3V OD/ 4.7K PU	I2C0 clock.

2.8.5 SD/SDIO interface (Optional)

The Zynq-7000 SoC SODIMM SOM optionally supports SD/SDIO interface on SODIMM Edge connector. The SD0 controller of Zynq-7000 SoC PS is used for SD/SDIO interface through MIO pins. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 2.0 Part A2. This is the optional feature and supported in Non WiFi Zynq-7000 SoC SODIMM SOM.

The Zynq-7000 SoC SODIMM SOM can support card detect input through PS GPIO. It is recommended to use SODIMM Edge connector pin 105 for card detect. The SD0 pins of Zynq-7000 SoC PS is 1.8V IO level and so the level translator is used between the SoC & SODIMM Edge connector to support 3.3V IO level.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
105	GPIO (PS_MIO48_501)	PS_MIO48_501/ B12	IO, 3.3V LVCMOS	General Purpose Input/output. Recommend to use as SD0 card detect.
107	SD0_DATA0 (PS_MIO42_501)	PS_MIO42_501/ E12	IO, 3.3V LVCMOS	SD0 DATA0
108	SD0_CMD (PS_MIO41_501)	PS_MIO41_501/ C17	IO, 3.3V LVCMOS	SD0 Command
109	SD0_CLK (PS_MIO40_501)	PS_MIO40_501/ D14	O, 3.3V LVCMOS	SD0 Clock
111	SD0_DATA1 (PS_MIO43_501)	PS_MIO43_501/ A9	IO, 3.3V LVCMOS	SD0 DATA1

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
112	SD0_DATA2 (PS_MIO44_501)	PS_MIO44_501/ F13	IO, 3.3V LVCMOS	SD0 DATA2
114	SD0_DATA3 (PS_MIO45_501)	PS_MIO45_501/ B15	IO, 3.3V LVCMOS	SD0 DATA3

Note: In Zynq-7000 SoC SODIMM SOM, SD0 interface signals from Zynq-7000 SoC PS can be connected to either ATWILC3000 Wi-Fi/Bluetooth module or to SODIMM Edge connector. In the default Wi-Fi/Bluetooth supported Zynq-7000 SoC SODIMM SOM, SD0 interface signals are connected to ATWILC3000 Wi-Fi module.

2.8.6 FPGA IOs – PL BANK34

The Zynq-7000 SoC SODIMM SOM supports 22 LVDS IOs/48 Single Ended (SE) IOs on SODIMM Edge connector from Zynq-7000 SoC PL Bank34. Upon these 22 LVDS IOs/48 SE IOs, upto three clock capable LVDS IOs/SE IOs (one MRCC and two SRCC) are available.

The IO voltage of PL Bank34 is connected from LDO1 output of the PMIC. So the PL Bank34 IO voltage can be configurable from 1.2V to 3.3V through PMIC. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage to PL Bank34. For more details about supported IO standard, refer the Zynq-7000 SoC datasheet.

The Zynq-7000 SoC PL Bank34 signals are routed as LVDS IO Pairs to SODIMM Edge connector in the Zynq-7000 SoC SODIMM SOM. Even though PL Bank34 signals are routed as LVDS IOs, these pins can be used as Single Ended IOs if required. By default, IO voltage of PL Bank34 is set as 3.3V to support 3.3V Single Ended IOs.

The SODIMM Edge connector pins 67, 69, 90, 92, 119 & 121 are the clock capable pins of PL Bank34. The Zynq-7000 SoC SODIMM SOM supports 3.3V, 50Mhz external clock oscillator and connected to “N18” MRCC pin of the PL Bank34. This clock can be used as reference clock for PL if required.

Important Note: If 50MHz external reference clock has to be used in PL, then IO voltage of PL BANK34 has to be set to 3.3V only through PMIC LDO1.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
34	PL_IO_L1N_T0_34	L1N_34/ T10	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel1 Negative if Bank34 IO voltage is set to 1.8V.
35	PL_IO_L2N_T0_34	L2N_34/ U12	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel2 Negative if Bank34 IO voltage is set to 1.8V.
36	PL_IO_L1P_T0_34	L1P_34/ T11	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel1 Positive if Bank34 IO voltage is set to 1.8V.
37	PL_IO_L2P_T0_34	L2P_34/ T12	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel2 Positive if Bank34 IO voltage is set to 1.8V.
38	PL_IO_L10N_T1_34	L10N_34/ W15	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel10 Negative if Bank34 IO voltage is set to 1.8V.
39	PL_IO_L10P_T1_34	L10P_34/ V15	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel10 Positive if Bank34 IO voltage is set to 1.8V.
42	PL_IO_L18N_T2_34	L18N_34/ W16	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel18 Negative if Bank34 IO voltage is set to 1.8V.
43	PL_IO_L23N_T3_34	L23N_34/ P18	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel23 Negative if Bank34 IO voltage is set to 1.8V.
44	PL_IO_L18P_T2_34	L18P_34/ V16	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel18 Positive if Bank34 IO voltage is set to 1.8V.
45	PL_IO_L23P_T3_34	L23P_34/ N17	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel23 Positive if Bank34 IO voltage is set to 1.8V.
47	PL_IO_L13N_T2_MRCC_34	L13N_34/ P19	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
61	PL_IO_L8N_T1_34	L8N_34/ Y14	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel8 Negative if Bank34 IO voltage is set to 1.8V.
62	PL_IO_L4N_T0_34	L4N_34/ W13	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel4 Negative if Bank34 IO voltage is set to 1.8V.
63	PL_IO_L8P_T1_34	L8P_34/ W14	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel8 Positive if Bank34 IO voltage is set to 1.8V.
64	PL_IO_L4P_T0_34	L4P_34/ V12	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel4 Positive if Bank34 IO voltage is set to 1.8V.
66	PL_IO_L7N_T1_34	L7N_T1/ Y17	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel7 Negative if Bank34 IO voltage is set to 1.8V.
67	PL_IO_L11N_T1_SRCC_34	L11N_34/ U15	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel11 Negative if Bank34 IO voltage is set to 1.8V.
68	PL_IO_L7P_T1_34	L7P_34/ Y16	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel7 Positive if Bank34 IO voltage is set to 1.8V.
69	PL_IO_L11P_T1_SRCC_34	L11P_34/ U14	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel11 Positive if Bank34 IO voltage is set to 1.8V.
70	PL_IO_L17P_T2_34	L17P_34/ Y18	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel17 Positive if Bank34 IO voltage is set to 1.8V.
71	PL_IO_L6N_T0_VREF_34	L6N_34/ R14	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel6 Negative if Bank34 IO voltage is set to 1.8V.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
73	PL_IO_L6P_T0_34	L6P_34/ P14	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel6 Positive if Bank34 IO voltage is set to 1.8V.
74	PL_IO_L17N_T2_34	L17N_34/ Y19	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel17 Negative if Bank34 IO voltage is set to 1.8V.
75	PL_IO_0_34	0_34/ R19	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin.
76	PL_IO_25_34	25_34/ T19	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin.
80	PL_IO_L3P_T0_DQS_PUDC_B_34	L3P_34/ U13	IO, 3.3V LVCMOS/1K PU	Bank34 User I/O Single ended pin.
86	PL_IO_L9P_T1_DQS_34	L9P_34/ T16	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel9 Positive if Bank34 IO voltage is set to 1.8V.
89	PL_IO_L9N_T1_DQS_34	L9N_34/ U17	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel9 Negative if Bank34 IO voltage is set to 1.8V.
90	PL_IO_L12P_T1_MRCC_34	L12P_34/ U18	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel12 Positive if Bank34 IO voltage is set to 1.8V.
91	PL_IO_L19P_T3_34	L19P_34/ R16	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel19 Positive if Bank34 IO voltage is set to 1.8V.
92	PL_IO_L12N_T1_MRCC_34	L12N_34/ U19	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel12 Negative if Bank34 IO voltage is set to 1.8V.
93	PL_IO_L19N_T3_VREF_34	L19N_34/ R17	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel19 Negative if Bank34 IO voltage is set to 1.8V.
94	PL_IO_L22P_T3_34	L22P_34/ W18	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel22 Positive if Bank34 IO voltage is set to 1.8V

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
96	PL_IO_L22N_T3_34	L22N_34/ W19	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel22 Negative if Bank34 IO voltage is set to 1.8V.
97	PL_IO_L5P_T0_34	L5P_34/ T14	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel5 Positive if Bank34 IO voltage is set to 1.8V.
98	PL_IO_L21P_T3_DQS_ 34	L21P_34/ V17	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel21 Positive if Bank34 IO voltage is set to 1.8V.
99	PL_IO_L5N_T0_34	L5N_34/ T15	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel5 Negative if Bank34 IO voltage is set to 1.8V.
100	PL_IO_L21N_T3_DQS_ 34	L21N_34/ V18	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel21 Negative if Bank34 IO voltage is set to 1.8V.
101	PL_IO_L20P_T3_34	L20P_34/ T17	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel20 Positive if Bank34 IO voltage is set to 1.8V.
102	PL_IO_L16P_T2_34	L16P_34/ V20	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel16 Positive if Bank34 IO voltage is set to 1.8V.
103	PL_IO_L20N_T3_34	L20N_34/ R18	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel20 Negative if Bank34 IO voltage is set to 1.8V.
104	PL_IO_L16N_T2_34	L16N_34/ W20	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel16 Negative if Bank34 IO voltage is set to 1.8V.
110	PL_IO_L24N_T3_34	L24N_34/ P16	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin.
119	PL_IO_L14N_T2_SRCC _34	L14N_34/ P20	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel14 Negative if Bank34 IO voltage is set to 1.8V.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
120	PL_IO_L15N_T2_DQS_34	L15N_34/ U20	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel15 Negative if Bank34 IO voltage is set to 1.8V.
121	PL_IO_L14P_T2_SRCC_34	L14P_34/ N20	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel14 Positive if Bank34 IO voltage is set to 1.8V.
122	PL_IO_L15P_T2_DQS_34	L15P_34/ T20	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. Same pin can be configured as Bank34 LVDS Channel15 Positive if Bank34 IO voltage is set to 1.8V.
123	PL_IO_L3N_T0_DQS_34	L3N_34/ V13	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin.

2.8.7 FPGA IOs – PL BANK35

The Zynq-7000 SoC SODIMM SOM supports 50 Single Ended (SE) IOs on SODIMM Edge connector from Zynq-7000 SoC PL Bank35. Upon these 48 SE IOs, upto three clock capable SE IOs (one MRCC and two SRCC) and upto 16 analog input channels are available.

The IO voltage of PL Bank35 is connected from LDO4 output of the PMIC. So the PL Bank35 IO voltage can be configurable from 1.2V to 3.3V through PMIC. While using as Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage to PL Bank35. For more details about supported IO standard, refer the Zynq-7000 SoC datasheet.

The Zynq-7000 SoC PL Bank35 signals are routed as SE IOs to SODIMM Edge connector in the Zynq-7000 SoC SODIMM SOM. By default, IO voltage of PL Bank35 is set as 3.3V to support 3.3V Single Ended IOs.

The SODIMM Edge connector pins 144, 150, 136, 158, 152 & 159 are the clock capable pins of PL Bank35. The Zynq-7000 SoC SODIMM SOM optionally supports external differential clock oscillator and connected to “H16 & H17” MRCC pins of the PL Bank35 for reference clock if required.

The Zynq-7000 SoC has a flexible analog-to-digital converter (XADC) with programmable logic to address a broad range of analog data acquisition and monitoring requirements. The Zynq-7000 SoC XADC has two 12-bit 1 mega samples per second (MSPS) ADCs, on-chip thermal and on-chip voltage sensors. These two ADCs can be configured to simultaneously sample two external-input analog channels. The track and hold amplifiers support a range of analog input signal types, including unipolar, bipolar, and differential. The Zynq-7000 SoC SODIMM SOM supports only on-chip reference and doesn’t support external 1.25V reference IC. For more details on XADC Interface, refer the Zynq-7000 SoC TRM.

Note: In Zynq-7000 SoC SODIMM SOM, PL BANK35 pins L20 and L19 from Zynq-7000 SoC can be connected to either ATWILC3000 Bluetooth module or to SODIMM Edge connector. By default, these are connected to Bluetooth module.

Important Note: In Zynq-7000 SoC SODIMM SOM, if On-SOM Bluetooth support is required, then BANK35 IO voltage has to be set to 3.3V only

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
125	PL_IO_L23P_T3_35	L23P_35/ M14	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
126	PL_IO_L21P_T3_DQS_ AD14P_35	L21P_35/ N15	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel14 positive.
132	PL_IO_L22N_T3_AD7 N_35	L22N_35/ L15	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
133	PL_IO_L23N_T3_35	L23N_35/ M15	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
134	PL_IO_L20P_T3_AD6P _35	L20P_35/ K14	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel6 Positive.
136	PL_IO_L12P_T1_MRC C_35	L12P_35/ K17	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
138	PL_IO_L22P_T3_AD7P _35	L22P_35/ L14	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel7 Positive.
139	PL_IO_L24P_T3_AD15 P_35	L24P_35/ K16	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel15 Positive.
140	PL_IO_L21N_T3_DQS_ AD14N_35	L21N_35/ N16	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
143	PL_IO_L8N_T1_AD10 N_35	L8N_35/ M18	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI UART Receive Data.*
144	PL_IO_L11N_T1_SRCC _35	L11N_35/ L17	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Module Chip Enable.*
145	PL_IO_L8P_T1_AD10P _35	L8P_35/ M17	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel10 Positive. *Note: This pin is optionally connected to WIFI UART Transmit Data.*
146	PL_IO_L7P_T1_AD2P_ 35	L7P_35/ M19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel2 Positive. *Note: This pin is optionally connected to WIFI Bluetooth Clear to Send.*
147	PL_IO_L7N_T1_AD2N _35	L7N_35/ M20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Bluetooth Request to Send.*

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
148	PL_IO_L9P_T1_DQS_AD3P_35[1]	L9P_35/ L19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel3 Positive.
149	PL_IO_L9N_T1_DQS_AD3N_35[1]	L9N_35/ L20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
150	PL_IO_L11P_T1_SRCC_35	L11P_35/ L16	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Module SD_CLK.*
152	PL_IO_L14P_T2_AD4P_ SRCC_35	L14P_35/ J18	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel4 Positive. *Note: This pin is optionally connected to WIFI Module SD_DATA0.*
153	PL_IO_L10N_T1_ AD11N_35	L10N_35/ J19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Module SD_CMD.*
154	PL_IO_L10P_T1_AD11P_35	L10P_35/ K19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel11 Positive. *Note: This pin is optionally connected to WIFI Module Reset.*
155	PL_IO_L6N_T0_VREF_ 35	L6N_35/ F17	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Module SD_DATA3.*
156	PL_IO_L16P_T2_35	L16P_35/ G17	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Module SD_DATA2.*
157	PL_IO_25_35	25_35/ J15	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Module Interrupt.*
158	PL_IO_L12N_T1_MRCC_35	L12N_35/ K18	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
159	PL_IO_L14N_T2_AD4N_ SRCC_35	L14N_35/ H18	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. *Note: This pin is optionally connected to WIFI Module SD_DATA1.*
161	PL_IO_L6P_T0_35	L6P_35/ F16	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
162	PL_IO_L17P_T2_AD5P_35	L17P_35/ J20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
163	PL_IO_L24N_T3_ AD15N_35	L24N_35/ J16	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
164	PL_IO_L17N_T2_AD5N_35	L17N_35/ H20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
165	PL_IO_L18N_T2_AD13N_35	L18N_35/ G20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
166	PL_IO_L20N_T3_AD6N_35	L20N_35/ J14	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
167	PL_IO_L19P_T3_35	L19P_35/ H15	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
168	PL_IO_L16N_T2_35	L16N_35/ G18	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
170	PL_IO_L15P_T2_DQS_AD12P_35	L15P_35/ F19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel12 Positive.
171	PL_IO_L18P_T2_AD13P_35	L18P_35/ G19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel13 Positive.
172	PL_IO_L15N_T2_DQS_AD12N_35	L15N_35/ F20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
173	PL_IO_L19N_T3_VREF_35	L19N_35/ G15	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
174	PL_IO_L1P_T0_AD0P_35	L1P_35/ C20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel0 Positive
175	PL_IO_L5P_T0_AD9P_35	L5P_35/ E18	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel9 Positive
176	PL_IO_L4P_T0_35	L4P_35/ D19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
177	PL_IO_L3N_T0_DQS_AD1N_35	L3N_35/ D18	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
178	PL_IO_L4N_T0_35	L4N_35/ D20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
179	PL_IO_L5N_T0_AD9N_35	L5N_35/ E19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
181	PL_IO_L3P_T0_DQS_AD1P_35	L3P_35/ E17	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel1 Positive
189	PL_IO_L1N_T0_AD0N_35	L1N_35/ B20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.
190	PL_IO_L2N_T0_AD8N_35	L2N_35/ A20	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
194	PL_IO_0_35	IO_0/ G14	IO, 3.3V LVCMOS/ 10KPU	Bank35 User I/O Single ended pin.
196	PL_IO_L2P_T0_AD8P_ 35	L2P_35/ B19	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. Same pin can be configured as Analog input channel8 Positive.

[1]*Note: In Zynq-7000 SoC SODIMM SOM, these signals from Zynq-7000 SoC Bank35 can be connected to either ATWILC3000 Wi-Fi/Bluetooth module or to SODIMM Edge connector. In the default Wi-Fi/Bluetooth supported Zynq-7000 SoC SODIMM SOM, these signals are connected to ATWILC3000 Wi-Fi module.*

2.8.8 FPGA IOs – PL BANK13

The Zynq-7000 SoC SODIMM SOM supports 12 LVDS IOs/25 Single Ended (SE) IOs on SODIMM Edge connector from Zynq-7000 SoC PL Bank13. Upon these 12 LVDS IOs/25 Single Ended (SE), upto four clock capable SE pins (two MRCC and two SRCC) are available. The SODIMM Edge connector pins 18, 19, 26, 28, 52, 54, 53 & 55 are the clock capable pins.

The IO voltage of this PL Bank13 is fixed to 3.3V to support 3.3V SE IOs. Optionally, 1.8V IO voltage can be supported to PL Bank13 in Zynq-7000 SoC SODIMM SOM to support LVDS IOs. Please contact iWave to support 1.8V IO voltage for PL Bank13.

Important Note: In Zynq-7000 SoC, PL BANK13 is not available in Z-7007S and Z-7010 devices and so BANK13 IOs on SODIMM edge connector is NC in Z-7007S and Z-7010 SoC based SODIMM SOM.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
7	PL_IO_L19N_T3_VREF_13	L19N_13/ U5	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel19 Negative if Bank13 IO voltage is set to 1.8V.
9	PL_IO_L19P_T3_13	L19P_13/ T5	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel19 Positive if Bank13 IO voltage is set to 1.8V.
10	PL_IO_L6N_T0_VREF_13	L6N_13/ V5	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin.
18	PL_IO_L11N_T1_SRCC_13	L11N_13/ V7	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel11 Negative if Bank13 IO voltage is set to 1.8V.
19	PL_IO_L11P_T1_SRCC_13	L11P_13/ U7	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel11 Positive if Bank13 IO voltage is set to 1.8V.
21	PL_IO_L22P_T3_13	L22P_13/ V6	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel22 Positive if Bank13 IO voltage is set to 1.8V.
22	PL_IO_L15P_T2_DQS_13	L15P_13/ V8	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel15 Positive if Bank13 IO voltage is set to 1.8V.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
23	PL_IO_L22N_T3_13	L22N_13/ W6	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel22 Negative if Bank13 IO voltage is set to 1.8V.
24	PL_IO_L15N_T2_DQS_ 13	L15N_13/ W8	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel15 Negative if Bank13 IO voltage is set to 1.8V.
26	PL_IO_L12P_T1_MRC C_13	L12P_13/ T9	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel12 Positive if Bank13 IO voltage is set to 1.8V.
28	PL_IO_L12N_T1_MRC C_13	L12N_13/ U10	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel12 Negative if Bank13 IO voltage is set to 1.8V.
29	PL_IO_L20P_T3_13	L20P_13/ Y12	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel20 Positive if Bank13 IO voltage is set to 1.8V.
30	PL_IO_L18P_T2_13	L18P_13/ W11	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel18 Positive if Bank13 IO voltage is set to 1.8V.
31	PL_IO_L20N_T3_13	L20N_13/ Y13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel20 Negative if Bank13 IO voltage is set to 1.8V.
33	PL_IO_L18N_T2_13	L18N_13/ Y11	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel18 Negative if Bank13 IO voltage is set to 1.8V.
48	PL_IO_L17N_T2_13	L17N_13/ U8	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel17 Negative if Bank13 IO voltage is set to 1.8V..
50	PL_IO_L17P_T2_13	L17P_13/ U9	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel17 Positive if Bank13 IO voltage is set to 1.8V.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
52	PL_IO_L13N_T2_MRCC_13	L13N_13/ Y6	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel13 Negative if Bank13 IO voltage is set to 1.8V.
53	PL_IO_L14N_T2_SRCC_13	L14N_13/ Y8	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel14 Negative if Bank13 IO voltage is set to 1.8V.
54	PL_IO_L13P_T2_MRCC_13	L13P_13/ Y7	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel13 Positive if Bank13 IO voltage is set to 1.8V.
55	PL_IO_L14P_T2_SRCC_13	L14P_13/ Y9	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel14 Positive if Bank13 IO voltage is set to 1.8V
56	PL_IO_L21N_T3_DQS_13	L21N_13/ V10	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel21 Negative if Bank13 IO voltage is set to 1.8V.
57	PL_IO_L16N_T2_13	L16N_13/ W9	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel16 Negative if Bank13 IO voltage is set to 1.8V
58	PL_IO_L21P_T3_DQS_13	L21P_13/ V11	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel21 Positive if Bank13 IO voltage is set to 1.8V.
59	PL_IO_L16P_T2_13	L16P_13/ W10	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. Same pin can be configured as Bank13 LVDS Channel16 Positive if Bank13 IO voltage is set to 1.8V.

2.8.9 JTAG Interface

The Zynq-7000 SoC SODIMM SOM supports JTAG interface on SODIMM Edge connector. This provides debug and test control with the maximum security. Internally the Zynq-7000 AP SoC device implements both an ARM debug access port (DAP) inside the Processing System (PS) as well as a standard JTAG test access port (TAP) controller inside the Programmable Logic (PL). In cascaded JTAG chain mode, both the TAP and DAP are visible from external JTAG debug tools or a JTAG tester. Zynq-7000 SoC JTAG pins are 3.3V IO level.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
191	JTAG_TDO	TDO/F6	O, 3.3V CMOS	JTAG Test Data Output.
195	JTAG_TDI	TDI/G6	I, 3.3V CMOS	JTAG Test Data Input.
197	JTAG_TCK	TCK/F9	I, 3.3V CMOS	JTAG Test Clock.
199	JTAG_TMS	TMS/J6	I, 3.3V CMOS	JTAG Test Mode Select.

2.8.10 Power Input

The Zynq-7000 SoC SODIMM SOM works with single 3.3V power input (VCC) from SODIMM Edge connector and generates all other required powers internally On-SOM itself. Zynq-7000 SoC SODIMM SOM also supports VCC_RTC coin cell power input from SODIMM Edge connector to PMIC VBBAT for real time clock.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
20, 32, 46, 60, 72, 88, 106, 124, 142, 160, 180 & 192	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
1, 5, 13, 27, 40, 41, 51, 65, 79, 95, 113, 131, 151, 169, 185, 186, 198	GND	NA	Power	Ground.
183	VRTC_3V0	NA	I, 3V Power	3V coin cell input for RTC.

2.8.11 Reset Signal

The Zynq-7000 SoC SODIMM SOM supports PS_SRST_B input from SODIMM Edge connector. Reset button input from SODIMM Edge connector is the active low signal which is connected to PMIC Power Enable. This pin can be used to restart the power cycle of Zynq-7000 SoC CPU by connecting push button in the carrier board.

SODIMM Pin No.	SODIMM Edge Connector Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
187	PS_SRST_B_501	PS_SRST_B_501 /B10	I, 3.3V CMOS	Active low reset button input. *Important Note: This pin is directly connected to PMIC Power Enable pin. Use this pin only for connecting the reset push button in the carrier board.*

2.9 Zynq-7000 SoC PS Pin Multiplexing on SODIMM

The Zynq-7000 SoC PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of the Zynq-7000 PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Zynq-7000 SoC SODIMM SOM with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring Processor System Pin information of Zynq-7000 SoC device.

Table 5: PS IOMUX on Zynq-7000 SoC SODIMM SOM

Interface/ Function	SODIMM Edge Pin Number	Zynq 7000 SoC PS Pin Number	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Function 16	Function 17	Function 18	Function 19
On SOM Features from PS																						
QSPI FLASH	NA	PS_MIO0_500	GPIO-0	NAND Flash_CS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	NOR_CS0	SRAM_CS0
	NA	PS_MIO1_500	GPIO-1		QSPI0_SS_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-		NOR_CS1/AD25	SRAM_CS1/AD25
	NA	PS_MIO2_500	GPIO-2	NAND Flash_ALE	QSPI0_IO_0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DATA8		-
	NA	PS_MIO3_500	GPIO-3	NAND Flash_WE_B	QSPI0_IO_1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DATA9	SRAM/NOR_D0	-
	NA	PS_MIO4_500	GPIO-4	NAND Flash_DATA2	QSPI0_IO_2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DATA10	SRAM/NOR_D1	-
	NA	PS_MIO5_500	GPIO-5	NAND Flash_DATA0	QSPI0_IO_3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DATA11	SRAM/NOR_D2	-
	NA	PS_MIO6_500	GPIO-6	NAND Flash_DATA1	QSPI0_IO_SCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DATA12	SRAM/NOR_D3	-
	NA	PS_MIO7_500	GPIO-7	NAND Flash_CLE		-	-	-	-	-	-	-	-	-	-	-	-	-	-	DATA13	SRAM/NOR_OE_B	-
	NA	PS_MIO8_500	GPIO-8	NAND Flash_RE_B	-	-	-	-	-	-	UART1_TX				CAN1_TX	-	-	-		DATA14	SRAM/NOR_BLS_B	-
eMMC Flash	NA	PS_MIO9_500	GPIO-9	NAND Flash_DATA4	-	-	-	-	-	-	UART1_RX				CAN1_RX	-	-	-		DATA15	SRAM/NOR_D6	-
	NA	PS_MIO10_500	GPIO-10	NAND Flash_DATA5	-	-	SD1_DATA0	-	SPI1_MOSI	UART0_RX	-	I2C0_SCL		CAN0_RX		-	-	-	PJTAG_TDI	DATA2	SRAM/NOR_D7	-
	NA	PS_MIO11_500	GPIO-11	NAND Flash_DATA6	-	-	SD1_CMD	-	SPI1_MISO	UART0_TX	-	I2C0_SDA		CAN0_TX		-	-	-	PJTAG_TDO	DATA3	SRAM/NOR_D4	-
	NA	PS_MIO12_500	GPIO-12	NAND Flash_DATA7	-	-	SD1_CLK	-	SPI1_SCK	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	-	-	PJTAG_TCK	CLK		-
	NA	PS_MIO13_500	GPIO-13	NAND Flash_DATA3	-	-	SD1_DATA1	-	SPI1_SS0	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	-	-	PJTAG_TMS	CTL	SRAM/NOR_D5	-
	NA	PS_MIO14_500	GPIO-14	NAND Flash_Busy	-	-	SD1_DATA2	-	-	UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	-	-	CLK_IN	-	DATA0		-
	NA	PS_MIO15_500	GPIO-15		-	-	SD1_DATA3	-	-	UART0_TX	-	I2C0_SDA	-	CAN0_TX	-	-	-	RST_OUT	-	DATA1	SRAM/NOR_A0	-
ENET0	NA	PS_MIO16_501	GPIO-16	ETH0_TX_CLK	-	SD0_CLK	-	SPI0_CLK	-	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX		Timer_Wave Out		-	DATA4	SRAM/NOR_A1	-
	NA	PS_MIO17_501	GPIO-17	ETH0_TXD0	-	SD0_CMD	-	SPI0_MISO	-	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX		Timer_CLK_In		-	DATA5	SRAM/NOR_A2	-
	NA	PS_MIO18_501	GPIO-18	ETH0_TXD1	-	SD0_DATA 0	-	SPI0_SS0	-	UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	Timer_Wave Out	-		-	DATA6	SRAM/NOR_A3	-
	NA	PS_MIO19_501	GPIO-19	ETH0_TXD2	-	SD0_DATA 1	-	-	-	UART0_TX	-	I2C0_SDA	-	CAN0_TX	-	Timer_CLK_In	-		-	DATA7	SRAM/NOR_A4	-
	NA	PS_MIO20_501	GPIO-20	ETH0_TXD3	-	SD0_DATA 2	-	-	-	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	-	-	-		SRAM/NOR_A5	-
	NA	PS_MIO21_501	GPIO-21	ETH0_TX_CTL	-	SD0_DATA 3	-	SPI0_MOSI	-	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	-	-	-		SRAM/NOR_A6	-
	NA	PS_MIO22_501	GPIO-22	ETH0_RX_CLK	-	-	SD1_DATA0	-	SPI1_MOSI	UART0_RX		I2C0_SCL	-	CAN0_RX	-	-	-	-	PJTAG_TDI	DATA2	SRAM/NOR_A7	-
	NA	PS_MIO23_501	GPIO-23	ETH0_RXD0	-	-	SD1_CMD	-	SPI1_MISO	UART0_TX		I2C0_SDA	-	CAN0_TX	-	-	-	-	PJTAG_TDO	DATA3	SRAM/NOR_A8	-
	NA	PS_MIO24_501	GPIO-24	ETH0_RXD1	-	-	SD1_CLK	-	SPI1_SCK	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	-	-	PJTAG_TCK	CLK	SRAM/NOR_A9	-
	NA	PS_MIO25_501	GPIO-25	ETH0_RXD2	-	-	SD1_DATA1	-	SPI1_SS0	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	-	-	PJTAG_TMS	CTL	SRAM/NOR_A10	-
	NA	PS_MIO26_501	GPIO-26	ETH0_RXD3	-	-	SD1_DATA2	-	-	UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	-	-	CLK_IN	-	DATA0	SRAM/NOR_A11	-

Interface/ Function	SODIMM Edge Pin Number	Zynq 7000 SoC PS Pin Number	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Function 16	Function 17	Function 18	Function 19
	NA	PS_MIO27_501	GPIO-27	ETH0_RX_CTL	-	-	SD1_DATA3	-	-	UART0_TX		I2C0_SDA		CAN0_TX	-	-	-	RST_OUT	-	DATA1	SRAM/NOR_A12	-
	NA	PS_MIO52_501	GPIO-52	ETH0_MDC	-	-	-	-	-	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	-	CLK_IN	-	-	-	-
	NA	PS_MIO53_501	GPIO-53	ETH0_MDIO	-	-	-	-	-	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	-	RST_OUT	-	-	-	-
USB0	NA	PS_MIO28_501	GPIO-28	ETH1_TX_CLK	USB0_DATA4	SD0_CLK	-	SPI0_CLK	-	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	Timer_Wave Out	-	-	-	SRAM/NOR_A13	-
	NA	PS_MIO29_501	GPIO-29	ETH1_TXD0	USB0_DIR	SD0_CMD	-	SPI0_MISO	-	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	Timer_CLK_In	-	-	-	SRAM/NOR_A14	-
	NA	PS_MIO30_501	GPIO-30	ETH1_TXD1	USB0_STP	SD0_DATA 0	-	SPI0_SS0		UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	Timer_Wave Out	-	-	-	-	SRAM/NOR_A15	-
	NA	PS_MIO31_501	GPIO-31	ETH1_TXD2	USB0_NXT	SD0_DATA 1	-	-	-	UART0_TX	-	I2C0_SDA	-	CAN0_TX	-	Timer_CLK_In	-	-	-	-	SRAM/NOR_A16	-
	NA	PS_MIO32_501	GPIO-32	ETH1_TXD3	USB0_DATA0	SD0_DATA 2	-	-	-	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	-	-	-	-	SRAM/NOR_A17	-
	NA	PS_MIO33_501	GPIO-33	ETH1_TX_CTL	USB0_DATA1	SD0_DATA 3	-	SPI0_MOSI	-	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	-	-	-	-	SRAM/NOR_A18	-
	NA	PS_MIO34_501	GPIO-34	ETH1_RX_CLK	USB0_DATA2	-	SD1_DATA0	-	SPI1_MOSI	UART0_RX		I2C0_SCL	-	CAN0_RX	-	-	-	-	PJTAG_TDI	-	SRAM/NOR_A19	-
	NA	PS_MIO35_501	GPIO-35	ETH1_RXD0	USB0_DATA3	-	SD1_CMD	-	SPI1_MISO	UART0_TX		I2C0_SDA	-	CAN0_TX	-	-	-	-	PJTAG_TDO	-	SRAM/NOR_A20	-
	NA	PS_MIO36_501	GPIO-36	ETH1_RXD1	USB0_CLK	-	SD1_CLK	-	SPI1_SCK	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	-	-	PJTAG_TCK	-	SRAM/NOR_A21	-
	NA	PS_MIO37_501	GPIO-37	ETH1_RXD2	USB0_DATA5	-	SD1_DATA1	-	SPI1_SS0	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	-	-	PJTAG_TMS	-	SRAM/NOR_A22	-
	NA	PS_MIO38_501	GPIO-38	ETH1_RXD3	USB0_DATA6	-	SD1_DATA2	-	-	UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	-	-	CLK_IN	-	-	SRAM/NOR_A23	-
	NA	PS_MIO39_501	GPIO-39	ETH1_RX_CTL	USB0_DATA7	-	SD1_DATA3	-	-	UART0_TX	-	I2C0_SDA	-	CAN0_TX	-	-	-	RST_OUT	-	-	SRAM/NOR_A24	-
SODIMM Edge connector Features from PS																						
I2C0	116	PS_MIO46_501	GPIO-46	USB1_DATA2	-	-	SD1_DATA0	-	SPI1_MOSI	UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	-	-	-	PJTAG_TDI	-	-	-
	115	PS_MIO47_501	GPIO-47	USB1_DATA3	-	-	SD1_CMD	-	SPI1_MISO	UART0_TX	-	I2C0_SDA	-	CAN0_TX	-	-	-	-	PJTAG_TDO	-	-	-
UART0	117	PS_MIO50_501	GPIO-50	USB1_DATA6	-	-	SD1_DATA2	-	-	UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	-	-	CLK_IN	-	-	-	-
	118	PS_MIO51_501	GPIO-51	USB1_DATA7	-	-	SD1_DATA3	-	-	UART0_TX	-	I2C0_SDA	-	CAN0_TX	-	-	-	RST_OUT	-	-	-	-
SD0 (Optional)	109	PS_MIO40_501	GPIO-40	USB1_DATA4	-	SD0_CLK	-	SPI0_CLK	-	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	Timer_Wave Out	-	-	-	-	-
	108	PS_MIO41_501	GPIO-41	USB1_DIR	-	SD0_CMD	-	SPI0_MISO	-	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	Timer_CLK_In	-	-	-	-	-
	107	PS_MIO42_501	GPIO-42	USB1_STP	-	SD0_DATA 0	-	SPI0_SS0	-	UART0_RX	-	I2C0_SCL	-	CAN0_RX	-	Timer_Wave Out	-	-	-	-	-	-
	111	PS_MIO43_501	GPIO-43	USB1_NXT	-	SD0_DATA 1	-	-	-	UART0_TX	-	I2C0_SDA	-	CAN0_TX	-	Timer_CLK_In	-	-	-	-	-	-
	112	PS_MIO44_501	GPIO-44	USB1_DATA0	-	SD0_DATA 2	-	-	-	-	UART1_TX	-	I2C1_SCL	-	CAN1_TX	-	-	-	-	-	-	-
	114	PS_MIO45_501	GPIO-45	USB1_DATA1	-	SD0_DATA 3	-	SPI0_MOSI	-	-	UART1_RX	-	I2C1_SDA	-	CAN1_RX	-	-	-	-	-	-	-
	105	PS_MIO48_501	GPIO-48	USB1_CLK	-	-	SD1_CLK	-	SPI1_SCK	-	UART1_TX	-	I2C1_SCL	-	-	-	-	-	PJTAG_TCK	-	-	-

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq-7000 SoC SODIMM SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Zynq-7000 SoC SODIMM SOM.

Table 6: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VIN_3V3[1]	3.15	3.3	3.45	±50mV
2	VRTC_3V0[2]	2.8	3	3.3	±20mV

[1] Zynq-7000 SoC SODIMM SOM is designed to work with VIN_3V3 input power rail from SODIMM Edge connector.

[2] Zynq-7000 SoC SODIMM SOM uses this voltage as backup power source to PMIC RTC when VIN_3V3 is off. This is an optional power and required only if RTC functionality is used.

Important Note: Once the VIN_3V3 input power is applied to SOM, SOM will take around 30ms for all the powers to get stable and come out of reset, Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.2 Power Consumption

Table 7: Power Consumption[1]

Task/Status	Power Rail	Current Drawn/Power Consumption
Bluetooth file transfer	VIN_3V3	0.884A/2.9W
Ethernet ping test	VIN_3V3	0.912A/3W
Wi-Fi ping test	VIN_3V3	0.913A/3W
Dhrystone	VIN_3V3	1.01A/3.33W
File transfer between USB and eMMC	VIN_3V3	1.023A/3.38W
Maximum Power test (Only PS): • Ethernet ping test • Bluetooth file transfer • File transfer between USB and eMMC • Dhrystone	VIN_3V3	1.04A/3.432W
RTC coin cell power (when VIN_3V3 is off)	VRTC_3V0	1.4uA

[1] Power consumption measurements have been done in Zynq-7020 SoC based SODIMM Development platform (iW-G28D-SM20-3D512M-E008G-LCA) with iWave's Linux4.14.0 BSP (iW-PRFOZ-SC-01-R2.0-REL1.0-Linux4.14.0).

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of Zynq-7000 SoC SODIMM SOM.

Table 8: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C
Humidity – Operating[2]	-	95%RH

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

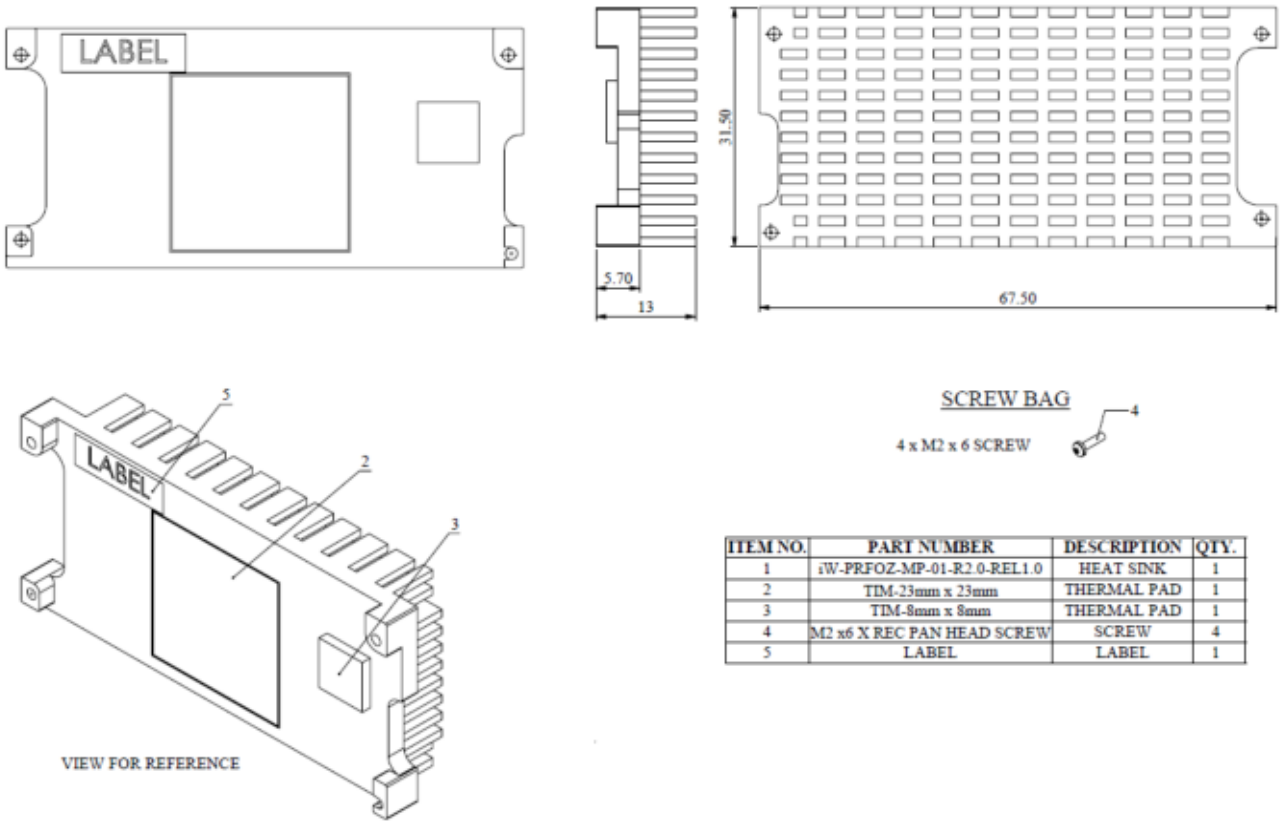
[2] To meet this humidity specification, conformal coating needs to be done on the board. By default, iWave boards doesn't come with conformal coating. Please contact iWave to support conformal coating.

3.2.2 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the SoC.

iWave supports Heat Sink Solution for Zynq-7000 SoC SODIMM SOM. Please refer the below figure for Heat Sink dimension details. For Heat Sink ordering information, please refer section 4 ORDERING INFORMATION.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	iW-PRFOZ-MP-01-R2.0-REL1.0	HEAT SINK	1
2	TIM-23mm x 23mm	THERMAL PAD	1
3	TIM-8mm x 8mm	THERMAL PAD	1
4	M2 x6 X REC PAN HEAD SCREW	SCREW	4
5	LABEL	LABEL	1

Figure 6: Zynq-7000 SoC SODIMM SOM Heat Sink

3.2.3 RoHS Compliance

iWave's Zynq-7000 SoC SODIMM SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's Zynq-7000 SoC SODIMM SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 MechanicalCharacteristics

3.3.1 SODIMM SOM Mechanical Dimensions

The Zynq-7000 SoC SODIMM SOM PCB size is 67.6mm x 37mm x 1mm with 10g weight. Mechanical dimension of the SOM is shown below. Please refer the JEDEC Physical standard DDR S.O.DIMM specification for SODIMM Edge connector mechanical details.

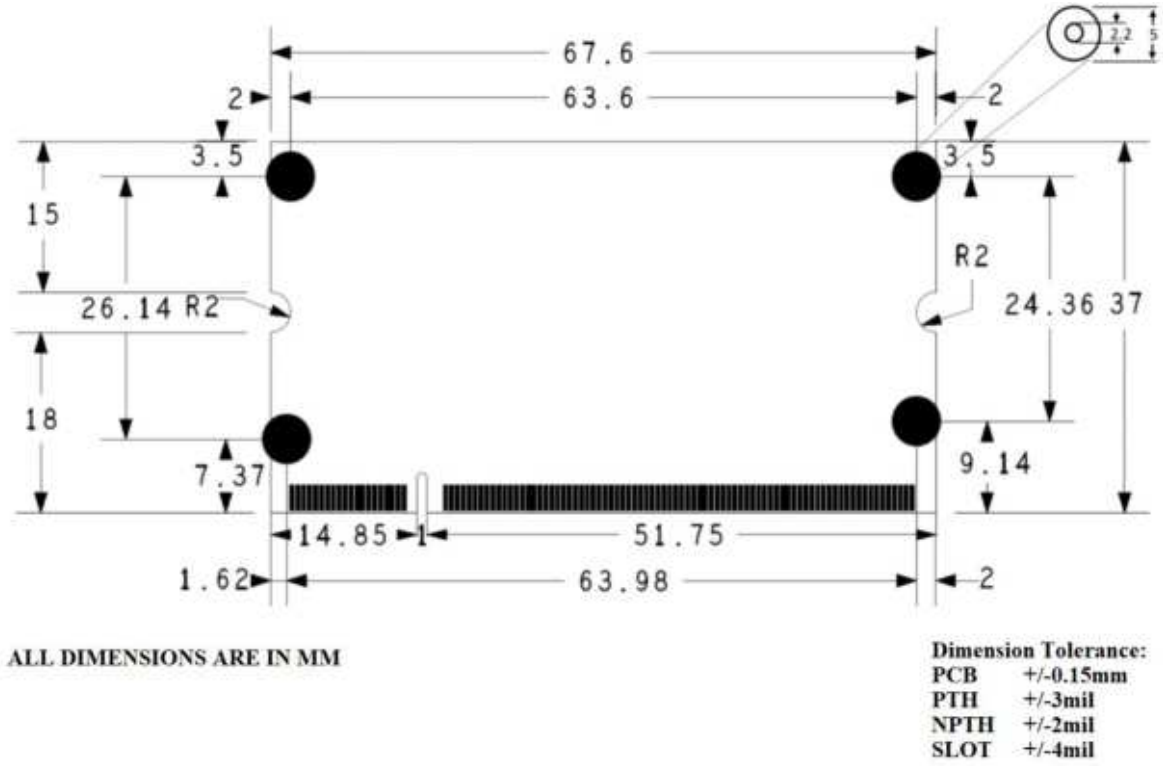


Figure 7: Mechanical dimension of Zynq-7000 SoC SODIMM SOM - Top View

The Zynq-7000 SoC SODIMM SOM PCB thickness is 1mm±0.1mm, top side maximum height component is Bulk Capacitor (2.37mm) followed by QSPI Flash (2.03mm) and bottom side maximum height component is MOSFET (1.75mm) followed by LDO Regulator (1.23mm). Please refer the below figure which gives height details of the Zynq-7000 SoC SOM.



Figure 8: Mechanical dimension of Zynq-7000 SoC SODIMM SOM- Side View

3.3.2 Guidelines to insert the SODIMM SOM into Carrier board

- Make sure that the carrier board is completely powered off.
- Insert the module into the socket at a slight angle (approximately 30 degrees). Note that the socket and module are both keyed, which means the module can be installed one way only.
- To seat the module into the socket, apply firm, even pressure to each end of the module until you feel it slip down into the socket.
- With the module properly seated in the socket, rotate the module downward, as indicated in the illustration. Continue pressing downward until the clips at each end of the socket lock into position.
- Once the SOM have been installed, Carrier board can be Powered ON with 5V power supply.

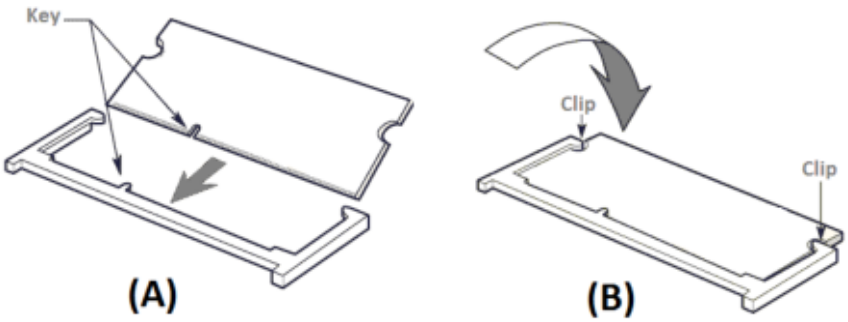


Figure 9: SODIMM SOM Insertion procedure

3.3.1 SODIMM SOM removing procedure from Carrier board

When you remove the SODIMM SOM module, pull away the retention clips (A) on each side of the memory module. The memory module pops up. Grasp the edge of the memory module (B), and gently pull the SOM module out of the connector.

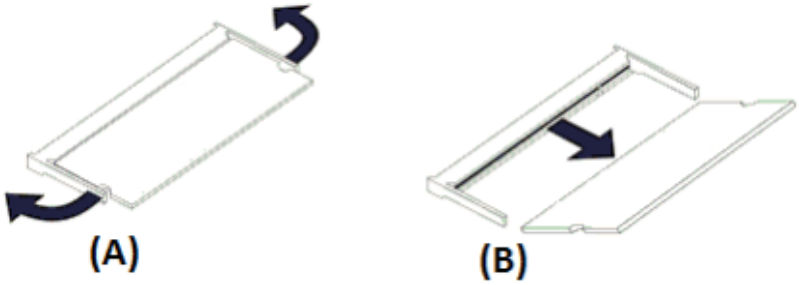


Figure 10: SODIMM SOM Removing Procedure

Important Note: Before touching any electronic components, make sure you are properly grounded by using some static control device to prevent static electricity stored on your body or clothing from damaging the system.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Zynq-7000 SoC SODIMM SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 9: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Zynq 7020 SoC SODIMM SOM		
iW-G28M-SM20-3D512M-E008G-LIA	With Zynq 7020 SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Linux	Industrial
iW-G28M-SM20-3D512M-E008G-BIA	With Zynq 7020 SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Boot code	Industrial
iW-G28M-SM20-3D512M-E008G-LIE	With Zynq 7020 SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Linux	Industrial
iW-G28M-SM20-3D512M-E008G-BIE	With Zynq 7020 SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Boot code	Industrial
Zynq 7010 SoC SODIMM SOM		
iW-G28M-SM10-3D512M-E008G-LIA	With Zynq 7010SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Linux	Industrial
iW-G28M-SM10-3D512M-E008G-BIA	With Zynq 7010 SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Boot code	Industrial
iW-G28M-SM10-3D512M-E008G-LIE	With Zynq 7010SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Linux	Industrial
iW-G28M-SM10-3D512M-E008G-BIE	With Zynq 7010 SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Boot code	Industrial
Zynq 7014S SoC SODIMM SOM		
iW-G28M-SM14-3D512M-E008G-LIA	With Zynq 7014S SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Linux	Industrial
iW-G28M-SM14-3D512M-E008G-BIA	With Zynq 7014S SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Boot code	Industrial
iW-G28M-SM14-3D512M-E008G-LIE	With Zynq 7014S SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Linux	Industrial
iW-G28M-SM14-3D512M-E008G-BIE	With Zynq 7014S SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Boot code	Industrial

Product Part Number	Description	Temperature
Zynq 7007S SoC SODIMM SOM		
iW-G28M-SM07-3D512M-E008G-LIA	With Zynq 7007S SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Linux	Industrial
iW-G28M-SM07-3D512M-E008G-BIA	With Zynq 7007S SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT - Boot code	Industrial
iW-G28M-SM07-3D512M-E008G-LIE	With Zynq 7007S SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Linux	Industrial
iW-G28M-SM07-3D512M-E008G-BIE	With Zynq 7007S SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT - Boot code	Industrial
Heat Sink		
iW-HSKALU-CLASLR-SS03	Heat Sink for Zynq-7000 SoC SODIMM SOM	-

Important Note: Some of the above-mentioned Part Number is subject to MOQ purchase. Please contact iWave for further details.

Note: For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

5. APPENDIX

5.1 Zynq-7000 SoC SODIMM SOM Development Platform

iWave Systems supports iW-RainboW-G28D – Zynq-7000 SoC SODIMM SOM Development Platform which is targeted for quick validation of Zynq-7000 SoC based SODIMM SOM. iWave's Zynq-7000 SoC SODIMM Development Board incorporates Zynq-7000 SoC SODIMM SOM and SODIMM Carrier board with complete BSP support. For more details on Zynq-7000 SoC SODIMM SOM Development Platform, visit the below web link.

https://www.iwavesystems.com/zynq-7000-development-board.html



Figure 11: Zynq-7000 SoC SODIMM SOM Development Platform


iWave
Embedding Intelligence