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ICM7217

4 Digit (LED) Presettable Up/Down Counter

General Description

The Maxim ICM7217 family of 4 digit presettable up/down counters contain a 4 digit, 7 segment LED display driver and a presettable comparison (predetermining) register. The counter and comparison register can be preset using either thumbwheel switches, jumpers, or external digital logic.

The ICM7217 (common anode) and ICM7217A (common cathode) are decade counters with a maximum count of 9999. The ICM7217B (common anode) and ICM7217C (common cathode) are modulo 60 counters intended for hours/minutes or minute/seconds timing applications, and have a maximum count of 5959.

These devices also provide multiplexed BCD outputs, a Carry/Borrow output allowing ICM7217s to be cascaded, a Zero output which indicates when the count is equal to zero, and an Equal output which indicates when the count is equal to the value contained in the comparison register. The ICM7217 also has a Reset input and a display latch with store input.

Applications

The Maxim ICM7217 significantly reduces the number of components required in many timing, counting and frequency counter applications.

Typical applications include:

Predetermining Batch Counter
Tachometer
Over/Under Speed Detector
Count Down/Elapsed Timer
Unit Counter
Frequency Counter

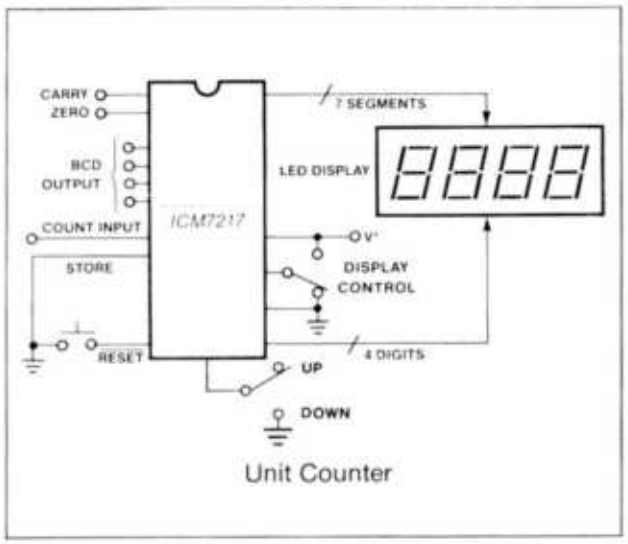
Features

- Pin for Pin Second Source!
- 4 Digit Up/Down Counter
- Directly Drives LED Display
- Presettable Counter and Compare Register
- Interfaces with Thumbwheel Switches or Digital Logic
- Can Be Cascaded
- Multiplexed BCD I/O
- Up/Down, Store and Reset Inputs
- Monolithic, Low Power CMOS Design

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7217IJI	-20°C to +85°C	28 Lead CERDIP
ICM7217IPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217AIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217AIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217BIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217BIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217CIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217CIPI	-20°C to +85°C	28 Lead Plastic DIP

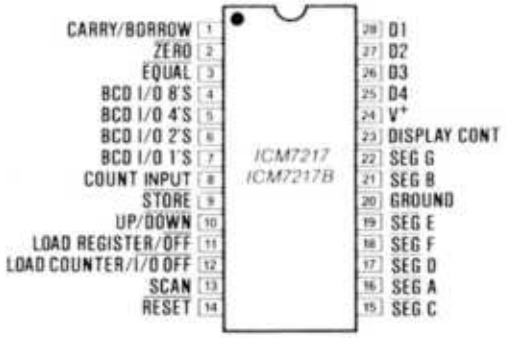
Typical Operating Circuit



Unit Counter

Pin Configuration

Top View



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-0931; Rev 0; 4/86

ICM7217

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 500mA
Power Dissipation
28 Pin CERDIP 1.0W
derate 25mW/°C above 50°C
28 Pin Plastic (copper leadframe) 1.0W
derate 25mW/°C above 50°C

Temperature Range
Operating ..... −20°C to +85°C
Plastic Chip Carrier (Quad) Package (Q) ..... 0°C to +70°C
Storage ..... −65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Segment Output Current 100mA
Input Voltage (any terminal) (Note 1) ..... −0.3V to (V^+ +0.3V)

Note 1: The maximum input voltage may be exceeded if the maximum input current is limited to 1mA.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C, test circuit, display diode drop = 1.7V, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Lowest Power Mode)	I^+ (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 2)		350	500	μA
Supply Current OPERATING	I^+_{ON}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+		4.5	5	5.5	V
Digit Driver Output Current	I_{DIG}	Common Anode, $V_{OUT} = V^+ - 2.0V$	140	200		mA peak
SEGment Driver Output Current	I_{SEG}	Common Anode, V_{OUT} = +1.5V	−20	−30		mA peak
Digit Driver Output Current	I_{DIG}	Common Cathode, V_{OUT} = +1.0	−50	−70		mA peak
SEGment Driver Output Current	I_{SEG}	Common Cathode, $V_{OUT} = V^+ - 2V$	10	12.5		mA peak
Digit and Segment Leakage Current	I_{LK}	LR Low	−100		+100	μA
ST, RS, UP/DN Input Low Voltage	V_{IL}				0.8	V
ST, RS, UP/DN Input High Voltage	V_{IH}		2.4			V
ST, RS, UP/DN Input Pullup Current	I_P	$V_{OUT} = V^+ - 2V$ (Note 2)	5	25	100	μA
Three Level Input Voltages Input High Input Floating Input Low	 V_{INH} V_{INF} V_{INL}	LR, LC, DC, V^+ = 5V	 4.2 2.0		 2.7 0.6	V
Three Level Impedance	Z_{IN}			100		kΩ
BCD I/O Input High Voltage	V_{BIH}	Common Anode V^+ = 5.0V	1.8			V
		Common Cathode V^+ = 5.0V	$V^+ - 0.6$			V
BCD I/O Input Low Voltage	V_{BIL}	Common Anode V^+ = 5.0V			0.8	V
		Common Cathode V^+ = 5.0V			$V^+ - 1.8$	V
BCD I/O Pullup Current	V_{BPU}	Common Cathode $V_{IN} = V^+ - 2V$ (Note 2)	5	25	300	μA
BCD I/O Pulldown Current	V_{BPD}	Common Anode V_{IN} = +1.3V (Note 2)	5	25	300	μA
BCD I/O, CARRY/BORROW, ZERO, EQUAL Outputs Output High Current	I_{BOH}	$V_{OH} = V^+ - 1.5V$	−1			mA
BCD I/O, CARRY/BORROW, ZERO, EQUAL Outputs Output Low Current	I_{BOL}	V_{OL} = +0.4V	+2			mA

Note 2: The Up/Down, Store, Reset and BCD I/O as inputs have pullup or pulldown devices which typically draw 50μA each when connected to the opposite supply.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C, test circuit, display diode drop = 1.7V, unless noted.)

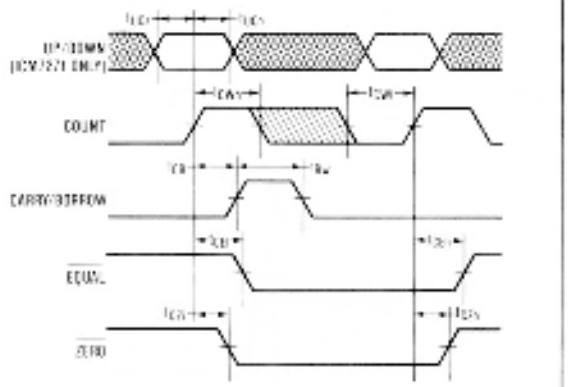
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Count Input Frequency	f_{IN}	V^+ = 5V ± 10%, −20°C < T_A < +70°C	0	5	2	MHz
Count Input Threshold	V_{TH}	V^+ = 5V	0.8	2	3.5	V
Count Input Hysteresis	V_{HYS}	V^+ = 5V		0.5		V
Count Input Leakage	I_{IN}		−1		+1	µA
Display Multiplex Rate	f_{MUX}	Not Loading	100	625		Hz
		Loading	200	—	5000	
Display Scan Oscillator Frequency	f_{DS}	Free-running (SCAN Terminal Open Circuit)		2.5		kHz
Interdigit Blanking Time	t_{idb}		750	3000		ns
Operating Temperature Range	T_A	Industrial Temperature Range	−20		+85	°C

Pin Descriptions

PIN NUMBER		PIN NAME	FUNCTION
COMMON ANODE ICM7217 ICM7271B	COMMON CATHODE ICM7217A ICM7217C		
24	24	V^+	Positive Power Supply. 5V ± 10%
20	19	GROUND	Ground.
28,27,26,25	18,17,16,15	D1,D2,D3,D4	These Digit Drive outputs directly drive the anodes (ICM7217 and ICM7217B) or the cathodes (ICM7217A and ICM7217C) of seven segment LED displays. D1 is the rightmost or least significant digit.
16,21,15,17, 19,18,22	23,27,25,28 22,26,21	Segments A–G	These Segment Drive outputs directly drive 7 segment LED displays. Current limiting resistors are NOT required.
7,6,5,4	7,6,5,4	BCD I/O 1,2,4,8	During normal operation these pins are BCD outputs, whose data corresponds to the count latched into the Store register. The data is multiplexed, digit by digit, going from the most significant digit (1000's) to the least significant digit (1's). The BCD data is valid approximately 6µs before the leading edge of each digit (rising edge of ICM7217/B digit outputs, falling edge of ICM7217A/C common Cathode outputs). During Load Counter and Load Register operations, the BCD I/O pins are inputs. BCD input data is latched by the trailing edge each digit period during Load Counter and Load register operations. The BCD input voltage levels are skewed to allow the use of thumbwheel switches connected to the digit driver to load BCD data. A positive voltage level is an input logic zero for the ICM7217A/C common cathode versions.
8	8	COUNT	Positive-going transitions of the COUNT input increment or decrement the counter, except when RESET is low or a load counter operation is in progress. The COUNT input is compatible with CMOS. TTL compatibility can be ensured by using a 4.7 kilohm pullup resistor on the TTL output. The COUNT input has 500mV of hysteresis, allowing the use of slow risetime input signals.
9	9	STORE	When STORE is low, the counter's contents appear at the LED digit and segment outputs, and at the BCD outputs. When STORE goes high, the current count is latched into the display latch, and that latched data appears at the LED drive and BCD outputs. Store has an internal 25µA pullup.
10	10	UP/DOWN	The counter counts up with each rising edge of Count when UP/DOWN is high. Conversely, the counter decrements with each rising edge of Count when UP/DOWN is low. UP/DOWN must be set up 300 nanoseconds before the rising edge of Count, and must be held stable for 750 nanoseconds after the rising edge of Count. Transitions on UP/DOWN during the 750 nanoseconds after the rising edge of Count may erroneously increment or decrement the upper counter stages.

Pin Descriptions

PIN NUMBER		PIN NAME	FUNCTION
COMMON ANODE ICM7217 ICM7271B	COMMON CATHODE ICM7217A ICM7217C		
14	14	RESET	Driving RESET low resets the counter to 0000. RESET does not clear the display latch unless both RESET and STORE are low. Since the RESET operation is performed by placing 0 on the internal BCD data bus and presetting all four counter stages, simultaneous RESET and Load register operations will load 0000 into the comparison registers. To avoid erroneous loading of zeroes into the comparison register, do not take RESET low unless LOAD REGISTER has been low or floating for at least 5 milliseconds. The RESET input has an internal 25µA pullup, but it should be actively driven or pulled up with an external 4.7 kilohm when the ICM7217 is used in electrically noisy environments.
1	1	CARRY/BORROW	The CARRY/BORROW output is a short positive going pulse (typically 1µs long) that occurs at the 9999 to 0000 transition when counting up, and the 0000 to 9999 transition when counting down. The CARRY/BORROW output is used to drive the COUNT input of a second ICM7217 in an 8 digit counter.
2	2	ZERO	This output is low whenever the counter's contents are 0000, independent of the display latch contents. The ZERO output is not valid during a load counter operation (while LOAD COUNTER is high and for 5 milliseconds after LOAD COUNTER was high).
3	3	EQUAL	This output is low whenever the counter's contents equals the contents of the comparison register. This output is not valid during Load Counter and Load Register operations (while LOAD COUNTER or LOAD REGISTER is high, and for 5 milliseconds after either LOAD COUNTER or LOAD REGISTER was high).
13	13	SCAN	In most applications, the scan pin is left floating and the internal multiplex scan frequency of 2500Hz is used. Connecting a capacitor between V^+ and the SCAN pin lowers the multiplex oscillator frequency. If desired, the SCAN pin can be externally driven. The internal digit multiplex counter advances with each positive-going edge at SCAN, and the digit outputs are enabled only while the SCAN pin is low. LED display brightness can be controlled by varying the duty cycle at the SCAN input. The SCAN pin is internally disconnected and the internal oscillator is used during Load Counter and Load Register operations. This increases the scan frequency to 8kHz, reducing the time required for a load counter or load register operation.
23	20	DISPLAY CONTROL	This is a three-level input with internal 100 kilohm resistors which bias the pin to 2.5V when it is floating. Leading Zero Blanking is enabled when this pin is floated or driven to 2.5V. Leading Zero Blanking is inhibited when this pin is connected to Ground. The segment drivers are disabled and the LED display is blanked when this pin is connected to V^+. BCD outputs and digit outputs remain active.
11	11	LOAD REGISTER/OFF	This is a three-level input. Leave the pin floating or drive it to 2.5V for normal operation. Connect the LOAD REGISTER/OFF pin to ground to put the ICM7217 into the shutdown mode. This puts the segments drivers, the digit drivers, and the BCD I/O into a high impedance state. The ICM7217 will continue to count normally while in the shutdown mode. A high pulse (100ns minimum) starts the LOAD REGISTER operation. The SCAN pin is disconnected from external circuitry and the multiplex counter is reset to D4. The digits are then scanned in the sequence D4, D3, D2, D1; and the internal comparison register is loaded with the data present at the BCD I/O pins at the end of each digit period. At the end of the D1 digit period, the LOAD REGISTER is still high. If thumbwheel switches are connected as shown in Figure 1, the value on the thumbwheel switches is loaded into the comparison register.
12	12	LOAD COUNTER/ I/O OFF	The LOAD COUNTER/I/O OFF pin is a three-level input. Leave it floating or drive it to 2.5V for normal operation. Connecting LOAD COUNTER/I/O OFF to ground puts the BCD output into a high impedance state, but does not affect the LED drive outputs. A high pulse (100ns minimum) starts the LOAD COUNTER operation. The LOAD COUNTER operation presets counter contents to the value on the thumbwheel switches (Figure 1), in the same manner as the load register operation described above.



ICM7217/COUNT and Output Timing

SYM.	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{UCS}	UP/$\overline{DOWN}$ setup time (min.)		300		ns
t_{UCH}	UP/$\overline{DOWN}$ hold time (min.)		750		ns
t_{CWH}	COUNT pulse high (min.)		100	250	ns
t_{CWL}	COUNT pulse low (min.)		100	250	ns
t_{CB}	COUNT to CARRY/ BORROW delay		750		ns
t_{BW}	CARRY/ BORROW pulse width		100		ns
t_{CEI}	COUNT to $\overline{EQUAL}$ delay		500		ns
t_{CZI}	COUNT to $\overline{ZERO}$ delay		300		ns

Typical Applications

Four Digit, Preset and Predetermining Counter

The test circuits, Figures 1 and 2, are complete four digit up/down counters with preset and predetermining (comparison) capability. Momentarily pressing the Load Counter switch will preset the counter to the number set into the thumbwheel switches. Similarly, momentarily pressing the Load Register switch will load the predetermining or comparison register with the number set into the thumbwheel switches.

When the Store switch is closed, the displayed count follows the counter. Opening the Store switch "freezes" the display at the current count. Closing the Reset switch at any time clears the counter to 0000.

The ZERO output goes low whenever the counter content is 0000, and the EQUAL output goes low whenever the count reaches the value in the predetermining or comparison register.

Eight Digit Counter

The CARRY/BORROW output is used to cascade two 4 digit counter sections to form an eight digit counter. If leading zero blanking is desired, drive the Display Control pin of the least significant ICM7217 with an NPN transistor whose base is connected to the Zero output of the most significant ICM7217.

Multiple Setpoints

Analog switches such as the CD4066 can drive the BCD I/O pins. In Figure 3, the number set on thumbwheel switch A is loaded into the comparison register, the number on thumbwheel switch B presets the counter.

Trailing Zero Display

In some applications leading zero blanking is desired, but a count of 0000 must result in a display of a single 0 in the rightmost digit. Figure 4 performs this task by driving Display Control to the "disable leading zero blanking" state whenever digit D1 is active.

Batch Counter or Divide by N Counter

The circuit of Figure 5A will put out a pulse each time the count reaches the number loaded into the comparison register.

RESET is taken low each time the count reaches the preset number, resetting the counter to 0000. The AND gate is used for feedback to RESET, since a simple RC circuit can "lockup" if the comparison register is loaded with 0000.

Figure 5B is a similar circuit, except that the counter counts down, and is preset each time the count reaches zero. Since the Load Counter (preset) operation may take as long as 5 milliseconds, this circuit should be used only with signals of 12,000 counts per minute (200Hz) or less.

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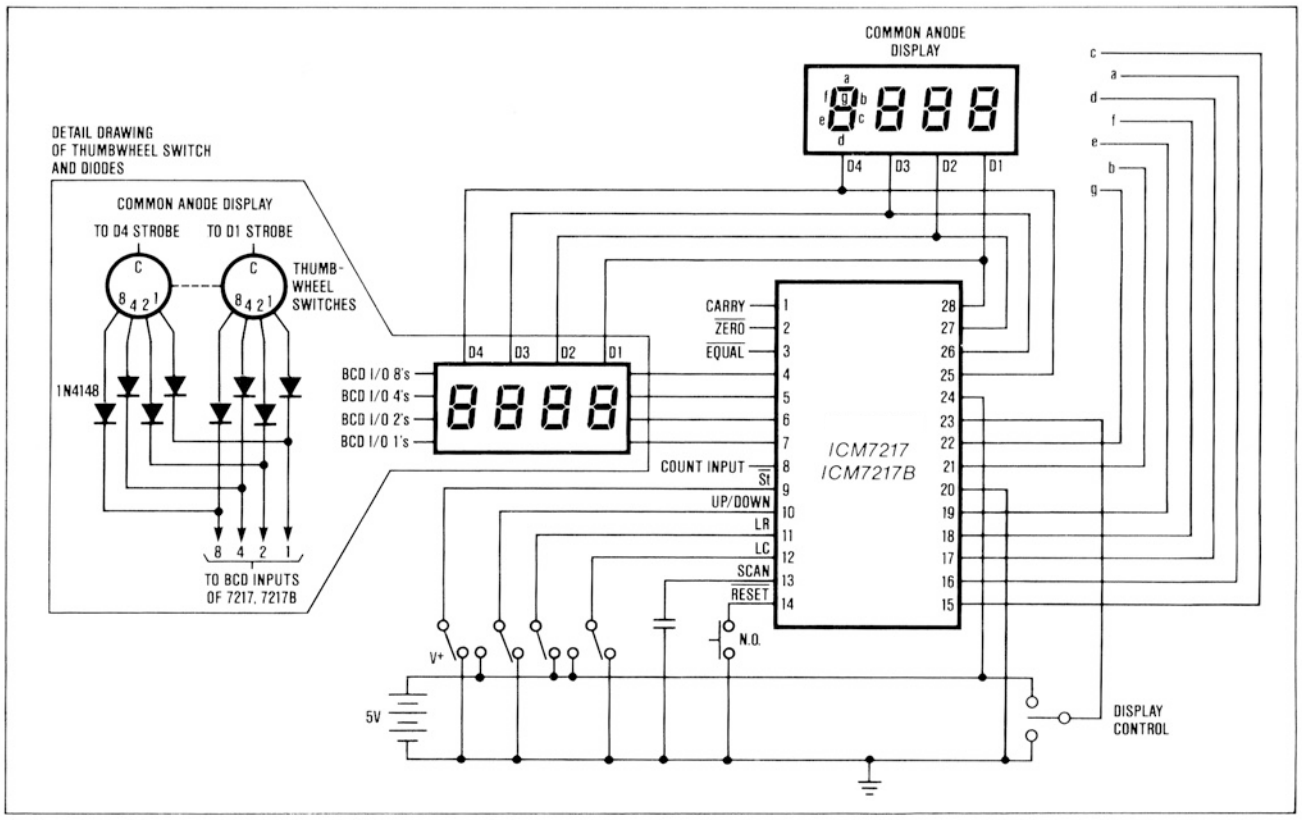


Figure 1. Basic Up/Down Counter with Common Anode LED Display.

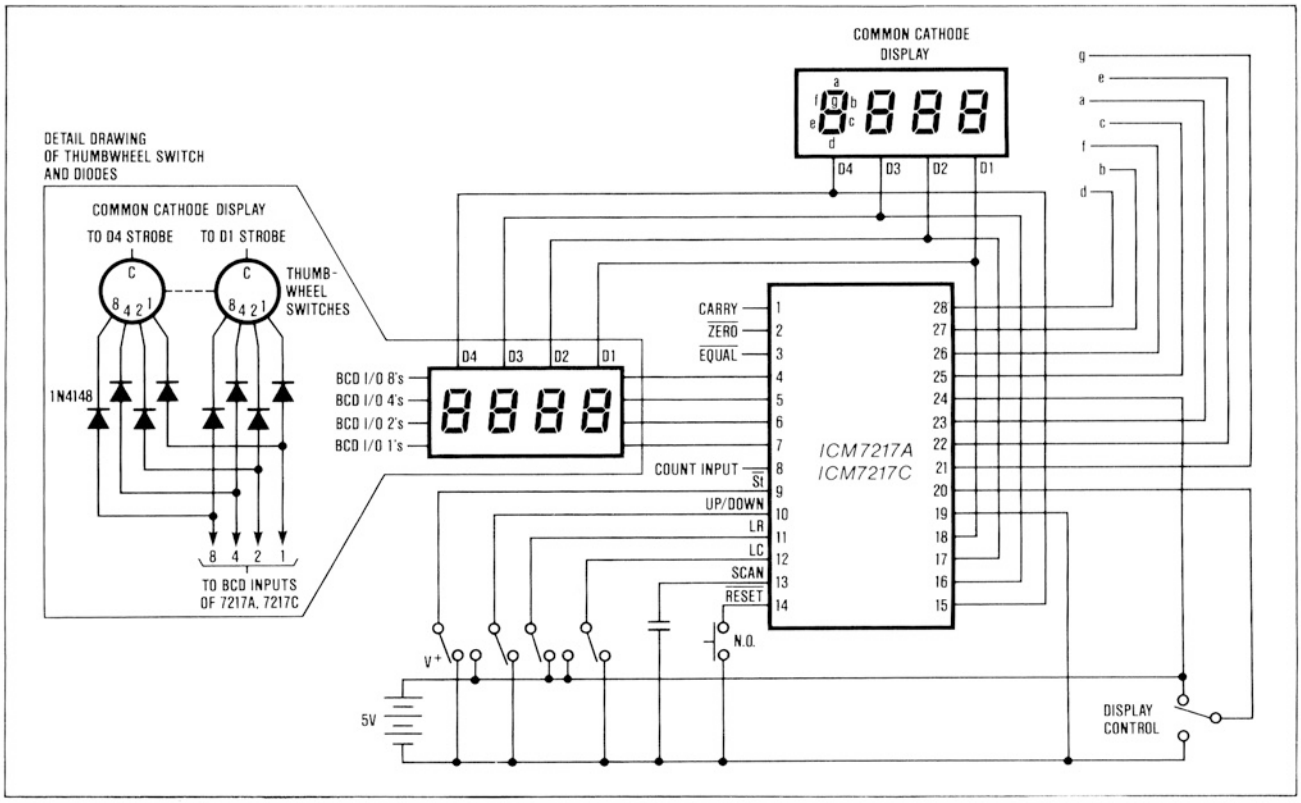


Figure 2. Basic Up/Down Counter with Common Cathode LED Display.

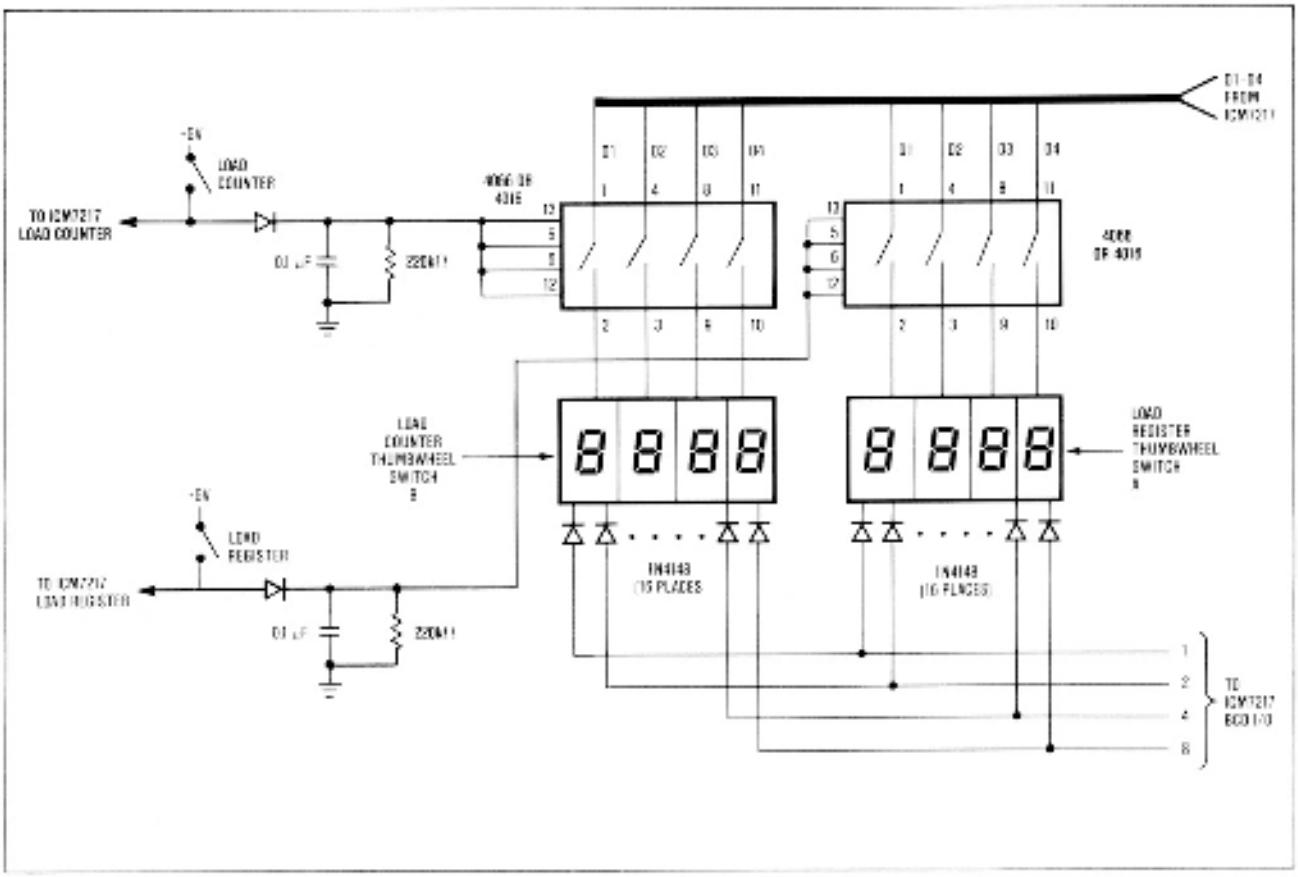


Figure 3. Multiple Thumbwheel Switches

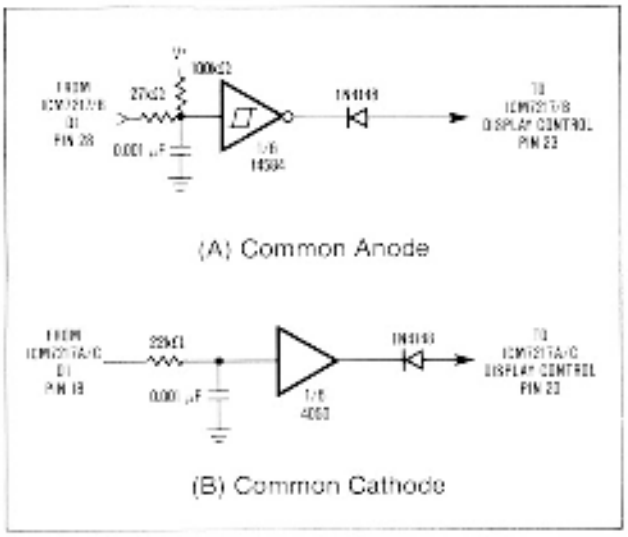


Figure 4. Trailing Zero Display

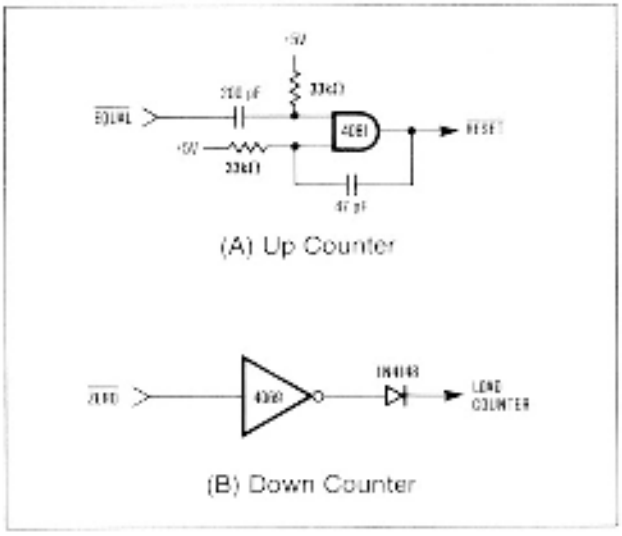


Figure 5. Connections for Divide-By-N Batch Counters.

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Application Hints

1. Use a minimum of 47µF in parallel with a 0.1µF ceramic bypass capacitor between V^+ and ground, in the immediate vicinity of the ICM7217. This bypassing is required to reduce the power supply ripple created by the high current multiplexed LED drive signals.
2. Use the Common Anode versions (ICM7217 and ICM7217B) where the brightest LED display is desired.
3. The SCAN pin can be used to control digit sequencing while reading BCD output data with a microprocessor, but the SCAN pin is disconnected and the multiplex rate is increased to 2kHz during the load register and load counter operations.
4. Load counter and load register operations continue for up to 5 milliseconds after the LOAD COUNTER or LOAD REGISTER pin has returned to the floating state. During this 5 millisecond period, RESET will load a zero into some or all of the digits of the counter or register. EQUALS and ZERO are not valid during this loading period, and the counter is inhibited during the load counter operation.
5. If the UP/DOWN input changes state during the 750ns after a positive transition at COUNT, the upper digits of the counter may be erroneously incremented or decremented. This is caused by the transmission of erroneous carry/borrow signals to adjacent digits when major bit changes occur in a digit counter coincident with an up/down input transition.

Pin Configuration

Top View



6. If the 200ns STORE high to RESET low setup time is not met, RESET may clear some of the bits in the display latch.
7. Data cannot be transferred directly from the counter to the comparison register. Use a 74C915 7-segment-to-BCD reverse decoder between the segment outputs and the BCD inputs.

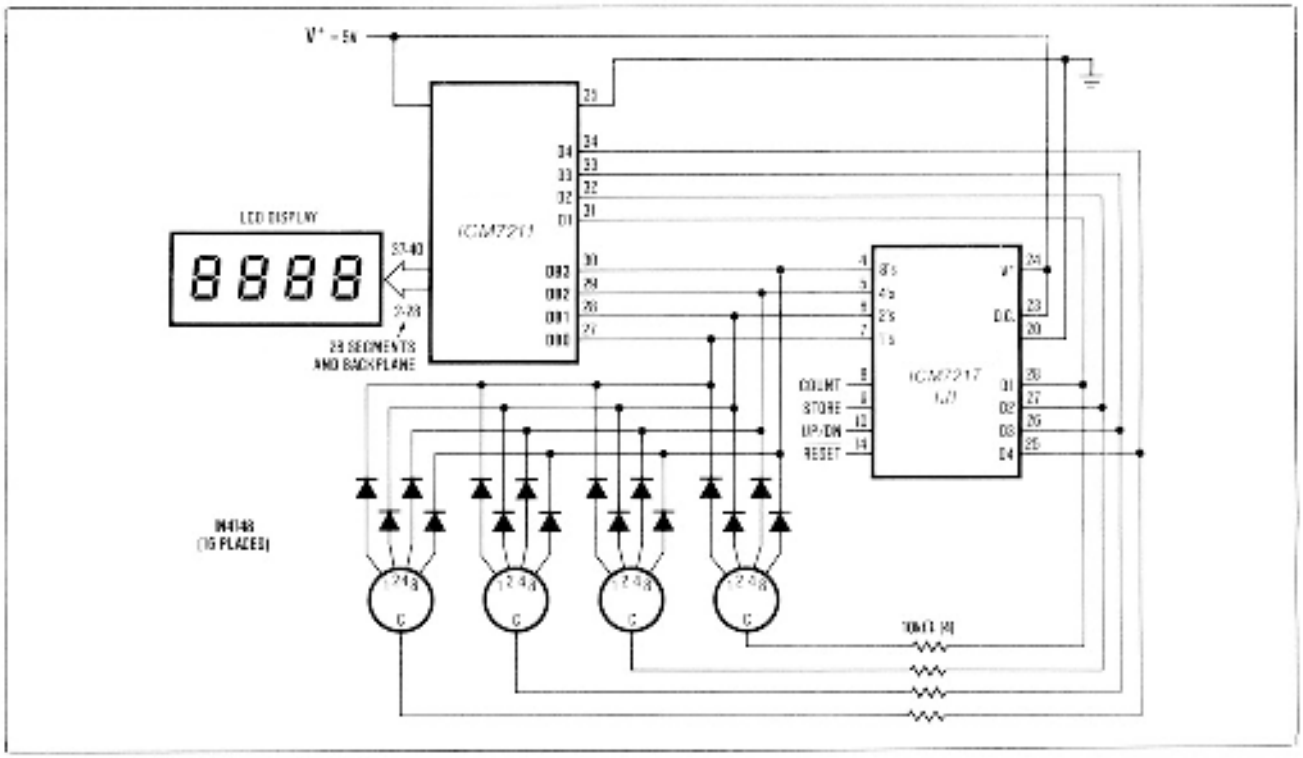


Figure 7. LCD interface using ICM7211

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