SMPS IC

SmartRectifier
IR1161LPBF

SmartRectifier Control IC

Features

- Secondary side synchronous rectification controller
- DCM, CrCM Flyback and resonant half-bridge topologies
- Direct sensing of MOSFET drain voltage up to 200V
- Max 500kHz switching frequency
- Anti-bounce logic and UVLO protection
- Micropower start-up & ultra-low quiescent current
- 50ns turn-off propagation delay
- Programmable Minimum On Time
- Vcc Operating voltage range 4.75V to 18V
- Cycle by Cycle MOT Check Circuit
- Lead-free
- Compatible with 0.3W Standby, Energy Star, CECP, etc.

Applications

- Charger, AC-DC adapters

Product Summary

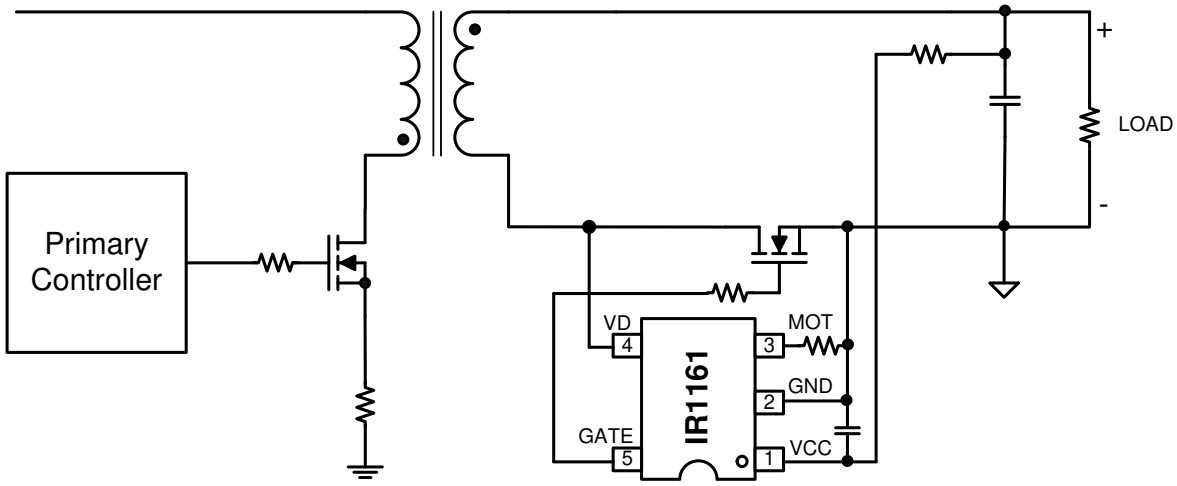
Topology	Flyback, Resonant Half-bridge
VD	200V
V_{CC}	4.75V ~ 18V
I_{o+} & I_{o-}	+1A & -2.5A
Turn on Propagation Delay	50ns (typical)
Turn off Propagation Delay	50ns (typical)

Package Options



5-Pin SOT-23

Application Diagram



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IR1161LPBF	5L-SOT-23	Tape and Reel	3000	IR1161LTRPBF

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Description

The IR1161 is a synchronous rectification control IC designed to drive an N-Channel power MOSFET in a secondary output rectifier circuit. The MOSFET gate is switched on and off to bypass its body diode during the of the conduction period to minimize power dissipation, remaining off during the blocking period. The drain to source voltage is accurately sensed to determine the direction and magnitude of the current allowing the IR1161 to turn the MOSFET on and off at close to zero current.

An integrated cycle-by-cycle minimum on time (MOT) protection circuit automatically detects a no load condition and turns off the gate driver output preventing negative current from flowing through the MOSFET.

Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression, which allows reliable operation in all operating modes.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any pin. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	Remarks
V_{CC}	Supply Voltage	-0.3	20	V	
V_D	Cont. Drain Sense Voltage	-1	200		
V_D	Pulse Drain Sense Voltage	-3	200		
V_{MOT}	MOT Voltage	-0.3	3.5		
V_{GATE}	Gate Voltage	-0.3	V_{CC}+0.3		V_{CC}=18V, Gate off
T_J	Operating Junction Temperature	-40	150	°C	
T_S	Storage Temperature	-55	150		
$R_{\theta JA}$	Thermal Resistance	—	212†	°C/W	
P_D	Package Power Dissipation	—	590†	mW	T_{AMB}=25°C

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Supply voltage	4.75	18	V
V_D	Drain Sense Voltage	-3 ††	200	
T_J	Junction Temperature	-40	125	°C
Fsw	Switching Frequency	—	500	kHz

†† V_D -3V negative spike width ≤100ns

Recommended Component Values

Symbol	Component	Min.	Max.	Units
R_{MOT}	MOT pin resistor value	5	100	kΩ
CV_{CC}	V_{CC} decoupling capacitor value	1	—	µF

Electrical Characteristics

V_{CC}=12V and T_A=25°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to GND pin.

Symbol	Definition	Min.	Typ.	Max.	Units	Remarks
Supply Section						
V_{CC}	Supply Voltage Operating Range	4.75	—	18	V	
$V_{CC\ ON}$	V_{CC} Turn On Threshold	4.25	4.5	4.75		
$V_{CC\ UVLO}$	V_{CC} Turn Off Threshold (Under Voltage Lock Out)	4.15	4.4	4.65		
$V_{CC\ HYST}$	V_{CC} Turn On/Off Hysteresis	—	0.1	—		
I_{CC}	Operating Current	—	5.0	8.0	mA	C_{LOAD}=1nF, f_{SW}=300kHz
I_{QCC}	Quiescent Current	—	0.65	1.1		RMOT=50k
$I_{CC\ START}$	Start-up Current	—	10	50	µA	V_{CC}= $V_{CC\ ON}$ - 0.1V
Comparator Section						
V_{TH1}	Turn-off Threshold	-8	-4	0	mV	V_{CC}=5V to 15V
V_{TH2}	Turn-on Threshold	-263	-230	-197		
V_{HYST}	Hysteresis	—	230	—		
I_{IBIAS1}	Input Bias Current	-10	-7.5	—	µA	V_D=-50mV
I_{IBIAS2}	Input Bias Current	—	7	30		V_D=200V
One-Shot Section						
t_{BLANK}	Blanking Pulse Duration	8	13	24	µs	
V_{TH3}	Reset Threshold	1.06	1.18	1.31	V	
t_{BRST}	Blanking Time of Reset	—	400	—	ns	
V_{HYST3}	Hysteresis	—	70	—	mV	GBD
Minimum On Time Section						
T_{ONmin}	Minimum On Time	80	100	120	ns	RMOT=5k
		400	500	600	ns	RMOT=24k
		0.8	1	1.2	µs	RMOT=50k

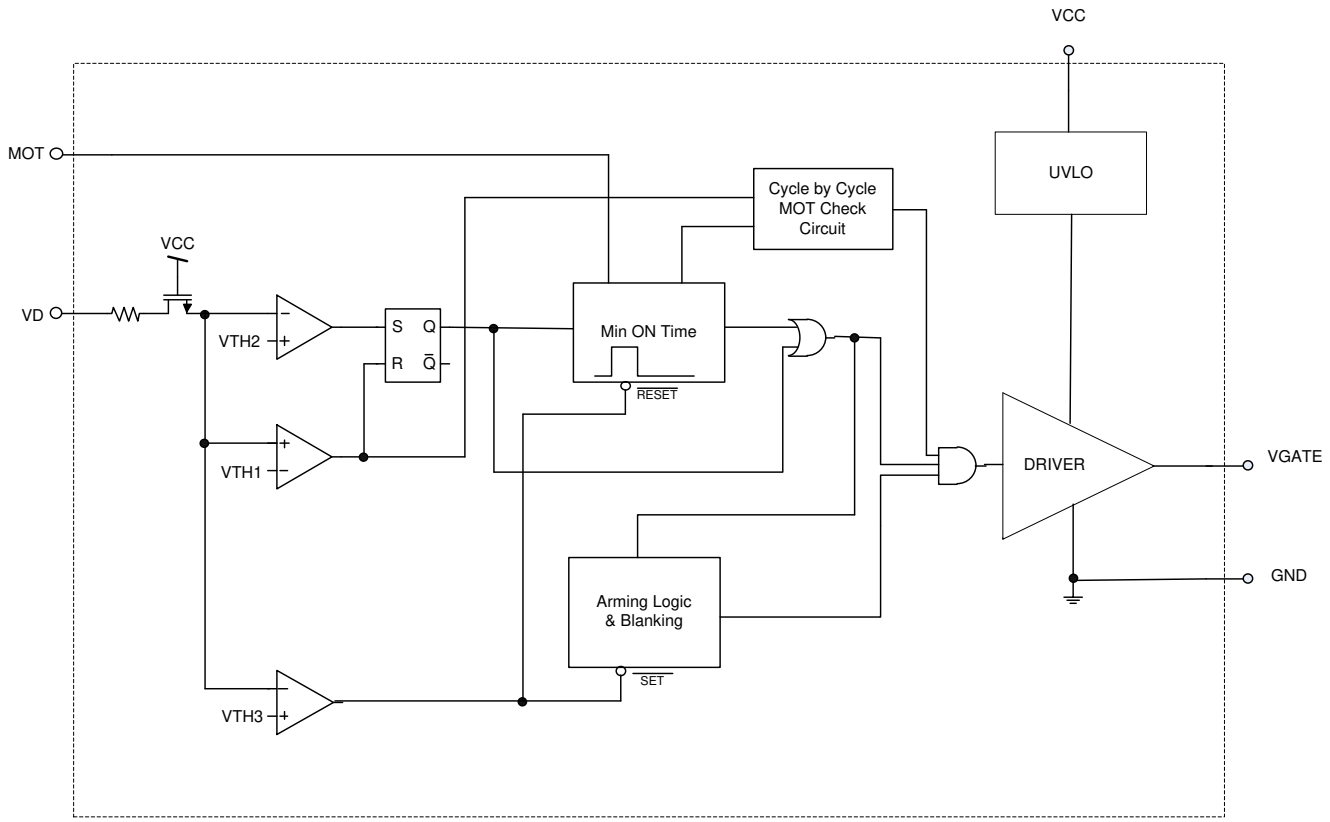
Electrical Characteristics

V_{CC}=12V and T_A=25°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to GND pin.

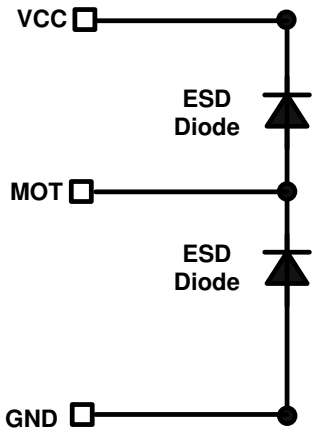
Symbol	Definition	Min.	Typ.	Max.	Units	Remarks
Gate Driver Section						
V_{GLO}	Gate Low Voltage	—	0.2	0.4	V	I_{GATE}=100mA, V_{CC}=12V
V_{GTH}	Gate High Voltage	11.5	11.9	V_{CC}		V_{CC}=12V, I_{GATE}=5mA
		4.5	4.9	V_{CC}		V_{CC}=5V, I_{GATE}=5mA
t_r	Rise Time	—	20	—	ns	C_{LOAD}=1nF, V_{CC}=12V
t_f	Fall Time	—	13	—		C_{LOAD}=1nF, V_{CC}=12V
t_{Don}	Turn on Propagation Delay	—	60	90		V_{DS} to V_{GATE} – V_{DS} goes down from 6V to -1V
t_{Doff}	Turn off Propagation Delay	—	50	60		V_{DS} to V_{GATE} – V_{DS} goes up from -1V to 6V
r_{up}	Pull up Resistance	—	9	—	Ω	I_{GATE}=100mA
r_{down}	Pull down Resistance	—	2	—		I_{GATE}=-100mA
$I_{O\ source}$	Output Peak Current (source)	—	1	—	A	GBD
$I_{O\ sink}$	Output Peak Current (sink)	—	2.5	—		GBD

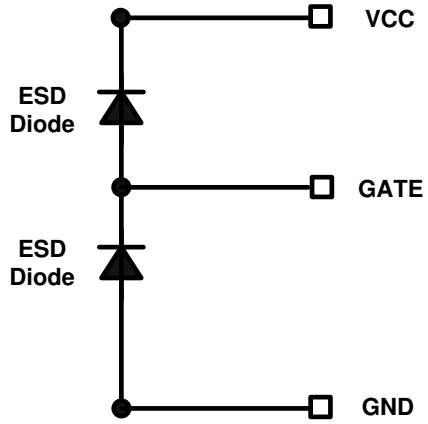
GBD – parameter is guaranteed by design and is not tested.

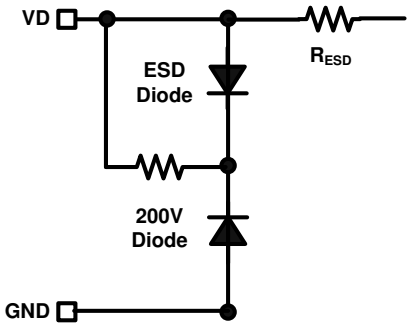
Functional Block Diagram



I/O Pin Equivalent Circuit Diagram



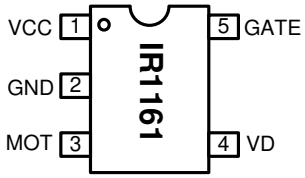




Pin Definitions

PIN#	Symbol	Description
1	VCC	Supply Voltage
2	GND	Ground
3	MOT	Minimum On Time Program Input
4	VD	FET Drain Sensing
5	GATE	Gate Drive Output

Pin Assignments



Detailed Pin Description

VCC: Power Supply
The supply voltage pin is monitored by the under voltage lockout circuit. It is possible to turn off the IC entering UVLO mode by pulling this pin below the minimum turn off threshold voltage for micro power consumption.
To avoid noise problems a bypass ceramic capacitor connected to Vcc and GND is needed, which should be placed as close as possible to the IC. A low value series resistor to Vcc may also be added if extra filtering is required. This pin is internally clamped to 20V.

GND: Ground
This is the IC ground reference connected to the SR MOSFET source.

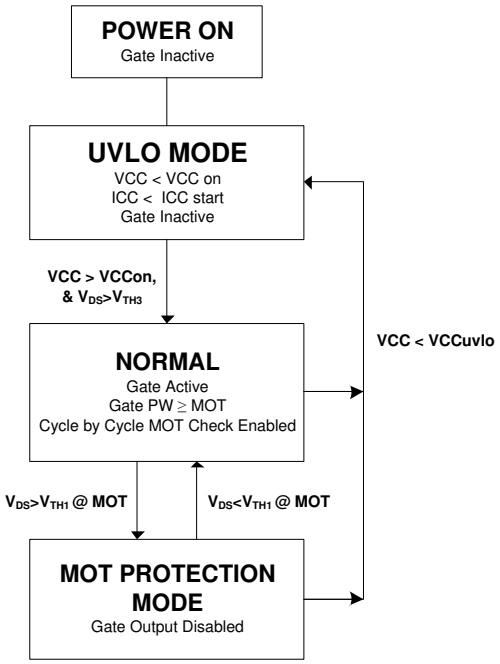
MOT: Minimum On Time
The MOT programming pin controls the amount of minimum on time. Once V_{TH2} is crossed for the first time, the gate signal will transition high and turn on the power MOSFET. Spurious ringing and oscillations can falsely trigger the input comparator to switch the output off. The MOT prevents this by blanking the input comparator to keep the SR MOSFET on for a minimum time. The MOT is typically programmed between 500ns and 2us by using an external resistor referenced to GND.

VD: Drain Voltage Sense
VD is the voltage sense pin for the SR MOSFET drain. This is a high voltage pin therefore particular care must be taken in properly routing the connection.
An additional RC filter can be placed at this input to improve noise immunity, however only small values (e.g. 100Ω + 100pF) may be used to avoid introducing significant delay to the control input.

GATE: Gate Drive Output
The gate drive output provides 1A source and 2.5A sink current capability. Although this output may be directly connected to the power MOSFET gate the use of a minimal gate resistor is recommended, especially when using multiple MOSFETs in parallel.
Care must be taken to keep the gate loop as short and as small as possible in order to minimize inductance and achieve optimal switching performance.

Application Information and Additional Details

State Diagram



UVLO Mode

The IC remains in the under-voltage lockout condition until VCC exceeds the turn on threshold voltage, $V_{CC\ ON}$. During the time the IC remains in the UVLO state, the gate drive circuit is inactive and only a very small quiescent current $I_{CC\ START}$ is consumed. UVLO mode is accessible from any other operating state whenever VCC < $V_{CC\ UVLO}$.

Normal Mode and Synchronized Enable Function

The IC enters into normal operating mode once the UVLO voltage has been exceeded. When the IC enters the Normal Mode, the GATE output remains disabled (stays low) for a start-up delay time in the range of 100us, then V_{DS} must transition above V_{TH3} two times to enable synchronous rectification. This ensures that the GATE output can never be enabled in the middle of a switching cycle. The first gate pulse after activation is blocked and the cycle by cycle MOT protection circuit is enabled. This logic avoids reverse currents through the SR MOSFET from occurring during startup. The gate will continuously drive the SR MOSFET after completing this startup sequence.

MOT Protection Mode

If the secondary current conduction time is shorter than the MOT (Minimum On Time), the following driver output pulse is disabled. This function can avoid reverse current from occurring when the system is switching at very low duty-cycles under very light or zero load conditions. System standby power consumption is reduced by disabling the GATE output. The cycle by cycle MOT check circuit is always activated under Normal Mode and MOT Protection Mode so that the IC will automatically resume normal operation only once the load increases to a level where the secondary current conduction time exceeds MOT.

General Description

The direction of the rectified current in the SR MOSFET is sensed by the IR1161 through its high voltage drain sensing input VD, which monitors the drain to source voltage drop. Conduction occurs through the body diode when the MOSFET is switched off and when it is switched on, the R_{DSon} acts as a shunt resistance. The GATE drive to the MOSFET is switched on only when current is flowing from source to drain. Internal blanking logic is used to prevent spurious transitions and guarantee correct operation under different load conditions.

The IR1161 is suitable for DCM or CrCM Flyback and Resonant Half-Bridge topologies.

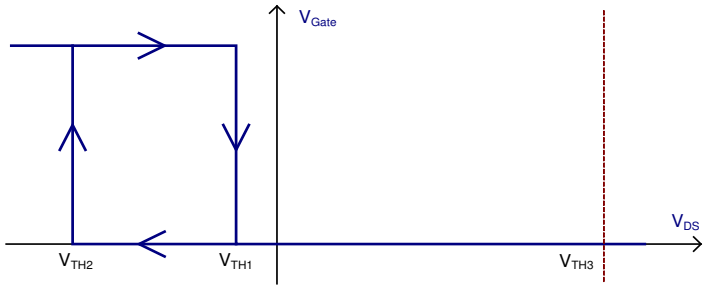


Figure 1: Input comparator thresholds

Flyback Application

The typical application circuit of IR1161 in Flyback converter is shown on page 1.

Turn-on phase

When the conduction phase of the SR MOSFET is initiated, current will start flowing through its body diode producing a negative V_{DS} voltage across it. The body diode has a much higher forward voltage drop than that created by the MOSFET on resistance and will therefore becoming more negative than the turn-on threshold V_{TH2}.

At that point the IR1161 will drive the gate high, which will in turn cause V_{DS} to transition to a much smaller negative voltage. This voltage step is usually accompanied by some amount of ringing that could potentially trigger the IR1161 to turn off prematurely. To prevent this, a Minimum On Time (MOT) blanking period is maintains the SR MOSFET on for a minimum period of time, which is externally adjustable.

Turn-off phase

At the end of the conduction period the current reduces to zero, causing V_{DS} to cross the turn-off threshold V_{TH1}. The IR1161 will then turn the SR MOSFET gate off and current will start flowing again through the body diode causing a negative going V_{DS} voltage step. Depending on the amount of residual current, V_{DS} could potentially trigger the turn on threshold once again. For this reason V_{TH2} is blanked for a certain amount of time (T_{BLANK}) after V_{TH1} has been triggered. The blanking time is internally set and is reset only by V_{DS} crossing the positive threshold V_{TH3} and remaining above this threshold for more than reset blanking time t_{BRST}. Once reset the IR1161 is ready for next conduction cycle.

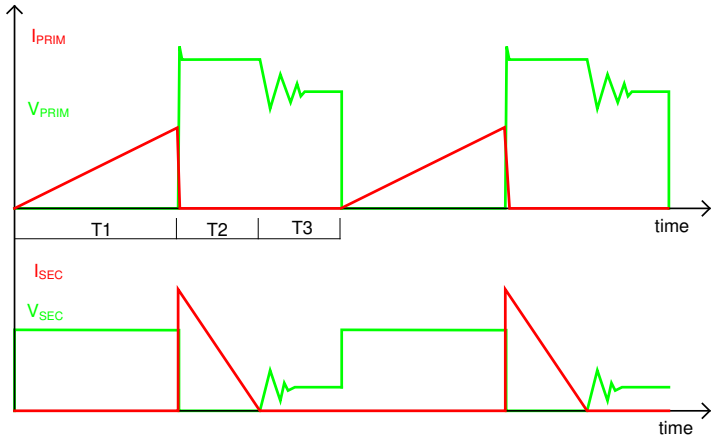


Figure 2: Flyback Primary and secondary currents and voltages for DCM mode

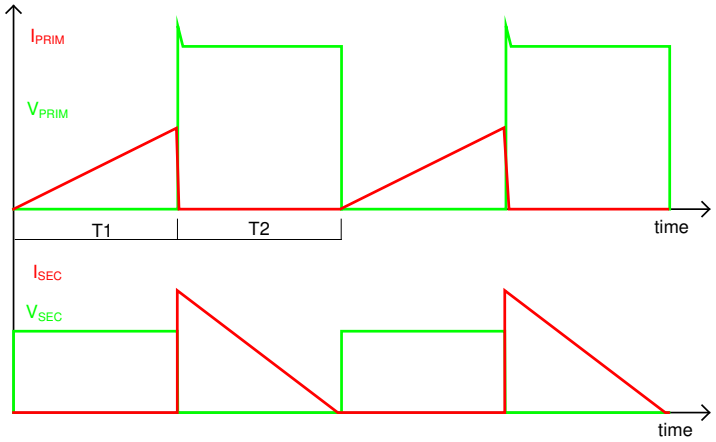


Figure 3: Flyback Primary and secondary currents and voltages for CrCM mode

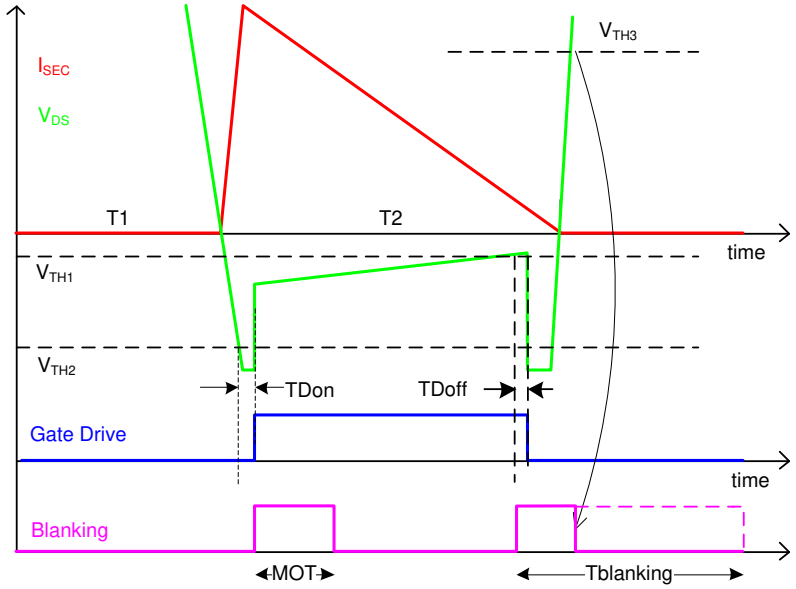


Figure 4: Flyback secondary side DCM/CrCM operation

Resonant Half-Bridge Application

The typical application circuit of IR1161 in LLC half-bridge is shown in Figure 5.

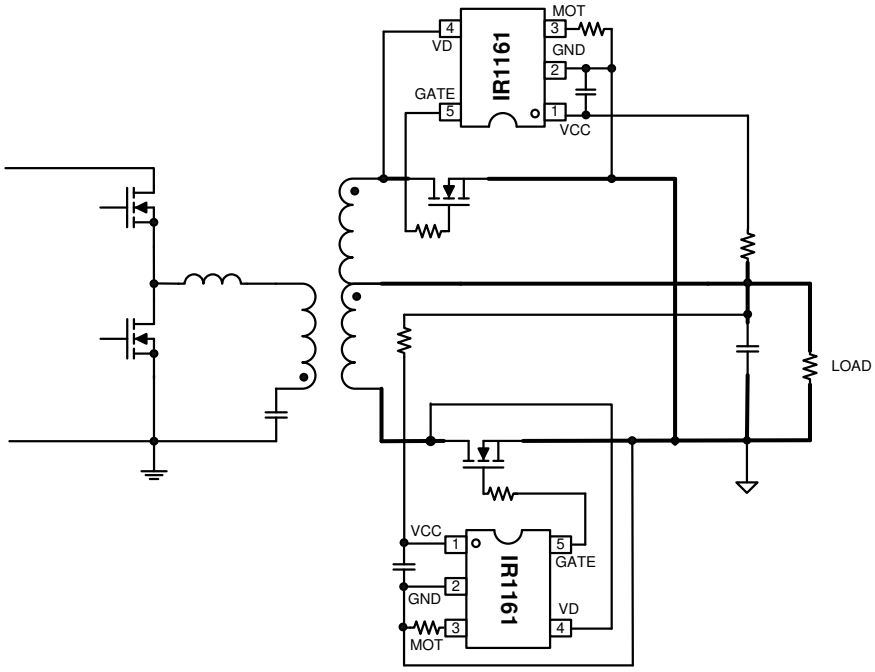


Figure 5: Resonant half-bridge application circuit

In the resonant half-bridge converter the turn-on phase and turn-off phase are similar to the Flyback except that the current shape is sinusoidal. The typical operating waveform is seen below in figure 6.

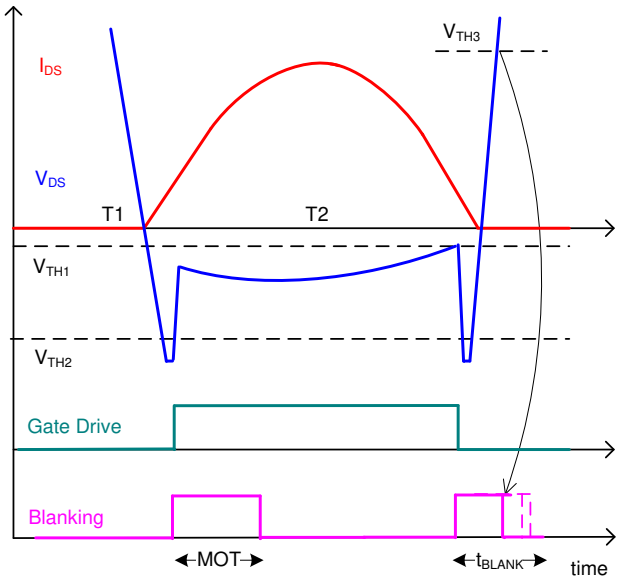


Figure 6: Resonant half-bridge operation waveform

Setting the MOT Time

The MOT time is set by an external resistor connected from the MOT pin to GND.

$T_{MOT} = 2 \times 10^{-11} \times R_{MOT}$

MOT Protection Mode

The MOT protection function is designed to avoid reverse current occurring in the SR MOSFET. This could happen at light load if the MOT time is set longer that the actual conduction time. The IR1161 disables the gate drive output in MOT protection mode as described in the previous section and automatically resumes normal operation when the load increases to a level where the current conduction time is longer than MOT.

This function works in both Flyback and resonant half-bridge topologies. Figure 7 illustrates operation in a DCM Flyback converter.

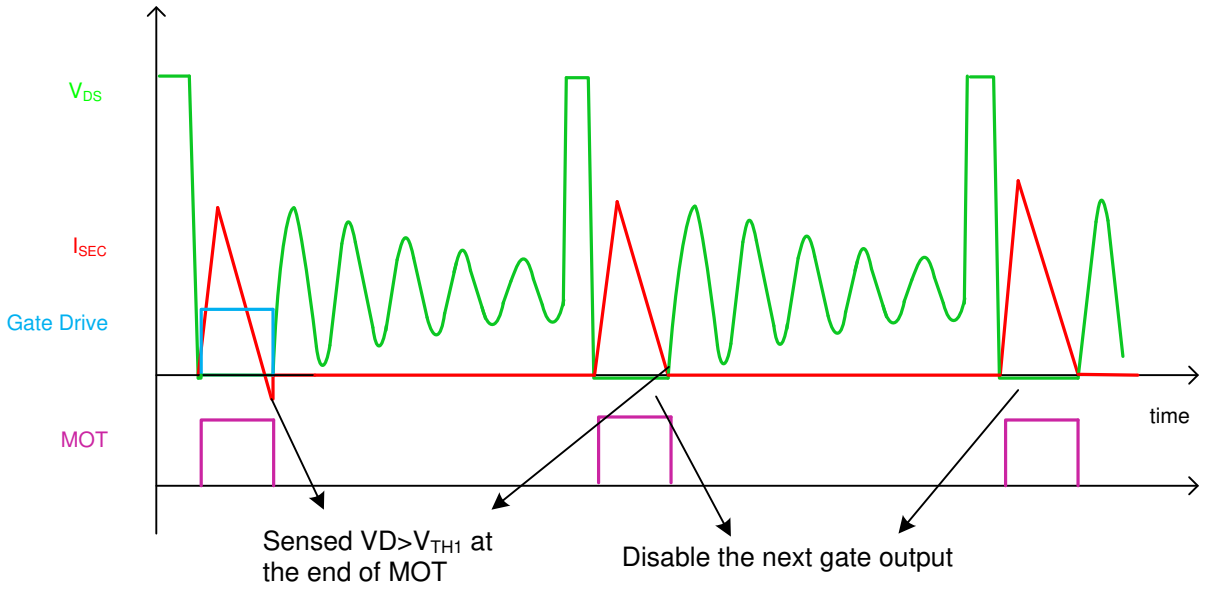


Figure 7: MOT Protection Mode

Synchronized Enable Function

This function guarantees that the GATE drive always switches high at the beginning of a switching cycle. This is essential since mid-cycle switch on with the MOT function would force the MOSFET to remain on past the conduction period leading to reverse conduction.

This function works in both Flyback and resonant half-bridge topologies. Figure 8 is an example in resonant half-bridge converter.

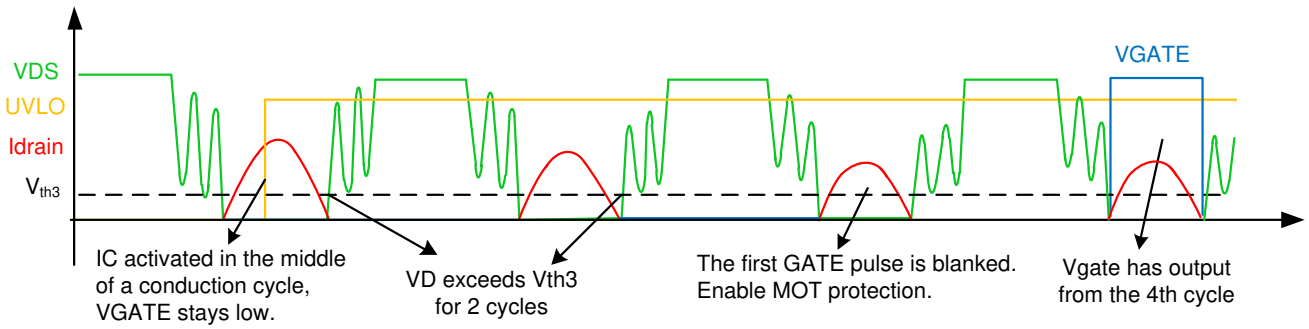


Figure 8: Synchronized Enable Function (resonant half-bridge)

Driving a Logic Level MOSFET

An external gate drive pull down circuit is recommended when driving a logic level MOSFET.
This is because during power up and power down the drain may be switching while the IR1161 remains in UVLO.
SR MOSFET drain to gate capacitance causes voltage pulses to appear at the gate that could have sufficient amplitude to reach the turn on threshold because the IR1161 gate sink capability is limited when VCC < 2V.
The following circuit ensures that the gate voltage remains below 1V under all conditions:

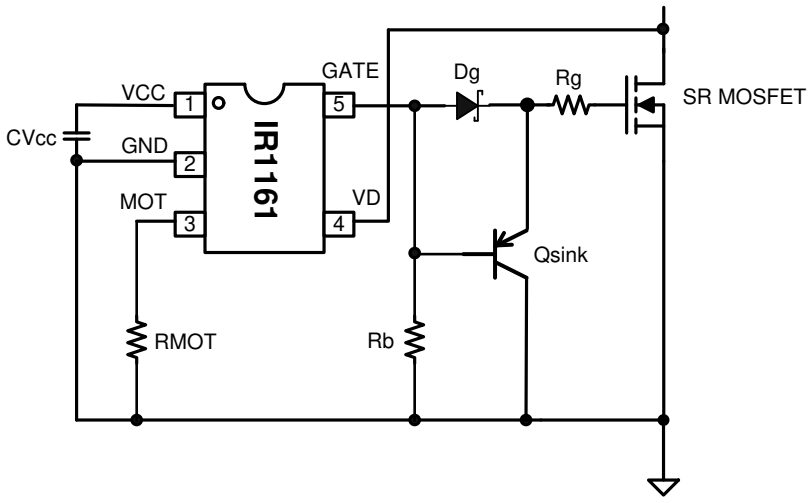


Figure 9: Gate drive circuit for logic level SR MOSFET

Vcc Clamping Circuit

The IR1161 can be directly biased by the converter output voltage V_{OUT} if this falls within the recommended range of Vcc although a low value series resistor may be required for optimal noise filtering. For higher system output voltages a clamping circuit is recommended to limit Vcc. This also lowers the gate drive voltage and reduces losses if V_{OUT} is above 15V.

Many clamping circuits are available from simple zener diode clamping to bipolar linear regulators. Figure 10 is one example; in this circuit the Vcc voltage will be clamped to a voltage of V_{OUT} - V_{ZD1} - V_{BE}. The circuit also provides turn-on delay to the IR1161, which will activate only when the output voltage exceeds V_{CCON} + V_{ZD1} + V_{BE}. R1 and R2 are optional for more precise control of the Vcc clamping voltage.

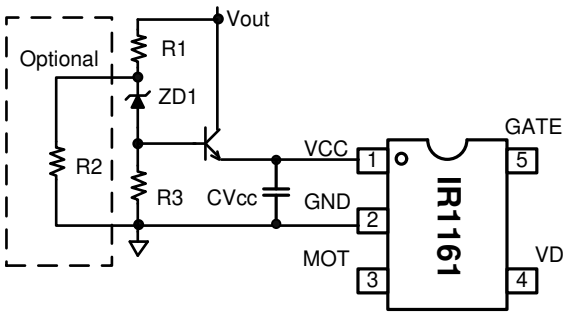


Figure 10: Vcc clamping circuit

Shutdown Circuit

The IR1161 can be disabled by pulling V_{CC} below the $V_{CC\ UVLO}$ threshold.

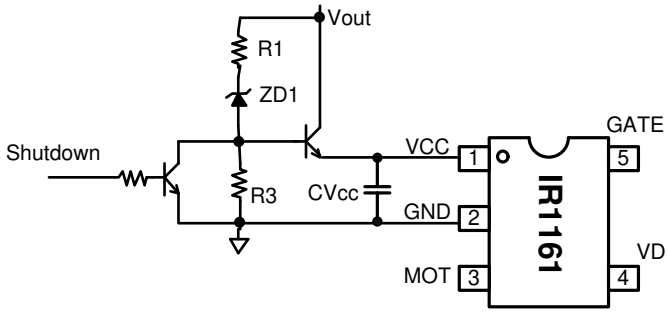


Figure 11: IR1161 Enable/Disable circuit

General Timing Waveform

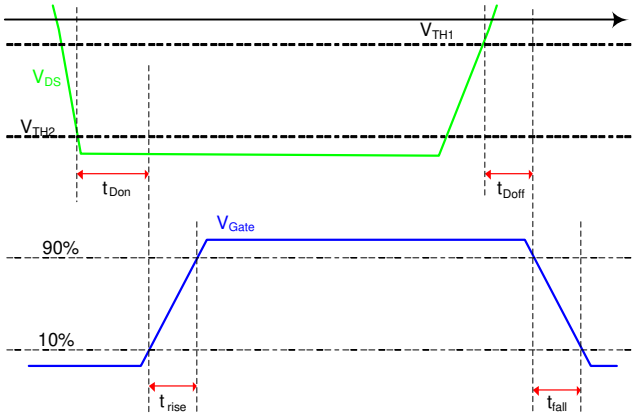


Figure 12: Timing waveform

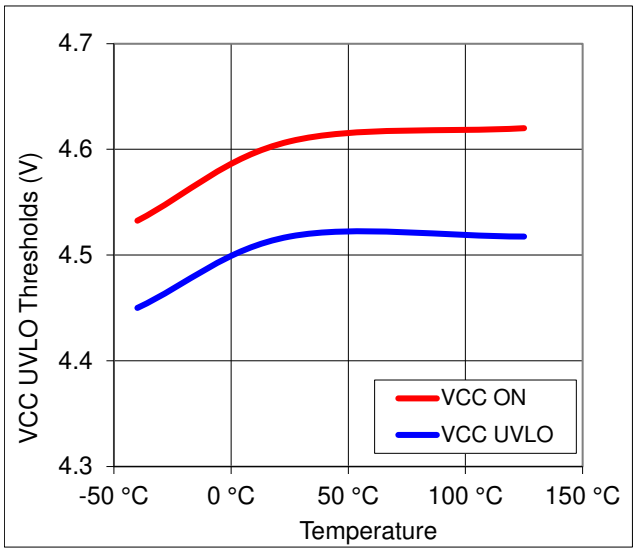


Figure 13: Undervoltage Lockout vs. Temperature

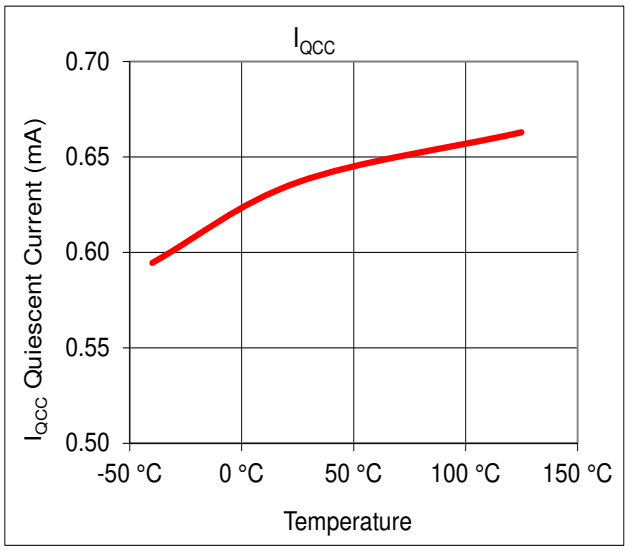


Figure 14: Icc Quiescent Current vs. Temperature

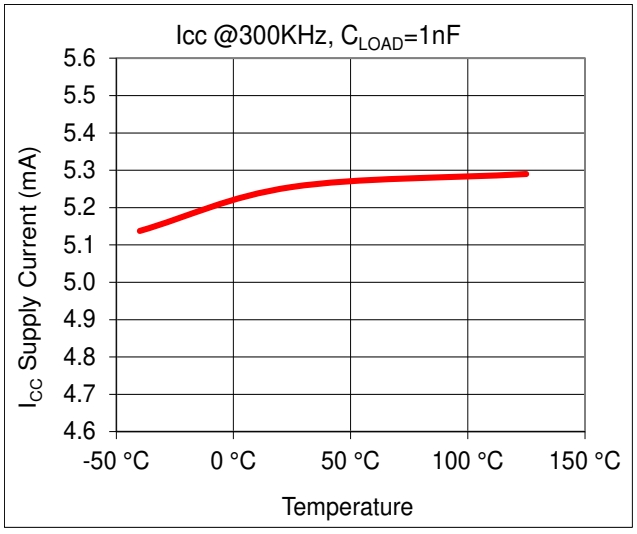


Figure 15: Icc Supply Current @1nF Load vs. Temperature

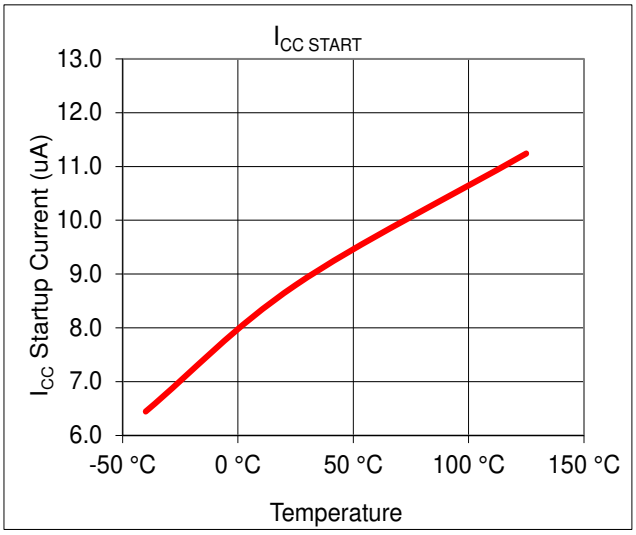


Figure 16: Icc Startup Current vs. Temperature

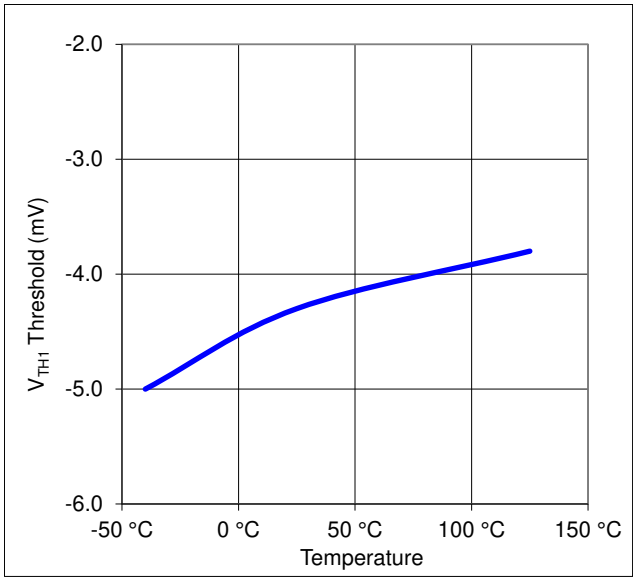


Figure 17: V_{TH1} vs. Temperature

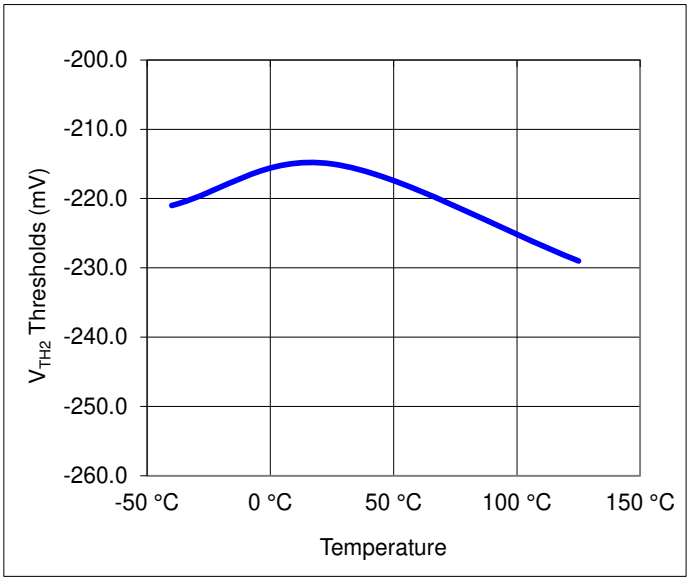


Figure 18: V_{TH2} vs. Temperature

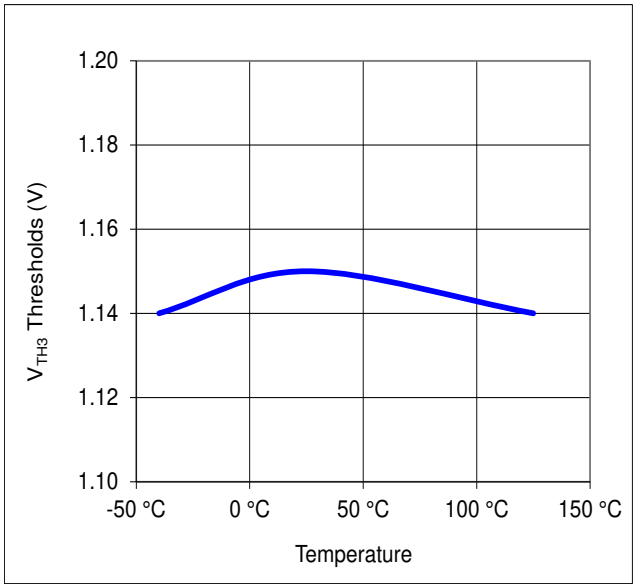


Figure 19: V_{TH3} vs. Temperature

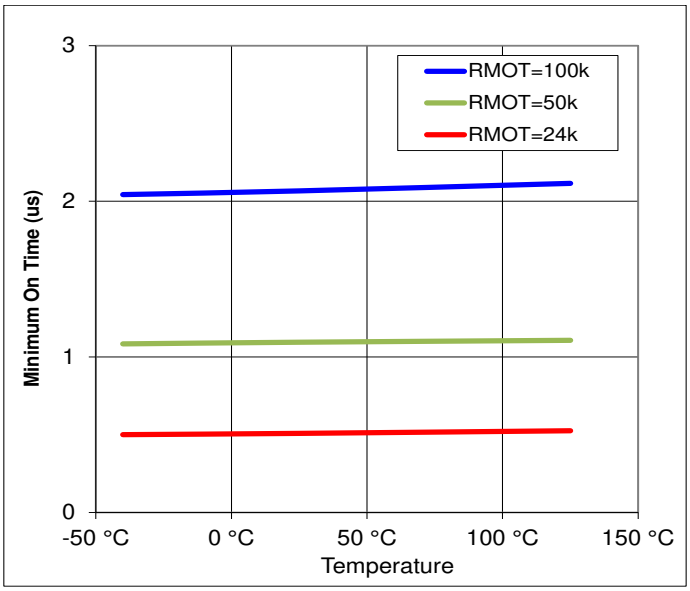


Figure 20: MOT Time vs. Temperature

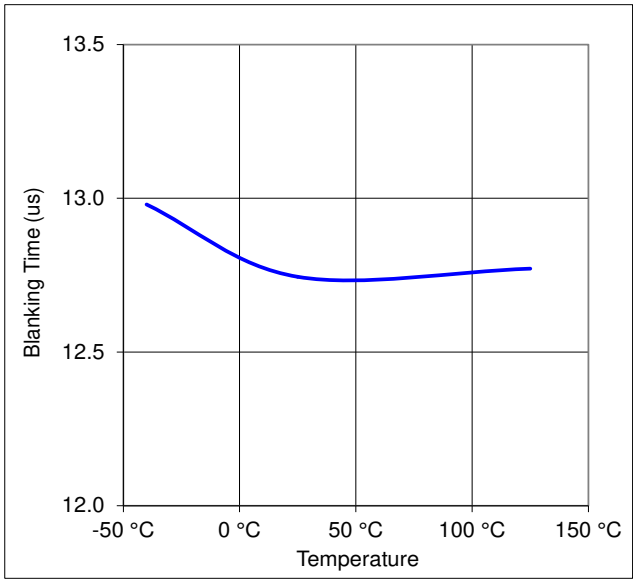


Figure 21: Blanking Time vs. Temperature

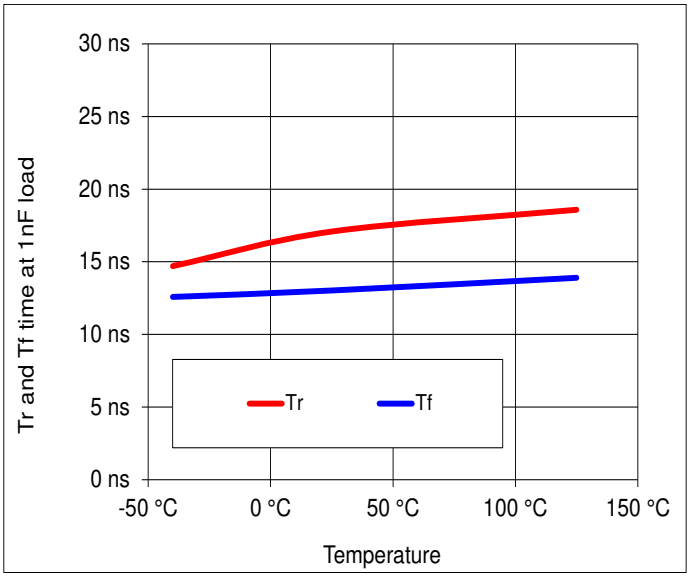


Figure 22: Tr and Tf vs. Temperature

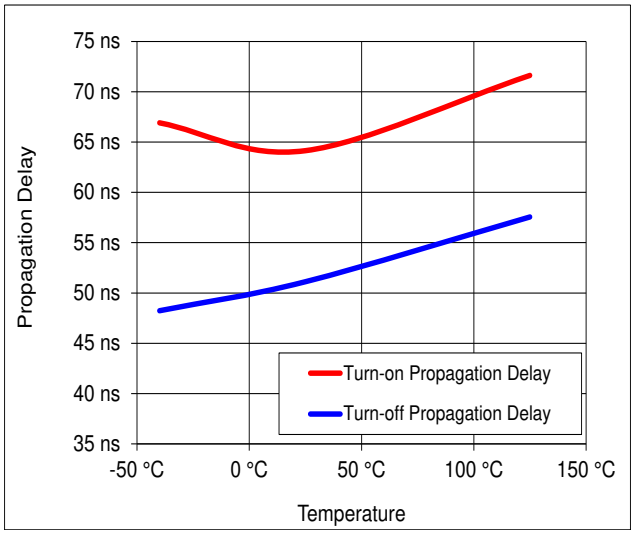


Figure 23: T_{DON} and T_{DOFF} vs. Temperature

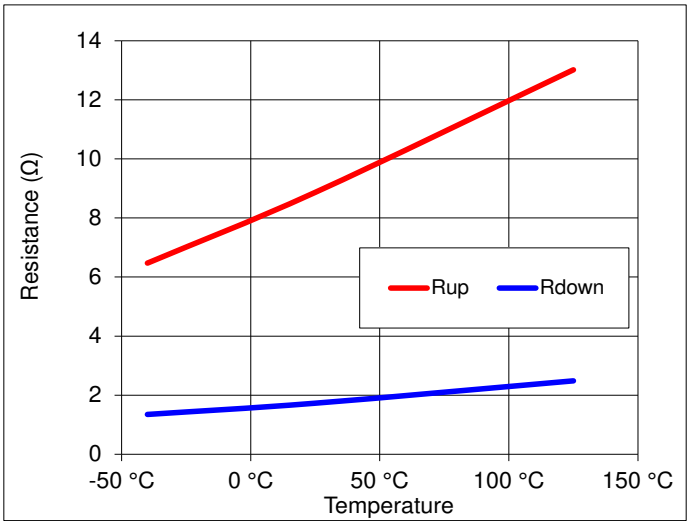
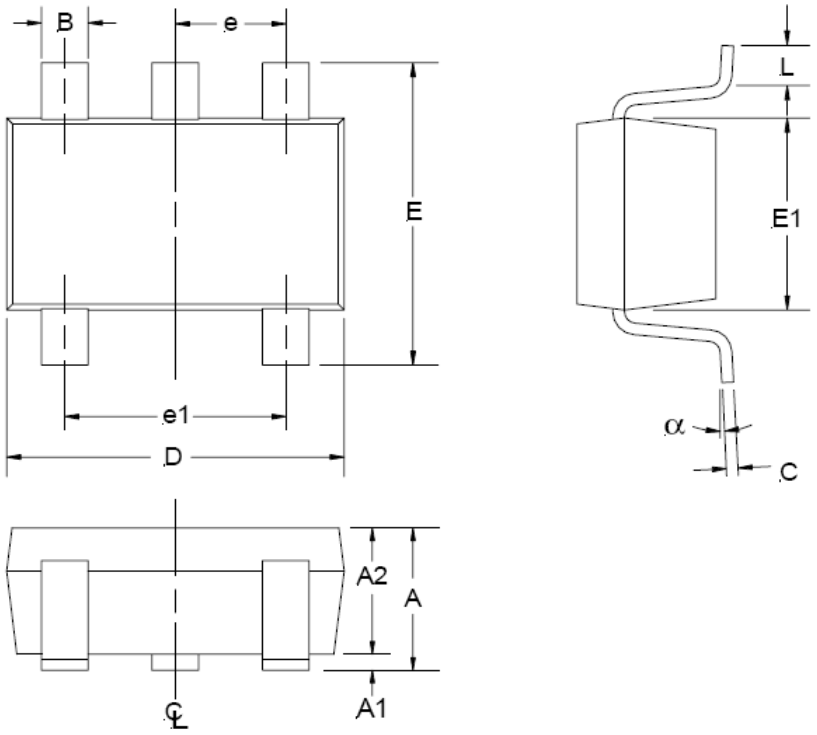


Figure 24: R_{UP} and R_{DOWN} vs. Temperature

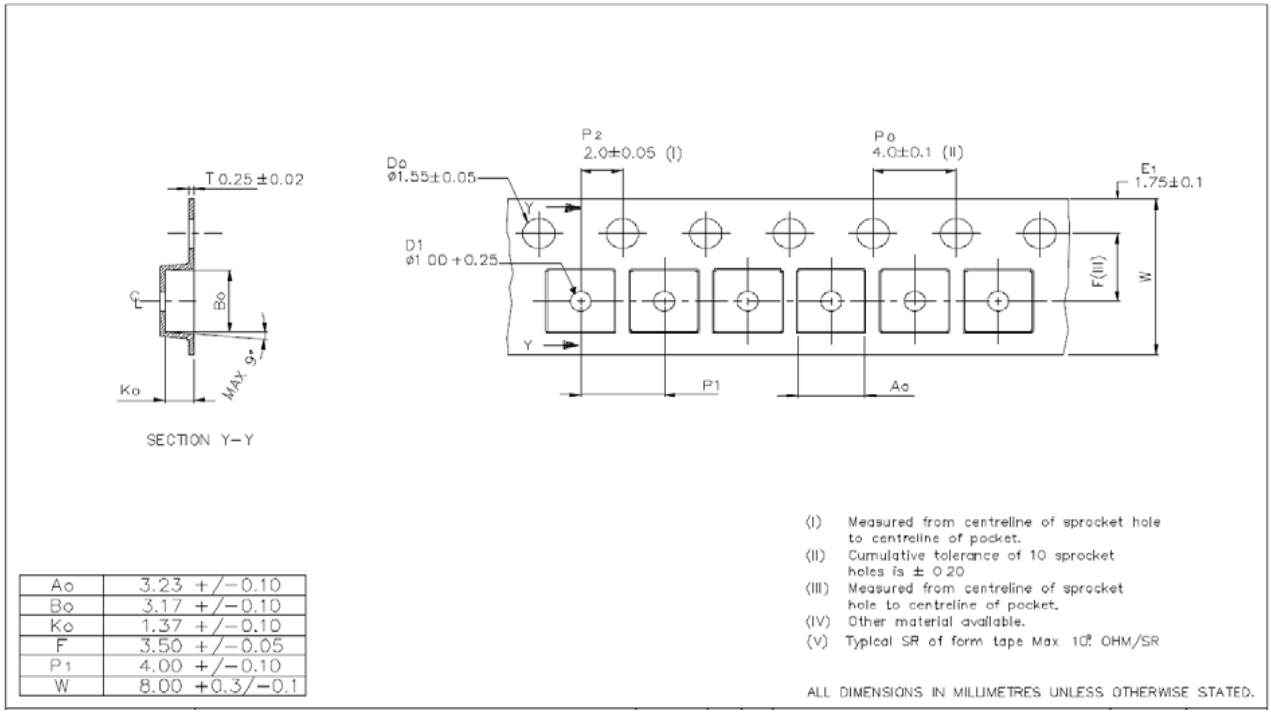
Package Details: 5 Lead SOT23



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.25	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 REF	
e1	1.90 REF	
L	0.35	0.55
α	0°	10°

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

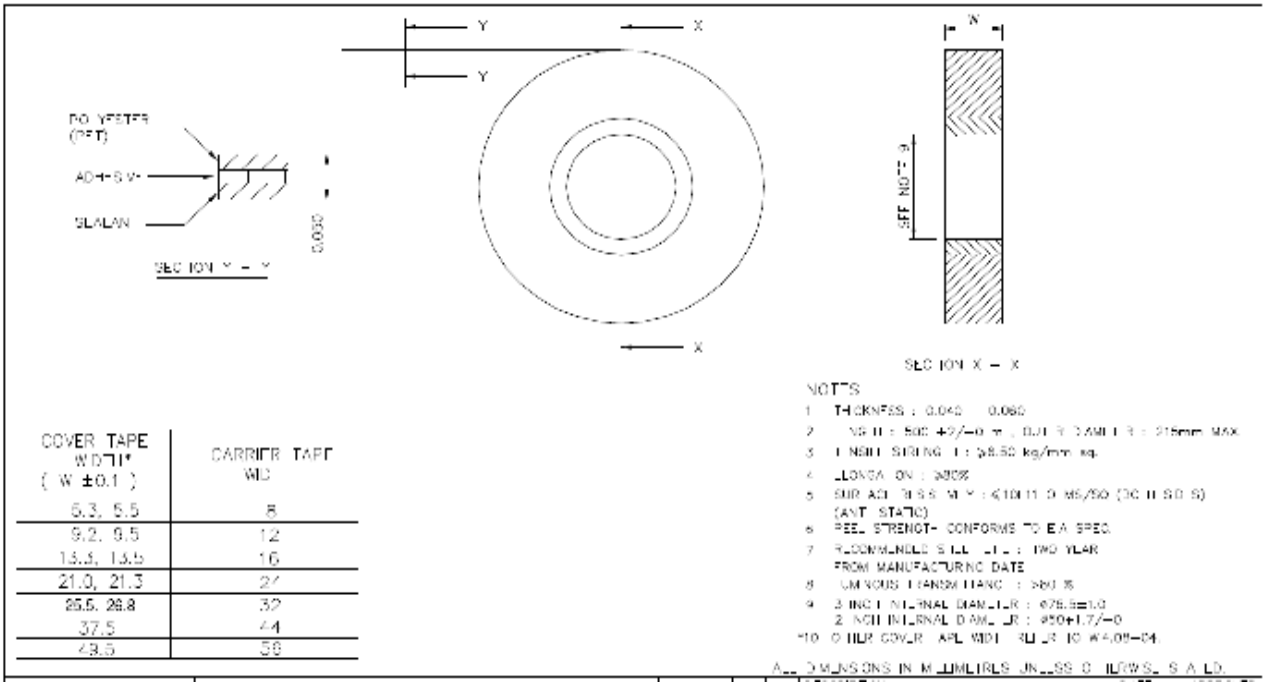
Tape and Reel Details: 5 Lead SOT23



Ao	3.23 +/−0.10
Bo	3.17 +/−0.10
Ko	1.37 +/−0.10
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^{5} OHM/SR

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

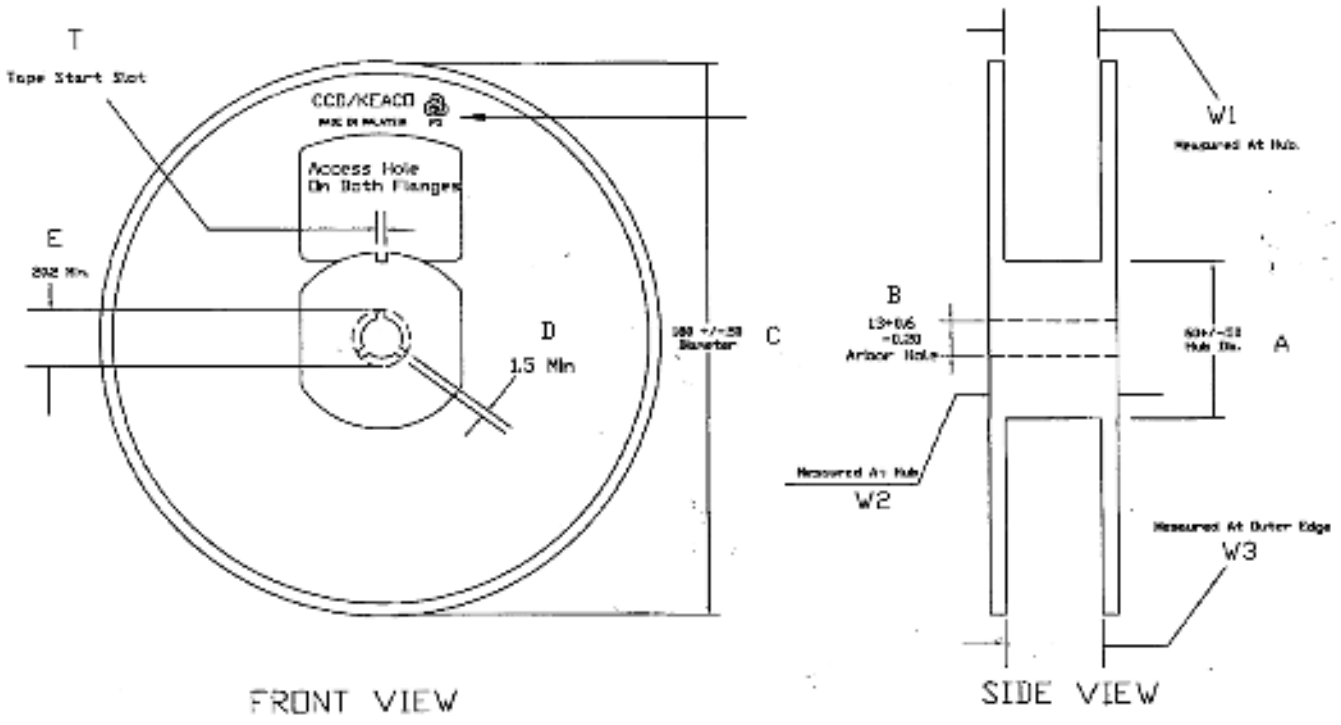


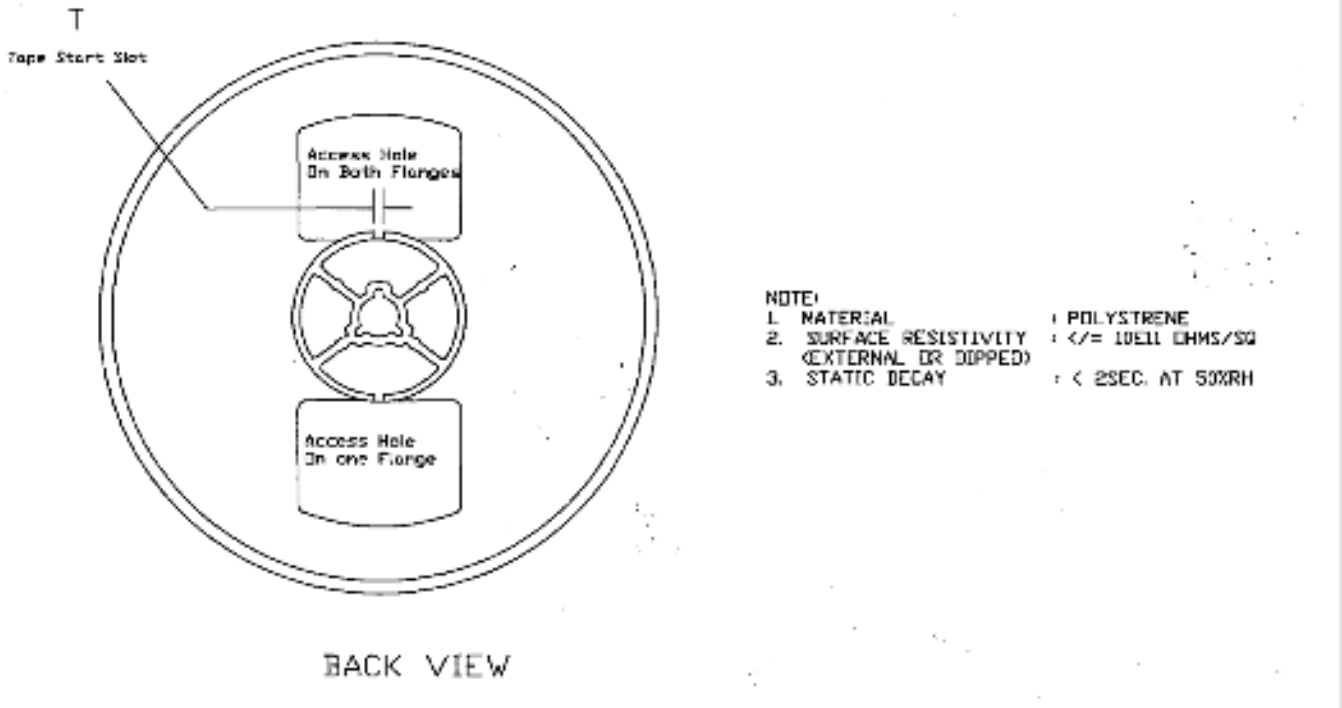
COVER TAPE WIDTH (W ±0.1)	CARRIER TAPE WID
5.3, 5.5	8
9.2, 9.5	12
13.3, 13.5	16
21.0, 21.3	24
25.5, 26.8	32
37.5	44
49.5	56

NOTES
1 THICKNESS : 0.040 0.060
2 VOLUME : 500 +9/−0 cm³ ; 0.01 Ω/SQUARE Ω : 215mm MAX
3 TENSILE STRENGTH : 58.50 kg/mm sq.
4 ELONGATION : 320%
5 SURFACE RESISTIVITY : 10^{11} Ω MIN/SQ (DOUBLE COATED ANTI STATIC)
6 PEEL STRENGTH CONFORMS TO EIA SPEC.
7 RECOMMENDED SHELF LIFE : TWO YEAR FROM MANUFACTURING DATE
8 HUMIDITY TRANSMITTANCE : 500 %
9 A INCH INTERNAL DIAMETER : ø75.5±1.0
B INCH INTERNAL DIAMETER : ø50+1.7/−0
10 TOP COVER APEX WIDTH RUBBER IS ø4.0±0.4

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

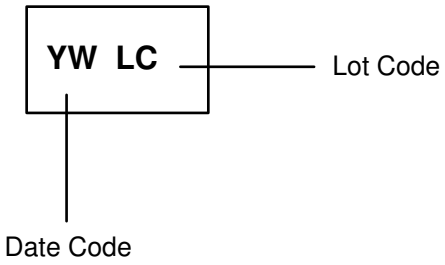
Tape and Reel Details: 5 Lead SOT23



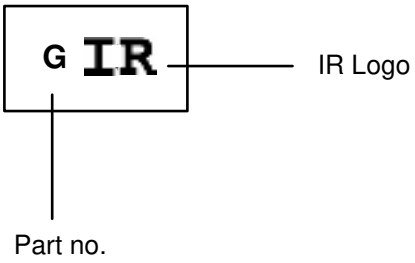


Part Marking Information: 5 Lead SOT23

Top Marking



Bottom Marking



Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. Infineon's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOT-23 5L	MSL1††† (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 1A (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at Infineon's web site www.infineon.com

†† Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

Revision History

Major changes since the last revision

Date	Description of change
June 1, 2015	First release
May 24, 2016	Changed MSL to level 1.
July 1, 2016	Changed format template with Infineon logo

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