ISO724xC-Q1 High-Speed, Quad-Channel Digital Isolators

1 Features

- 25Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1ns Maximum
  - Low Pulse-Width Distortion (PWD); 2ns Maximum
  - Low Jitter Content; 1ns Typ at 25Mbps
- Selectable Default Output (ISO7240CF)
- > 25-Year Life at Rated Working Voltage (See Insulation Characteristics Curves)
- 4kV ESD Protection
- Operates With 3.3V or 5V Supplies
- –40°C to +125°C Operating Temperature Range
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 61010-1, IEC 62368-1 certifications

2 Applications

- Factory Automation
  - Modbus
  - Profibus™
  - DeviceNet™ Data Buses
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

The ISO7240CF-Q1, ISO7241C-Q1, and ISO7242C-Q1 devices are quad-channel digital isolators with multiple channel configurations and output-enable functions. These devices have logic-input and logic-output buffers separated by Texas Instrument's silicon-dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices help block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7240C-Q1 family of devices has all four channels in the same direction. The ISO7241C-Q1 family of devices has three channels in the same direction and one channel in the opposition direction. The ISO7242C-Q1 family of devices has two channels in each direction.

The devices with the C suffix (C option) have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The devices with the M suffix (M option) have CMOS $V_{CC}/2$ input thresholds and do not have the input noise filter or the additional propagation delay.

The ISO7240CF device has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe output is a logic high when a logic high is placed on the CTRL pin or the pin is left unconnected. If a logic low signal is applied to the CTRL pin, the failsafe output becomes a logic-low output state. The input disable function of the ISO7240CF device prevents data from being passed across the isolation barrier to the output. When the inputs are disabled or V_{CC1} is powered down, the outputs are set by the CTRL pin.

These devices can be powered from 3.3V or 5V supplies on either side, in any combination. The signal input pins are 5V tolerant regardless of the voltage supply level that is used.

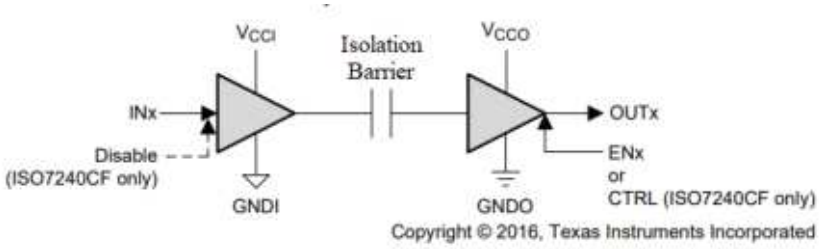
These devices are characterized for operation over the ambient temperature range of –40°C to +125°C.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)	PACKAGE SIZE(2)
ISO7240CF-Q1	DW (SOIC, 16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7241C-Q1			
ISO7242C-Q1			

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{CCI} and GNDI are supply and ground connections respectively for the input channels.
V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

Simplified Schematic

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4 Pin Configurations and Functions

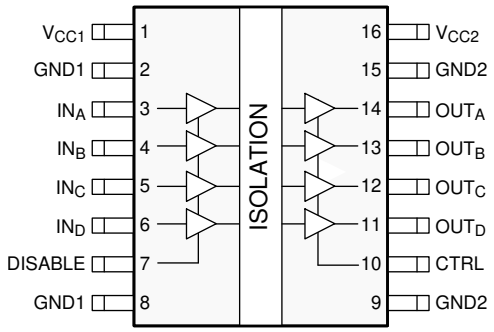


Figure 4-1. ISO7240CF-Q1 DW Package 16-Pin SOIC Top View

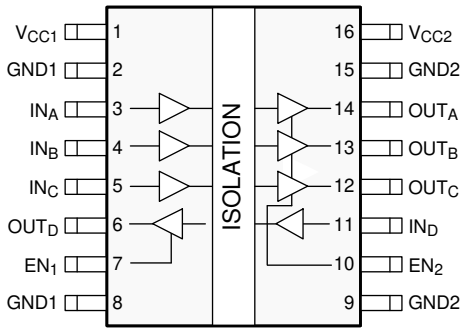


Figure 4-2. ISO7241C-Q1 DW Package 16-Pin SOIC Top View

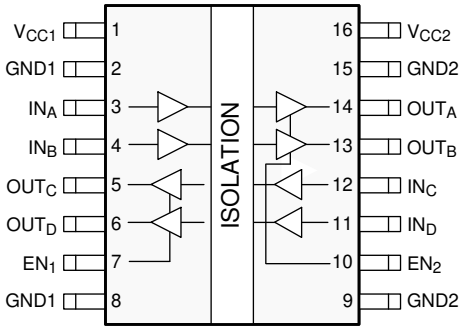


Figure 4-3. ISO7242C-Q1 DW Package 16-Pin SOIC Top View

Table 4-1. Pin Functions

PIN				Type[1]	DESCRIPTION
NAME	ISO7240CF-Q1	ISO7241C-Q1	ISO7242C-Q1		
CTRL	10	—	—	I	Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V_{CC1} is powered down. Output is high when CTRL is high or open and low when CTRL is low.
DISABLE	7	—	—	I	Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.
EN	—	—	—	I	Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.
EN_1	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN_1 is high or open and disabled when EN_1 is low.
EN_2	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN_2 is high or open and disabled when EN_2 is low.
GND1	2, 8	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9, 15	9, 15	—	Ground connection for V_{CC2}
IN_A	3	3	3	I	Input, channel A
IN_B	4	4	4	I	Input, channel B
IN_C	5	5	12	I	Input, channel C
IN_D	6	11	11	I	Input, channel D
NC	—	—	—	—	No Connect pins are floating with no internal connection
OUT_A	14	14	14	O	Output, channel A
OUT_B	13	13	13	O	Output, channel B
OUT_C	12	12	5	O	Output, channel C
OUT_D	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	16	—	Power supply, V_{CC2}

(1) I = Input; O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

See(1)

				VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}			–0.5 to 6	V
V_I	Voltage at IN, OUT, EN, DISABLE, CTRL			–0.5 to 6	V
ESD	Electrostatic discharge	Human-Body Model	All pins	±4	kV
		Field-Induced-Charged Device Model		±1	
T_J	Maximum junction temperature			150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	3.15		5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			mA
t_{ui}	Input pulse width	40			ns
$1/t_{ui}$	Signaling rate	0	30(1)	25	Mbps
V_{IH}	High-level input voltage (IN, DISABLE, CTRL, EN)	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN, DISABLE, CTRL, EN)	0		0.8	V
T_A	Operating free-air temperature	-40		125	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) Typical value at room temperature and well-regulated power supply.
(2) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.4 Thermal Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		168		°C/W
		High-K Thermal Resistance		68.6		
θ_{JB}	Junction-to-Board Thermal Resistance			33.5		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			33.9		°C/W

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

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5.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150C, C_L = 15 pF, Input a 25-Mbps 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation, ISO724xC				220	mW

5.6 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1	Certified according to UL 1577 Component Recognition Program
Basic certificate: 40047657	Master contract number: 220991	File number: E181974

5.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Thermal Characteristics			124	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Thermal Characteristics			190	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.8 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-III	
		Rated mains voltage ≤400 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification), V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3 V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1 V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.3 × V_{IORM}, t_m = 10 s	≤5	
		Method b: At routine test (100% production) V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.5 × V_{IORM} , t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	1	pF

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PARAMETER		TEST CONDITIONS	VALUE	UNIT
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 2500 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

5.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

, over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA
		25 Mbps			7	10.5	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
		25 Mbps			12	18	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps			15	24	
I_{CC2}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA
		25 Mbps			17	25	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		25 Mbps			18	28	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps			15	24	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel		0		μA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	V_{CC} – 0.8			V
			I_{OH} = –20 μA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
			I_{OL} = 20 μA			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	μA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V; Figure 6-5	25	50		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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5.10 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_2 at 3 V		0.5	1.2	mA
		25 Mbps			3	5	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7	mA
		25 Mbps			6.5	11	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	
		25 Mbps			9	14	
I_{CC2}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_2 at 3 V		9.5	15	mA
		25 Mbps			10.5	17	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	13	mA
		25 Mbps			11.5	18	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	
		25 Mbps			9	14	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	V_{CC} – 0.4			V
			I_{OH} = –20 µA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
			I_{OL} = 20 µA			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V; Figure 6-5	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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5.11 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			0.5	1.2	mA
		25 Mbps				3	5	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			4	7	mA
		25 Mbps				6.5	11	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6	10	mA
		25 Mbps				9	14	
I_{CC2}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			15	22	mA
		25 Mbps				17	25	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			13	20	mA
		25 Mbps				18	28	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			10	16	mA
		25 Mbps				15	24	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	ISO7240	V_{CC} – 0.4			V
				ISO724x (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20 µA		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.4	V
			I_{OL} = 20 µA				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V; Figure 6-5		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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5.12 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			1	3	mA
		25 Mbps				7	10.5	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
		25 Mbps				12	18	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			10	16	mA
		25 Mbps				15	24	
I_{CC2}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			9.5	15	mA
		25 Mbps				10.5	17	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			8	13	mA
		25 Mbps				11.5	18	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6	10	mA
		25 Mbps				9	14	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	ISO7240	V_{CC} – 0.4			V
				ISO724x (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20 µA		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.4	V
			I_{OL} = 20 µA				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V; Figure 6-5		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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5.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 6-1	25		56	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)				4	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7240C, ISO7241C			3.5	ns
		ISO7242C			4	
t_r	Output signal rise time	See Figure 6-1		2		ns
t_f	Output signal fall time			2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-3		18		µs
t_{wake}	Wake time from input disable	See Figure 6-4		15		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.14 Switching Characterstics: V_{CC1} and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 6-1	18		45	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				5	
$t_{sk(pp)}$	Part-to-part skew (2)				8	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7240C, ISO7241C			3	ns
		ISO7242C			4	
t_r	Output signal rise time	See Figure 6-1		2.4		ns
t_f	Output signal fall time			2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-3		12		µs
t_{wake}	Wake time from input disable	See Figure 6-4		15		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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5.15 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 6-1		20		51	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See Figure 6-1	ISO7240C, ISO7241C			3	ns
			ISO7242C			4	
$t_{sk(pp)}$	Part-to-part skew (2)					10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7240C, ISO7241C				3	ns
		ISO7242C				4	
t_r	Output signal rise time	See Figure 6-1			2.4		ns
t_f	Output signal fall time				2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 6-2			15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-3			12		µs
t_{wake}	Wake time from input disable	See Figure 6-4			15		µs

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.16 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 6-1	20		50	ns
PWD(1)	See Figure 6-1	ISO7240C, ISO7241C			3	
		ISO7242C			4	
PWD	See Figure 6-1				3	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
t_r	Output signal rise time	See Figure 6-1		2.4		ns
t_f	Output signal fall time			2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-3		18		µs
t_{wake}	Wake time from input disable	See Figure 6-4		15		µs

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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5.17 Insulation Characteristics Curves

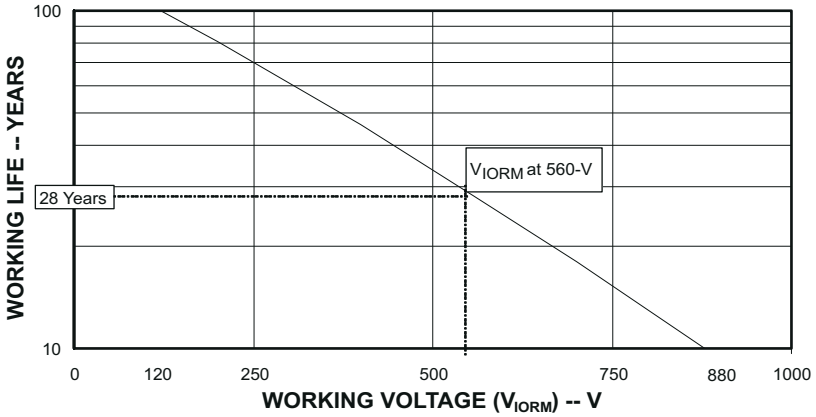


Figure 5-1. Time Dependent Dielectric Breakdown Testing Results

5.18 Typical Characteristic

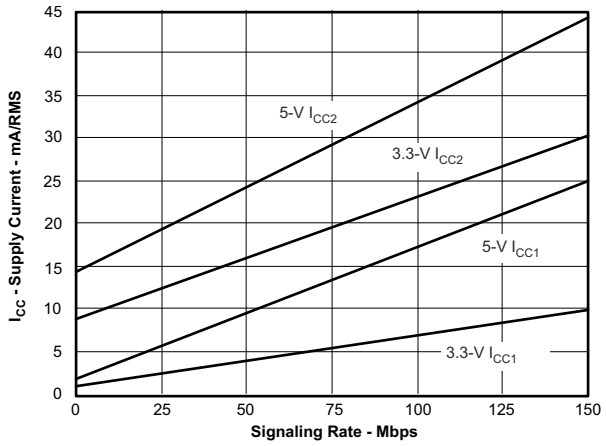


Figure 5-2. ISO7240C RMS Supply Current vs Signaling Rate

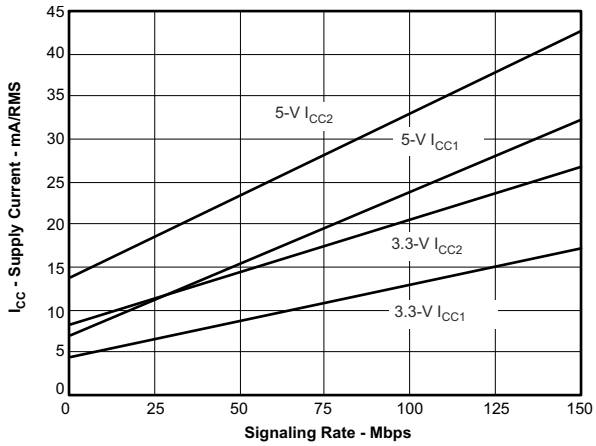


Figure 5-3. ISO7241C RMS Supply Current vs Signaling Rate

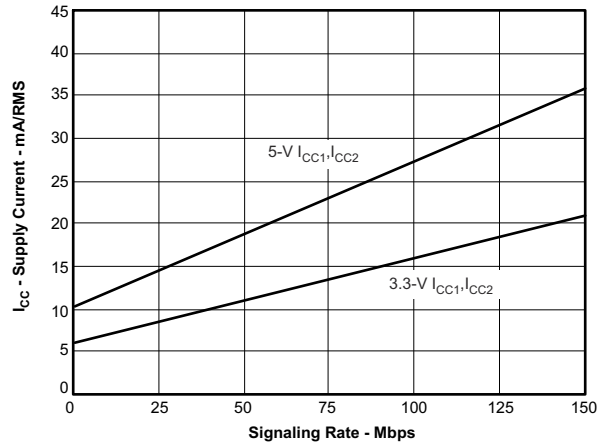


Figure 5-4. ISO7242C RMS Supply Current vs Signaling Rate

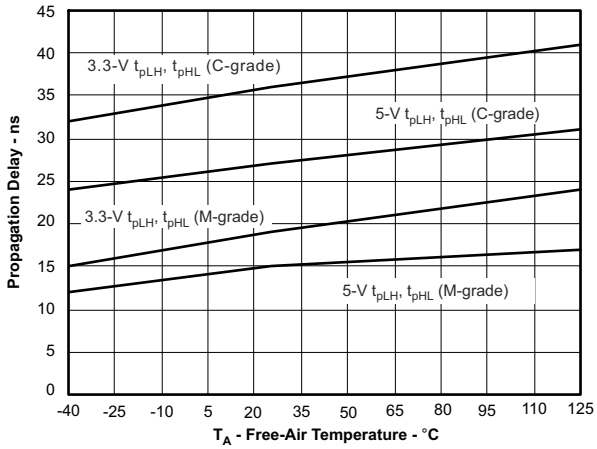


Figure 5-5. Propogation Delay vs Free-Air Temperature

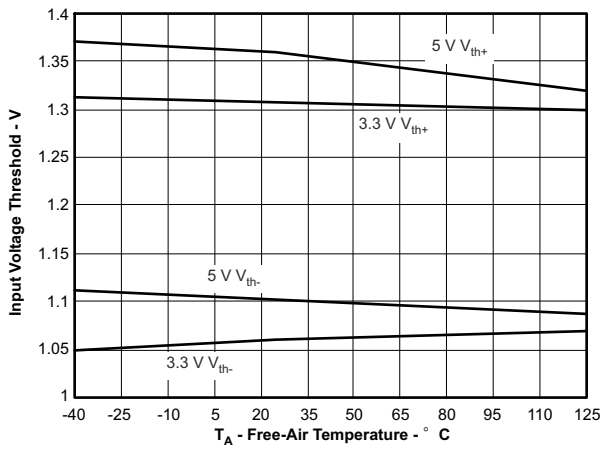


Figure 5-6. Input Voltage Threshold vs Free-Air Temperature

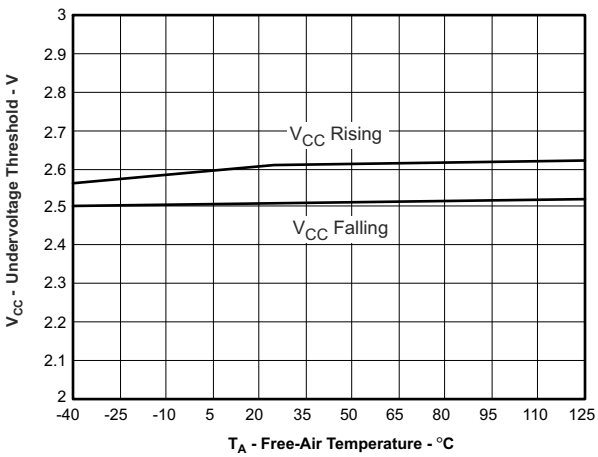


Figure 5-7. V_{CC1} Failsafe Threshold vs Free-Air Temperature

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5.18 Typical Characteristic (continued)

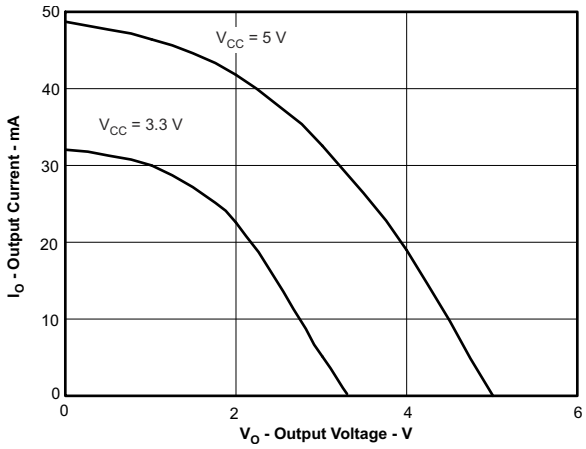


Figure 5-8. High-Level Output Current vs High-Level Output Voltage

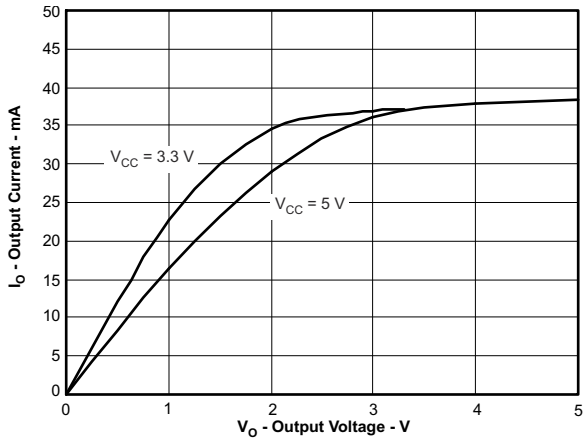
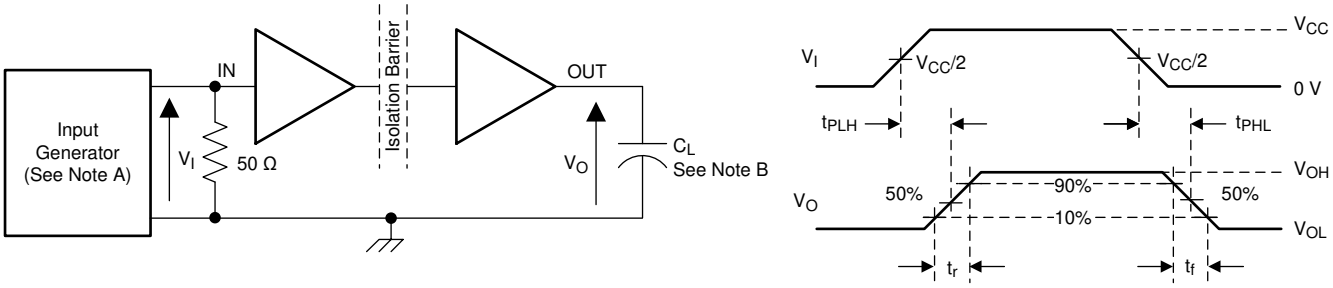


Figure 5-9. Low-Level Output Current vs Low-Level Output Voltage

6 Parameter Measurement Information

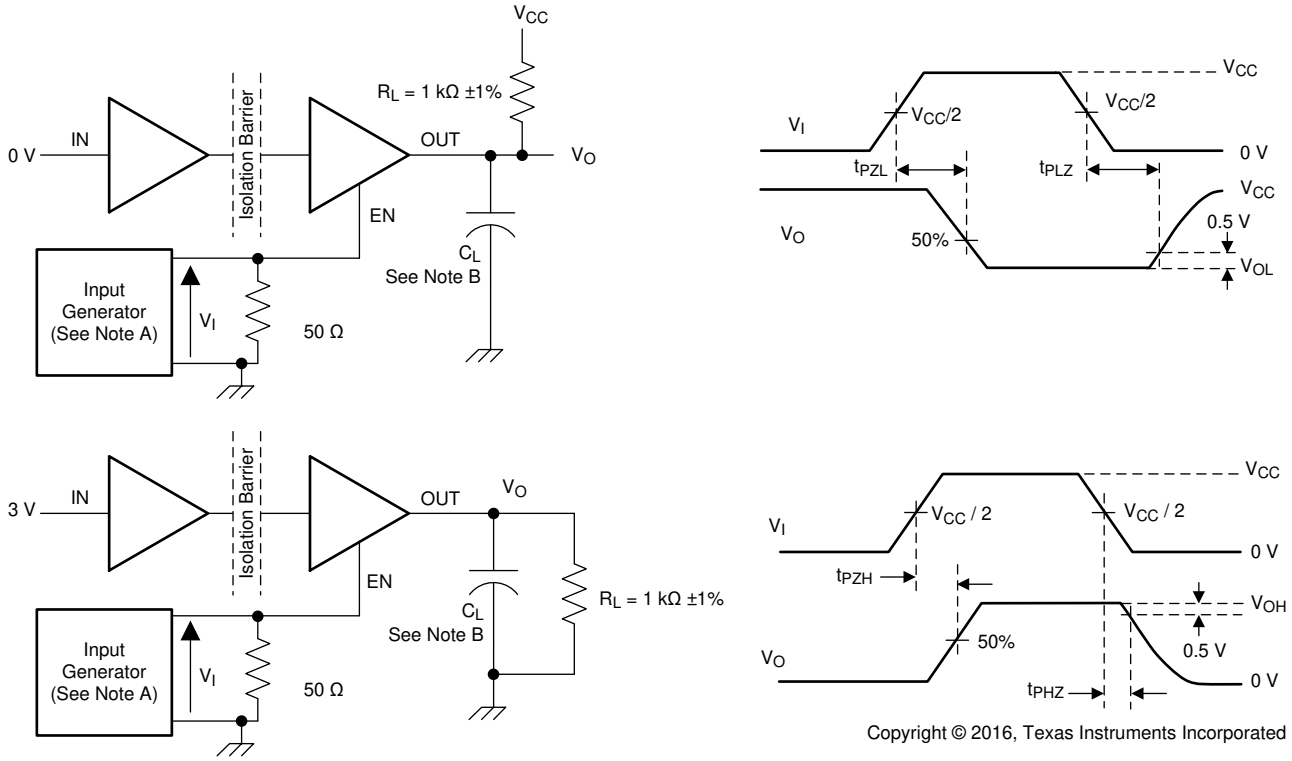


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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-1. Switching Characteristic Test Circuit and Voltage Waveforms



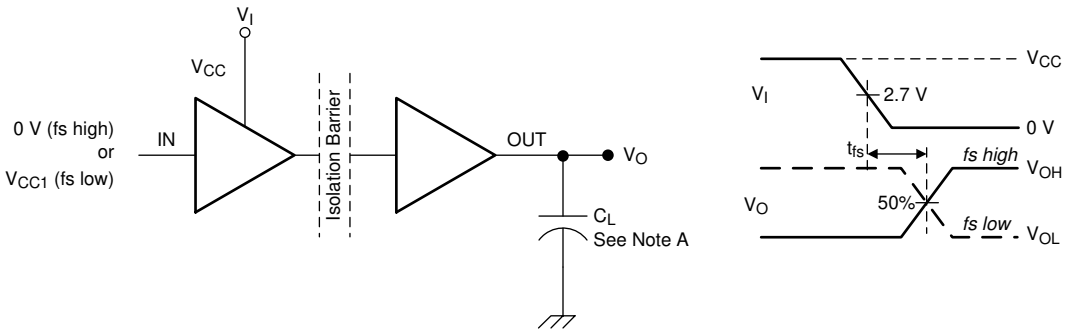
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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

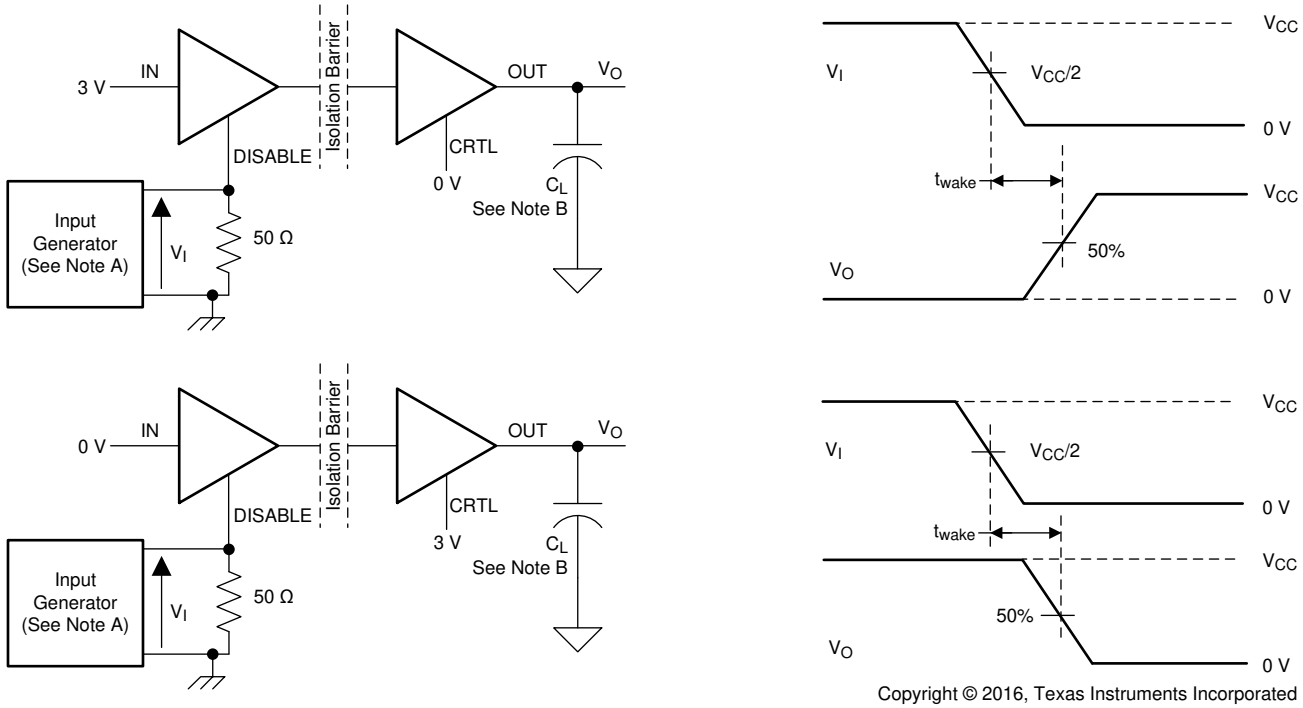
Figure 6-2. Enable or Disable Propagation-Delay Time Test Circuit and Waveform

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A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-3. Failsafe Delay Time Test Circuit and Voltage Waveforms



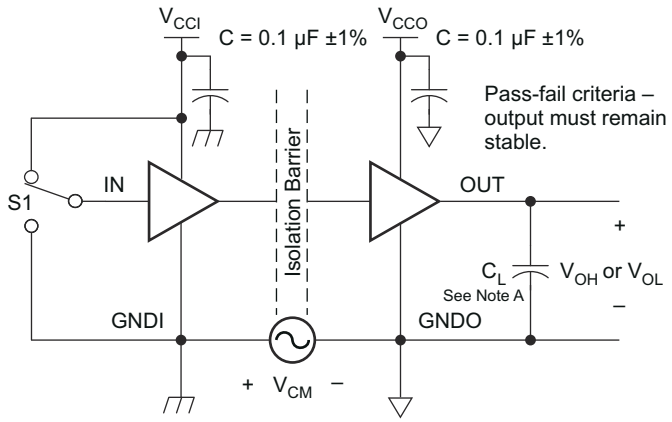
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The test that yields the longest time is used in this data sheet.

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

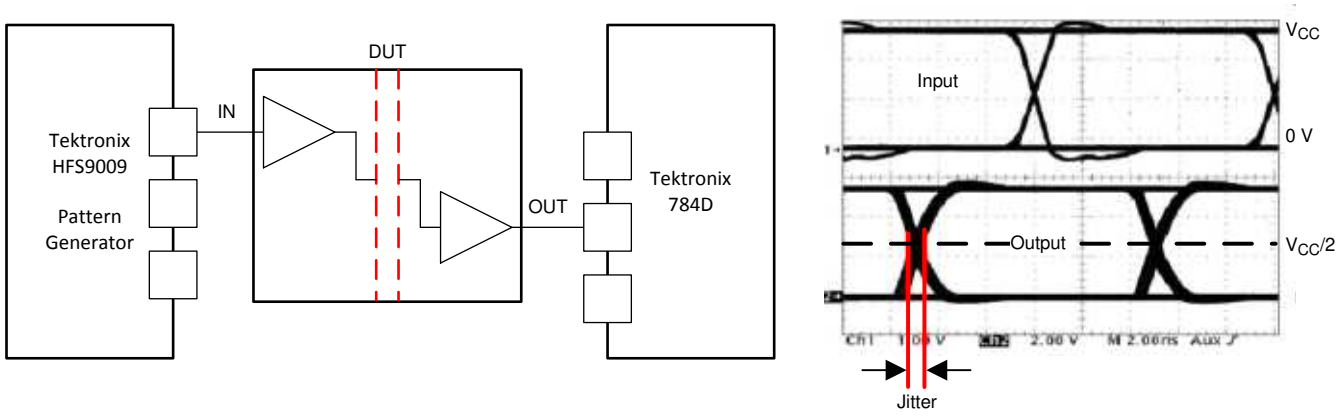
Figure 6-4. Wake Time From Input Disable Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

Figure 6-5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



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PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 6-6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

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7 Detailed Description

7.1 Overview

The ISO724x-Q1 family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

7.2 Functional Block Diagram

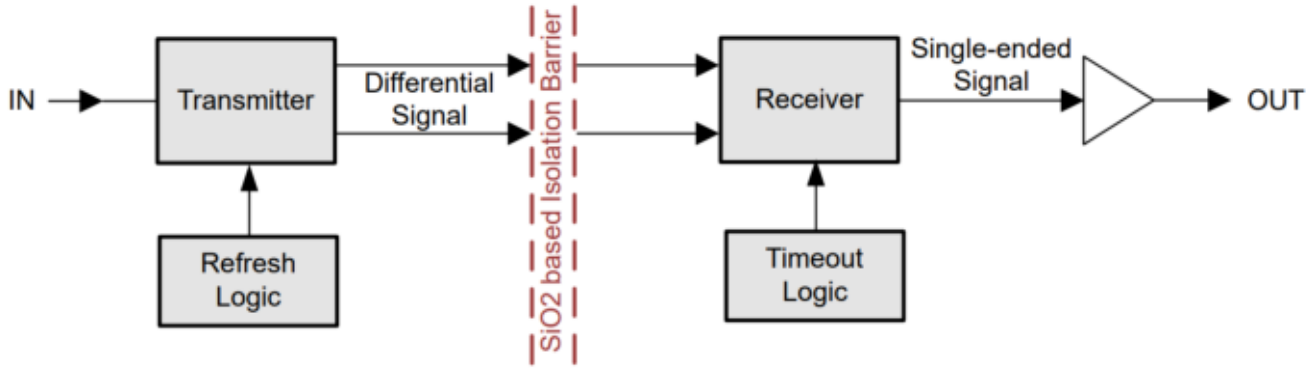


Figure 7-1. Conceptual Block Diagram of a Digital Isolator

7.3 Feature Description

The ISO724x-Q1 family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. Table 7-1 lists these device features.

Table 7-1. Device Features

PRODUCT(1)	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7240CF	25 Mbps	≅1.5 V (TTL)	4/0
ISO7241C	25 Mbps	≅1.5 V (TTL)	3/1
ISO7242C	25 Mbps	≅1.5 V (TTL)	2/2

(1) For the most current package and ordering information, see the *Section 11* section, or see the TI website at www.ti.com.

7.4 Device Functional Modes

List of ISO724x-Q1 functional modes.

Table 7-2. Device Function Table ISO724x-Q1

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

7.4.1 Device I/O Schematics

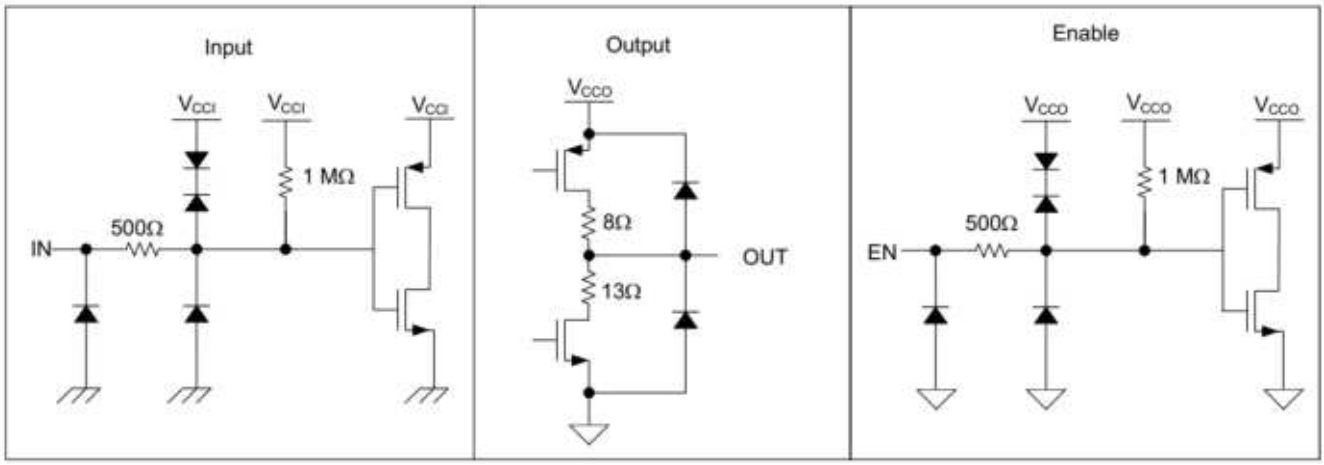


Figure 7-2. Device I/O Schematics

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO724x-Q1 family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

8.2.1 Isolated Data Acquisition System for Process Control

The ISO724x-Q1 family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in Figure 8-1.

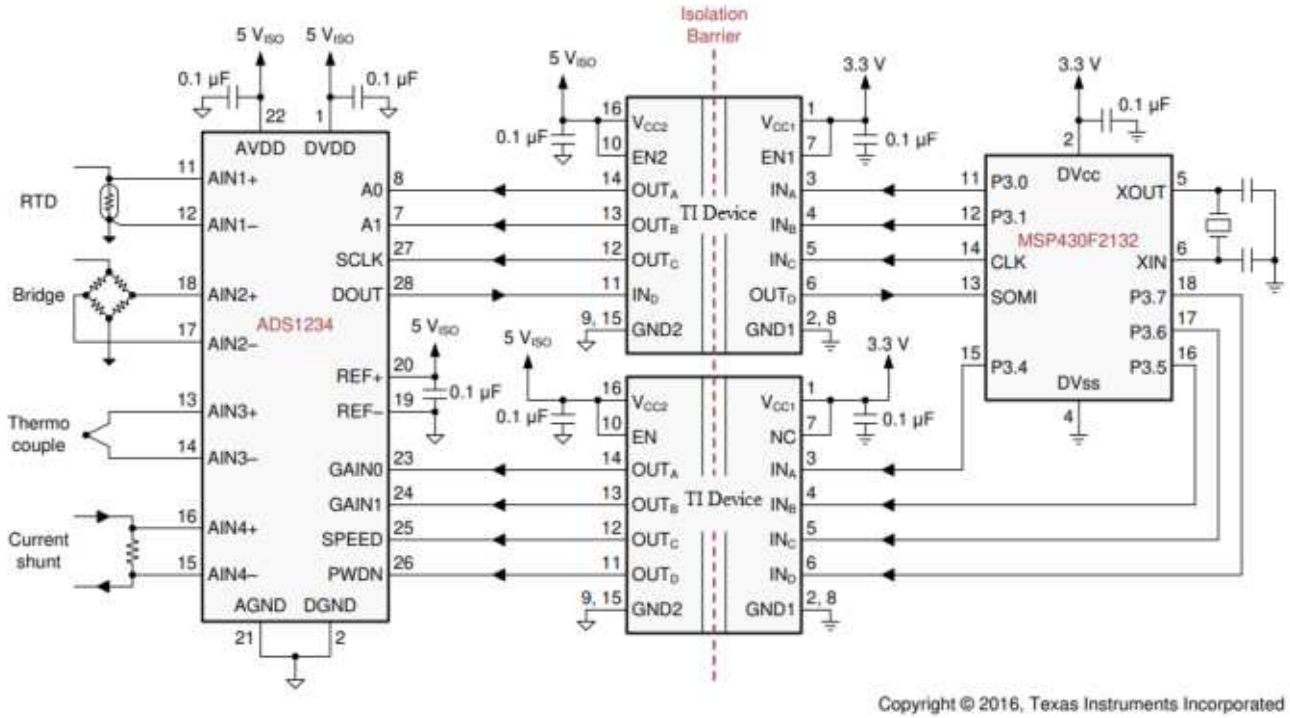


Figure 8-1. Isolated Data Acquisition System for Process Control

8.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x-Q1 family of devices only require two external bypass capacitors to operate.

8.2.1.2 Detailed Design Procedure

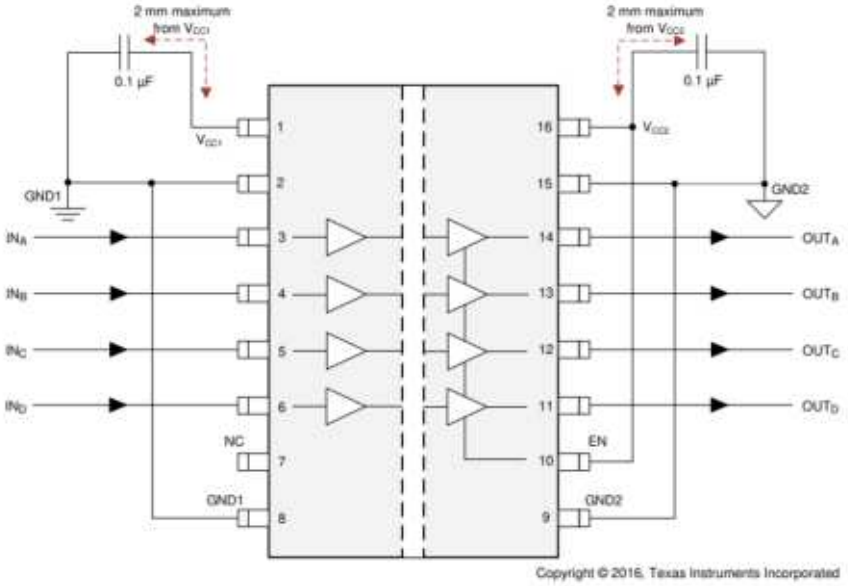


Figure 8-2. ISO7240x-Q1 Typical Circuit Hook-Up

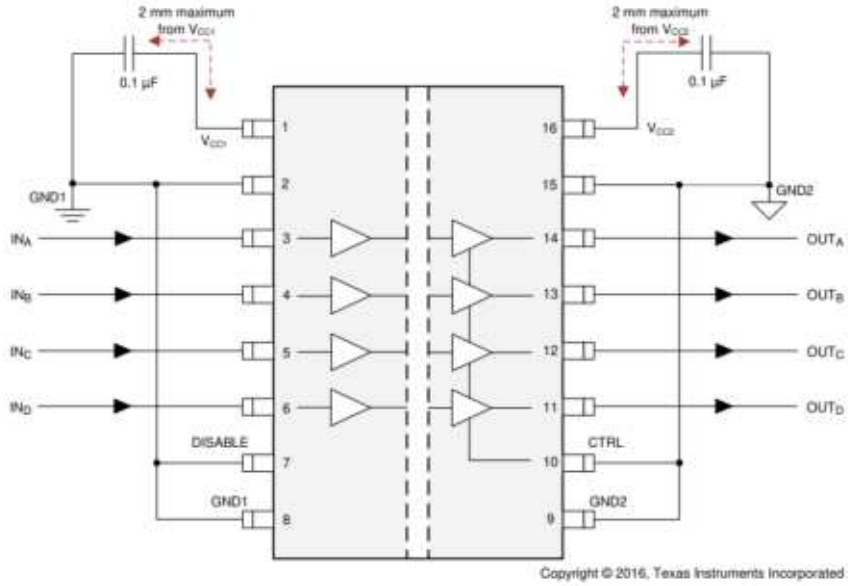


Figure 8-3. ISO7240CF-Q1 Typical Circuit Hook-Up

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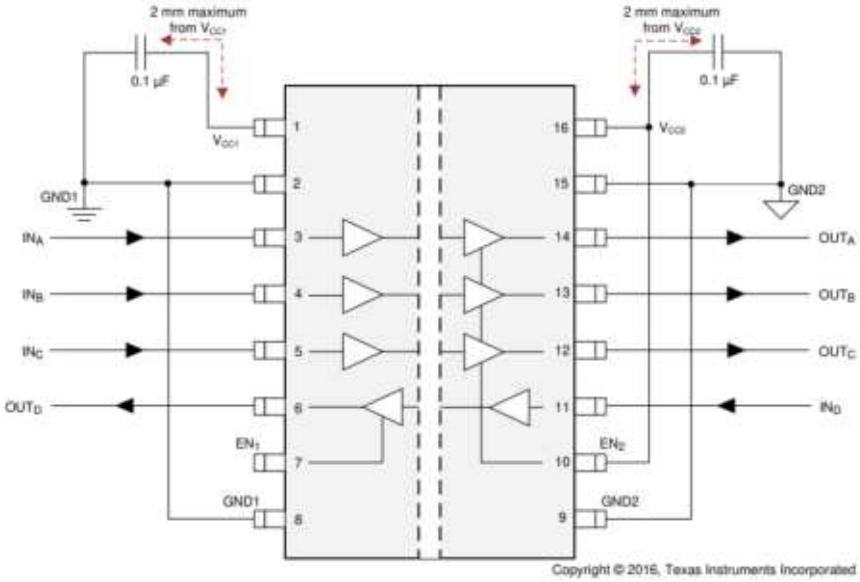


Figure 8-4. ISO7241x-Q1 Typical Circuit Hook-Up

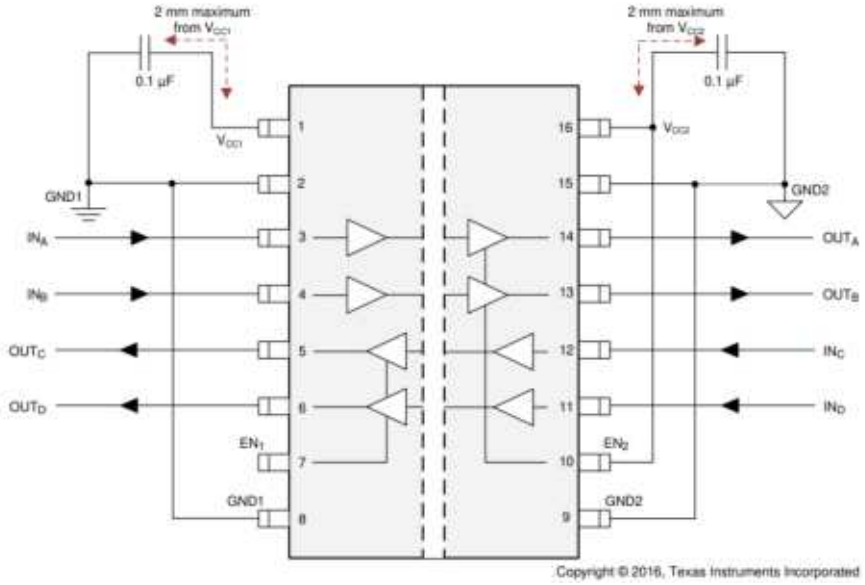


Figure 8-5. ISO7242x-Q1 Typical Circuit Hook-Up

8.2.2 Isolated SPI for an Analog Input Module with 16 Inputs

The ISO7241x-Q1 family of devices and several other components from Texas Instruments can be used to create an isolated SPI for an input module with 16 inputs.

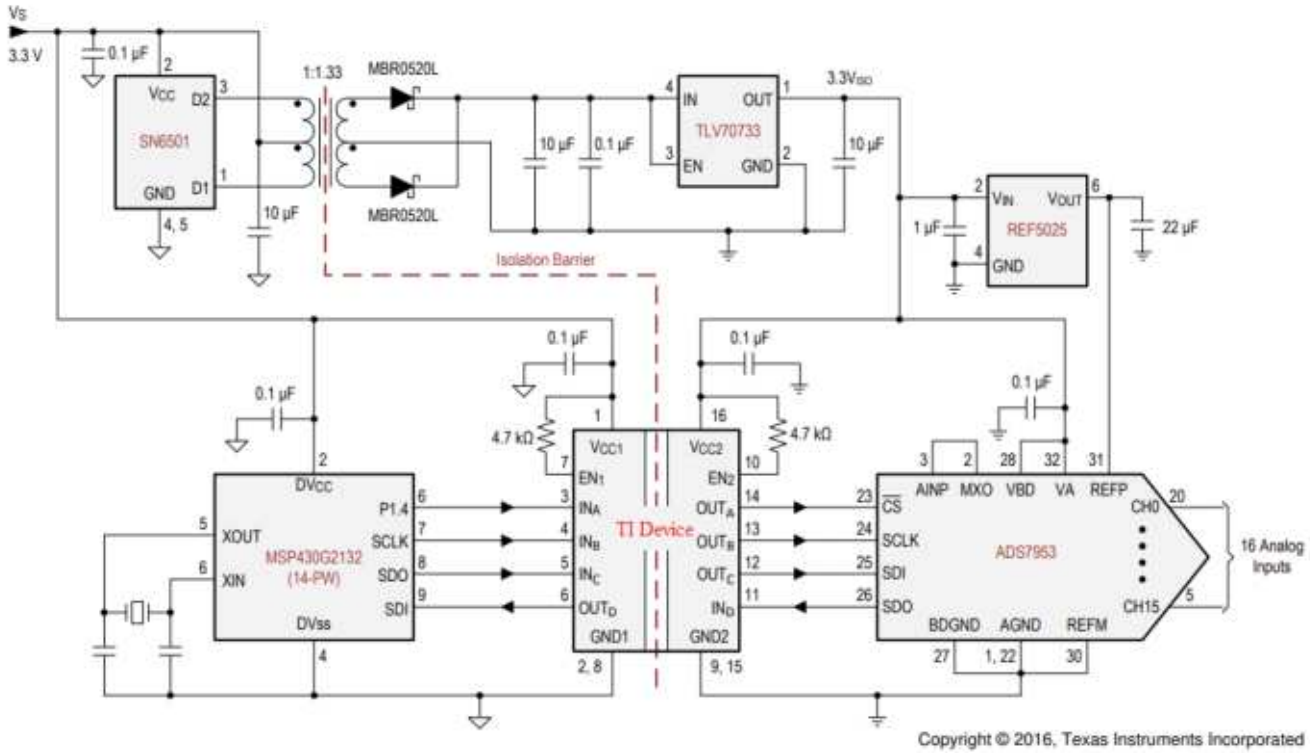


Figure 8-6. Isolated SPI for an Analog Input Module With 16 Inputs

8.2.2.1 Design Requirements

See the *Design Requirements* in *Section 8.2.1*.

8.2.2.2 Detailed Design Procedure

See the *Detailed Design Procedure* in *Section 8.2.1*.

8.2.3 Isolated RS-232 Interface

Figure 8-7 shows a typical isolated RS-232 interface implementation.

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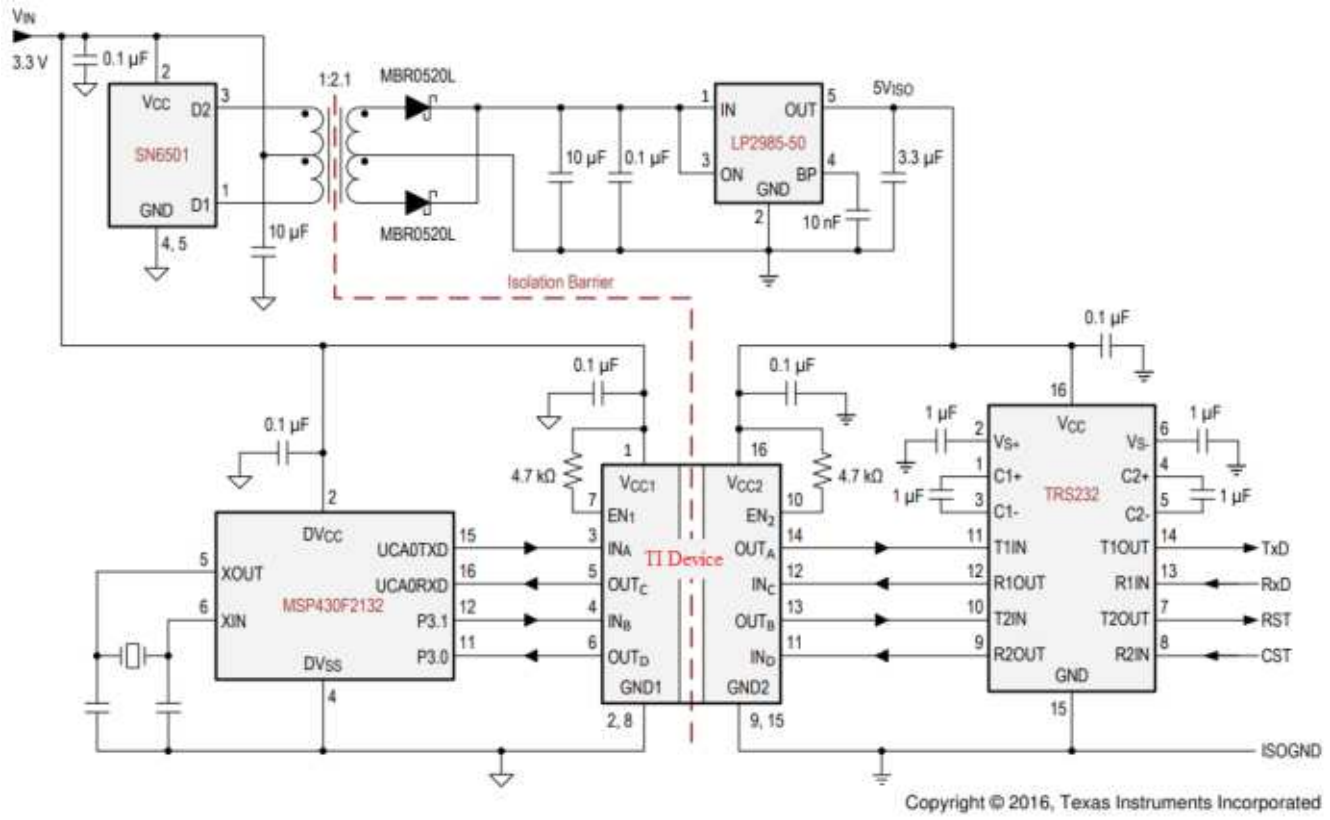


Figure 8-7. Isolated RS-232 Interface

8.2.3.1 Design Requirements

See the *Design Requirements* in *Section 8.2.1*.

8.2.3.2 Detailed Design Procedure

See the *Detailed Design Procedure* in *Section 8.2.1*.

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies*.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 8-8). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

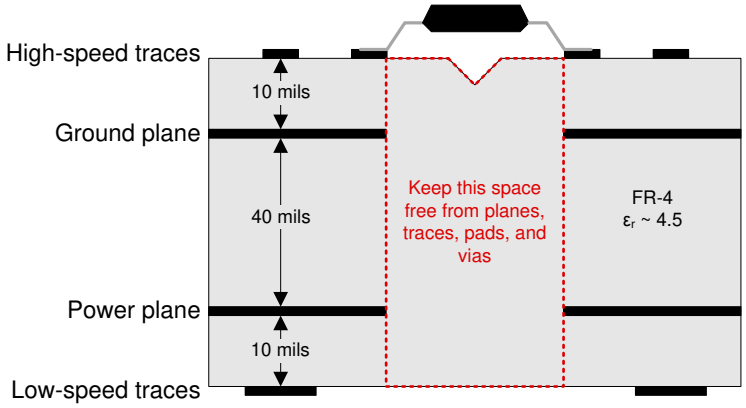


Figure 8-8. Recommended Layer Stack

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- *Digital Isolator Design Guide*
- *Isolation Glossary*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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DeviceNet™ is a trademark of Open DeviceNet Vendors Association.
TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2025) to Revision D (October 2025)	Page
• Added fixes for typos and errors in *Insulation Specifications* table	5
• Changed 'Plan to certify' with 'Certified' in all 3 places in the 2nd row in the *Safety-Related Certifications* section	5
• Changed 'Certificate planned' with 'Basic certificate: 40047657' in VDE column, 'Master contract number: 220991' in CSA column, and 'File number: E181974' in UL column in the *Safety-Related Certifications* section	5
• Changed Typical ISO724x Application Circuit, *Isolated Data Acquisition System for Process Control*	21

Changes from Revision B (November 2024) to Revision C (February 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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- Changed the IEC 60664-1 RATINGS TABLE - Specification I-III test conditions From: Rated mains voltage ≤150 VRMS To: Rated mains voltage ≤300 VRMS. Added a row for the I-II specifications..... 6

Changes from Revision A (September 2011) to Revision B (November 2024) **Page**

- Updated reference from capacitive isolation to isolation barrier throughout the document..... 1
- Updated VDE V 0884-11 to DIN VDE 0884-17 throughout the document..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations..... 5
- Updated electrical and switching characteristics to match device performance..... 7
- Added the *Detailed Description*, *Overview*, *Feature Description*, *Functional Block Diagram*, and *Device Functional Modes* sections..... 19
- Added the *Typical Application*, *Power Supply Recommendations*, and *Layout* sections..... 21

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7240CFQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CFQ
ISO7240CFQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CFQ
ISO7241CQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241CQ
ISO7241CQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241CQ
ISO7242CQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242CQ
ISO7242CQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242CQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1 :

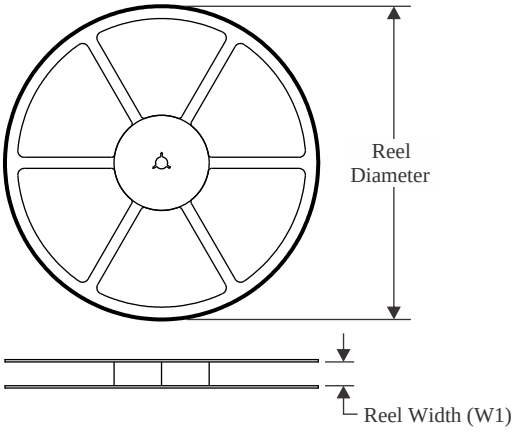
- Catalog : ISO7240CF, ISO7241C, ISO7242C

NOTE: Qualified Version Definitions:

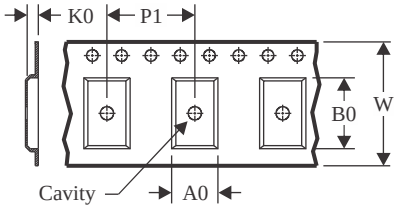
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

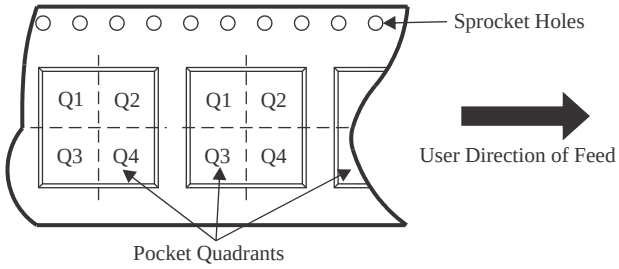


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

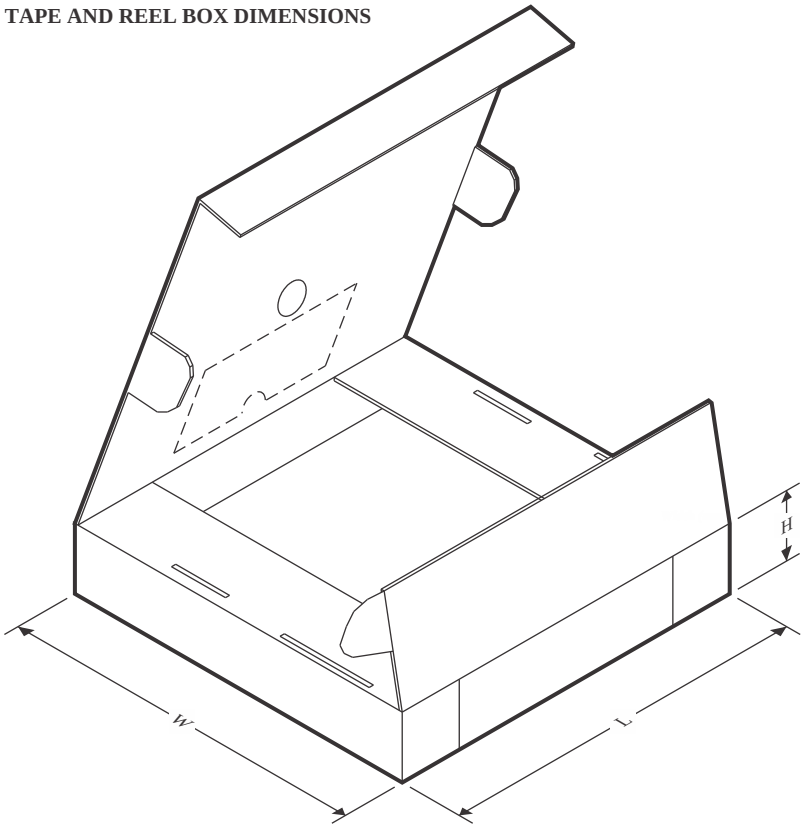
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CFQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240CFQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CFQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7240CFQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7241CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

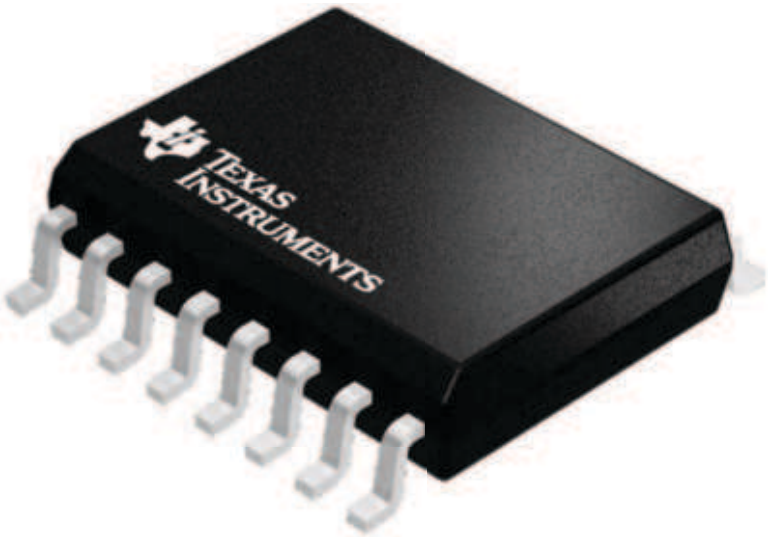
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

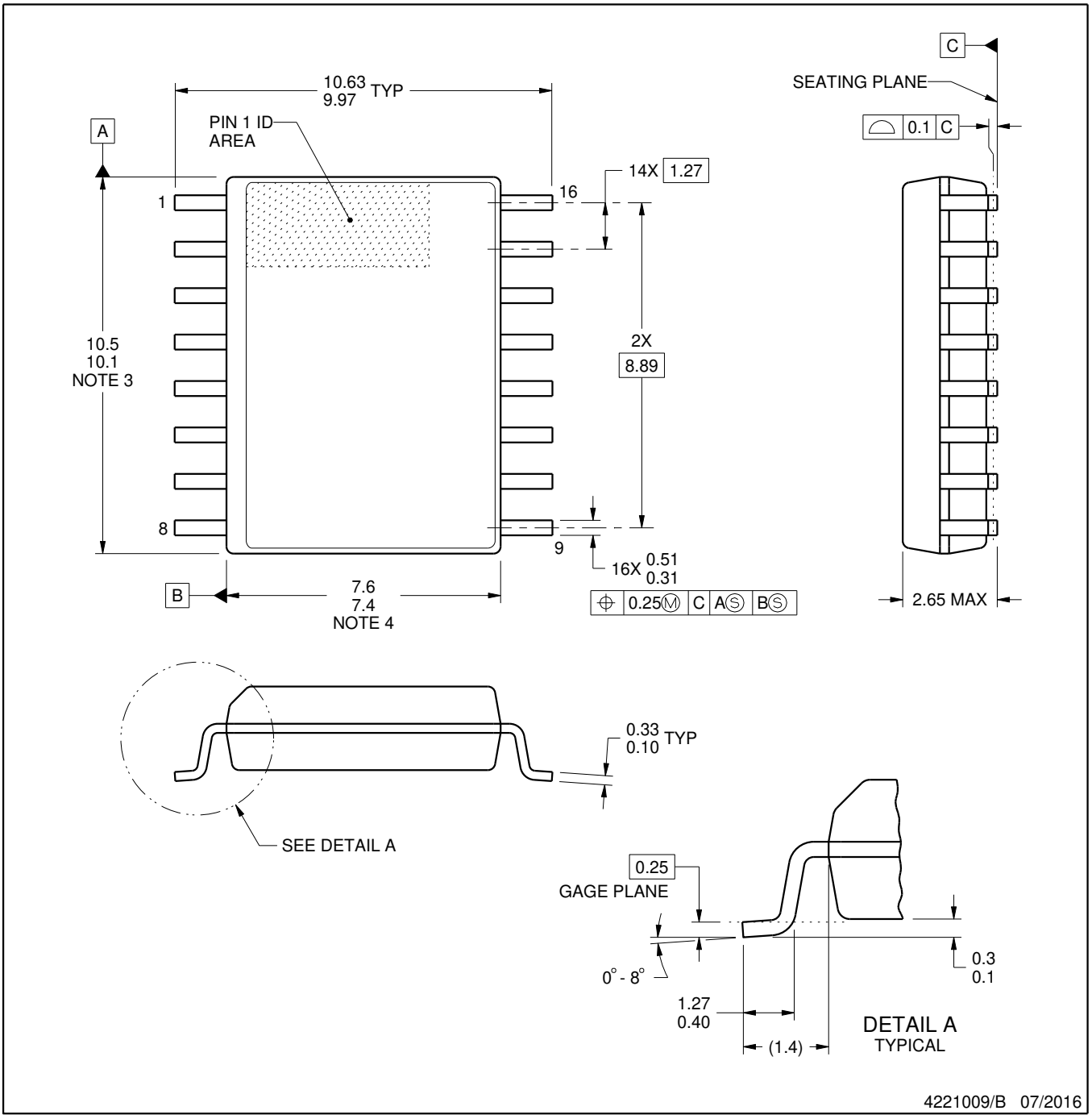


PACKAGE OUTLINE

DW0016B

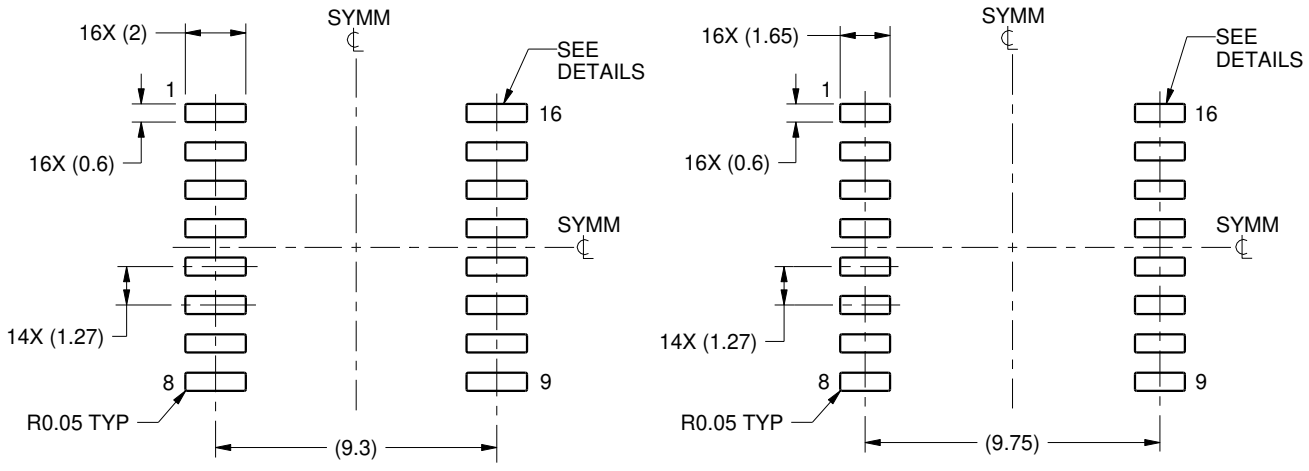
SOIC - 2.65 mm max height

SOIC

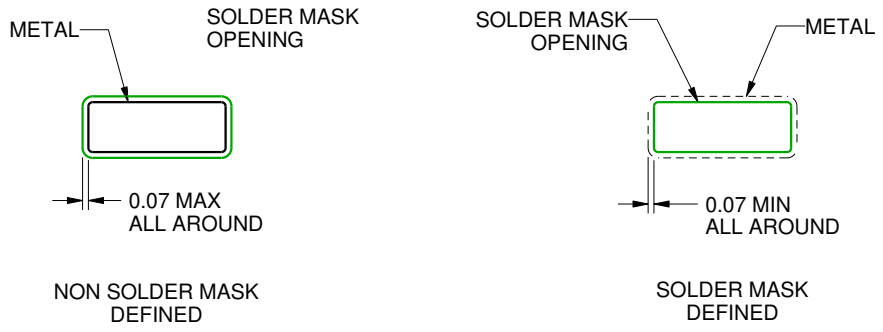


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

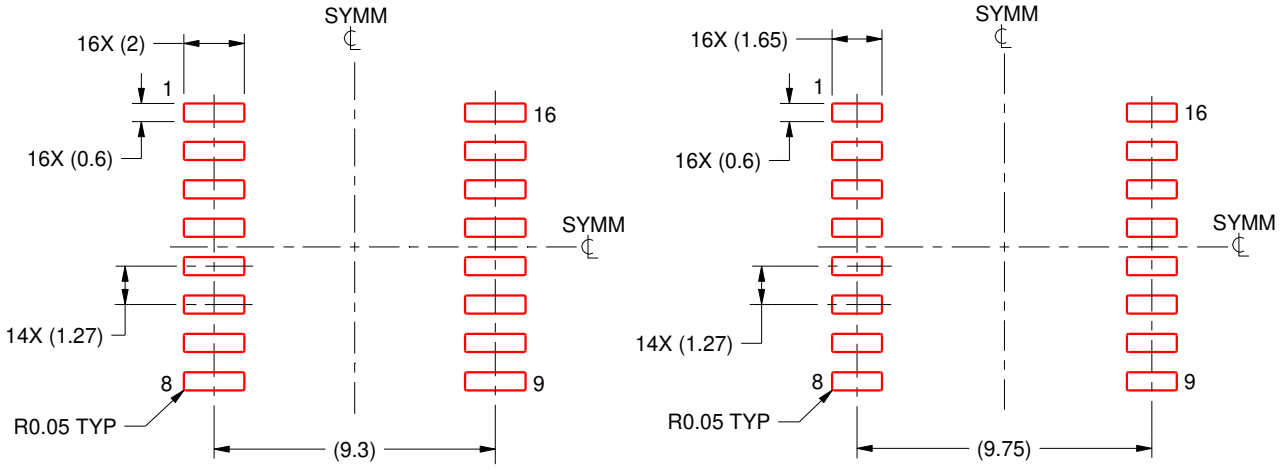
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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