Lead-Free Package Options Available!

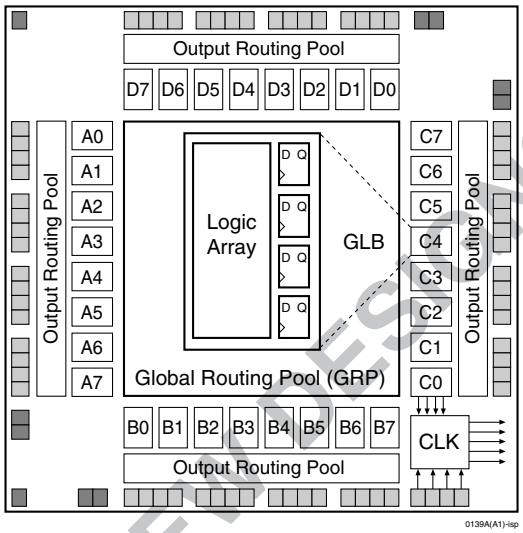
# ispLSI® 1032E

## In-System Programmable High Density PLD

## Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **6000 PLD Gates**
  - **64 I/O Pins, Eight Dedicated Inputs**
  - **192 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **$f_{max}$ = 125 MHz Maximum Operating Frequency**
  - **$t_{pd}$ = 7.5 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **In-System Programmable (ISP™) 5V Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Four Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
  - **Lead-Free Package Options**

## Functional Block Diagram




## Description

The ispLSI 1032E is a High Density Programmable Logic Device containing 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032E device offers 5V non-volatile in-system programmability of the logic, as well as the interconnects to provide truly reconfigurable systems. A functional superset of the ispLSI 1032 architecture, the ispLSI 1032E device adds two new global output enable pins.

The basic unit of logic on the ispLSI 1032E device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…D7 (see Figure 1). There are a total of 32 GLBs in the ispLSI 1032E device. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

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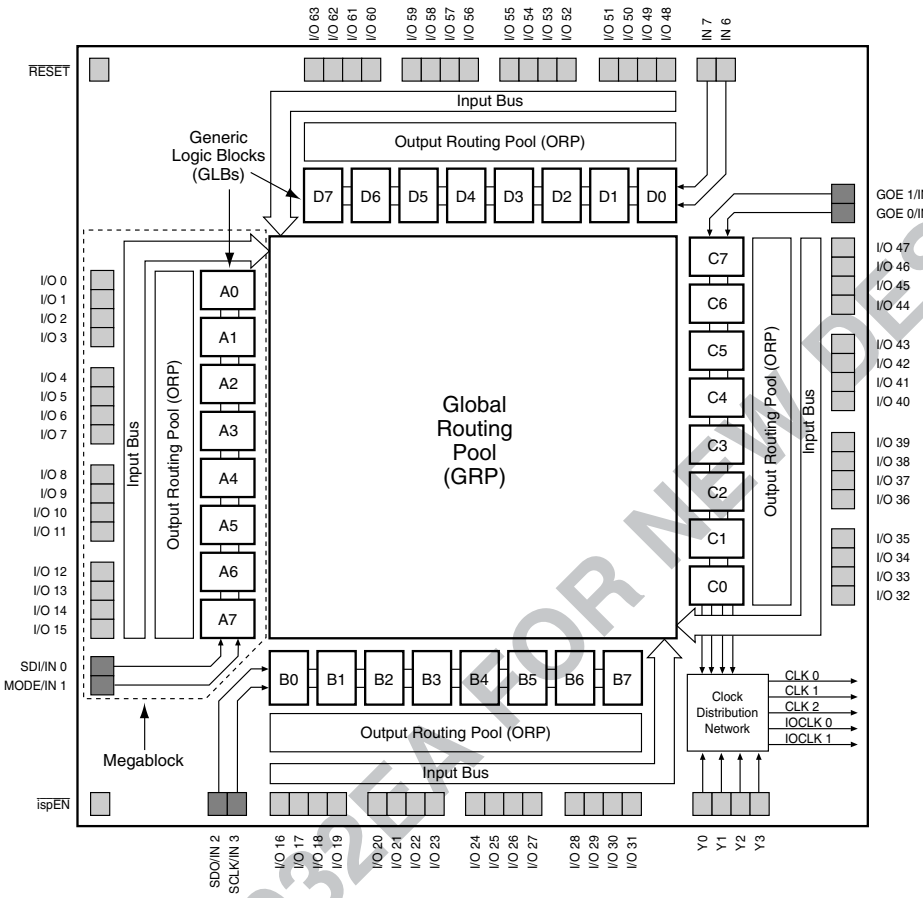
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## Functional Block Diagram

**Figure 1. ispLSI 1032E Functional Block Diagram**




The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI 1032E device contains four Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1032E device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI 1032E device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

USE ispLSI 1032E FOR NEW DESIGNS

## Absolute Maximum Ratings [1]

Supply Voltage $V_{cc}$ .....-0.5 to +7.0V

Input Voltage Applied..... -2.5 to $V_{CC}$ +1.0V

Off-State Output Voltage Applied ..... -2.5 to $V_{CC}$ +1.0V

Storage Temperature..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. ($T_J$) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Conditions

| SYMBOL | PARAMETER | | | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Commercial | $T_A$ = 0°C to + 70°C | 4.75 | 5.25 | V |
| | | Industrial | $T_A$ = -40°C to + 85°C | 4.5 | 5.5 | V |
| $V_{IL}$ | Input Low Voltage | | | 0 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | $V_{CC}$+1 | V |

Table 2-0005/1032E

## Capacitance ($T_A$=25°C, f=1.0 MHz)

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_1$ | Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance (Commercial/Industrial) | 8 | pf | $V_{CC}$= 5.0V, $V_{PIN}$= 2.0V |
| $C_2$ | Y0 Clock Capacitance | 15 | pf | $V_{CC}$= 5.0V, $V_{PIN}$= 2.0V |

Table 2-0006/1032E

## Data Retention Specifications

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|
| Data Retention | 20 | – | Years |
| Erase/Reprogram Cycles | 10000 | – | Cycles |

Table 2-0008/1032E

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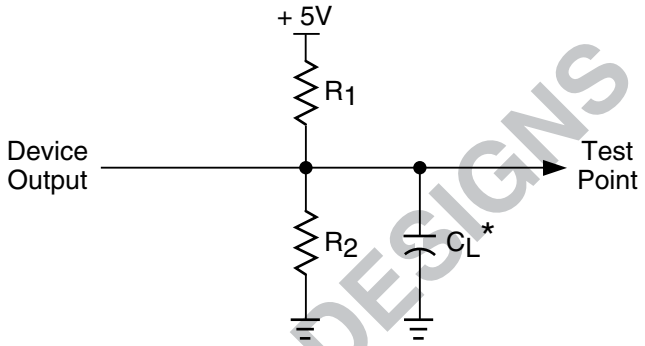
## Switching Test Conditions

| | | |
|---|---|---|
| Input Pulse Levels | GND to 3.0V | |
| Input Rise and Fall Time 10% to 90% | -125 | ≤ 2 ns |
| | Others | ≤ 3 ns |
| Input Timing Reference Levels | 1.5V | |
| Output Timing Reference Levels | 1.5V | |
| Output Load | See Figure 2 | |

Table 2-0003/1032E

3-state levels are measured 0.5V from steady-state active level.

**Figure 2. Test Load**




*$C_L$ includes Test Fixture and Probe Capacitance.

0213a

### Output Load Conditions (see Figure 2)

| TEST CONDITION | | R1 | R2 | CL |
|---|---|---|---|---|
| A | | 470Ω | 390Ω | 35pF |
| B | Active High | ∞ | 390Ω | 35pF |
| | Active Low | 470Ω | 390Ω | 35pF |
| C | Active High to Z at $V_{OH}$-0.5V | ∞ | 390Ω | 5pF |
| | Active Low to Z at $V_{OL}$+0.5V | 470Ω | 390Ω | 5pF |

Table 2-0004/1032E

## DC Electrical Characteristics

**Over Recommended Operating Conditions**

| SYMBOL | PARAMETER | CONDITION | | MIN. | TYP.[3] | MAX. | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8 mA | | – | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4 mA | | 2.4 | – | – | V |
| $I_{IL}$ | Input or I/O Low Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ (Max.) | | – | – | -10 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | 3.5V ≤ $V_{IN}$ ≤ $V_{CC}$ | | – | – | 10 | µA |
| $I_{IL-isp}$ | $\overline{ispEN}$ Input Low Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ | | – | – | -150 | µA |
| $I_{IL-PU}$ | I/O Active Pull-Up Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ | | – | – | -150 | µA |
| $I_{OS}$[1] | Output Short Circuit Current | $V_{CC}$ = 5V, $V_{OUT}$ = 0.5V | | – | – | -200 | mA |
| $I_{CC}$[2, 4] | Operating Power Supply Current | $V_{IL}$ = 0.5V, $V_{IH}$ = 3.0V | Commercial | – | 190 | – | mA |
| | | $f_{CLOCK}$ = 1 MHz | Industrial | – | 190 | – | mA |

Table 2-0007/1032E

1. One output at a time for a maximum duration of one second. $V_{OUT}$ = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at $V_{CC}$ = 5V and $T_A$ = 25°C.
4. Maximum $I_{CC}$ varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum $I_{CC}$.

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## External Timing Parameters

**Over Recommended Operating Conditions**

| PARAMETER | TEST COND.[4] | #[2] | DESCRIPTION[1] | -125 | | -100 | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| $t_{pd1}$ | A | 1 | Data Propagation Delay, 4PT Bypass, ORP Bypass | – | 7.5 | – | 10.0 | ns |
| $t_{pd2}$ | A | 2 | Data Propagation Delay, Worst Case Path | – | 10.0 | – | 12.5 | ns |
| $f_{max}$ (Int.) | A | 3 | Clock Frequency with Internal Feedback[3] | 125 | – | 100 | – | MHz |
| $f_{max}$ (Ext.) | – | 4 | Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$ | 91.0 | – | 71.0 | – | MHz |
| $f_{max}$ (Tog.) | – | 5 | Clock Frequency, Max. Toggle $\left(\frac{1}{twh + tw1}\right)$ | 167 | – | 125 | – | MHz |
| $t_{su1}$ | – | 6 | GLB Reg. Setup Time before Clock,4 PT Bypass | 5.0 | – | 7.0 | – | ns |
| $t_{co1}$ | A | 7 | GLB Reg. Clock to Output Delay, ORP Bypass | – | 5.0 | – | 6.0 | ns |
| $t_{h1}$ | – | 8 | GLB Reg. Hold Time after Clock, 4 PT Bypass | 0.0 | – | 0.0 | – | ns |
| $t_{su2}$ | – | 9 | GLB Reg. Setup Time before Clock | 6.0 | – | 8.0 | – | ns |
| $t_{co2}$ | – | 10 | GLB Reg. Clock to Output Delay | – | 6.0 | – | 7.0 | ns |
| $t_{h2}$ | – | 11 | GLB Reg. Hold Time after Clock | 0.0 | – | 0.0 | – | ns |
| $t_{r1}$ | A | 12 | Ext. Reset Pin to Output Delay | – | 10.0 | – | 13.5 | ns |
| $t_{rw1}$ | – | 13 | Ext. Reset Pulse Duration | 5.0 | – | 6.5 | – | ns |
| $t_{ptoeen}$ | B | 14 | Input to Output Enable | – | 12.0 | – | 15.0 | ns |
| $t_{ptoedis}$ | C | 15 | Input to Output Disable | – | 12.0 | – | 15.0 | ns |
| $t_{goeen}$ | B | 16 | Global OE Output Enable | – | 7.0 | – | 9.0 | ns |
| $t_{goedis}$ | C | 17 | Global OE Output Disable | – | 7.0 | – | 9.0 | ns |
| $t_{wh}$ | – | 18 | External Synchronous Clock Pulse Duration, High | 3.0 | – | 4.0 | – | ns |
| $t_{wl}$ | – | 19 | External Synchronous Clock Pulse Duration, Low | 3.0 | – | 4.0 | – | ns |
| $t_{su3}$ | – | 20 | I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3) | 3.0 | – | 3.5 | – | ns |
| $t_{h3}$ | – | 21 | I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3) | 0.0 | – | 0.0 | – | ns |

Table 2-0030A/1032E

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

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## External Timing Parameters

**Over Recommended Operating Conditions**

| PARAMETER | TEST COND.[4] | #[2] | DESCRIPTION[1] | -90 | | -80 | | -70 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{pd1}$ | A | 1 | Data Propagation Delay, 4PT Bypass, ORP Bypass | – | 10.0 | – | 12.0 | – | 15.0 | ns |
| $t_{pd2}$ | A | 2 | Data Propagation Delay, Worst Case Path | – | 12.5 | – | 15.0 | – | 17.5 | ns |
| $f_{max}$ (Int.) | A | 3 | Clock Frequency with Internal Feedback[3] | 90.0 | – | 80.0 | – | 70.0 | – | MHz |
| $f_{max}$ (Ext.) | – | 4 | Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$ | 69.0 | – | 61.0 | – | 56.0 | – | MHz |
| $f_{max}$ (Tog.) | – | 5 | Clock Frequency, Max. Toggle $\left(\frac{1}{twh + twl}\right)$ | 125 | – | 111 | – | 100 | – | MHz |
| $t_{su1}$ | – | 6 | GLB Reg. Setup Time before Clock,4 PT Bypass | 7.5 | – | 8.5 | – | 9.0 | – | ns |
| $t_{co1}$ | A | 7 | GLB Reg. Clock to Output Delay, ORP Bypass | – | 6.0 | – | 6.5 | – | 7.0 | ns |
| $t_{h1}$ | – | 8 | GLB Reg. Hold Time after Clock, 4 PT Bypass | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| $t_{su2}$ | – | 9 | GLB Reg. Setup Time before Clock | 8.5 | – | 10.0 | – | 11.0 | – | ns |
| $t_{co2}$ | – | 10 | GLB Reg. Clock to Output Delay | – | 7.0 | – | 7.5 | – | 8.0 | ns |
| $t_{h2}$ | – | 11 | GLB Reg. Hold Time after Clock | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| $t_{r1}$ | A | 12 | Ext. Reset Pin to Output Delay | – | 13.5 | – | 14.0 | – | 15.0 | ns |
| $t_{rw1}$ | – | 13 | Ext. Reset Pulse Duration | 6.5 | – | 8.0 | – | 10.0 | – | ns |
| $t_{ptoeen}$ | B | 14 | Input to Output Enable | – | 15.0 | – | 16.5 | – | 18.0 | ns |
| $t_{ptoedis}$ | C | 15 | Input to Output Disable | – | 15.0 | – | 16.5 | – | 18.0 | ns |
| $t_{goeen}$ | B | 16 | Global OE Output Enable | – | 9.0 | – | 10.0 | – | 12.0 | ns |
| $t_{goedis}$ | C | 17 | Global OE Output Disable | – | 9.0 | – | 10.0 | – | 12.0 | ns |
| $t_{wh}$ | – | 18 | External Synchronous Clock Pulse Duration, High | 4.0 | – | 4.5 | – | 5.0 | – | ns |
| $t_{wl}$ | – | 19 | External Synchronous Clock Pulse Duration, Low | 4.0 | – | 4.5 | – | 5.0 | – | ns |
| $t_{su3}$ | – | 20 | I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3) | 3.5 | – | 3.5 | – | 4.0 | – | ns |
| $t_{h3}$ | – | 21 | I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3) | 0.0 | – | 0.0 | – | 0.0 | – | ns |

Table 2-0030B/1032E

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

USE ispLSI 1032EA FOR NEW DESIGNS

## Internal Timing Parameters[1]

| PARAM. | # [2] | DESCRIPTION | -125 | | -100 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Inputs** | | | | | | | |
| $t_{iobp}$ | 22 | I/O Register Bypass | – | 0.3 | – | 0.3 | ns |
| $t_{iolat}$ | 23 | I/O Latch Delay | – | 1.9 | – | 2.3 | ns |
| $t_{iosu}$ | 24 | I/O Register Setup Time before Clock | 3.0 | – | 3.5 | – | ns |
| $t_{ioh}$ | 25 | I/O Register Hold Time after Clock | 0.0 | – | 0.0 | – | ns |
| $t_{ioco}$ | 26 | I/O Register Clock to Out Delay | – | 4.6 | – | 5.0 | ns |
| $t_{ior}$ | 27 | I/O Register Reset to Out Delay | – | 4.6 | – | 5.0 | ns |
| $t_{din}$ | 28 | Dedicated Input Delay | – | 2.3 | – | 2.7 | ns |
| **GRP** | | | | | | | |
| $t_{grp1}$ | 29 | GRP Delay, 1 GLB Load | – | 1.8 | – | 1.9 | ns |
| $t_{grp4}$ | 30 | GRP Delay, 4 GLB Loads | – | 2.0 | – | 2.4 | ns |
| $t_{grp8}$ | 31 | GRP Delay, 8 GLB Loads | – | 2.3 | – | 2.4 | ns |
| $t_{grp16}$ | 32 | GRP Delay, 16 GLB Loads | – | 2.8 | – | 3.0 | ns |
| $t_{grp32}$ | 33 | GRP Delay, 32 GLB Loads | – | 3.8 | – | 4.2 | ns |
| **GLB** | | | | | | | |
| $t_{4ptbpc}$ | 34 | 4 Prod.Term Bypass Path Delay (Combinatorial) | – | 3.9 | – | 5.3 | ns |
| $t_{4ptbpr}$ | 35 | 4 Prod. Term Bypass Path Delay (Registered) | – | 4.0 | – | 5.3 | ns |
| $t_{1ptxor}$ | 36 | 1 Prod.Term/XOR Path Delay | – | 3.6 | – | 4.6 | ns |
| $t_{20ptxor}$ | 37 | 20 Prod. Term/XOR Path Delay | – | 5.0 | – | 5.8 | ns |
| $t_{xoradj}$ | 38 | XOR Adjacent Path Delay [3] | – | 5.0 | – | 6.3 | ns |
| $t_{gbp}$ | 39 | GLB Register Bypass Delay | – | 0.4 | – | 1.0 | ns |
| $t_{gsu}$ | 40 | GLB Register Setup Time before Clock | 0.1 | – | 0.5 | – | ns |
| $t_{gh}$ | 41 | GLB Register Hold Time after Clock | 4.5 | – | 5.8 | – | ns |
| $t_{gco}$ | 42 | GLB Register Clock to Output Delay | – | 2.3 | – | 2.5 | ns |
| $t_{gro}$ | 43 | GLB Register Reset to Output Delay | – | 4.9 | – | 6.2 | ns |
| $t_{ptre}$ | 44 | GLB Prod.Term Reset to Register Delay | – | 3.9 | – | 4.5 | ns |
| $t_{ptoe}$ | 45 | GLB Prod. Term Output Enable to I/O Cell Delay | – | 5.4 | – | 7.2 | ns |
| $t_{ptck}$ | 46 | GLB Prod. Term Clock Delay | 2.9 | 4.0 | 3.5 | 4.7 | ns |
| **ORP** | | | | | | | |
| $t_{orp}$ | 47 | ORP Delay | – | 1.0 | – | 1.0 | ns |
| $t_{orpbp}$ | 48 | ORP Bypass Delay | – | 0.0 | – | 0.0 | ns |

Table 2-0036A/1032E

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

USE ispLSI 1032EA FOR NEW DESIGNS

## Internal Timing Parameters[1]

| PARAM. | # [2] | DESCRIPTION | -90 | | -80 | | -70 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| **Inputs** | | | | | | | | | |
| $t_{iobp}$ | 22 | I/O Register Bypass | – | 0.3 | – | 0.3 | – | 0.3 | ns |
| $t_{iolat}$ | 23 | I/O Latch Delay | – | 2.3 | – | 2.7 | – | 3.3 | ns |
| $t_{iosu}$ | 24 | I/O Register Setup Time before Clock | 3.5 | – | 3.5 | – | 4.0 | – | ns |
| $t_{ioh}$ | 25 | I/O Register Hold Time after Clock | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| $t_{ioco}$ | 26 | I/O Register Clock to Out Delay | – | 5.0 | – | 5.4 | – | 6.1 | ns |
| $t_{ior}$ | 27 | I/O Register Reset to Out Delay | – | 5.0 | – | 5.4 | – | 6.0 | ns |
| $t_{din}$ | 28 | Dedicated Input Delay | – | 2.6 | – | 2.8 | – | 2.8 | ns |
| **GRP** | | | | | | | | | |
| $t_{grp1}$ | 29 | GRP Delay, 1 GLB Load | – | 2.1 | – | 2.2 | – | 2.5 | ns |
| $t_{grp4}$ | 30 | GRP Delay, 4 GLB Loads | – | 2.3 | – | 2.5 | – | 2.5 | ns |
| $t_{grp8}$ | 31 | GRP Delay, 8 GLB Loads | – | 2.6 | – | 2.8 | – | 3.2 | ns |
| $t_{grp16}$ | 32 | GRP Delay, 16 GLB Loads | – | 3.2 | – | 3.5 | – | 4.0 | ns |
| $t_{grp32}$ | 33 | GRP Delay, 32 GLB Loads | – | 4.4 | – | 4.8 | – | 5.6 | ns |
| **GLB** | | | | | | | | | |
| $t_{4ptbpc}$ | 34 | 4 Prod.Term Bypass Path Delay (Combinatorial) | – | 5.7 | – | 7.1 | – | 8.8 | ns |
| $t_{4ptbpr}$ | 35 | 4 Prod. Term Bypass Path Delay (Registered) | – | 6.1 | – | 6.7 | – | 7.2 | ns |
| $t_{1ptxor}$ | 36 | 1 Prod.Term/XOR Path Delay | – | 5.6 | – | 6.6 | – | 8.3 | ns |
| $t_{20ptxor}$ | 37 | 20 Prod. Term/XOR Path Delay | – | 6.8 | – | 7.8 | – | 8.7 | ns |
| $t_{xoradj}$ | 38 | XOR Adjacent Path Delay [3] | – | 7.1 | – | 8.2 | – | 9.2 | ns |
| $t_{gbp}$ | 39 | GLB Register Bypass Delay | – | 0.4 | – | 1.3 | – | 1.6 | ns |
| $t_{gsu}$ | 40 | GLB Register Setup Time before Clock | 0.2 | – | 0.5 | – | 0.5 | – | ns |
| $t_{gh}$ | 41 | GLB Register Hold Time after Clock | 6.8 | – | 7.9 | – | 8.8 | – | ns |
| $t_{gco}$ | 42 | GLB Register Clock to Output Delay | – | 2.9 | – | 2.9 | – | 2.9 | ns |
| $t_{gro}$ | 43 | GLB Register Reset to Output Delay | – | 6.3 | – | 6.4 | – | 6.8 | ns |
| $t_{ptre}$ | 44 | GLB Prod.Term Reset to Register Delay | – | 5.1 | – | 5.5 | – | 5.8 | ns |
| $t_{ptoe}$ | 45 | GLB Prod. Term Output Enable to I/O Cell Delay | – | 7.1 | – | 8.0 | – | 9.0 | ns |
| $t_{ptck}$ | 46 | GLB Prod. Term Clock Delay | 4.1 | 5.3 | 4.5 | 5.8 | 4.8 | 6.2 | ns |
| **ORP** | | | | | | | | | |
| $t_{orp}$ | 47 | ORP Delay | – | 1.0 | – | 1.0 | – | 1.0 | ns |
| $t_{orpbp}$ | 48 | ORP Bypass Delay | – | 0.0 | – | 0.0 | – | 0.0 | ns |

Table 2-0036B/1032E

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

USE ispLSI 1032EA FOR NEW DESIGNS

## Internal Timing Parameters[1]

| PARAM. | # | DESCRIPTION | -125 | | -100 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Outputs** | | | | | | | |
| $t_{ob}$ | 49 | Output Buffer Delay | – | 1.3 | – | 2.0 | ns |
| $t_{sl}$ | 50 | Output Buffer Delay, Slew Limited Adder | – | 9.9 | – | 10.0 | ns |
| $t_{oen}$ | 51 | I/O Cell OE to Output Enabled | – | 4.3 | – | 5.1 | ns |
| $t_{odis}$ | 52 | I/O Cell OE to Output Disabled | – | 4.3 | – | 5.1 | ns |
| $t_{goe}$ | 53 | Global OE | – | 2.7 | – | 3.9 | ns |
| **Clocks** | | | | | | | |
| $t_{gy0}$ | 54 | Clk Delay, Y0 to Global GLB Clk Line (Ref. clk) | 1.4 | 1.4 | 1.5 | 1.5 | ns |
| $t_{gy1/2}$ | 55 | Clk Delay, Y1 or Y2 to Global GLB Clk Line | 1.4 | 1.4 | 1.5 | 1.5 | ns |
| $t_{gcp}$ | 56 | Clk Delay, Clock GLB to Global GLB Clk Line | 0.8 | 1.8 | 0.8 | 1.8 | ns |
| $t_{ioy2/3}$ | 57 | Clk Delay, Y2 or Y3 to I/O Cell Global Clk Line | 0.0 | 0.0 | 0.0 | 0.0 | ns |
| $t_{iocp}$ | 58 | Clk Delay, Clk GLB to I/O Cell Global Clk Line | 0.8 | 1.8 | 0.8 | 1.8 | ns |
| **Global Reset** | | | | | | | |
| $t_{gr}$ | 59 | Global Reset to GLB and I/O Registers | – | 2.8 | – | 4.3 | ns |

1. Internal Timing Parameters are not tested and are for reference only.

Table 2-0037A/1032E

USE ispLSI 1032EA FOR NEW DESIGNS

## Internal Timing Parameters[1]

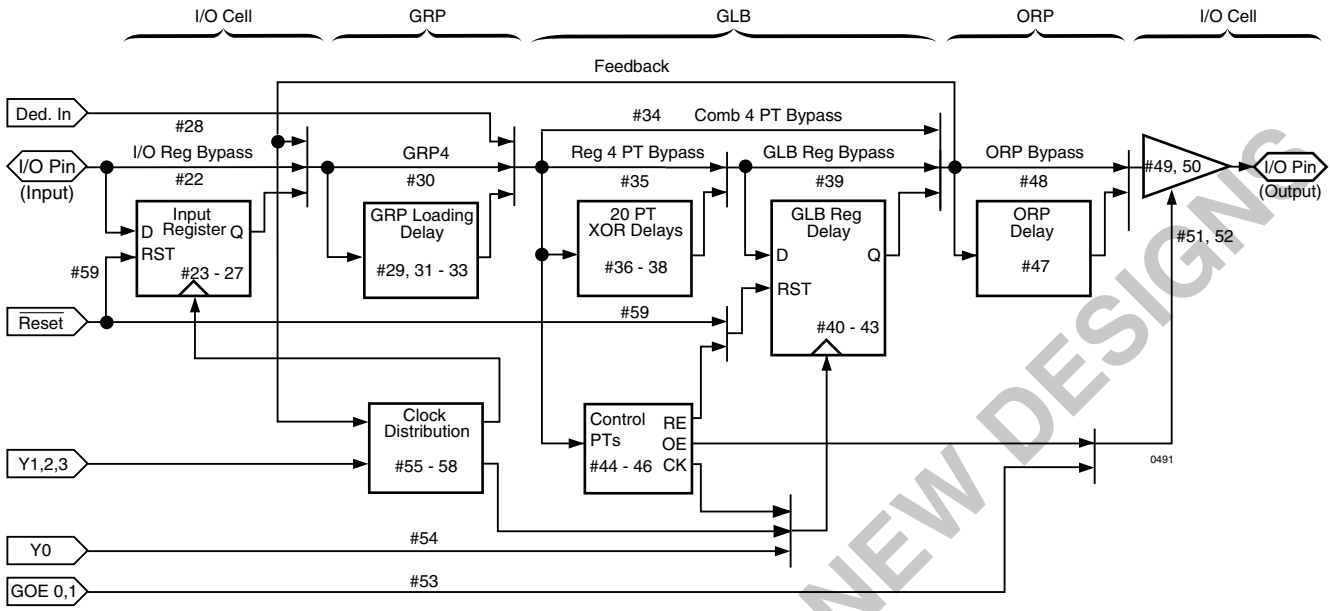
| PARAM. | # | DESCRIPTION | -90 | | -80 | | -70 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| **Outputs** | | | | | | | | | |
| $t_{ob}$ | 49 | Output Buffer Delay | – | 1.7 | – | 2.1 | – | 2.6 | ns |
| $t_{sl}$ | 50 | Output Buffer Delay, Slew Limited Adder | – | 10.0 | – | 10.0 | – | 10.0 | ns |
| $t_{oen}$ | 51 | I/O Cell OE to Output Enabled | – | 5.3 | – | 5.7 | – | 6.2 | ns |
| $t_{odis}$ | 52 | I/O Cell OE to Output Disabled | – | 5.3 | – | 5.7 | – | 6.2 | ns |
| $t_{goe}$ | 53 | Global OE | – | 3.7 | – | 4.3 | – | 5.8 | ns |
| **Clocks** | | | | | | | | | |
| $t_{gy0}$ | 54 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 1.4 | 1.4 | 1.5 | 1.5 | 1.5 | 1.5 | ns |
| $t_{gy1/2}$ | 55 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 2.4 | 2.9 | 2.6 | 3.1 | 1.5 | 1.5 | ns |
| $t_{gcp}$ | 56 | Clock Delay, Clock GLB to Global GLB Clock Line | 0.8 | 1.8 | 0.8 | 1.8 | 0.8 | 1.8 | ns |
| $t_{ioy2/3}$ | 57 | Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | ns |
| $t_{iocp}$ | 58 | Clock Delay, Clock GLB to I/O Cell Global Clock Line | 0.8 | 1.8 | 0.8 | 1.8 | 0.8 | 1.8 | ns |
| **Global Reset** | | | | | | | | | |
| $t_{gr}$ | 59 | Global Reset to GLB and I/O Registers | – | 4.5 | – | 4.5 | – | 4.6 | ns |

1. Internal Timing Parameters are not tested and are for reference only.

Table 2-0037B/1032E

USE ispLSI 1032EA FOR NEW DESIGNS

## ispLSI 1032E Timing Model




### Derivations of tsu, th and tco from the Product Term Clock[1]

**t**su = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) – (**t**iobp + **t**grp4 + **t**ptck(min))
= (#22 + #30 + #37) + (#40) – (#22 + #30 + #46)
2.2 ns = (0.3 + 2.0 + 5.0) + (0.1) – (0.3 + 2.0 + 2.9)

**t**h = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gh) – (**t**iobp + **t**grp4 + **t**20ptxor)
= (#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
3.5 ns = (0.3 + 2.0 + 4.0) + (4.5) – (0.3 + 2.0 + 5.0)

**t**co = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#22 + #30 + #46) + (#42) + (#47 + #49)
10.9 ns = (0.3 + 2.0 + 4.0) + (2.3) + (1.0 + 1.3)

### Derivations of tsu, th and tco from the Clock GLB [1]

**t**su = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) – (**t**gy0(min) + **t**gco + **t**gcp(min))
= (#22 + #30 + #37) + (#40) – (#54 + #42 + #56)
2.9 ns = (0.3 + 2.0 + 5.0) + (0.1) – (1.4 + 2.3 + 0.8)

**t**h = Clock (max) + Reg h - Logic
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) – (**t**iobp + **t**grp4 + **t**20ptxor)
= (#54 + #42 + #56) + (#41) – (#22 + #30 + #37)
2.7 ns = (1.4 + 2.3 + 1.8) + (4.5) – (0.3 + 2.0 + 5.0)

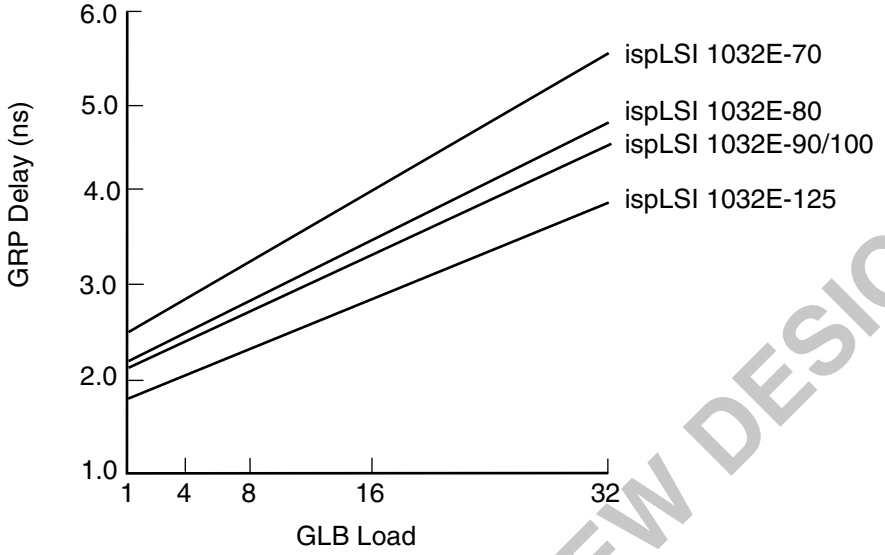
**t**co = Clock (max) + Reg co + Output
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#54 + #42 + #56) + (#42) + (#47 + #49)
5.5 ns = (1.4 + 2.3 + 1.8) + (2.3) + (1.0 + 1.3)

1. Calculations are based upon timing specifications for the ispLSI 1032E-125.

Table 2-0042a/1032E

USE ispLSI 1032EA FOR NEW DESIGNS

## Maximum GRP Delay vs GLB Loads

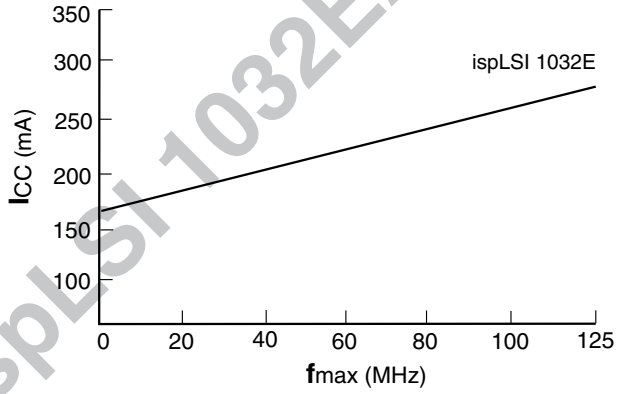



GRP/GLB/1032E

## Power Consumption

Power consumption in the ispLSI 1032E device depends on two primary factors: the speed at which the device is operating, and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**




Notes: Configuration of eight 16-bit counters
Typical current at 5V, 25°C

$I_{CC}$ can be estimated for the ispLSI 1032E using the following equation:

$I_{CC}$(mA) = 15 + (# of PTs * 0.59) + (# of nets * Max freq * 0.0078)

Where:

# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The $I_{CC}$ estimate is based on typical conditions ($V_{CC}$ = 5.0V, room temperature) and an assumption of four GLB loads on average exists. These values are for estimates only. Since the value of $I_{CC}$ is sensitive to operating conditions and the program in the device, the actual $I_{CC}$ should be verified.

0127/1032E

USE ispLSI 1032EA FOR NEW DESIGNS

## Pin Description

| NAME | PLCC PIN NUMBERS | TQFP PIN NUMBERS | DESCRIPTION |
|---|---|---|---|
| I/O 0 - I/O 3<br>I/O 4 - I/O 7<br>I/O 8 - I/O 11<br>I/O 12 - I/O 15<br>I/O 16 - I/O 19<br>I/O 20 - I/O 23<br>I/O 24 - I/O 27<br>I/O 28 - I/O 31<br>I/O 32 - I/O 35<br>I/O 36 - I/O 39<br>I/O 40 - I/O 43<br>I/O 44 - I/O 47<br>I/O 48 - I/O 51<br>I/O 52 - I/O 55<br>I/O 56 - I/O 59<br>I/O 60 - I/O 63 | 26, 27, 28, 29,<br>30, 31, 32, 33,<br>34, 35, 36, 37,<br>38, 39, 40, 41,<br>45, 46, 47, 48,<br>49, 50, 51, 52,<br>53, 54, 55, 56,<br>57, 58, 59, 60,<br>68, 69, 70, 71,<br>72, 73, 74, 75,<br>76, 77, 78, 79,<br>80, 81, 82, 83,<br>3, 4, 5, 6,<br>7, 8, 9, 10,<br>11, 12, 13, 14,<br>15, 16, 17, 18 | 17, 18, 19, 20,<br>21, 22, 23, 28,<br>29, 30, 31, 32,<br>33, 34, 35, 36,<br>40, 41, 42, 43,<br>44, 45, 46, 47,<br>48, 53, 54, 55,<br>56, 57, 58, 59,<br>67, 68, 69, 70,<br>71, 72, 73, 78,<br>79, 80, 81, 82,<br>83, 84, 85, 86,<br>90, 91, 92, 93,<br>94, 95, 96, 97,<br>98, 3, 4, 5,<br>6, 7, 8, 9 | Input/Output Pins - These are the general purpose I/O pins used by the logic array. |
| GOE 0/IN 4[3] | 67 | 66 | This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin. |
| GOE 1/IN 5[3] | 84 | 87 | This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin. |
| IN 6, IN 7 | 2, 19 | 89, 10 | Dedicated input pins to the device. |
| $\overline{\text{ispEN}}$ | 23 | 14 | Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. |
| SDI/IN 0[2] | 25 | 16 | Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 is also used as one of the two control pins for the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. |
| MODE/IN 1[2] | 42 | 37 | Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. |
| SDO/IN 2[2] | 44 | 39 | Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. |
| SCLK/IN 3[2] | 61 | 60 | Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. |
| $\overline{\text{RESET}}$ | 24 | 15 | Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. |
| Y0 | 20 | 11 | Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device. |
| Y1 | 66 | 65 | Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device. |
| Y2 | 63 | 62 | Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device. |
| Y3 | 62 | 61 | Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device. |
| GND | 1, 22, 43, 64 | 13, 38, 63, 88 | Ground (GND) |
| VCC | 21, 65 | 12, 64 | Vcc |
| NC[1] | | 1, 2, 24, 25,<br>26, 27, 49, 50,<br>51, 52, 74, 75,<br>76, 77, 99, 100 | No connect. |

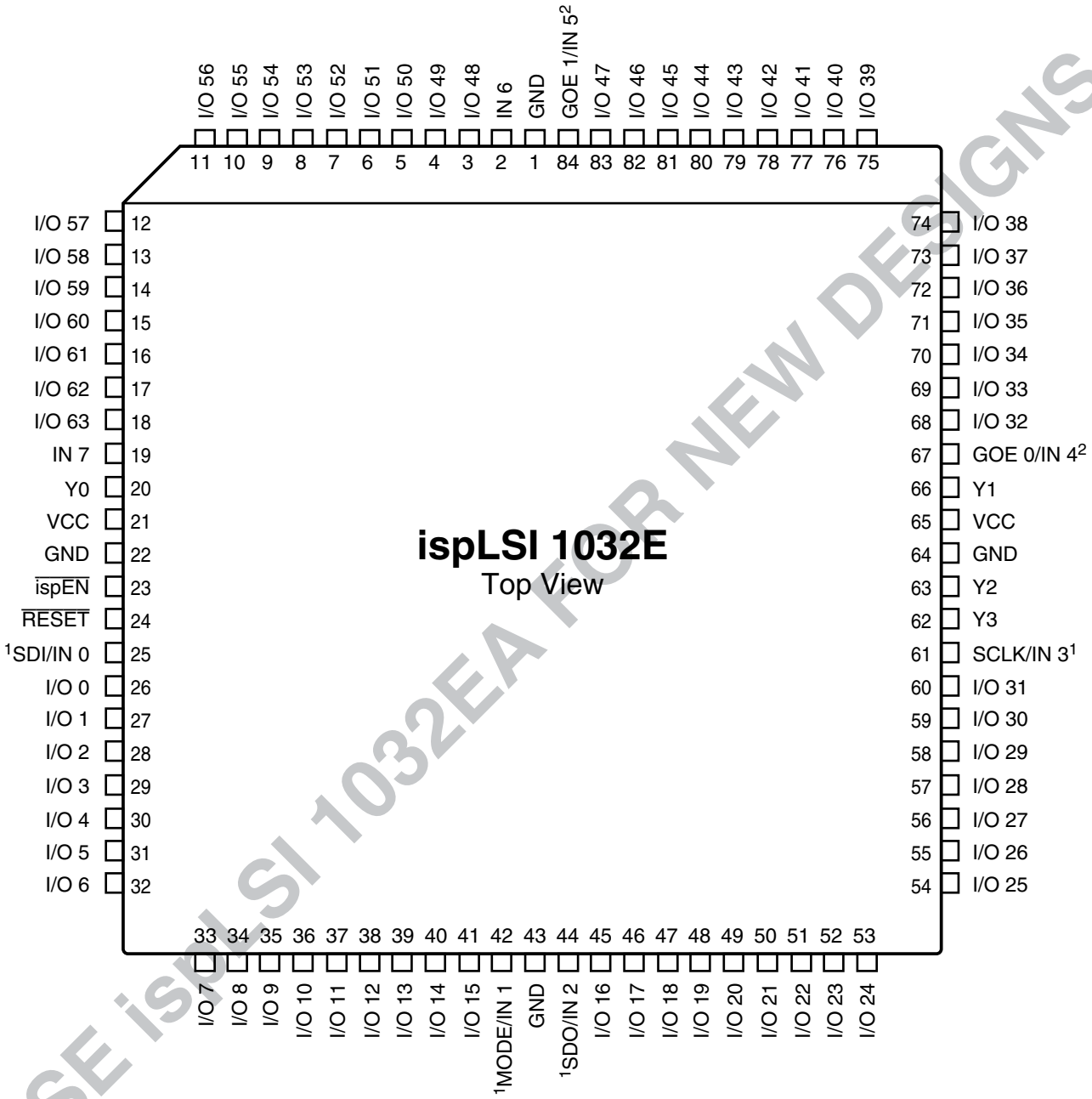
Table 2-0002A/1032E

1. NC pins are not to be connected to any active signals, Vcc or GND.
2. Pins have dual function capability.
3. Pins have dual function capability which is software selectable.

USE ispLSI 1032E FOR NEW DESIGNS

## Pin Configurations

**ispLSI 1032E 84-Pin PLCC Pinout Diagram**



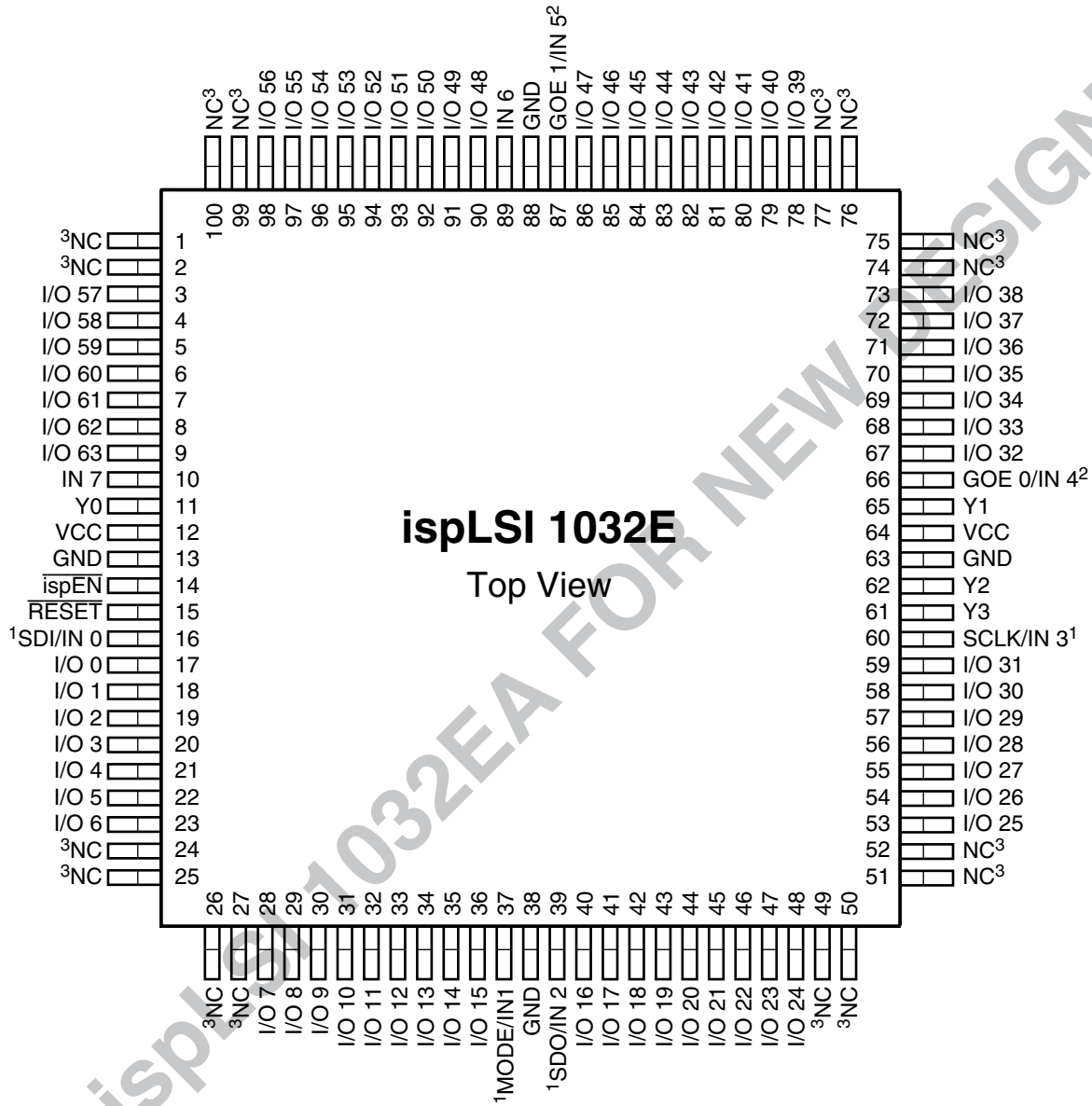

1. Pins have dual function capability.
3. Pins have dual function capability which is software selectable.

0123-32-isp

USE ispLSI 1032EA FOR NEW DESIGNS

## Pin Configurations

**ispLSI 1032E 100-Pin TQFP Pinout Diagram**

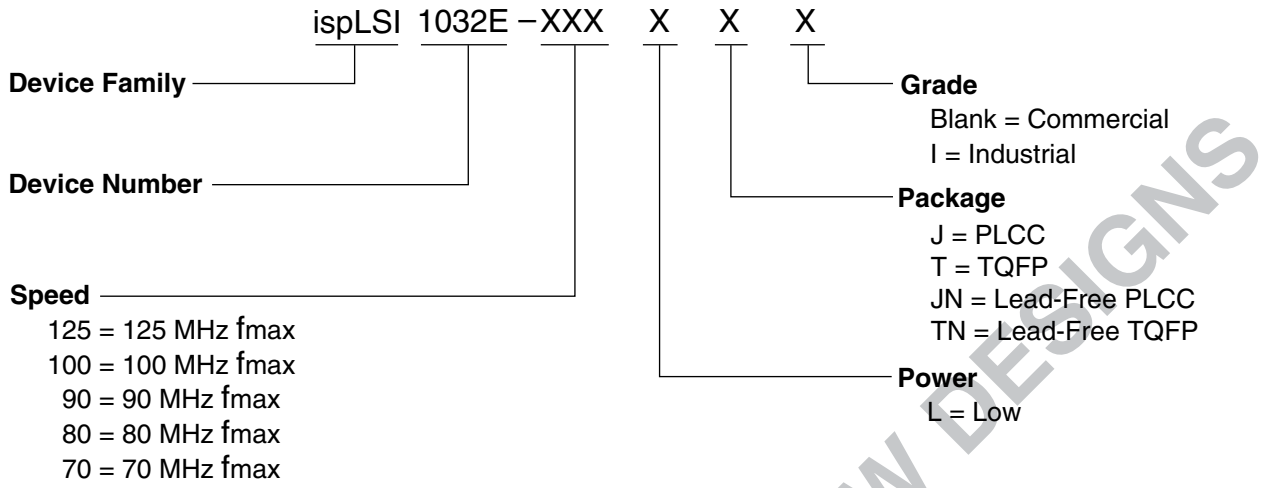



1. Pins have dual function capability.
2. Pins have dual function capability which is software selectable.
3. NC pins are not to be connected to any active signal, VCC or GND.

0766A-32E-isp

USE ispLSI 1032EA FOR NEW DESIGNS

## Part Number Description




## ispLSI 1032E Ordering Information

### Conventional Packaging

**COMMERCIAL**

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|---|---|---|---|---|
| ispLSI | 125 | 7.5 | ispLSI 1032E-125LJ | 84-Pin PLCC |
| | 125 | 7.5 | ispLSI 1032E-125LT | 100-Pin TQFP |
| | 100 | 10 | ispLSI 1032E-100LJ | 84-Pin PLCC |
| | 100 | 10 | ispLSI 1032E-100LT | 100-Pin TQFP |
| | 90 | 10 | ispLSI 1032E-90LJ[1] | 84-Pin PLCC |
| | 90 | 10 | ispLSI 1032E-90LT[1] | 100-Pin TQFP |
| | 80 | 12 | ispLSI 1032E-80LJ[1] | 84-Pin PLCC |
| | 80 | 12 | ispLSI 1032E-80LT[1] | 100-Pin TQFP |
| | 70 | 15 | ispLSI 1032E-70LJ | 84-Pin PLCC |
| | 70 | 15 | ispLSI 1032E-70LT | 100-Pin TQFP |

1. Converted to -100 speed grade per PCN# 001-97.

**INDUSTRIAL**

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|---|---|---|---|---|
| ispLSI | 70 | 15 | ispLSI 1032E-70LJI | 84-Pin PLCC |
| | 70 | 15 | ispLSI 1032E-70LTI | 100-Pin TQFP |

USE ispLSI 1032EA FOR NEW DESIGNS

## ispLSI 1032E Ordering Information (Cont.)

### Lead-Free Packaging

**COMMERCIAL**

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|---|---|---|---|---|
| ispLSI | 125 | 7.5 | ispLSI 1032E-125LJN | Lead-Free 84-Pin PLCC[1] |
| | 125 | 7.5 | ispLSI 1032E-125LTN | Lead-Free 100-Pin TQFP |
| | 100 | 10 | ispLSI 1032E-100LJN | Lead-Free 84-Pin PLCC[1] |
| | 100 | 10 | ispLSI 1032E-100LTN | Lead-Free 100-Pin TQFP |
| | 70 | 15 | ispLSI 1032E-70LJN | Lead-Free 84-Pin PLCC[1] |
| | 70 | 15 | ispLSI 1032E-70LTN | Lead-Free 100-Pin TQFP |

1. 84-PLCC lead-free package is MSL4. Refer to "Handling Moisture Sensitive Packages" document on www.latticesemi.com.

**INDUSTRIAL**

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|---|---|---|---|---|
| ispLSI | 70 | 15 | ispLSI 1032E-70LJNI | Lead-Free 84-Pin PLCC[1] |
| | 70 | 15 | ispLSI 1032E-70LTNI | Lead-Free 100-Pin TQFP |

1. 84-PLCC lead-free package is MSL4. Refer to "Handling Moisture Sensitive Packages" document on www.latticesemi.com.

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| — | 08 | Previous Lattice release. |
| August 2006 | 09 | Updated for lead-free package options. |

USE ispLSI 1032EA FOR NEW DESIGNS