ON Semiconductor

Is Now



To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and onsemi and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

KAI-11002

4008 (H) x 2672 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAI−11002 Image Sensor is a high-performance 11-million pixel sensor designed for professional digital still camera applications. The 9.0 μm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The two high-speed outputs and binning capabilities allow for 1−3 frames per second (fps) video rate for the progressively scanned images. The vertical overflow drain structure provides anti-blooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD, Progressive Scan
Total Number of Pixels	4072 (H) × 2720 (V) = 11.1 M
Number of Effective Pixels	4033 (H) × 2688 (V) = 10.8 M
Number of Active Pixels	4008 (H) × 2672 (V) = 10.7 M
Number of Outputs	1 or 2
Pixel Size	9.0 μm (H) × 9.0 μm (V)
Active Image Size	37.25 mm (H) × 25.70 mm (V), 43.3 mm (Diagonal), 35 mm Optical Format
Aspect Ratio	3:2
Saturation Signal	60,000 e^-
Quantum Efficiency KAI−11002−ABA KAI−11002−CBA (RGB) KAI−11002−FBA (RGB)	 50% 32%, 34%, 40% 35%, 38%, 40%
Output Sensitivity	13 μV/e^-
Total Noise	30 e^-
Dark Current	< 50 mV/s
Dark Current Doubling Temperature	7°C
Dynamic Range	66 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	> 1000X
Smear	< −80 dB
Image Lag	< 10 e^-
Maximum Data Rate	28 MHz
Package	40-pin, CERDIP, 0.070″ Pin Spacing
Cover Glass	AR Coated or Clear Glass

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.



Figure 1. KAI−11002 Interline CCD Image Sensor

Features

- High Resolution
- High Sensitivity
- High Dynamic Range
- Low Noise Architecture
- High Frame Rate
- Binning Capability for Higher Frame Rate
- Electronic Shutter

Applications

- Industrial Inspection
- Aerial Photography

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2016

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−11002 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−11002−AAA−CR−B1*	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Grade 1	KAI−11002−AAA Serial Number
KAI−11002−AAA−CR−B2*	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Grade 2	
KAI−11002−AAA−CR−AE*	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Sample	
KAI−11002−AAA−CP−B1	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, Grade 1	
KAI−11002−AAA−CP−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, Grade 2	
KAI−11002−AAA−CP−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, Engineering Sample	
KAI−11002−ABA−CD−BX	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Special Grade	KAI−11002−ABA Serial Number
KAI−11002−ABA−CD−B0	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 0	
KAI−11002−ABA−CD−B1	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 1	
KAI−11002−ABA−CD−B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	
KAI−11002−ABA−CD−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Boht Sides), Engineering Sample	
KAI−11002−ABA−CR−B1*	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Grade 1	
KAI−11002−ABA−CR−B2*	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Grade 2	
KAI−11002−ABA−CR−AE*	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Sample	
KAI−11002−ABA−CP−B1	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, Grade 1	
KAI−11002−ABA−CP−B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, Grade 2	
KAI−11002−ABA−CP−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass, Engineering Sample	
KAI−11002−FBA−CD−B1	Gen2 Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 1	KAI−11002−FBA Serial Number
KAI−11002−FBA−CD−B2	Gen2 Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	
KAI−11002−FBA−CD−AE	Gen2 Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KAI−11002−CAA−CD−B1*	Gen1 Color (Bayer RGB), No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 1	KAI−11002−CAA Serial Number
KAI−11002−CAA−CD−B2*	Gen1 Color (Bayer RGB), No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	
KAI−11002−CAA−CD−AE*	Gen1 Color (Bayer RGB), No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	

Table 2. ORDERING INFORMATION − KAI−11002 IMAGE SENSOR (continued)

Part Number	Description	Marking Code
KAI−11002−CBA−CD−B1*	Gen1 Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 1	KAI−11002−CBA Serial Number
KAI−11002−CBA−CD−B2*	Gen1 Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	
KAI−11002−CBA−CD−AE*	Gen1 Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	

*Not recommended for new designs.

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAI−11002−12−30−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

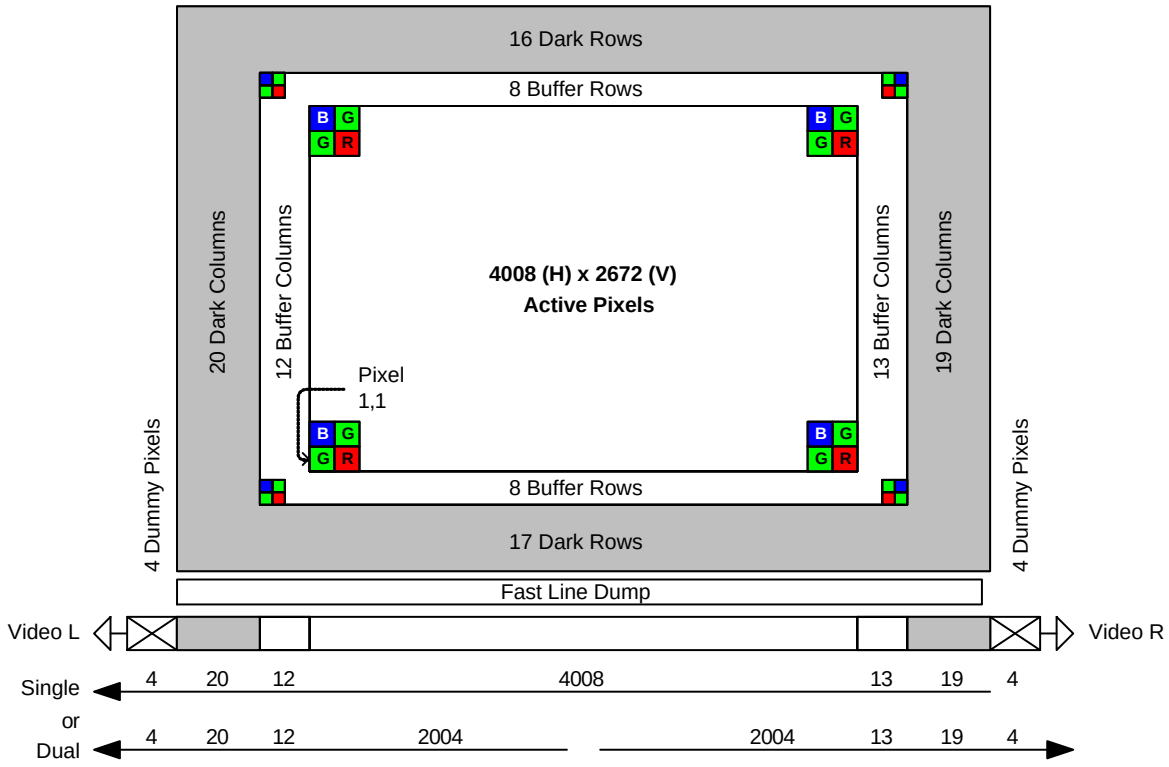


Figure 2. Block Diagram

There are 17 light shielded rows followed 2,688 photoactive rows and finally 16 more light shielded rows. The first 8 and the last 8 photoactive rows are buffer rows giving a total of 2,672 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 4 empty pixels of each line do not receive charge from the vertical shift register. The next 20 pixels receive charge from the left light shielded edge followed by 4,033 photosensitive pixels and finally 19 more light shielded pixels from the right edge of the sensor. The first 12 and last 13 photosensitive pixels are buffer pixels giving a total of 4,008 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. For the Video L each row consists of 4 empty pixels followed by 20 light shielded pixels followed by 2,016 photosensitive pixels. For the Video R each row consists of 4 empty pixels followed by 19 light shielded pixels followed by 2,017 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

The dark rows are not entirely dark and so should not be used for a dark reference level. Use the dark columns on the left or right side of the image sensor as a dark reference.

Of the dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns.

Pixel

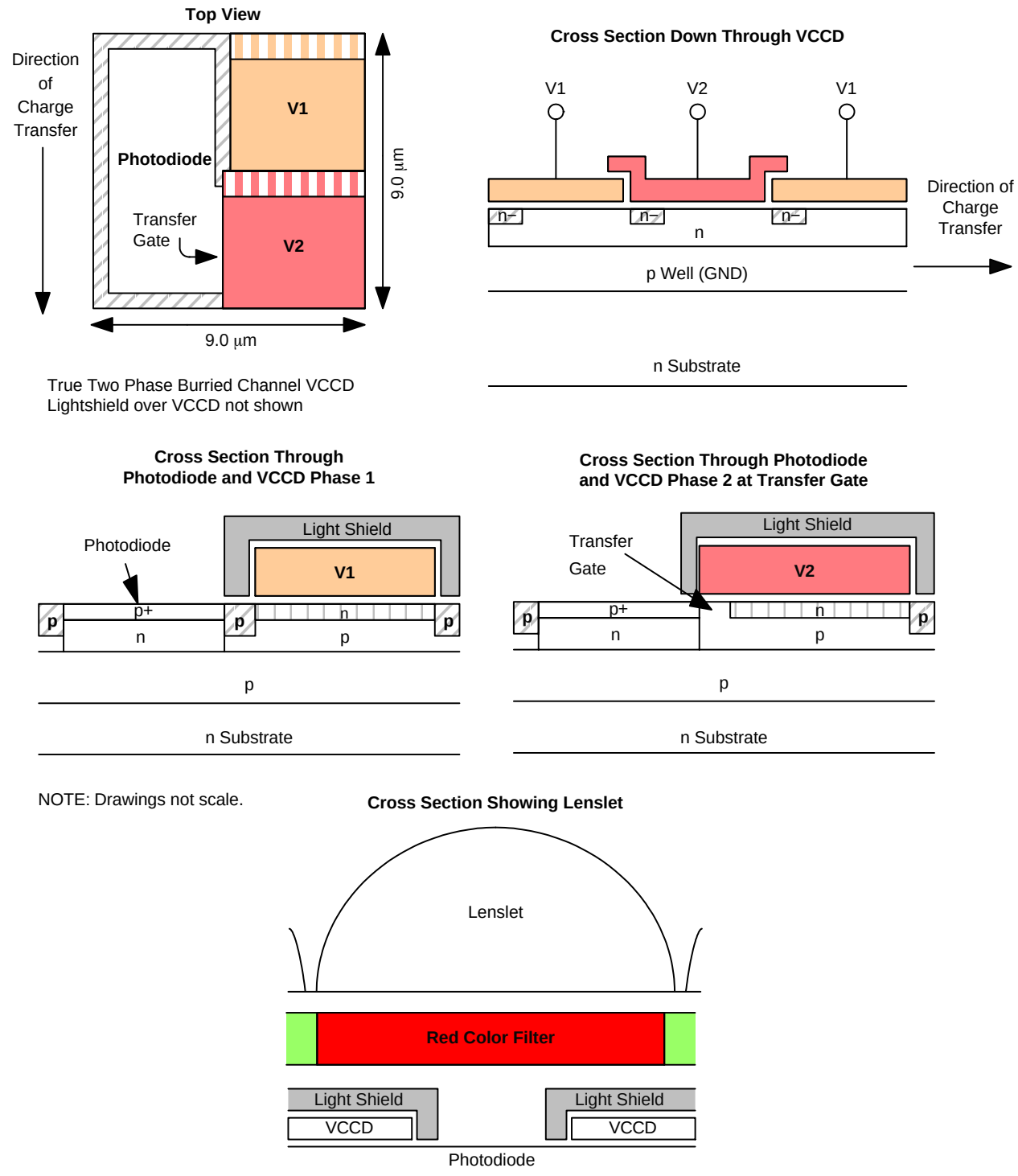


Figure 3. Pixel Architecture

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Vertical to Horizontal Transfer

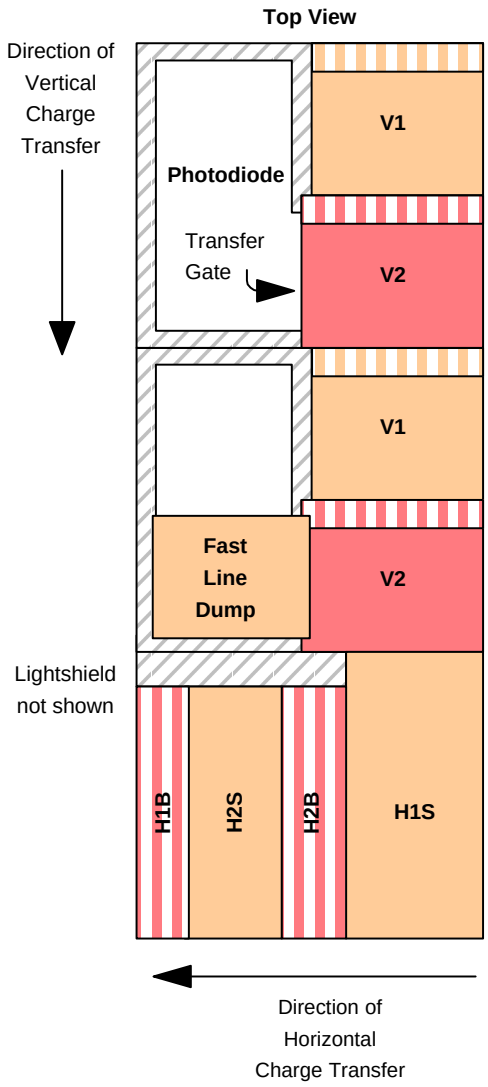


Figure 4. Vertical to Horizontal Transfer Architecture

When the V1 and V2 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. H1 must be stopped in the high state and H2 must be stopped in the low state. The HCCD clocking may begin t_{HD} μs after the falling edge of the V1 and V2 pulse.

Charge is transferred from the last vertical CCD phase into the H1S horizontal CCD phase. Refer to Figure 26 for an example of timing that accomplishes the vertical to horizontal transfer of charge.

If the fast line dump is held at the high level (FDH) during a vertical to horizontal transfer, then the entire line is removed and not transferred into the horizontal register.

Horizontal Register to Floating Diffusion

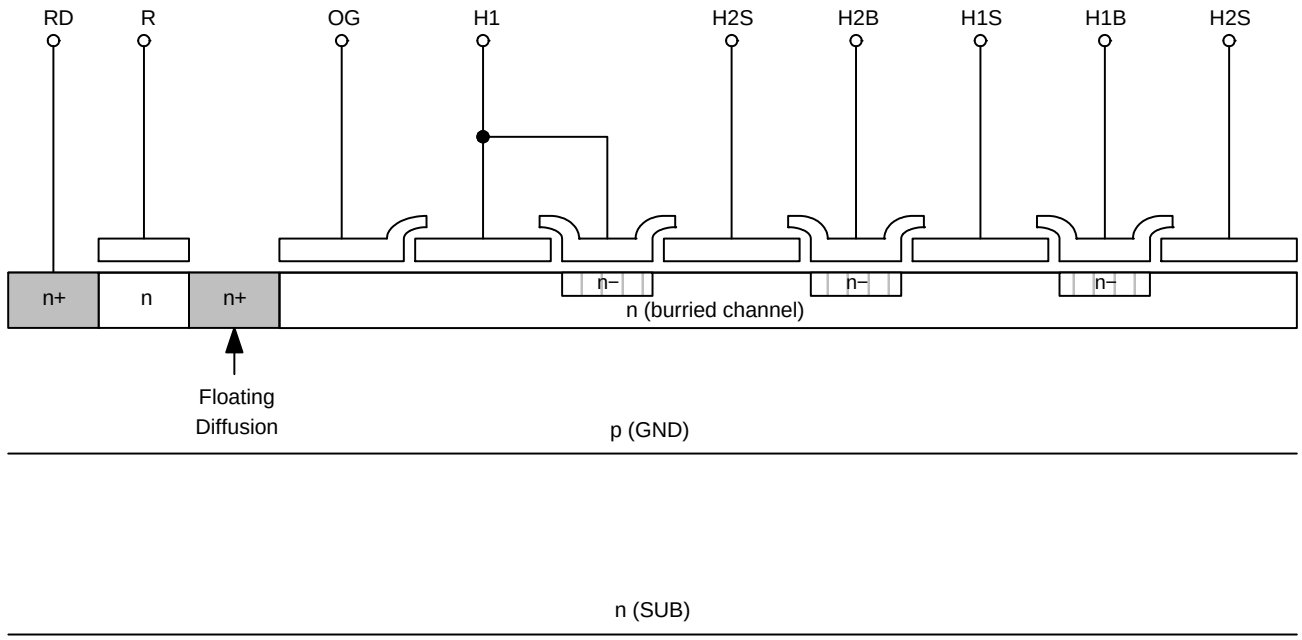


Figure 5. Horizontal Register to Floating Diffusion Architecture

The HCCD has a total of 4,080 pixels. The 4,072 vertical shift registers (columns) are shifted into the center 4,072 pixels of the HCCD. There are 4 pixels at both ends of the HCCD, which receive no charge from a vertical shift register. The first 4 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 20 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 4,033 clock cycles will contain photo-electrons (image data). Finally, the last 19 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 20 dark columns at the start of the line and the 19 dark columns at the end of the line, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 18 columns of the 20 column dark reference at the start of the line. Only use the center 17 columns of the 19 column dark reference at the end of the line.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter (SUB), VCCD (V1, V2), and fast line dump (FD) should be not be pulsed. This prevents unwanted noise from being introduced. The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video L output, or to the video R output (left/right image reversal). The HCCD is split into two equal halves of 2,040 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the H1BL, H2BL, H1BR, and H2BR timing inputs.

Horizontal Register Split

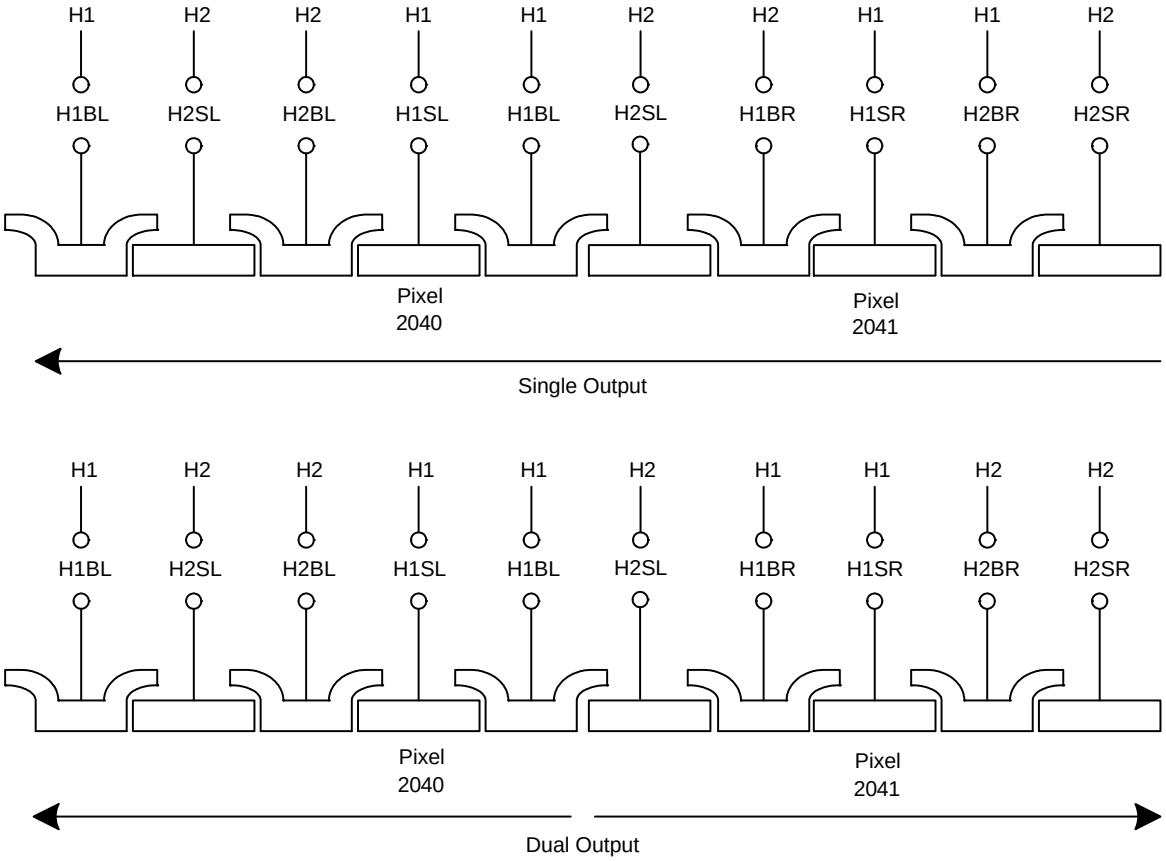


Figure 6. Horizontal Register

Single Output Operation

When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 2). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 18) and VOUTR (pin 19) to GND (zero volts).

The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H2BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H1BR. In other words, the clock driver generating the H1 timing should be connected to pins 8, 9, 13, and 11. The clock driver generating the H2 timing should be connected to pins 7, 10, 14, and 12. The horizontal CCD should be clocked for 4 empty pixels plus 20 light shielded pixels plus 4,032 photoactive pixels plus 20 light shielded pixels for a total of 4,076 pixels. H1BINL and H1BINR use the H1 timing, but should be generated from a separate clock driver for optimal performance.

Dual Output Operation

In dual output mode the connections to the H1BR and H2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 3, 18) should be connected to 15 V. The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H1BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H2BR. The clock driver generating the H1 timing should be connected to pins 8, 9, 13, and 12. The clock driver generating the H2 timing should be connected to pins 7, 10, 14, and 11. The horizontal CCD should be clocked for 4 empty pixels plus 20 light shielded pixels plus 2016 photoactive pixels for a total of 2,040 pixels. If the camera is to have the option of dual or single output mode, the clock driver signals sent to H1BR and H2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for H1BR and H2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the H1BR and H2BR clocks occur at the same time (within 3 ns) as the other HCCD clocks.

Output

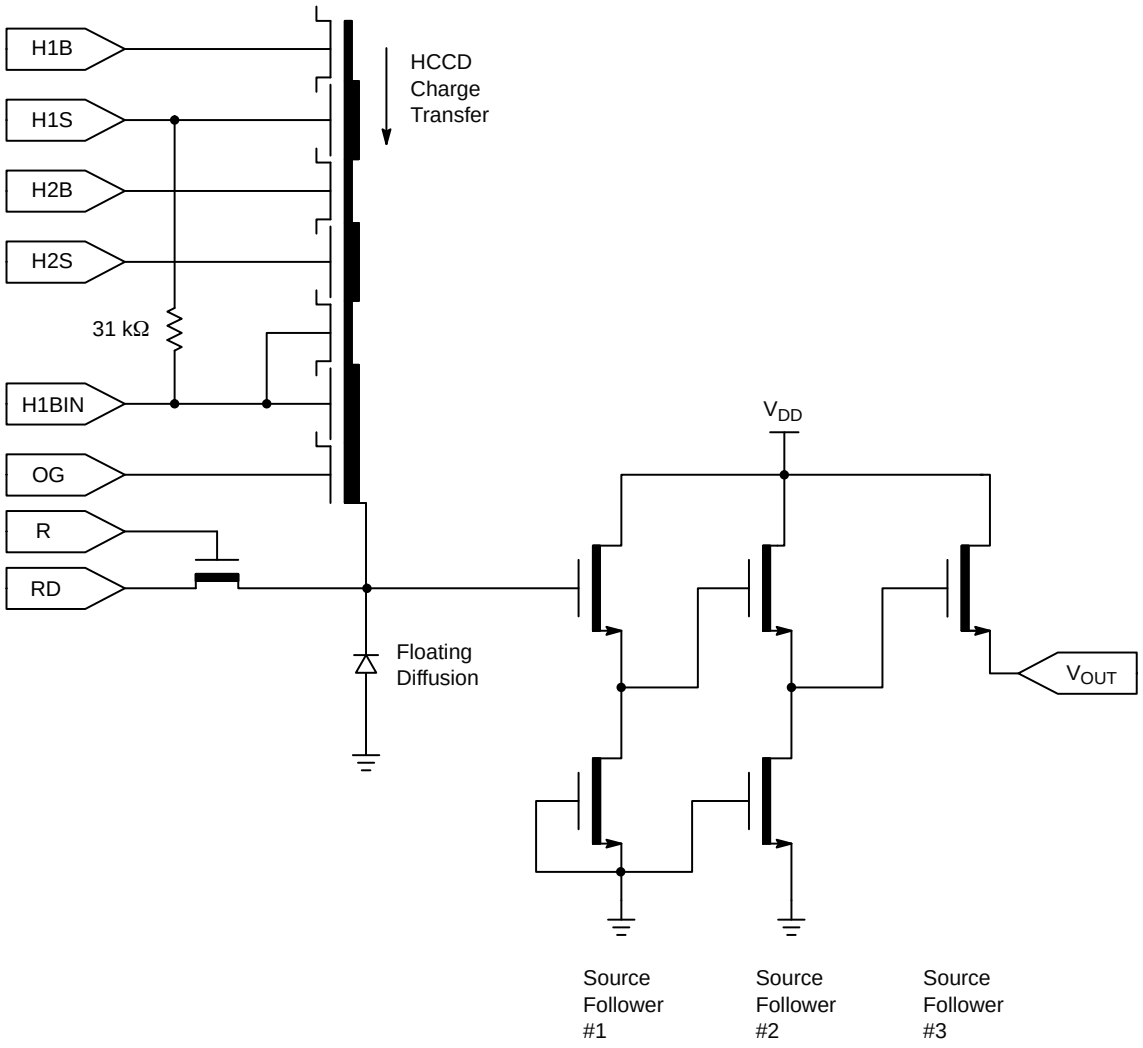


Figure 7. Output Architecture

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (FD) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression $\Delta V_{FD} = Q / \Delta C_{FD}$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron ($\mu V/e^-$). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD).

Pin Description and Physical Orientation

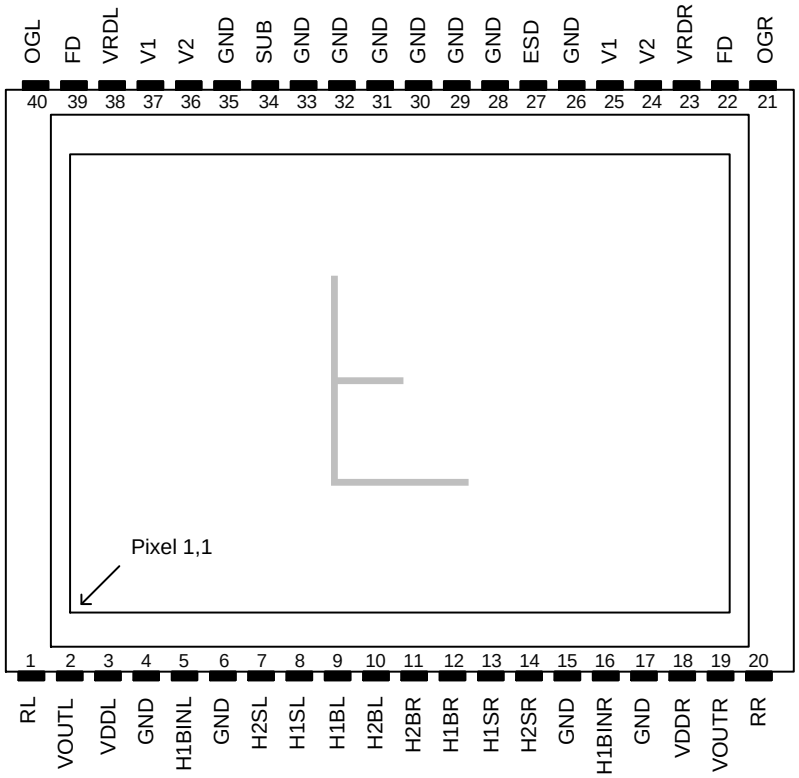


Figure 8. Pin Description

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	RL	Reset Gate, Left
2	VOUTL	Video Output, Left
3	VDDL	V_{DD}, Left
4	GND	Ground
5	H1BINL	H1 Last Phase, Left
6	GND	Ground
7	H2SL	H2 Storage, Left
8	H1SL	H1 Storage, Left
9	H1BL	H1 Barrier, Left
10	H2BL	H2 Barrier, Left
11	H2BR	H2 Barrier, Right
12	H1BR	H1 Barrier, Right
13	H1SR	H1 Storage, Right
14	H2SR	H2 Storage, Right
15	GND	Ground
16	H1BINR	H1 Last Phase, Right
17	GND	Ground
18	VDDR	V_{DD}, Right
19	VOUTR	Video Output, Right
20	RR	Reset Gate, Right

Pin	Name	Description
21	OGR	Output Gate, Right
22	FD	Fast Line Dump Gate
23	RDR	Reset Drain, Right
24	V2	Vertical Clock, Phase 2
25	V1	Vertical Clock, Phase 1
26	GND	Ground
27	ESD	ESD Protection
28	GND	Ground
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	GND	Ground
33	GND	Ground
34	SUB	Substrate
35	GND	Ground
36	V2	Vertical Clock, Phase 2
37	V1	Vertical Clock, Phase 1
38	RDL	Reset Drain, Left
39	FD	Fast Line Dump Gate
40	OGL	Output Gate, Left

NOTE: The pins are on a 0.070″ spacing.

IMAGING PERFORMANCE

Table 5. IMAGING PERFORMANCE OPERATIONAL CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.)

Description	Condition	Notes
Frame Time	1,732 ms	1
Horizontal Clock Frequency	10 MHz	
Light Source	Continuous Red, Green and Blue LED Illumination Centered at 450, 530 and 650 nm	2, 3
Operation	Nominal Operating Voltages and Timing	

1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP−8115.
3. For monochrome sensor, only green LED used.

Specifications

Table 6. PERFORMANCE SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Sample Plan	Temperature Tested at (°C)
ALL CONFIGURATIONS							
Maximum Photoresponse Non-Linearity (Notes 2, 3)	NL	N/A	2	−	%	Design	
Maximum Gain Difference between Outputs (Notes 2, 3)	ΔG	N/A	10	−	%	Design	
Max. Signal Error due to Non-Linearity Dif. (Notes 2, 3)	ΔNL	N/A	1	−	%	Design	
Horizontal CCD Charge Capacity	H_{Ne}	−	139	−	ke^-	Design	
Vertical CCD Charge Capacity	V_{Ne}	90	91	−	ke^-	Die	
Photodiode CCD Charge Capacity	P_{Ne}	58	60	−	ke^-	Die	
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999	−	N/A		Design	
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999	−	N/A		Design	
Photodiode Dark Current	I_{PD}	N/A N/A	− −	800 0.15	e/p/s nA/cm^2	Die	27, 40
Vertical CCD Dark Current	I_{VD}	N/A N/A	− −	3,800 0.5	e/p/s nA/cm^2	Die	27, 40
Image Lag	Lag	N/A	< 10	50	e^-	Design	
Anti-Blooming Factor	X_{AB}	100	300	N/A		Design	
Vertical Smear	Smr	N/A	−85	−75	dB	Design	
Total Noise (Note 4)	n_{e-T}	−	30	−	e^- rms	Design	
Dynamic Range (Note 5)	DR	−	66	−	dB	Design	
Output Amplifier DC Offset	V_{ODC}	4	9	14	V	Die	
Output Amplifier Bandwidth (Note 6)	f_{-3dB}	−	106	−	MHz	Die	
Output Amplifier Impedance	R_{OUT}	100	150	200	Ω	Die	
Output Amplifier Sensitivity	ΔV/ΔN	−	13	−	$\mu V/e^-$	Design	

Table 6. PERFORMANCE SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Sample Plan	Temperature Tested at (°C)
KAI−11002−ABA CONFIGURATION							
Peak Quantum Efficiency	QE_{MAX}	45	50	N/A	%	Design	
Peak Quantum Efficiency Wavelength	λQE	N/A	500	N/A	nm		
KAI−11002−FBA CONFIGURATION GEN2 COLOR							
Peak Quantum Efficiency Red Green Blue	QE_{MAX}	 − − −	 35 38 40	 N/A N/A N/A	%	Design	
Peak Quantum Efficiency Wavelength Red Green Blue	λQE	 − − −	 610 530 460	 N/A N/A N/A	nm	Design	
KAI−11002−CBA CONFIGURATION GEN1 COLOR (Note 7)							
Peak Quantum Efficiency Red Green Blue	QE_{MAX}	 − − −	 32 34 40	 N/A N/A N/A	%	Design	
Peak Quantum Efficiency Wavelength Red Green Blue	λQE	 − − −	 620 540 460	 N/A N/A N/A	nm	Design	

NOTE: N/A = Not Applicable.

1. Per color.
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning.
4. Includes system electronics noise, dark pattern noise and dark current shot noise at 30 MHz.
5. Uses 20LOG (P_{Ne} / n_{e-T}).
6. Last stage only, C_{LOAD} = 10 pF. Then $f_{-3dB} = (1 / (2n \cdot R_{OUT} \cdot C_{LOAD}))$.
7. This color filter set configuration (Gen1) is not recommended for new designs.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

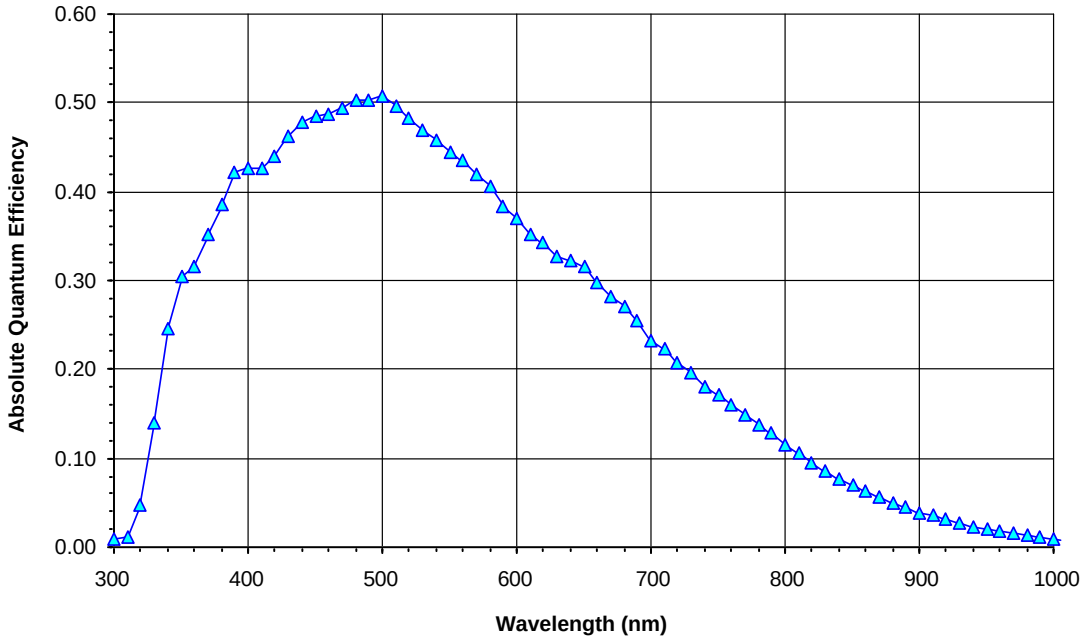


Figure 9. Monochrome with Microlens Quantum Efficiency

Monochrome without Microlens

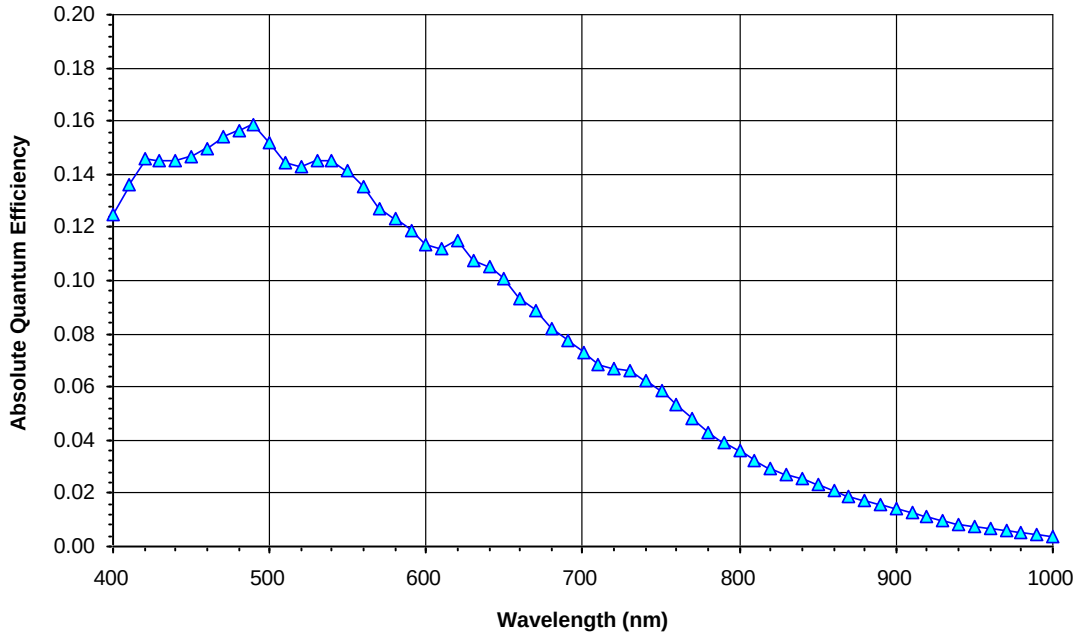


Figure 10. Monochrome without Microlens Quantum Efficiency

Color with Microlens

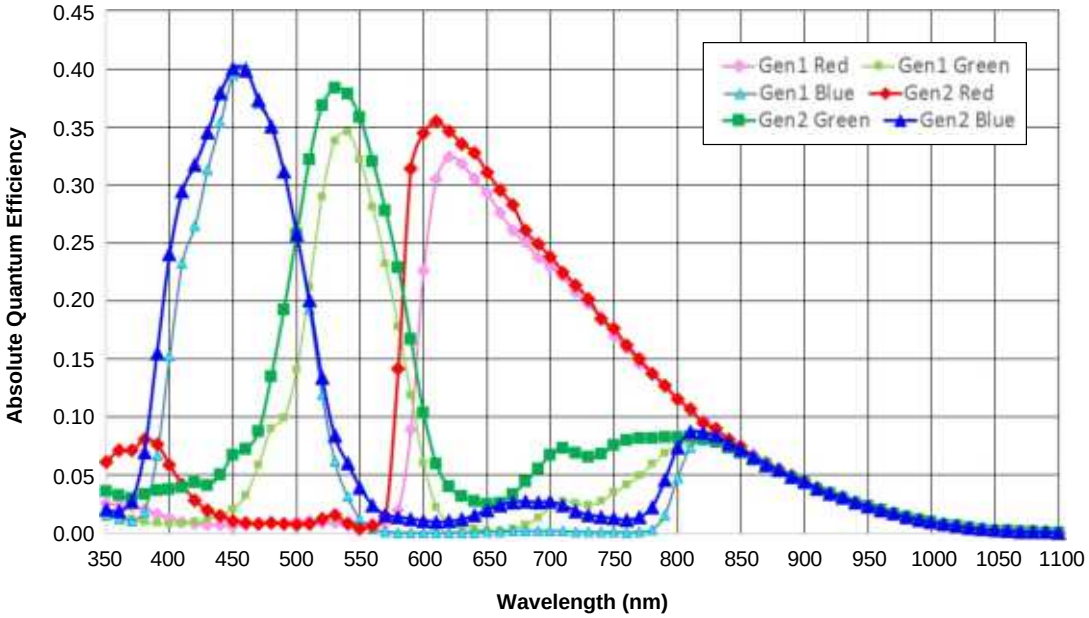


Figure 11. Color with Microlens Quantum Efficiency using AR Glass

Color without Microlens

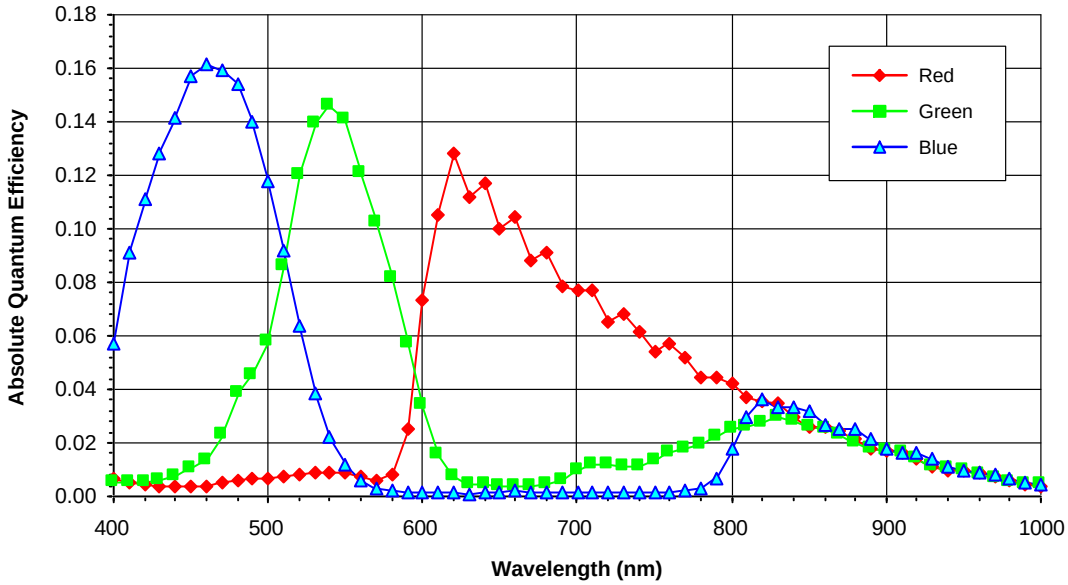


Figure 12. Color without Microlens Quantum Efficiency using AR Glass

Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

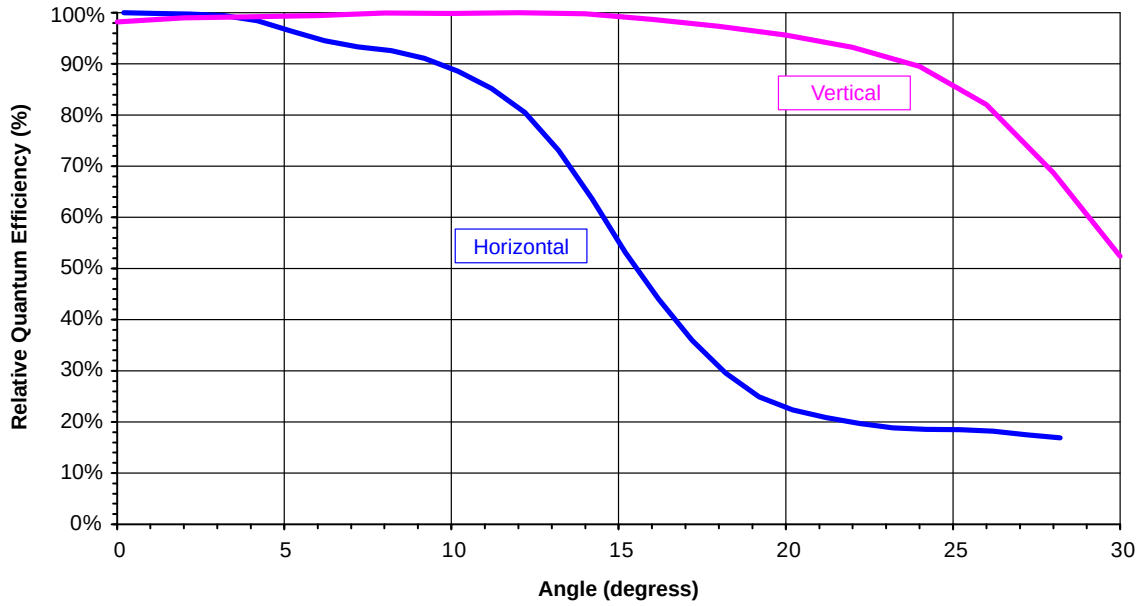


Figure 13. Monochrome with Microlens Angular Quantum Efficiency

Color with Microlens

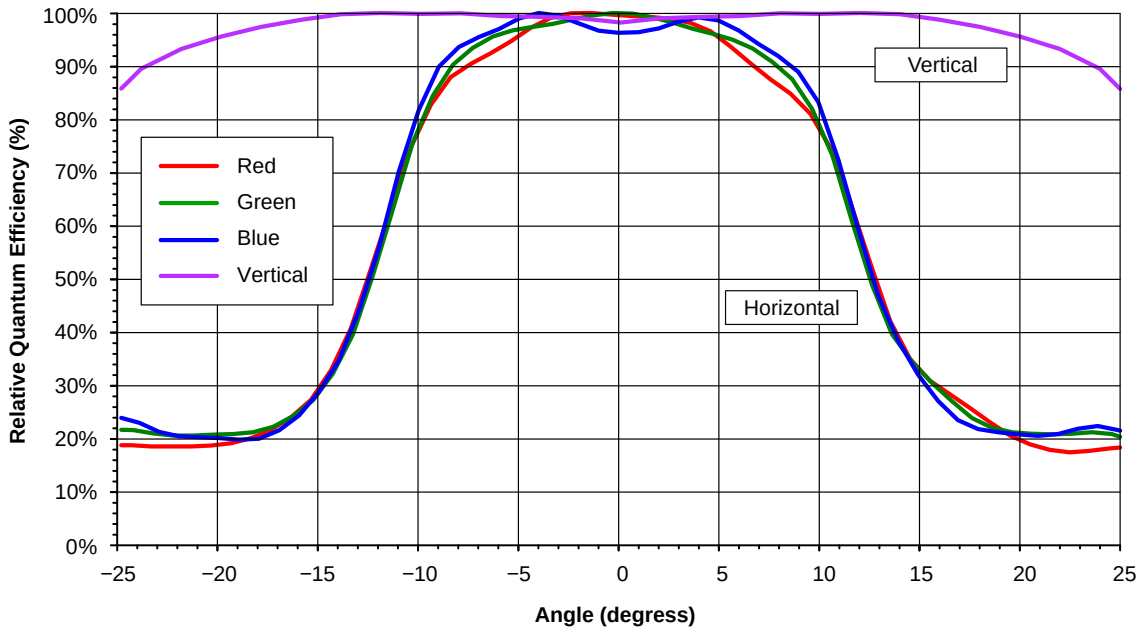


Figure 14. Color with Microlens Angular Quantum Efficiency

Power-Estimated

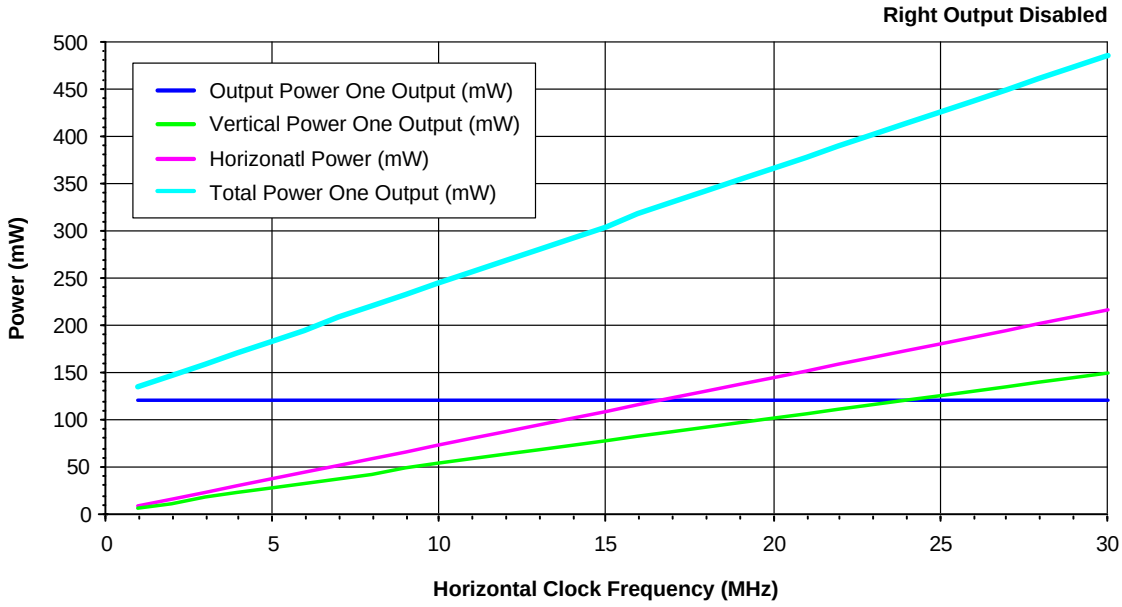


Figure 15. Power

Frame Rates − Continuous Mode

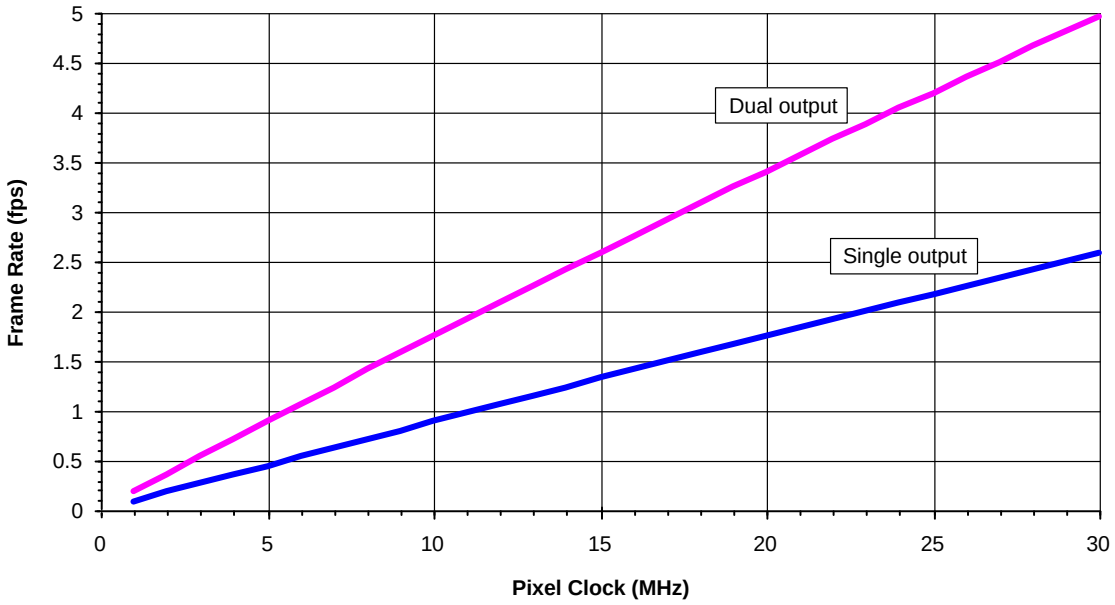


Figure 16. Frame Rates

DEFECT DEFINITIONS

Table 7. DEFECT DEFINITIONS (Notes 1, 2)

Description	Definition	Class X Monochrome with Microlens Only	Class 0 Monochrome with Microlens Only	Class 1	Class 2 Color Only	Class 2 Monochrome Only
Major Dark Field Defective Pixel	Defect ≥ 239 mV	100	100	100	200	200
Major Bright Field Defective Pixel	Defect ≥ 15%	100	100	100	200	200
Minor Dark Field Defective Pixel	Defect ≥ 123 mV	1,000	1,000	1,000	2,000	2,000
Cluster Defect	A group of 2 to “N” contiguous major defective pixels, but no more than “W” adjacent defects horizontally.	0	1 N = 10 W = 3	20 N = 10 W = 3	20 N = 10 W = 3	20 N = 12 W = 5
Column Defect	A group of more than 10 contiguous major defective pixels along a single column.	0	0	0	10	2

NOTE: Class X sensors are offered strictly “as available”. ON Semiconductor cannot guarantee delivery dates. Please call for availability.

1. There will be at least two non-defective pixels separating any two major defective pixels.
2. Tested at 27°C and 40°C.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps.

TEST DEFINITIONS

Test Regions of Interest

Active Area ROI: Pixel (1, 1) to Pixel (4008, 2672)
Center 100 by 100 ROI: Pixel (1954, 1336) to Pixel (2053, 1435)

Only the active pixels are used for performance and defect tests.

Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 17 for a pictorial representation of the regions.

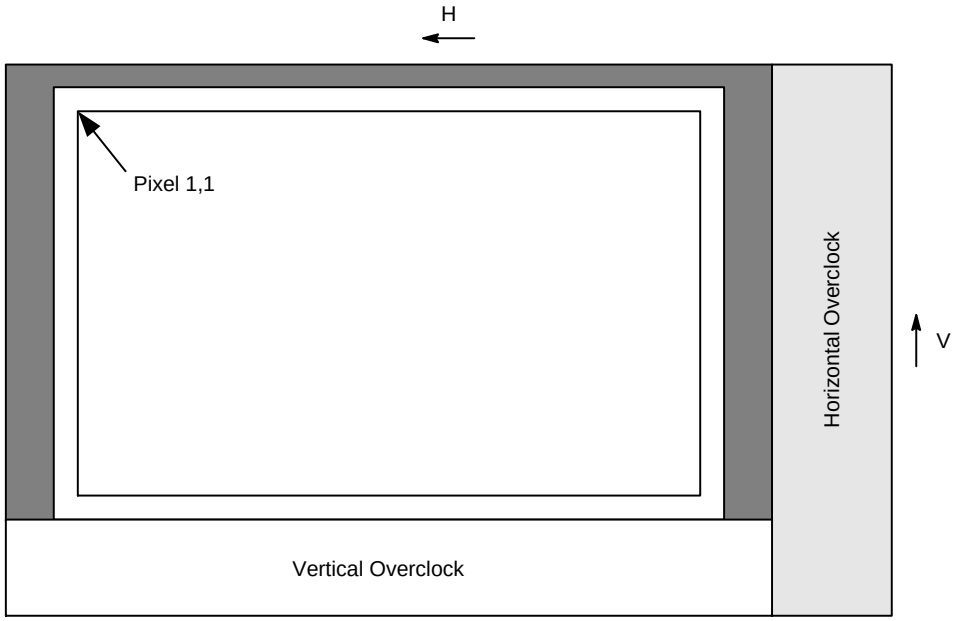


Figure 17. Overclock Regions of Interest

Tests

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 384 sub regions of interest, each of which is 167 by 167 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 40,000 electrons. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 60,000 electrons. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

$$\text{Bright Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

The sensor is then partitioned into 384 sub regions of interest, each of which is 167 by 167 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 520 mV (40,000 electrons).
- Dark defect threshold: 520 mV · 15% = 78 mV
- Bright defect threshold: 520 mV · 15% = 78 mV
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 167, 167.
  - Median of this region of interest is found to be 520 mV.
  - Any pixel in this region of interest that is ≥ (520 + 78 mV) 598 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is ≤ (520 − 78 mV) 442 mV in intensity will be marked defective.
- All remaining 384 sub regions of interest are analyzed for defective pixels in the same manner.

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Table 8. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit	Notes
Operating Temperature	T_{OP}	−50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	I_{OUT}	0.0	−40	mA	3
Off-Chip Load	C_L	−	10	pF	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Noise performance will degrade at higher temperatures.
2. T = 25°C. Excessive humidity will degrade MTTF.
3. Total for both outputs. Current is −20 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.

Table 9. MAXIMUM VOLTAGE RATINGS BETWEEN PINS

Description	Minimum	Maximum	Unit	Notes
RL, RR, H1BINL, H1BINR, H2SL, H1SL, H1BL, H2BL, H2BR, H1BR, H1SR, H2SR, OGL, OGR to ESD	0	17	V	
Pin to Pin with ESD Protection	−17	17	V	1
VDDL, VDDR to GND	0	25	V	

1. Pins with ESD protection are: RL, RR, H1BINL, H1BINR, H2SL, H1SL, H1BL, H2BL, H2BR, H1BR, H1SR, H2SR, OGL, and OGR.

Table 10. DC BIAS OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Maximum DC Current	Notes
Output Gate	OG	−3.0	−2.5	−2.0	V	1 μA	
Reset Drain	RD	10.5	11.5	12.0	V	1 μA	
Output Amplifier Supply	V_{DD}	14.5	15.0	15.5	V	2 mA	4
Ground	GND	0.0	0.0	0.0	V		
Substrate	SUB	8.0	TBD	17.0	V		1, 5
ESD Protection Disable	ESD	−9.0	−8.0	−7.0	V		2
Output Bias Current	I_{OUT}	−	−5	−10	mA		3

1. The operating of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is 60,000 electrons.
2. V_{ESD} must be at least 1 V more negative than H1L and H2L during sensor operation AND during camera power turn on.
3. An output load sink must be applied to V_{OUT} to activate output amplifier.
4. The maximum DC current is for one output unloaded. This is the maximum current that the first two stages of one output amplifier will draw. This value is with V_{OUT} disconnected.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

Power-Up Sequence

1. Substrate
2. ESD Protection
3. All Other Biases and Clocks

AC Operating Conditions

Table 11. CLOCK LEVELS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Vertical CCD Clock High	V2H	7.5	8.0	8.5	V	
Vertical CCD Clocks Midlevel	V1M, V2M	−0.2	0.0	0.2	V	
Vertical CCD Clocks Low	V1L, V2L	−9.5	−9.0	−8.5	V	
Horizontal CCD Clocks Amplitude	H1H, H2H	5.8	6.0	6.2	V	
Horizontal CCD Clocks Low	H1L, H2L	−4.2	−4.0	−3.8	V	
Reset Clock High	RH	1.3	1.5	1.7	V	
Reset Clock Low	RL	−3.7	−3.5	−3.3	V	
Electronic Shutter Voltage	$V_{SHUTTER}$	39	40	48	V	2
Fast Dump High	FDH	4.5	5.0	5.5	V	
Fast Dump Low	FDL	−9.5	−9.0	−8.5	V	1

1. FDL can use the same supply as Vertical CCD Clocks Low if desired.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

Table 12. CLOCK LINE CAPACITANCES

Clocks	Capacitance	Unit	Notes
V1 to GND	108	nF	1
V2 to GND	118	nF	1
V1 to V2	56	nF	
H1S to GND	27	pF	2
H2S to GND	27	pF	2
H1B to GND	13	pF	2
H2B to GND	4	pF	2
H1S to H2B and H2S	13	pF	2
H1B to H2B and H2S	13	pF	2
H2S to H1B and H1S	13	pF	2
H2B to H1B and H1S	13	pF	2
H1BIN to GND	20	pF	2
R to GND	10	pF	
FD to GND	20	pF	

1. Gate capacitance to GND is voltage dependent. Value is for nominal VCCD clock voltages.
2. For nominal HCCD clock voltages, these values are for half of the imager (H1SL, H1BL, H2SL, H2BL and H1BINL or H1SR, H1BR, H2SR, H2BR and H1BINR).

TIMING

Table 13. TIMING REQUIREMENTS

Description	Symbol	Min.	Nom.	Max.	Unit
HCCD Delay	t_{HD}	3.0	3.5	10.0	μs
VCCD Transfer Time	t_{VCCD}	3.0	3.5	20.0	μs
Photodiode Transfer Time	t_{V3rd}	8.0	10.0	15.0	μs
VCCD Pedestal Time	t_{3P}	100.0	120.0	200.0	μs
VCCD Delay	t_{3D}	15.0	20.0	80.0	μs
Reset Pulse Time	t_{R}	2.5	5.0	−	ns
Shutter Pulse Time	t_{S}	3.0	4.0	10.0	μs
Shutter Pulse Delay	t_{SD}	1.0	1.5	10.0	μs
HCCD Clock Period	t_{H}	33	−	200	ns
VCCD Rise/Fall Time	t_{VR}	0.0	0.1	1.0	μs
Fast Dump Gate Delay	t_{FD}	0.5	−	−	μs
Vertical Clock Edge Alignment	t_{VE}	0.0	−	100	ns

Main Timing − Continuous Mode

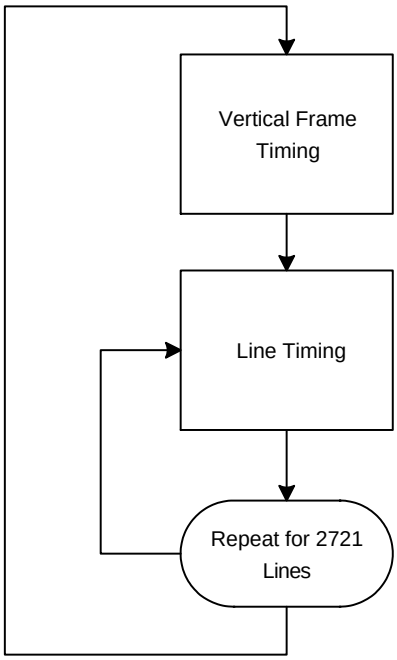


Figure 18. Main Timing − Continuous Mode

Frame Timing − Continuous Mode

Frame Timing without Binning

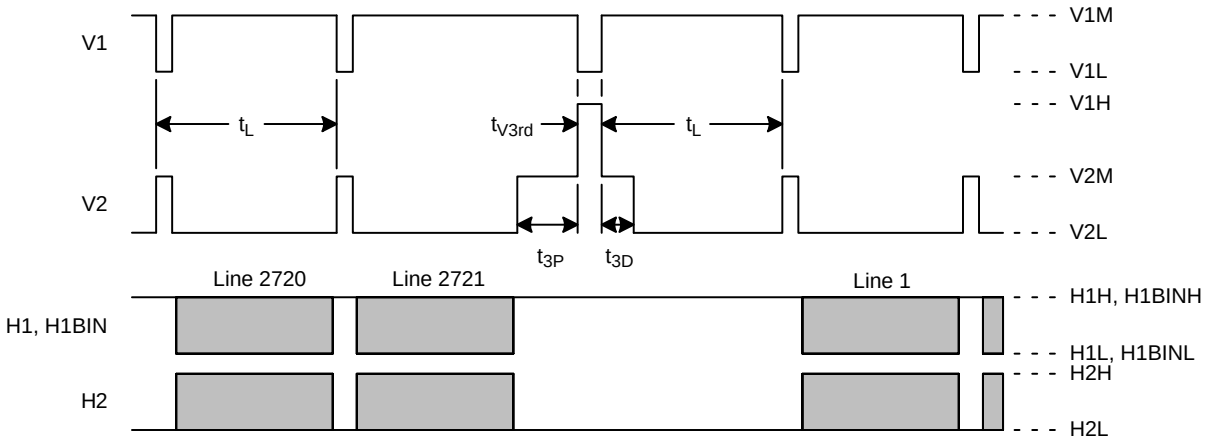


Figure 19. Frame Timing without Binning

Frame Timing for Vertical Binning by 2

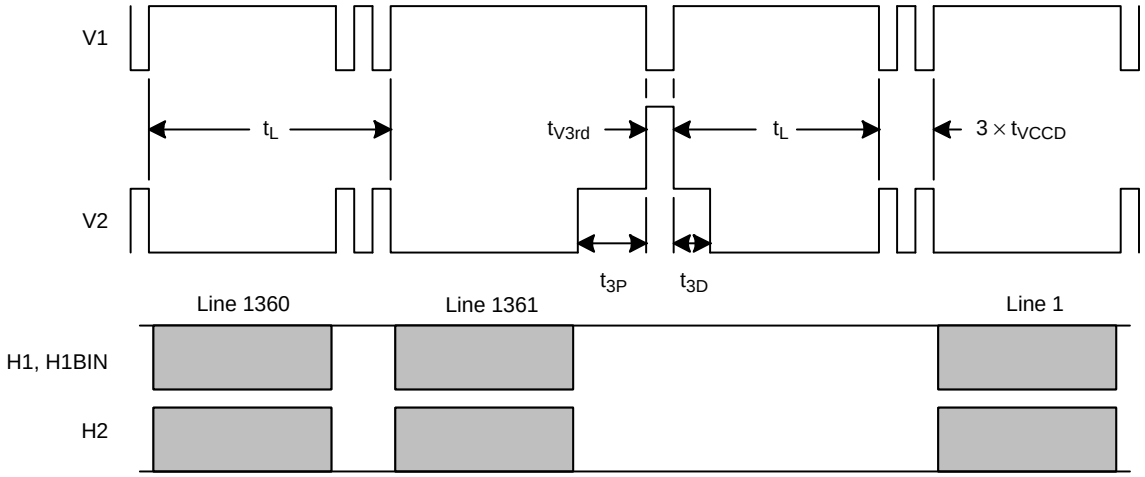


Figure 20. Frame Timing for Vertical Binning by 2

Frame Timing Edge Alignment

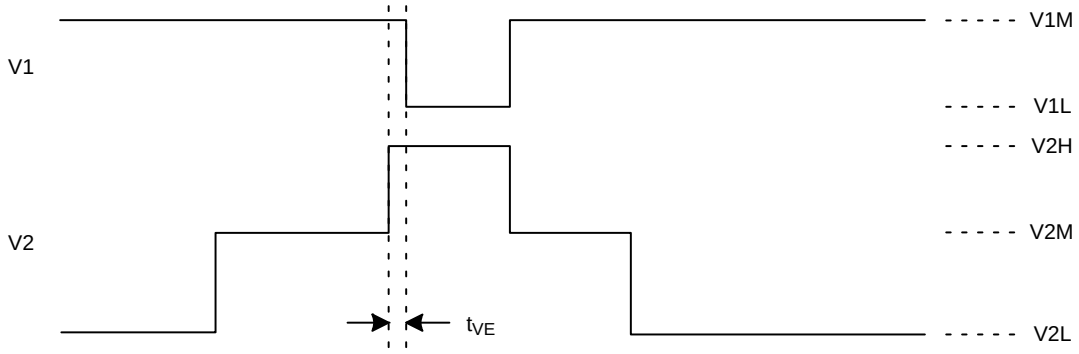


Figure 21. Frame Timing Edge Alignment

Line Timing − Continuous Mode

Line Timing Single Output

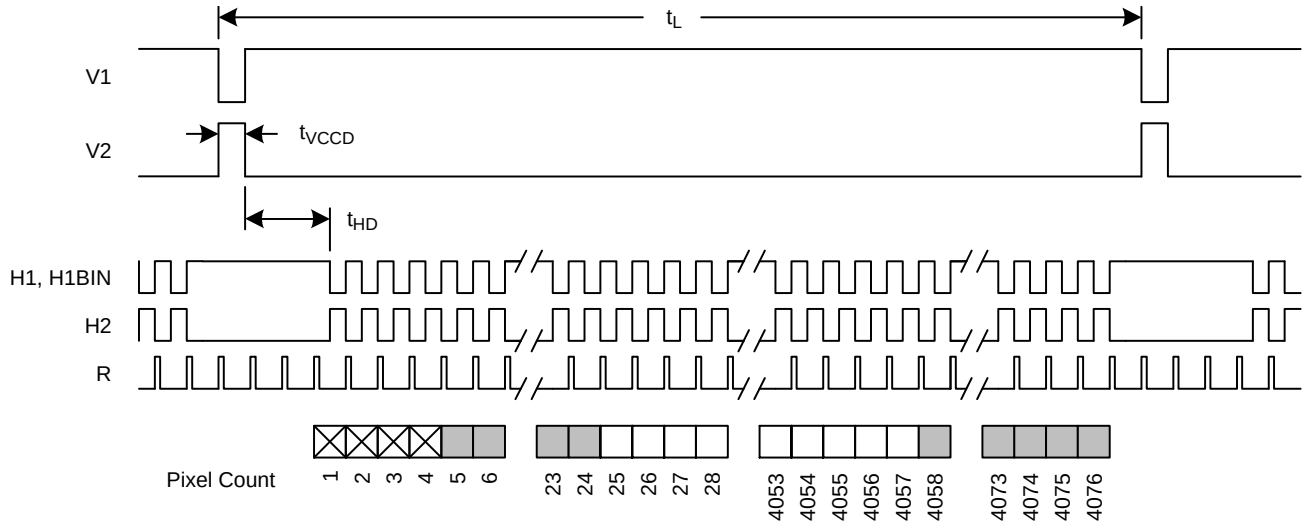


Figure 22. Line Timing Single Output

Line Timing Dual Output − Left Output

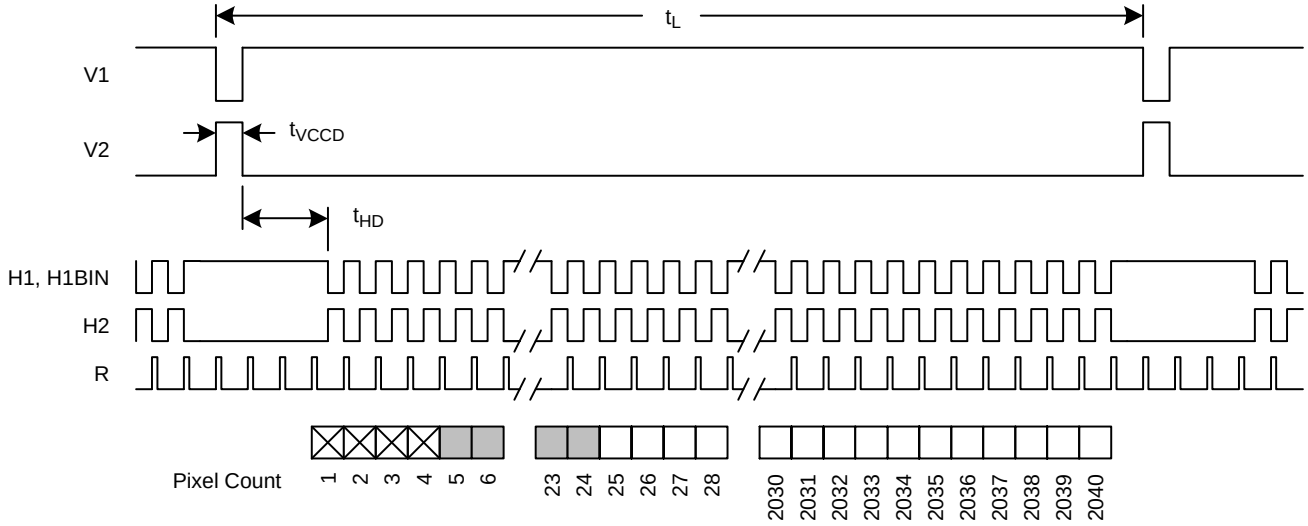


Figure 23. Line Timing Dual Output − Left Output

Line Timing Dual Output − Right Output

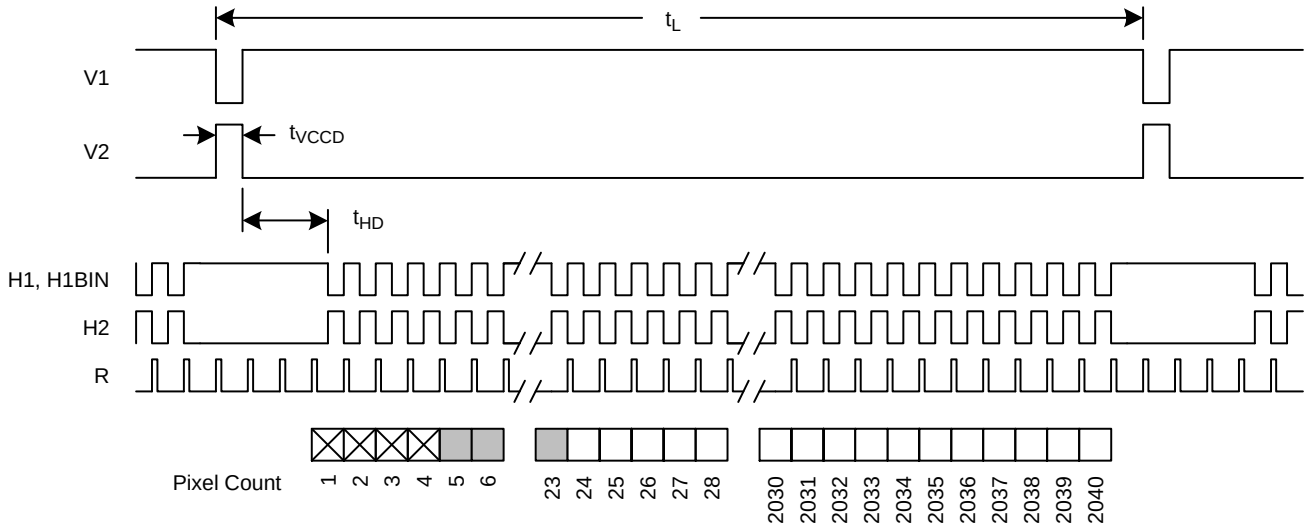


Figure 24. Line Timing Dual Output − Right Output

Line Timing Vertical Binning by 2

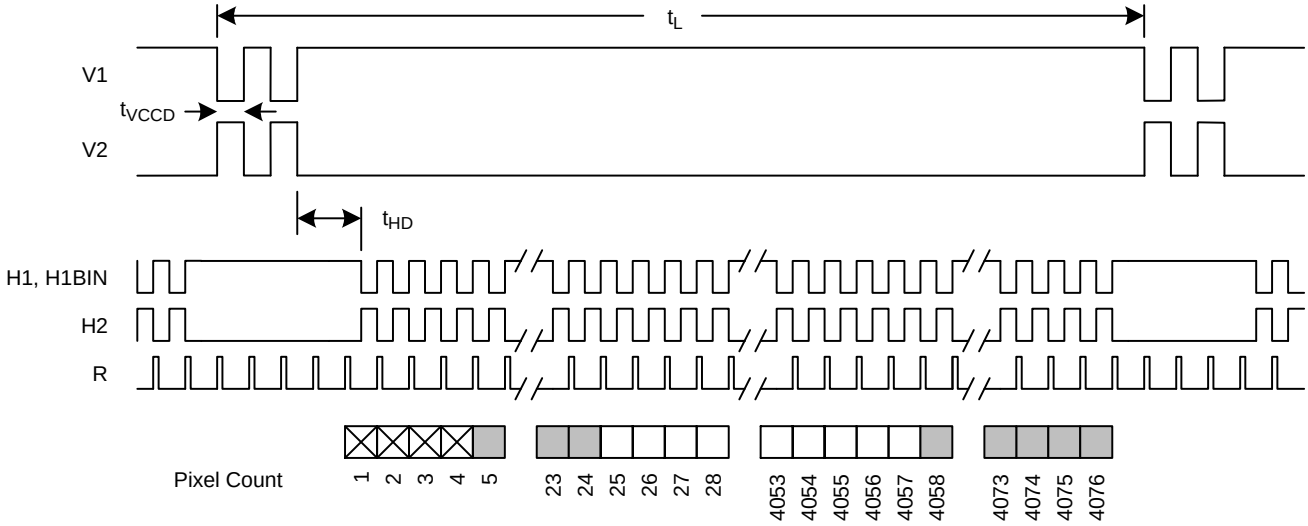


Figure 25. Line Timing Vertical Binning by 2

Line Timing Detail

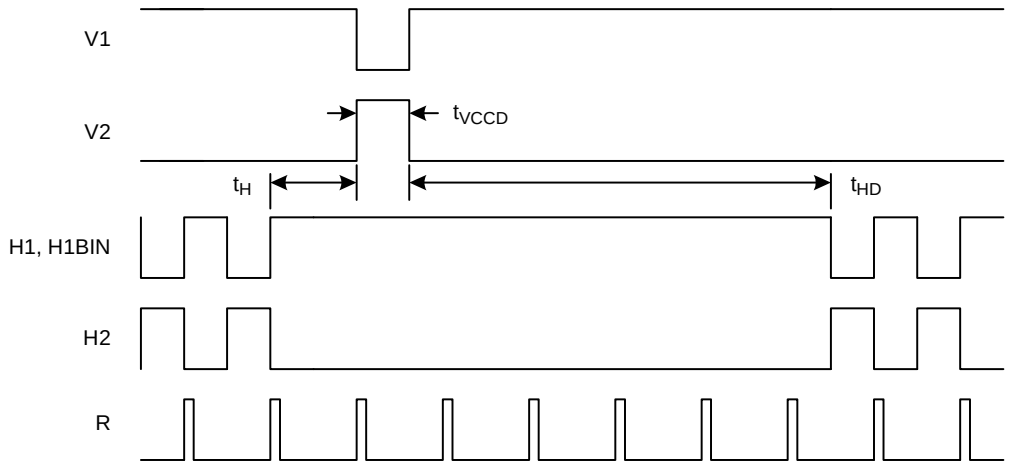


Figure 26. Line Timing Detail

Line Timing Binning by 2 Detail

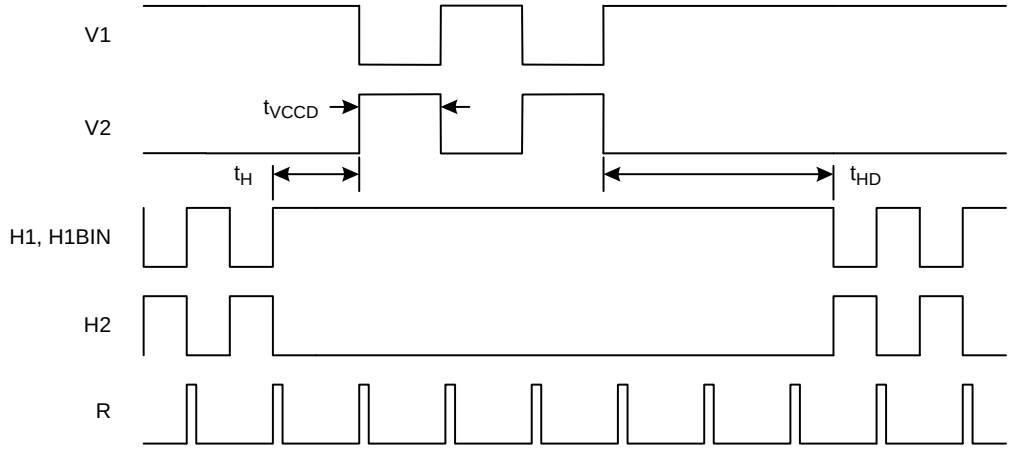


Figure 27. Line Timing Binning by 2 Detail

Line Timing Edge Alignment

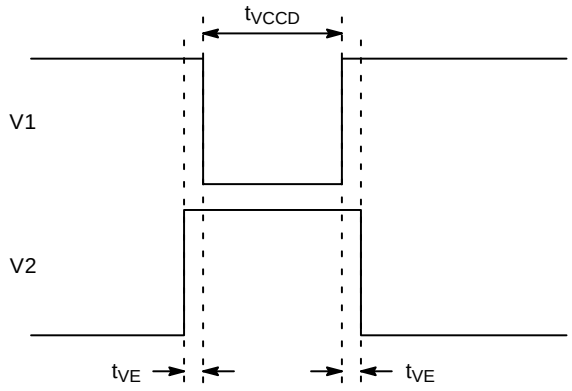


Figure 28. Line Timing Edge Alignment

Pixel Timing − Continuous Mode

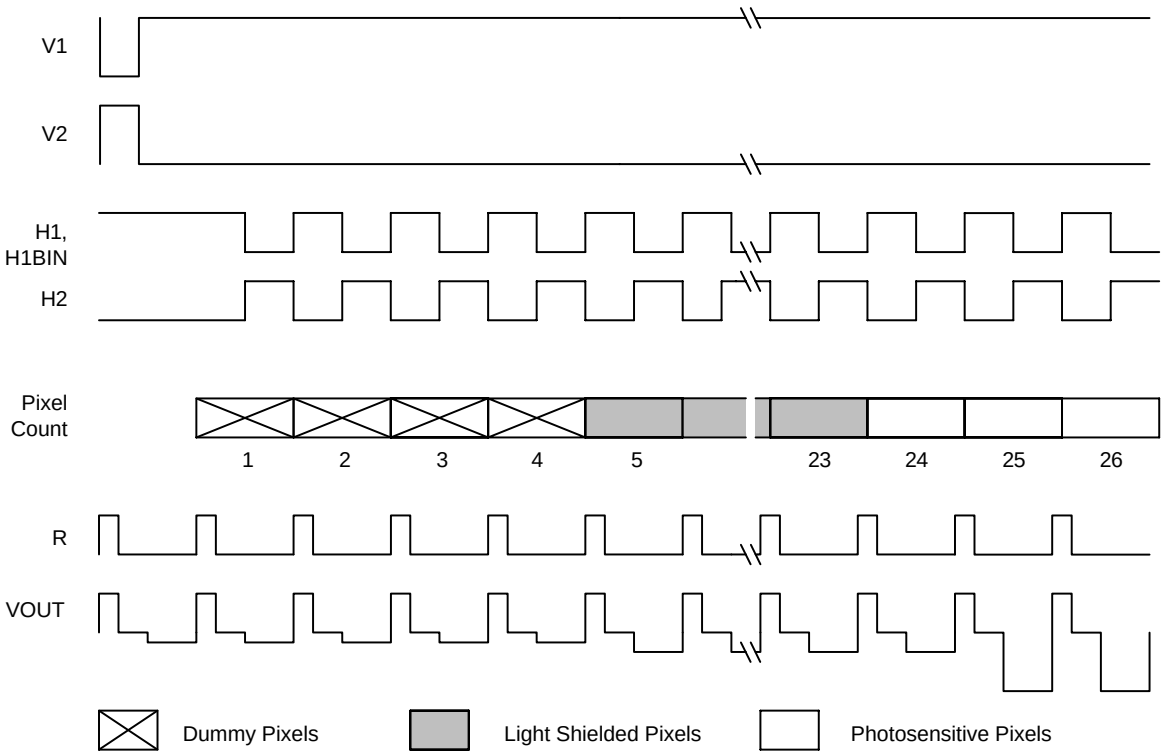


Figure 29. Pixel Timing

Pixel Timing Detail

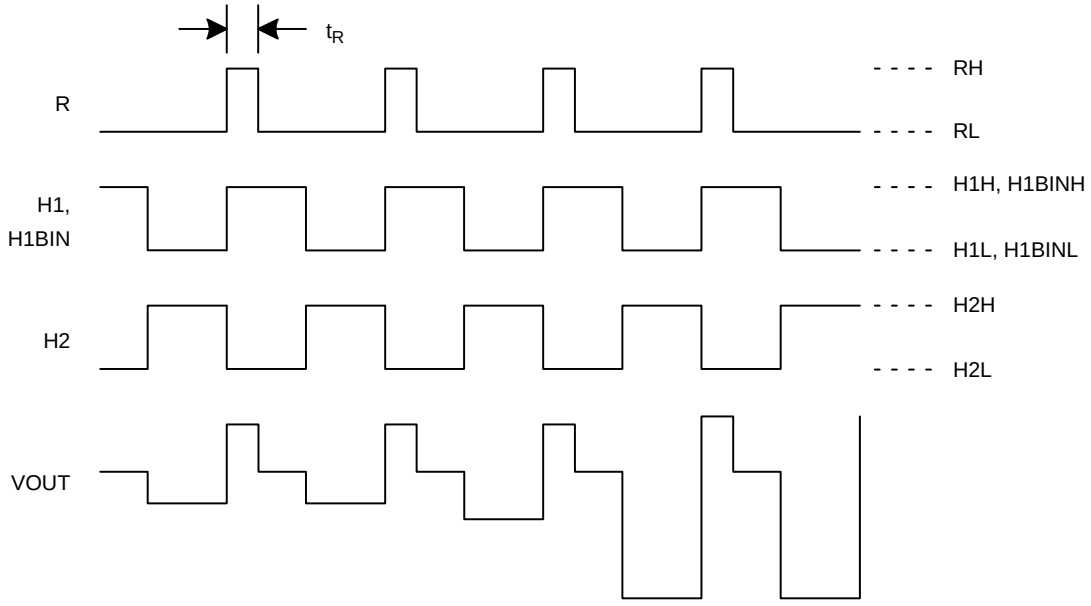


Figure 30. Pixel Timing Detail

Fast Line Dump Timing

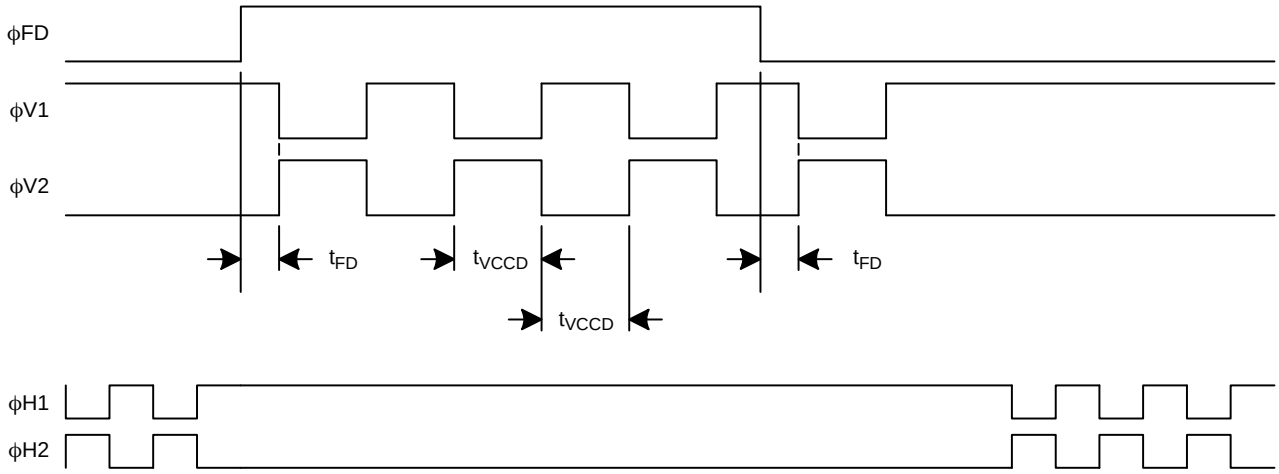


Figure 31. Fast Line Dump Timing

Electronic Shutter

Electronic Shutter Line Timing

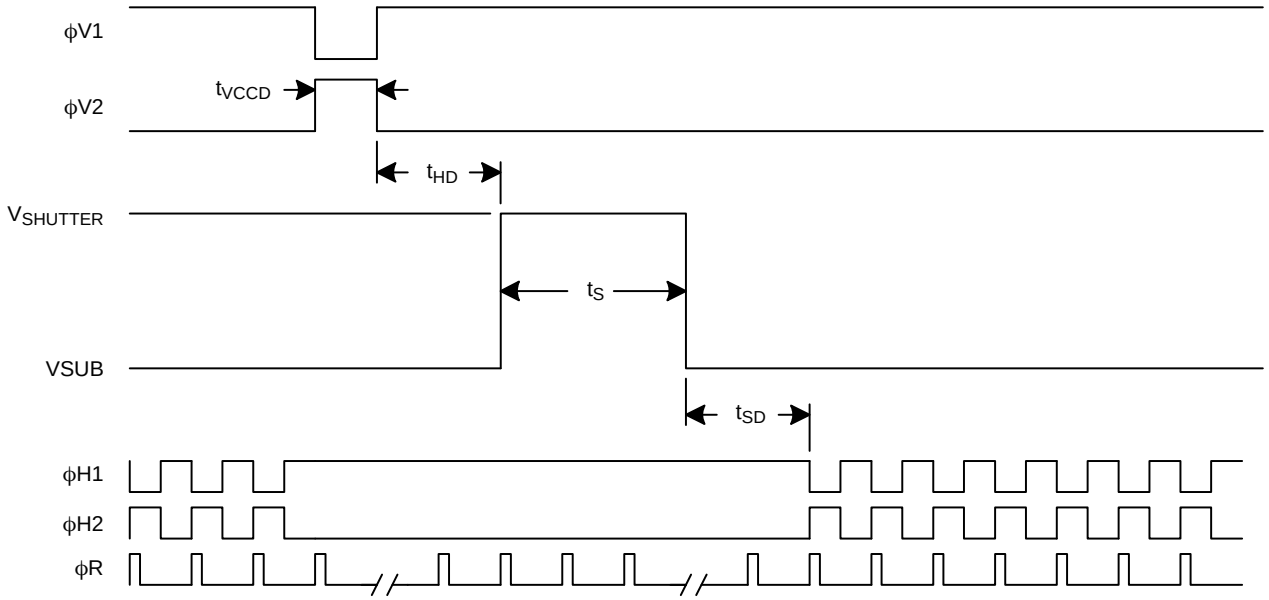


Figure 32. Electronic Shutter Line Timing

Electronic Shutter − Integration Time Definition

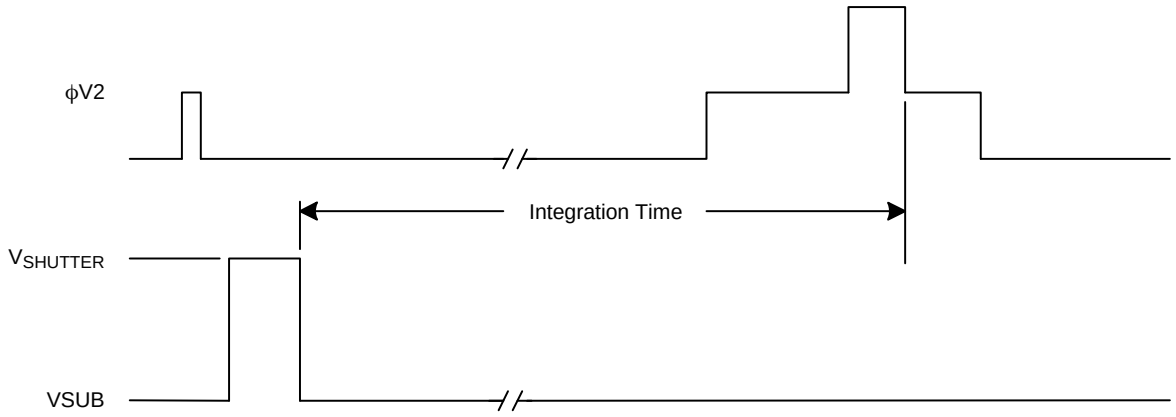


Figure 33. Integration Time Definition

Electronic Shutter Description

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 40 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 40 volts, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum anti-blooming protection.

The KAI−11002 VCCD has a charge capacity of 90,000 electrons (90 ke$^-$). If the SUB voltage is set such that the photodiode holds more than 90 ke$^-$, then when the charge is transferred from a full photodiode to VCCD,

the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size.

The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded, (for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming.

The amount of anti-blooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of anti-blooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) anti-blooming protection. A high VSUB voltage provides lower dynamic range and maximum anti-blooming protection. The optimal setting of VSUB is written on the container in which each KAI−11002 is shipped. The given VSUB voltage for each sensor is selected to provide anti-blooming protection for bright spots at least 100 times saturation, while maintaining at least 60 ke^- of dynamic range.

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of t_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 40 volts t_{INT} seconds before the photodiode to VCCD transfer pulse on V2. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD.

The figure below shows the DC bias (SUB) and AC clock ($V_{SHUTTER}$) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

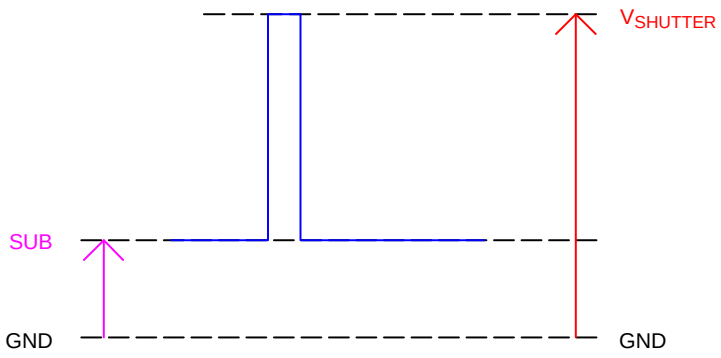


Figure 34. DC Bias and AC Clock Applied to the SUB Pin

STORAGE AND HANDLING

Table 14. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Unit	Notes
Storage Temperature	T_{ST}	−20	80	°C	1
Humidity	RH	5	90	%	2

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

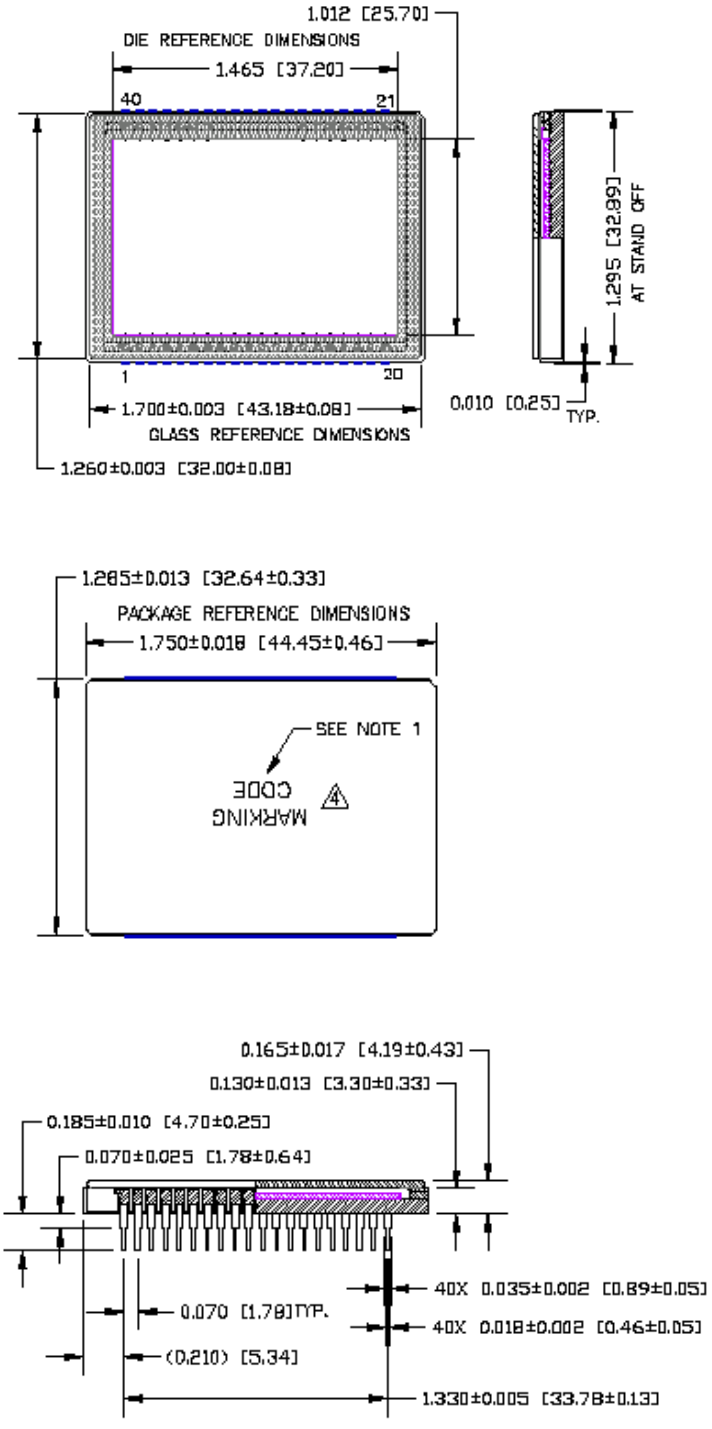
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Package

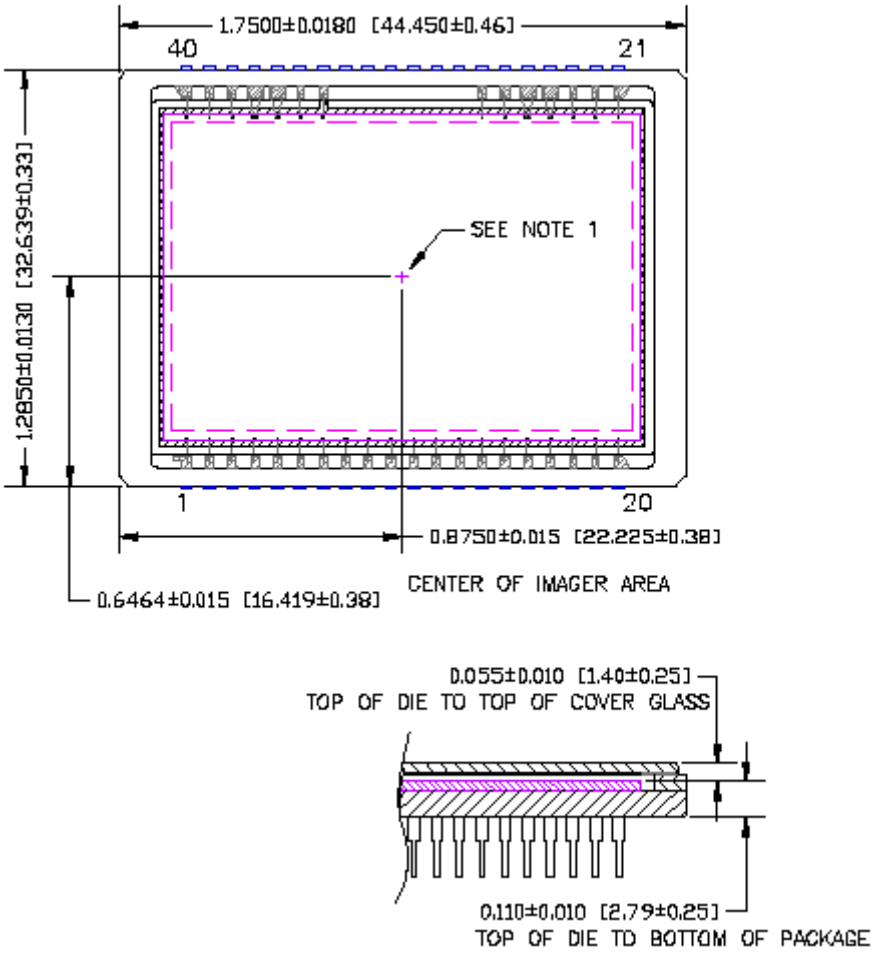


Notes:

1. See Ordering Information for marking code.
2. Cover glass is manually placed and visually aligned over die − location accuracy is not guaranteed.

Figure 35. Package Drawing

Die to Package Alignment

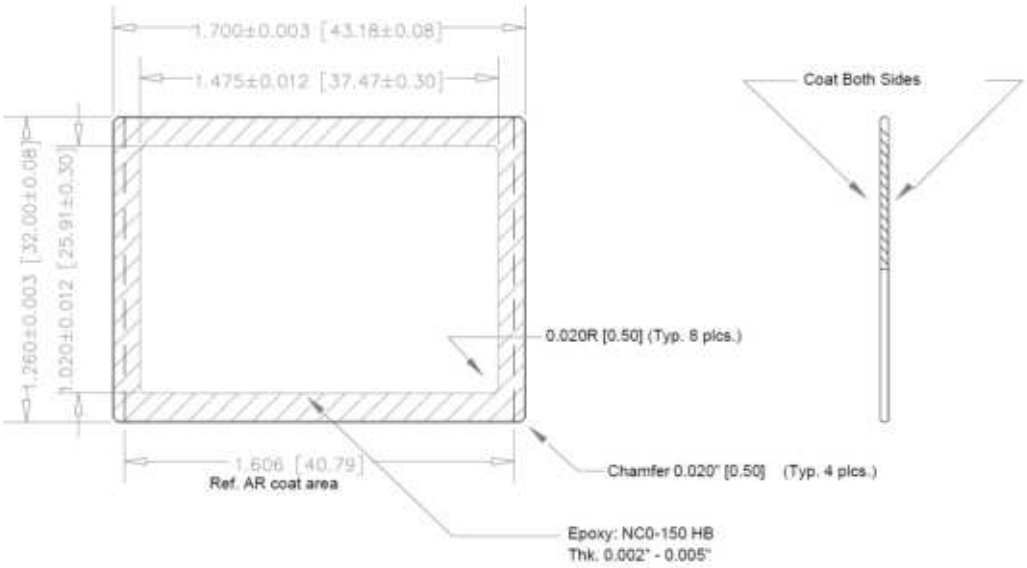


Notes:

1. Center of image is offset from center of package by (0.00, 0.10) mm nominal.
2. Die is aligned within ±1 degrees of any package cavity edge.

Figure 36. Die to Package Alignment

Glass





Notes:

Double Sided AR Coated Glass

1. Multi-Layer Anti-Reflective Coating on 2 Sides:
   Double Sided Reflectance:
   Range (mm)
   420−450 nm < 2%
   450−630 nm < 1%
   630−680 nm < 2%
2. Dust, Scratch Specification − 20 microns max.
3. Substrate − Schott D236T eco or equivalent
4. Epoxy: NCO−150HB
   Thickness: 0.002″−0.005″

Clear Glass

1. Materials: Substrate − Schott D236T eco or equivalent
2. No Epoxy
3. Dust, Scratch Count − 20 microns max.
4. Reflectance:
   420−435 nm < 10%
   435−630 nm < 10%
   630−680 nm < 10%

Figure 37. Glass Drawing

Glass Transmission

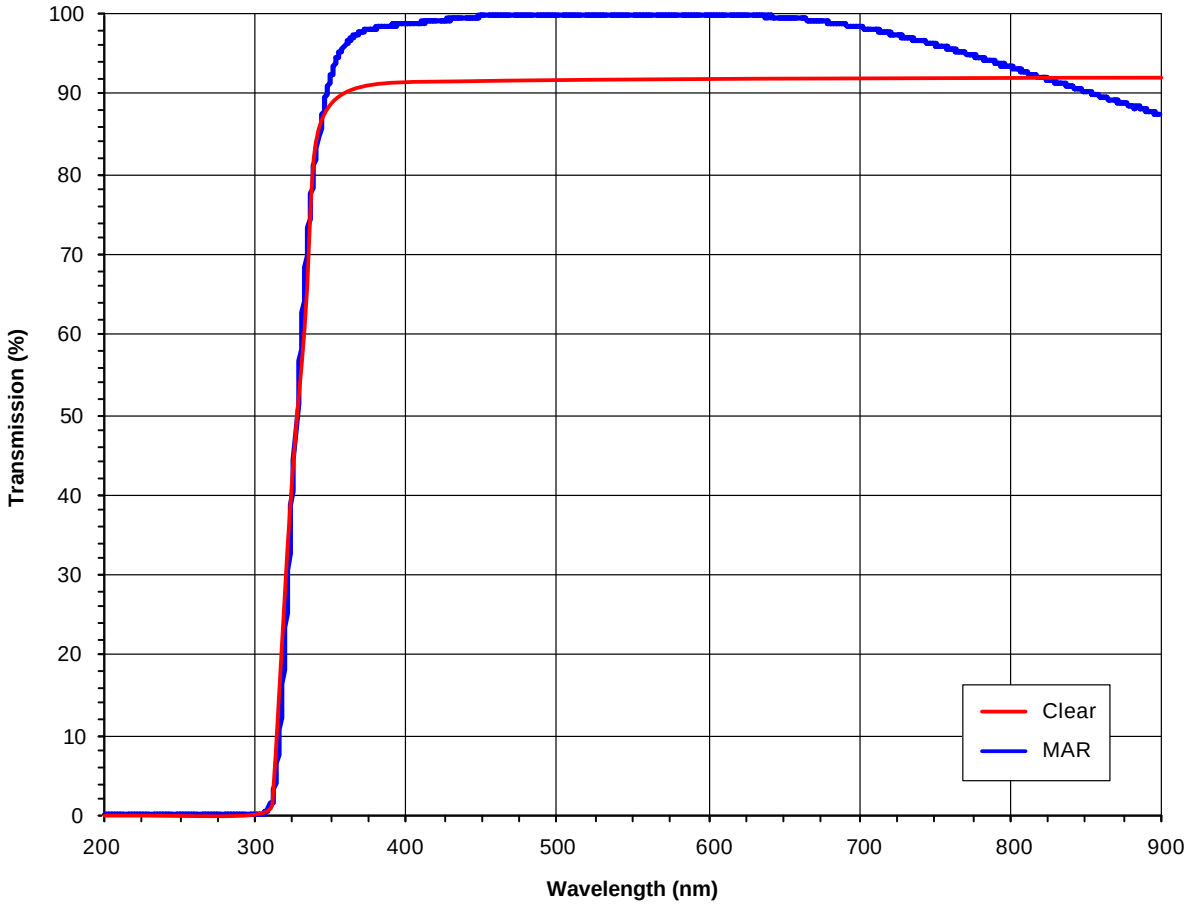


Figure 38. MAR and Clear Glass Transmission

ON Semiconductor and the ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative