Ordering number : ENA4817A

LC78211, 78212, 78213

CMOS LSI

Analog Function Switch

ON Semiconductor®

http://onsemi.com

Applications

Function switching under serial data control in amplifiers, receivers, and other electronic equipment.

Features

- Two sets of eight (or in the LC78213, seven) built-in circuits with three switching configurations available based on differing internal connections.
- Control according to serial data sent from a microprocessor, and easy connection to 5 V microprocessors.
- Two identical products can be connected to a shared bus due to the provision of a select pin (S).
- A reset pin that turns off all analog switches.
- A ±20 V withstand voltage rating allows these products to provide a wide dynamic range.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +20	V
	V_{EE} max	V_{EE}	–20 to +0.3	V
Maximum input voltage	VI1	DI, CL, CE, S, $\overline{RES}$	–0.3 to +20	V
	VI2	L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	V_{EE} – 0.3 to V_{DD} + 0.3	V
Analog switch potential difference when on	ΔVON	With the switch on	0.5	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	100	mW
Operating temperature range	Topr		–30 to +75	°C
Storage temperature range	Tstg		–40 to +125	°C

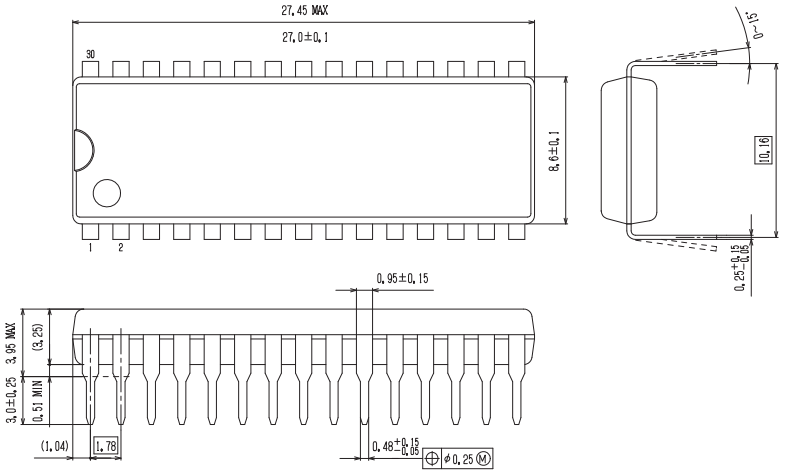
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

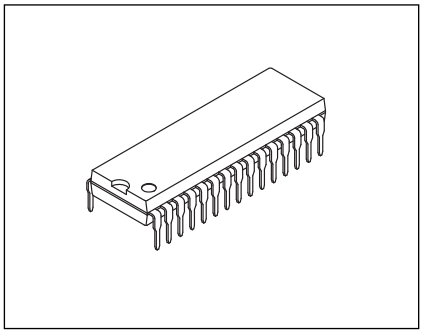
Package Dimensions

unit : mm

PDIP30 / DIP30SD (400mil)

CASE 646AZ





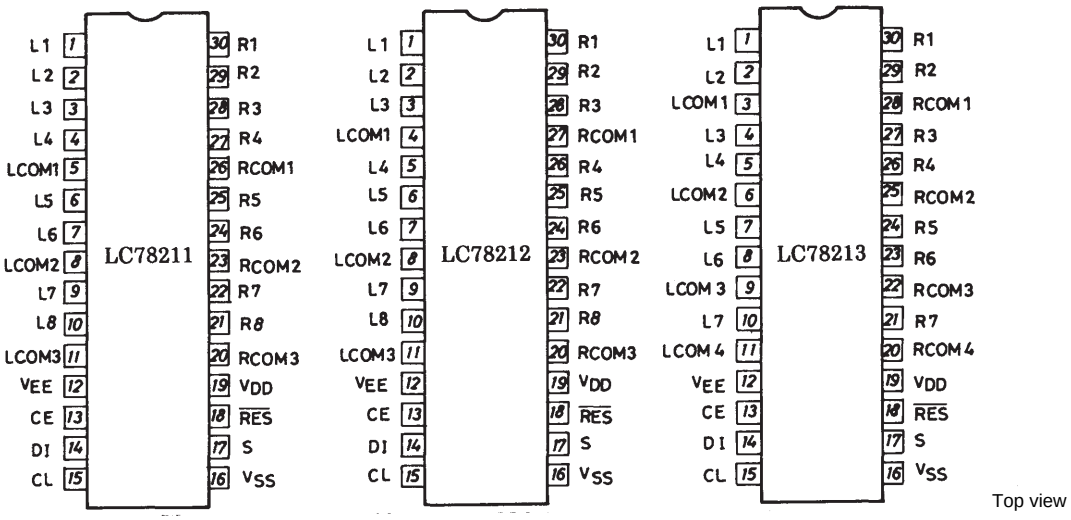
DIP30SD (400mil)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

Semiconductor Components Industries, LLC, 2013

Pin Assignments

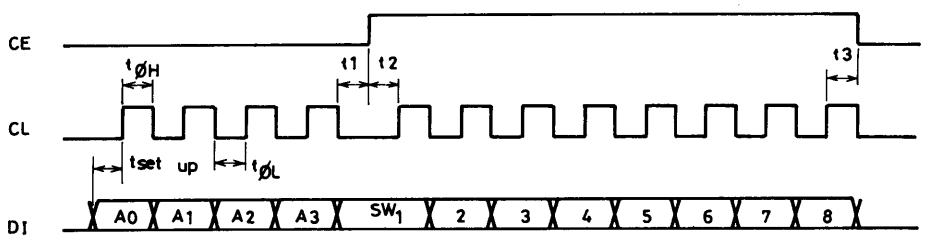


Top view

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V, $|V_{DD}| \geq |V_{EE}|$

Parameter	Symbol	Conditions	min	typ	max	Unit
Maximum supply voltage	V_{DD}	$V_{DD} - V_{EE} \geq 12$ V: V_{DD}	6.0		18.5	V
	V_{EE}	$V_{DD} - V_{EE} \geq 12$ V: V_{EE}	–18.5		0	V
Input high level voltage	$V_{IH}1$	DI, CL, CE	4.0		18.5	V
	$V_{IH}2$	S, $\overline{RES}$	0.7 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}1$	DI, CL, CE	0		0.7	V
	$V_{IL}2$	S, $\overline{RES}$	0		0.3 V_{DD}	V
Analog switch input voltage range	V_{IN}	L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	V_{EE}		V_{DD}	V
Low level clock pulse width	$t_{øL}$	CL	0.5			µs
High level clock pulse width	$t_{øH}$	CL	0.5			µs
Setup time	$t_{set\ up}$	CL, DI	0.5			µs
	t1*	CL, CE	0.5			µs
	t2*	CL, CE	0.5			µs
	t3*	CL, CE	0.5			µs
Minimum reset pulse width	t_{wRES}	$V_{DD} \geq 6$ V: $\overline{RES}$	1.0			µs
Hysteresis	V_H	CL, CE, DI	0.3			V

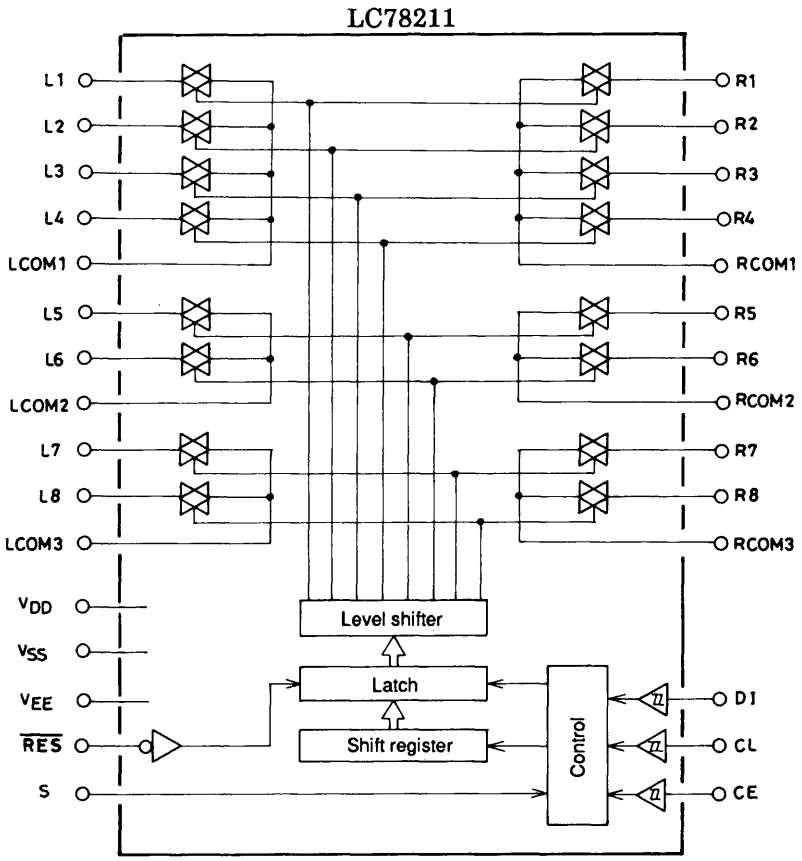
Note: * CE, CL and DI waveforms



Electrical Characteristics at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Analog switch on resistance	$R_{ON}1$	I = 1 mA, $V_{DD} - V_{EE}$ = 12 V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		150		Ω
	$R_{ON}2$	I = 1 mA, $V_{DD} - V_{EE}$ = 37 V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		70		Ω
Total harmonic distortion	THD1	V_{IN} = 1 Vrms, f = 1 kHz, $V_{DD} - V_{EE}$ = 37 V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		0.0015	0.01	%
	THD2	V_{IN} = 0.1 Vrms, f = 1 kHz, $V_{DD} - V_{EE}$ = 37 V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		0.01	0.05	%
Feedthrough	F_{TH}	V_{IN} = 0 dBV, f = 10 kHz, $V_{DD} - V_{EE}$ = 37 V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		55		dB
Crosstalk	CT	V_{IN} = 0 dBV, f = 10 kHz, $V_{DD} - V_{EE}$ = 37 V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		75		dB
Input high level current	I_{IH}	V_I = 18.5 V: DI, CL, CE, S, $\overline{RES}$			+10	μA
Input low level current	I_{IL}	V_I = 0 V: DI, CL, CE, S, $\overline{RES}$	–10			μA
Analog switch leakage current (off state)	I_{OFF}	$V_I = V_{EE}$ to V_{EE} + 37 V: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	–10		+10	μA
Current drain	I_{DD}	V_{DD}			1.0	mA

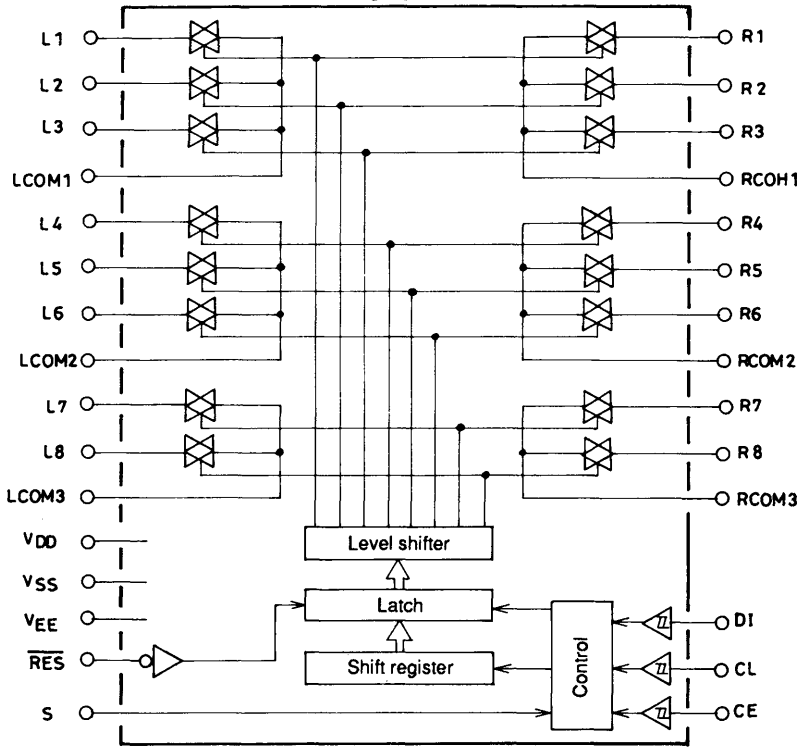
Equivalent Circuit Block Diagrams



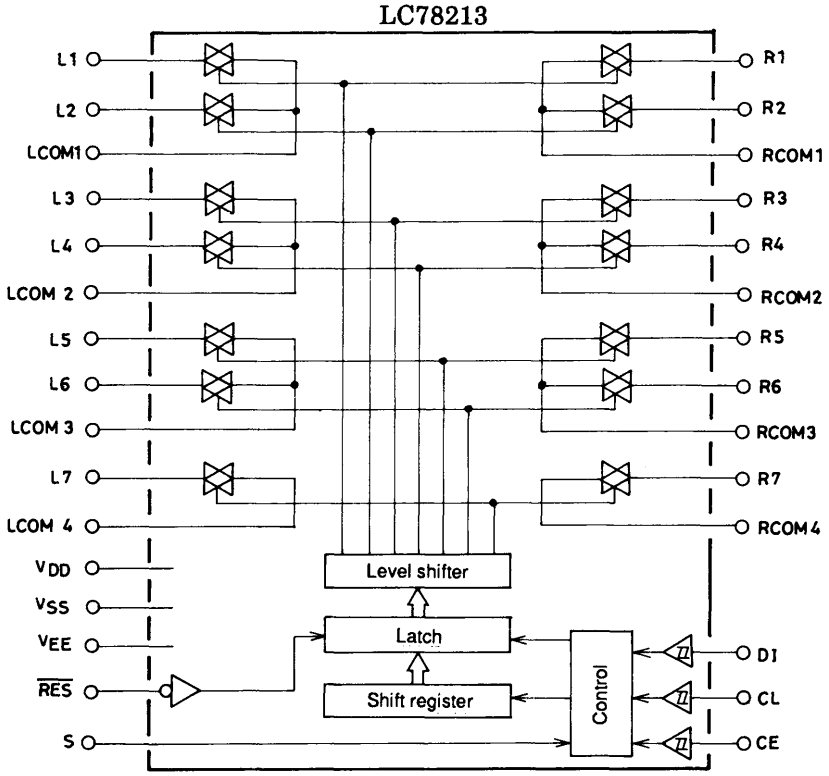
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LC78212



LC78213



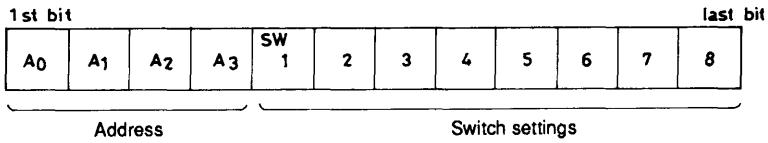
Pin Functions

<table>
<tr><th>Pin</th><th>I/O</th><th>Internal equivalent circuit</th><th>Pin function</th></tr>
<tr><td>V_{DD}, V_{SS}, V_{EE}</td><td></td><td></td><td>Power supply</td></tr>
<tr><td>L1 to L8, R1 to R8,
LCOM1 to LCOM4,
RCOM1 to RCOM4</td><td></td><td>See the block diagram.</td><td>Analog switch input and output</td></tr>
<tr><td>CL, DI, CE</td><td>I</td><td></td><td>Serial data input (Schmitt buffer)
CL.....Clock input
DI.....Data input
CE .....Chip enable</td></tr>
<tr><td>S</td><td>I</td><td></td><td>Selection of one of two chips
The address is set to the values shown in the table below according to the level input to the S pin.
<table>
<tr><th rowspan="2">Product</th><th rowspan="2">S pin level</th><th colspan="4">Address</th></tr>
<tr><th>A_0</th><th>A_1</th><th>A_2</th><th>A_3</th></tr>
<tr><td rowspan="2">LC78211</td><td>L</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>H</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td rowspan="2">LC78212</td><td>L</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>H</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td rowspan="2">LC78213</td><td>L</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>H</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td></td><td>Reset input
The states of the analog switches are undefined when power is first applied. Setting this pin low will force all switches the off state.</td></tr>
</table>

Operation

1. Data Input Procedure

   The LC78211, LC78212 and LC78213 are controlled by inputting specified data to the CL, DI and CE pins. The input data consists of 12 bits, of which four bits are address and eight bits are data.



   Bits correspond to the L1 to L8 and R1 to R8 analog switches, and a value of one turns the corresponding switch on, and a value of zero turns it off.

   0.....Off

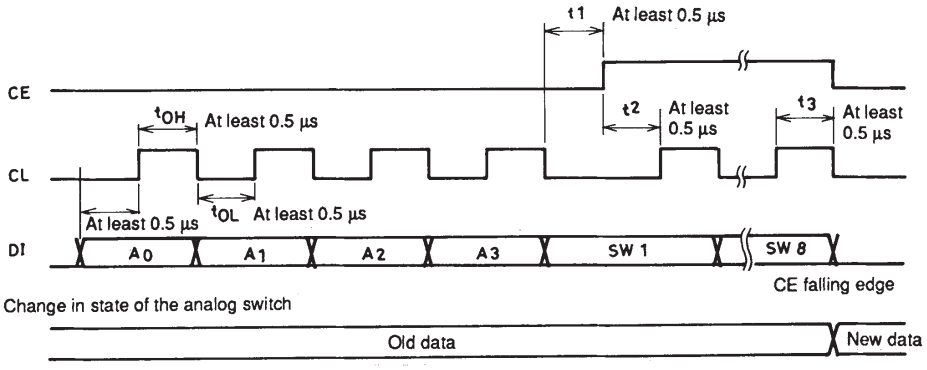
   1.....On

   The address is used when the chip is connected to a shared bus. The data (address) that must be transmitted depends on the S pin and the particular product as shown in the table below.

Product	S pin level	Address			
		A_0	A_1	A_2	A_3
LC78211	L	0	1	0	1
	H	1	1	0	1
LC78212	L	0	0	1	1
	H	1	0	1	1
LC78213	L	0	1	1	1
	H	1	1	1	1

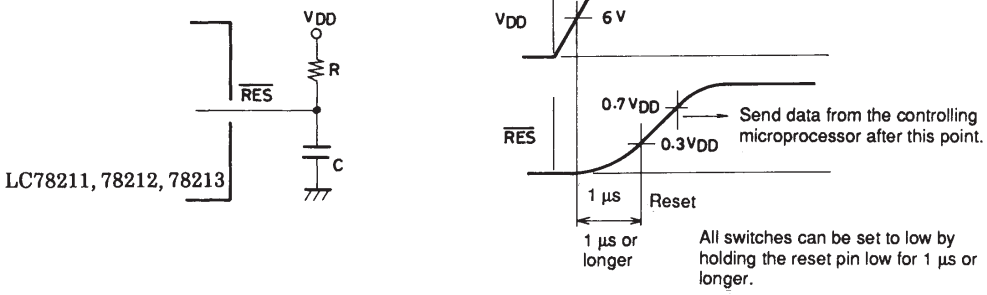
   Note: The bit for switch eight in the LC78213 is a “don’t care” bit, that is it can be either 0 or 1 without affecting chip function. This is because the LC78213 has two sets of seven (not eight) circuits.

2. DI, CL and CE Timing



Data is read in on the rising edge of CL and latched on the falling edge of CE.

3. Notes on the Reset Pin
The states of the analog switches are undefined when power is first applied. However, it is possible to use the reset pin to force all switches to the off state by connecting an RC circuit to this pin.



4. Using a CCB Bus with Multiple ICs
The LC78211, LC78212 and LC78213 retain their prior state until they receive data with a matching address.

5. Replacing Earlier Models
Caution is required when replacing an LC7821N, LC7823N and LC7823N with an LC78211, LC78212 and LC78213, since the S pin threshold levels differ.

6. Handling of Unused Input Pins
We recommend connecting any unused switch pin to V_{SS} through a resistor of up to a few 100 k to prevent damage from static electricity.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC78211-E	DIP30SD(400mil) (Pb-Free / Halogen Free)	20 / Fan-Fold
LC78212-E	DIP30SD(400mil) (Pb-Free / Halogen Free)	20 / Fan-Fold
LC78213-E	DIP30SD(400mil) (Pb-Free / Halogen Free)	20 / Fan-Fold

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