LM25005 42V, 2.5A Step-Down Switching Regulator

1 Features

- Integrated 42V, 160mΩ N-channel MOSFET
- Ultra-wide input voltage range: from 7V to 42V
- Internal bias regulator
- Adjustable output voltage: from 1.225V
- Feedback reference accuracy: 1.5%
- Current mode control with emulated inductor current ramp
- Single resistor oscillator frequency setting
- Oscillator synchronization input
- Programmable soft-start
- Shutdown and standby input
- Wide bandwidth error amplifier
- Thermal shutdown

2 Applications

- Industrial to high-efficiency point-of-load regulators
- Telecommunications infrastructure
- Factory automation and control

3 Description

The LM25005 switching regulator features all of the functions necessary to implement an efficient, high voltage buck regulator using a minimum of external components. This easy to use regulator includes a 42V, 160mΩ, N-channel MOSFET, with an output current capability of 2.5A.

The regulator control method is based upon current mode control using an emulated current ramp. Current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage applications.

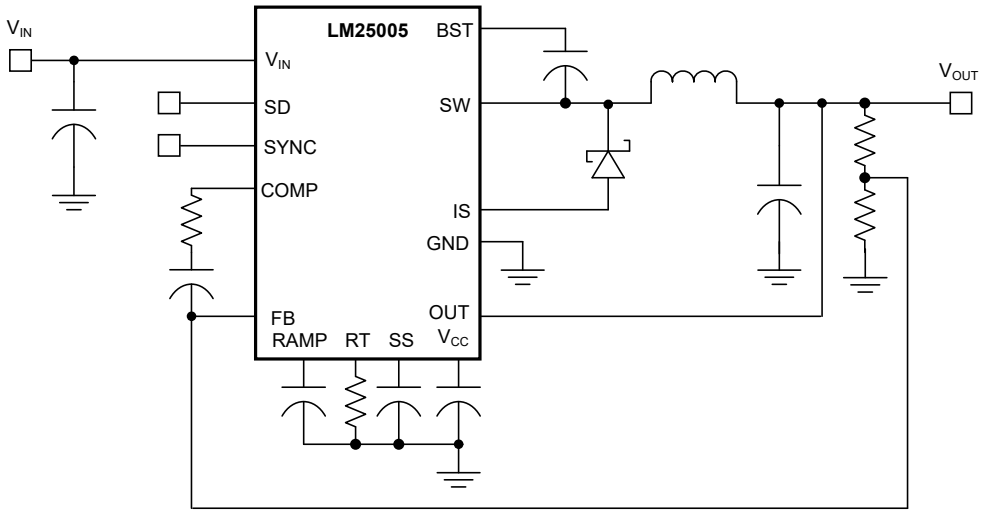
The operating frequency is programmable from 50kHz to 500kHz. An oscillator synchronization pin allows multiple LM25005 regulators to self-synchronize or synchronize to an external clock.

Additional protection features include current limit, thermal shutdown, and remote shutdown capability. The device is available in a power-enhanced HTSSOP package featuring an exposed die attach pad to aid thermal dissipation.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM25005	PWP (HTSSOP, 20)	6.5mm × 4.4mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

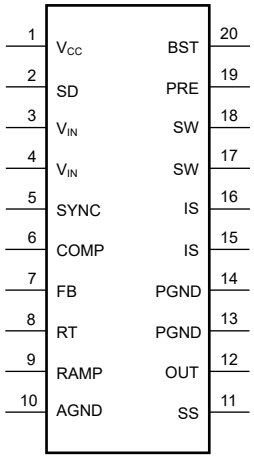


Figure 4-1. Top View 20-Lead HTSSOP

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	10	GND	Analog ground. Internal reference for the regulator control functions.
BST	20	P	Boost input for bootstrap capacitor. Connect an external capacitor between the BST and SW pins. A 22nF ceramic capacitor is recommended. The capacitor charges from VCC through an internal bootstrap diode during the off-time of the buck switch when the SW-node voltage is low
COMP	6	O	Output of the internal error amplifier, verify that the loop compensation network connects between this pin and the FB pin.
EP		P	Exposed pad. Exposed metal pad on the underside of the device. Connect this pad to the PCB ground plane to assist with heat spreading.
FB	7	I	Feedback signal from the regulated output. This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.225V.
IS	15, 16	P	Current sense. Current measurement connection for the freewheeling Schottky diode. An internal sense resistor and a sample-and-hold circuit sense the diode current near the conclusion of the off-time. This current measurement provides the DC level of the emulated current ramp.
OUT	12	I	Output voltage connection. Connect directly to the regulated output voltage.
PGND	13, 14	GND	Power ground. Low-side reference for the integrated PRE switch and the IS current sense resistor.
PRE	19	P	Precharge assist for the bootstrap capacitor. Connect this open-drain output to the SW pins to aid charging the bootstrap capacitor during light-load conditions or in applications where the output is precharged before the LM25005 is enabled. An internal precharge MOSFET is turned on for 250ns each cycle just prior to the on-time interval of the buck switch.
RAMP	9	I	Ramp control signal. An external capacitor connected between RAMP and AGND pins sets the ramp slope used for emulated peak current-mode control. Recommended capacitance range is 50pF to 2nF.
RT	8	I	Internal oscillator frequency set input. The internal oscillator is set with a single resistor connected between RT and AGND pins. The recommended switching frequency range is 50kHz to 500kHz.
SD	2	I	Shutdown or UVLO input. If the SD pin voltage is below 0.7V, the regulator is in a low power state. If the SD pin voltage is between 0.7V and 1.225V, the regulator is in standby mode. If the SD pin voltage is above 1.225V, the regulator is operational. Use an external voltage divider to set a line undervoltage shutdown threshold. If the SD pin is left open circuit, a 5µA pullup current source configures the regulator as fully operational.
SS	11	I	Soft-start. An external capacitor and an internal 10µA current source set the ramp rate for the rise of the error amplifier's reference. The SS pin is held low during standby, VCC UVLO and thermal shutdown.

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PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SW	17, 18	P	Switching node. The source terminal of the internal buck switch. Connect the SW pin to the external Schottky diode and to the buck inductor.
SYNC	5	I/O	Oscillator synchronization input or output. The internal oscillator can synchronize to an external clock with an external pulldown device. Multiple LM25005 regulators can synchronize together by connection of the SYNC pins.
VCC	1	I	Output of the bias regulator. Vcc tracks Vin up to 9V. Beyond 9V, Vcc is regulated to 7V. A 0.1uF to 1uF ceramic decoupling capacitor is required. Apply an external voltage (7.5V – 14V) to this pin to reduce internal power dissipation.
VIN	3, 4	P	Input supply voltage, nominal operating range: 7V to 42V

(1) I = inputs, O = outputs, P = power, I/O = bidirectional, GND = ground



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperate range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
	V_{IN} to GND	45		V
	BST to GND	60		V
	PRE to GND	45		V
	SW to GND (Steady State)	-1.5		V
	BST to V_{CC}	45		V
	V_{CC} to GND	14		V
	BST to SW	14		V
	OUT to GND	Limited to Vin		
	SD, SYNC, SS, FB to GND	7V		V
Junction temperature	T_J	-40	+150	C
Storage temperature	T_{stg}	-65	+150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22- C101(3)	±500	

(1) The human-body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{IN}			7		42	7
T_J	Operation junction temperature		−40		+125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device can occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

5.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		LM25005 PWP (HTSSOP) 20 pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.3	°C/W

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5.4 Thermal Resistance Characteristics (continued)

THERMAL METRIC[1]		LM25005 PWP (HTSSOP) 20 pins	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

5.5 Electrical Characteristics

Typical values correspond to T_J = 25°C, V_{IN} = 24V, R_T = 32.4kΩ. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
V_{CC} Reg	V_{CC} Regulator Output		6.85	7.15	7.45	V
	V_{CC} LDO Mode turn-off			9		V
	V_{CC} Current Limit	V_{CC} = 0V,		25		mA
VCC SUPPLY						
	V_{CC} UVLO Threshold	VCC Increasing	5.03	5.35	5.67	V
	V_{CC} Undervoltage Hysteresis			0.25		V
	Bias Current (Iin)	FB = 1.3V.		2	4.5	mA
	Shutdown Current (Iin)	SD = 0V.		48	85	µA
SHUTDOWN THRESHOLDS						
	Shutdown Threshold		0.47	0.7	0.9	V
	Shutdown Hysteresis			0.1		V
	Standby Threshold		1.17	1.225	1.28	V
	Standby Hysteresis			0.1		V
	SD Pull-up Current Source			5		µA
SWITCH CHARACTERISTICS						
	Buck Switch Rds(on)			170	340	mΩ
	BOOST UVLO			3.8		V
	BOOST UVLO Hysteresis			0.8		V
	Pre-charge Switch Rds(on)			70		Ω
	Pre-charge Switch on-time			265		ns
CURRENT LIMIT						
	Cycle by Cycle Current Limit Delay	RAMP = 2.5V.		75		ns
SOFT-START						
	SS Current Source		7	10	14	µA
OSCILLATOR						
	Frequency1		180	200	220	kHz
	Frequency2	R_T = 11kΩ.	425	485	545	kHz
	SYNC Source Impedance			11		kΩ
	SYNC Sink Impedance			110		Ω
	SYNC Threshold (falling)			1.4		V
	SYNC Frequency	R_T = 11kΩ.	550			kHz
	SYNC Pulse Width Minimum		15			ns
RAMP GENERATOR						
	Ramp Current 1	V_{IN} = 36V, V_{OUT} = 10V.	136	160	184	µA
	Ramp Current 2	V_{IN} = 10V, V_{OUT} = 10V.	18	25	32	µA
PWM COMPARATOR						
	Forced Off-time		416	500	575	ns
	Min On-time			80		ns

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Typical values correspond to T_J = 25°C, V_{IN} = 24V, R_T = 32.4kΩ. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	COMP to PWM Comparator Offset			0.7		V
ERROR AMPLIFIER						
	Feedback Voltage	Vfb = COMP.	1.207	1.225	1.243	µV
	FB Bias Current			10		nA
	DC Gain			70		dB
	COMP Sink / Source Current		3			mA
	Unity Gain Bandwidth			3		MHz
DIODE SENSE RESISTANCE						
D_{SENSE}				42		mΩ
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			165		°C
T_{SD-HYS}	Thermal Shutdown hysteresis			25		°C

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).

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5.6 Typical Characteristics

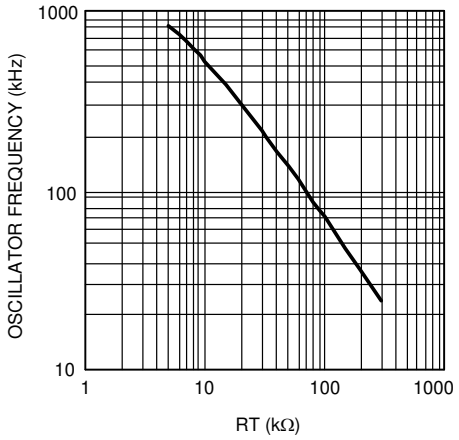


Figure 5-1. Oscillator Frequency vs R_T

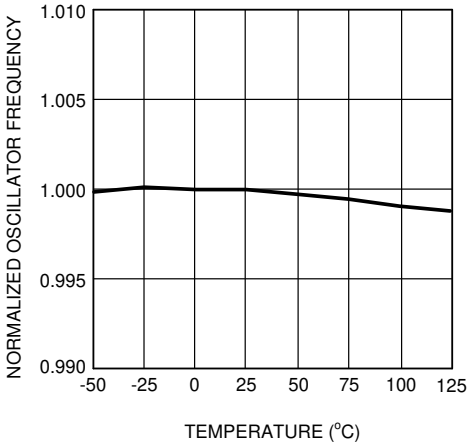


Figure 5-2. Oscillator Frequency vs Temperature F_{OSC} = 200kHz

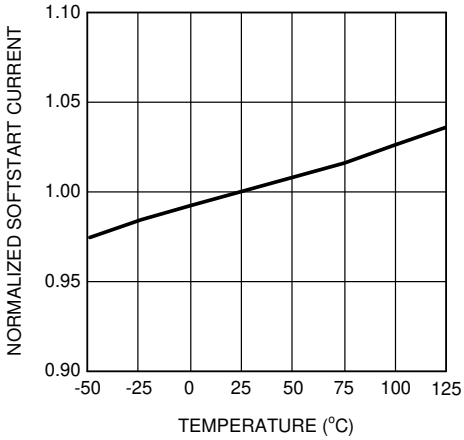


Figure 5-3. Soft Start Current vs Temperature

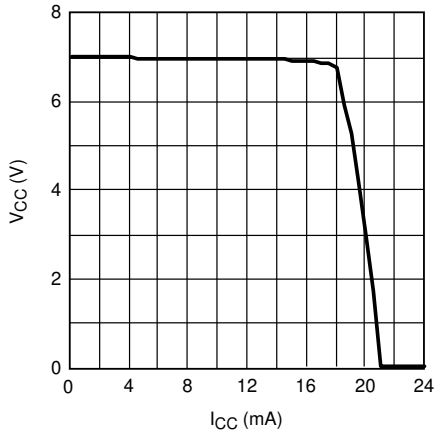


Figure 5-4. V_{CC} vs I_{CC}, V_{IN} = 12V

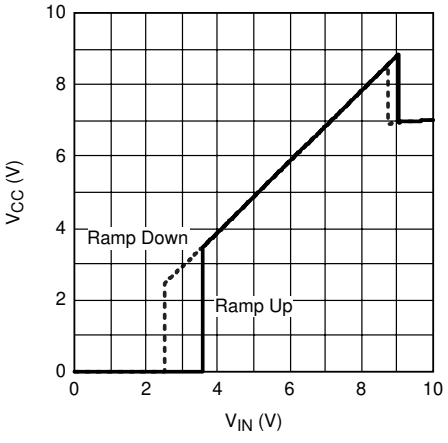


Figure 5-5. V_{CC} vs V_{IN}, R_L = 7kΩ

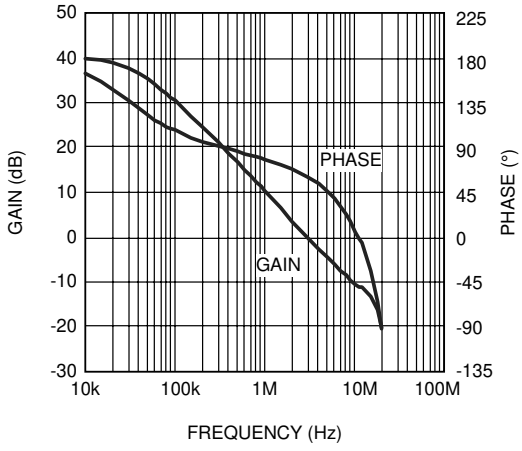


Figure 5-6. Error Amplifier Gain/Phase A_{VCL} = 101

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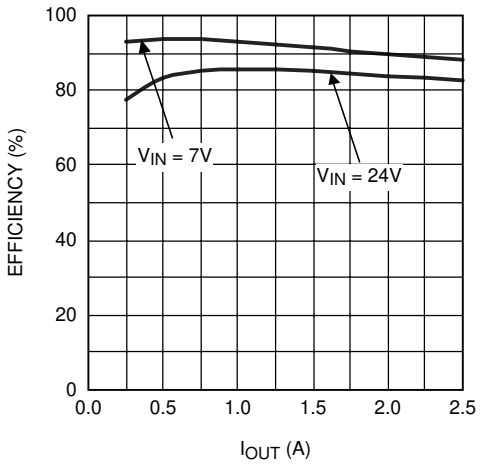


Figure 5-7. Demoboard Efficiency vs I_{OUT} and V_{IN}

6 Detailed Description

6.1 Overview

The LM25005 switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates a 42V N-Channel buck switch with an output current capability of 2.5 Amps.

The regulator control method is based on current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications.

The operating frequency is user programmable from 50kHz to 500kHz. An oscillator synchronization pin allows multiple LM25005 regulators to self synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225V.

Fault protection features include, current limiting, thermal shutdown and remote shutdown capability. The device is available in the HTSSOP package featuring an exposed pad to aid thermal dissipation.

The functional block diagram and typical application of the LM25005 are shown in the Section 6.2. The LM25005 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is well suited for telecom, industrial and automotive power bus voltage ranges.

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6.2 Functional Block Diagram

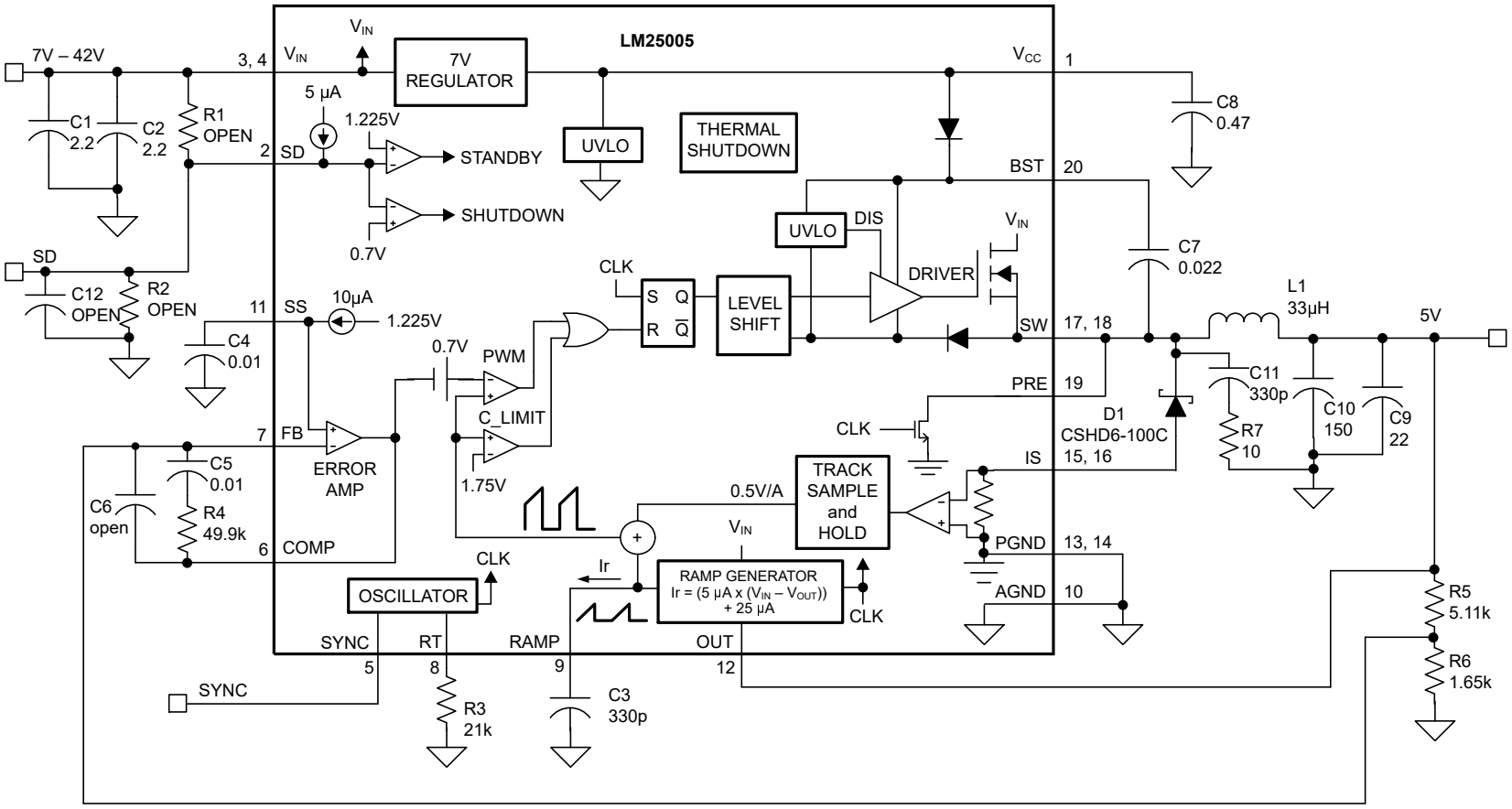


Figure 6-1. Typical Application Circuit and Functional Block Diagram

6.3 Feature Description

6.3.1 High Voltage Start-Up Regulator

The LM25005 contains a dual-mode internal high voltage startup regulator that provides the Vcc bias supply for the PWM controller and boot-strap MOSFET gate driver. The input pin (Vin) can be connected directly to the input voltage, as high as 42 Volts. For input voltages below 9V, a low dropout switch connects Vcc directly to Vin. In this supply range, Vcc is approximately equal to Vin. For Vin voltage greater than 9V, the low dropout switch is disabled and the Vcc regulator is enabled to maintain Vcc at approximately 7V. The wide operating range of 7V to 42V is achieved through the use of this dual mode regulator.

The output of the Vcc regulator is current limited to 20mA. Upon power up, the regulator sources current into the capacitor connected to the Vcc pin. When the voltage at the Vcc pin exceeds the Vcc UVLO threshold of 6.3V and the SD pin is greater than 1.225V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until Vcc falls below 5.3V or the SD pin falls below 1.125V.

Apply an auxiliary supply voltage to the Vcc pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 7.3V, the internal regulator essentially shuts off, reducing the IC power dissipation. The Vcc regulator series pass transistor includes a diode between Vcc and Vin. Do not forward bias the diode in normal operation. Therefore the auxiliary Vcc voltage never exceeds the Vin voltage.

In high voltage applications, take extra care to ensure that the Vin pin does not exceed the absolute maximum voltage rating of 45V. During line or load transients, voltage ringing on the Vin line that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the Vin and GND pins are essential.

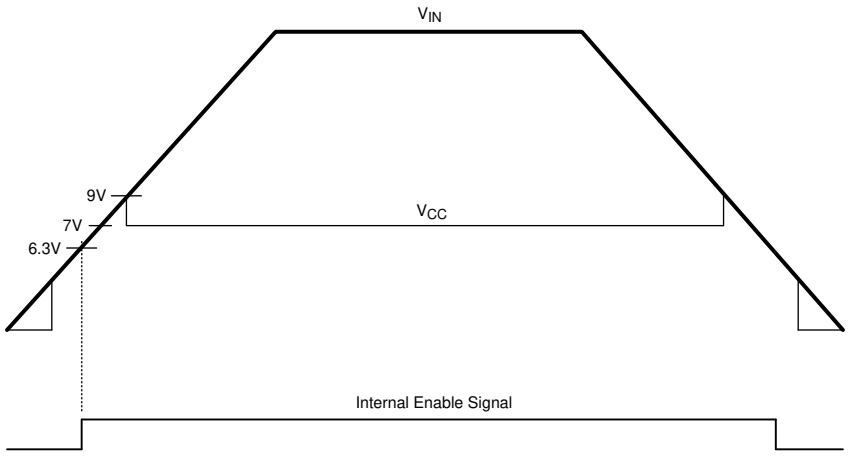


Figure 6-2. Vin and Vcc Sequencing

6.3.2 Oscillator and Sync Capability

The LM25005 oscillator frequency is set by a single external resistor connected between the RT pin and the AGND pin. Locate the R_T resistor very close to the device and connect the resistor directly to the pins of the IC (RT and AGND).To set a desired oscillator frequency (F), calculate the necessary value for the R_T resistor from the following equation:

$$R_T = \frac{\frac{1}{F} - 580 \times 10^{-9}}{135 \times 10^{-12}} \quad (1)$$

Use the SYNC pin to synchronize the internal oscillator to an external clock. The external clock must be of *higher frequency* than the free-running frequency set by the R_T resistor. A clock circuit with an open drain output is the recommended interface from the external clock to the SYNC pin. Verify that the clock pulse duration is greater than 15ns.

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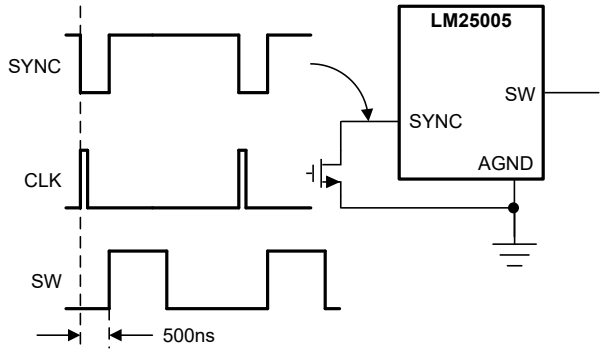


Figure 6-3. Sync From External Clock

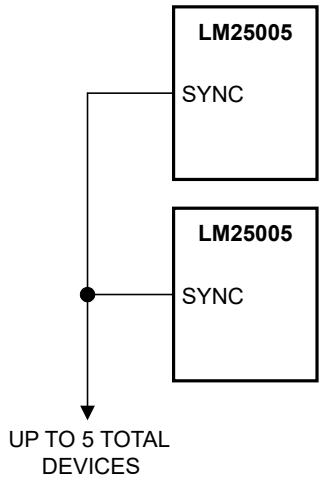


Figure 6-4. Sync From Multiple Devices

Multiple LM25005 or LM5005 devices synchronize together by connecting the SYNC pins. In this configuration all of the devices synchronize to the highest frequency device. The diagram in Figure 6-5 illustrates the SYNC input and output features of the LM25005. The internal oscillator circuit drives the SYNC pin with a strong pull-down and weak pull-up inverter. When the SYNC pin is pulled low, either by the internal oscillator or an external clock, the ramp cycle of the oscillator terminates and a new oscillator cycle begins. Thus, if the SYNC pins from the IC of several LM25005 connect together, the IC with the highest internal clock frequency pulls the connected SYNC pins low first and terminate the oscillator ramp cycles of the other IC. The LM25005 or LM5005 with the highest programmed clock frequency serve as the controller and control the switching frequency of the all the devices with lower oscillator frequency.

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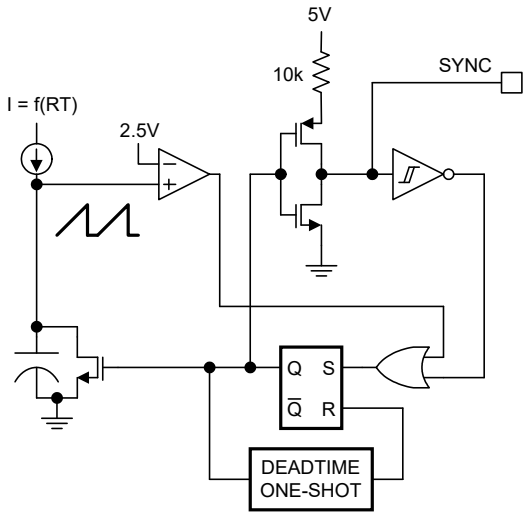


Figure 6-5. Simplified Oscillator Block Diagram and SYNC I/O Circuit

6.3.3 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.225V). The output of the error amplifier is connected to the COMP pin allowing the user to provide loop compensation components, generally a type II network, as illustrated in Section 6.2. This network creates a pole at DC, a zero and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

6.3.4 RAMP Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the output inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement can introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulse-width. In applications where the input voltage can be relatively large in comparison to the output voltage, controlling small pulse-widths and duty cycles is necessary for regulation. The LM25005 uses a unique ramp generator, which does not actually measure the buck switch current, but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements, a sample and hold DC level and an emulated current ramp.

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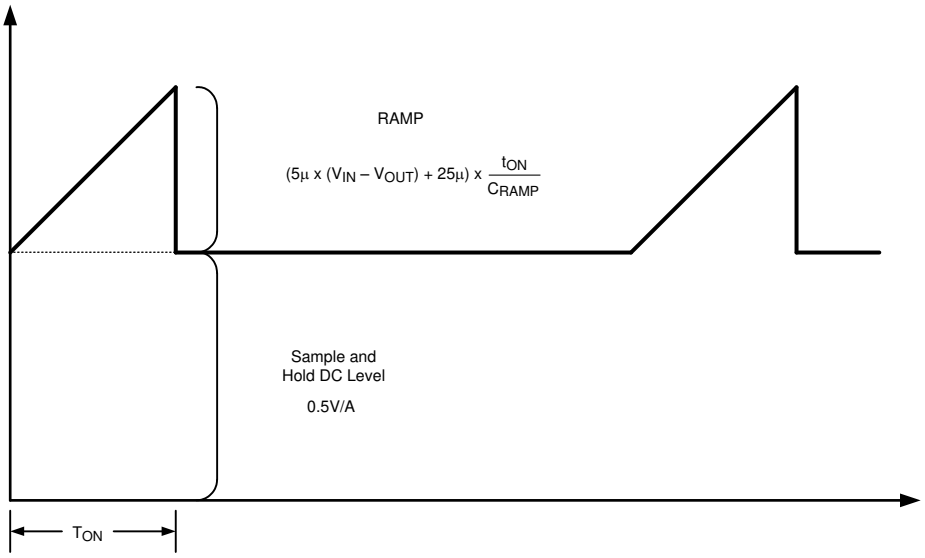


Figure 6-6. Composition of Current Sense Signal

The sample and hold DC level illustrated in Figure 6-6, is derived from a measurement of the re-circulating Schottky diode anode current. Connect the re-circulating diode anode to the IS pin. The diode current flows through an internal current sense resistor between the IS and PGND pins. The voltage level across the sense resistor is sampled and is held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample and hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the Vin and Vout voltages per the following equation:

$$I_{RAMP} = [5\mu \times (V_{IN} - V_{OUT})] + 25\mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor. Select the value of C_{RAMP}:

$$C_{RAMP} = L \times 10^{-5} \quad (3)$$

- L = value of the output inductor in Henrys

With this value, the scale factor of the emulated current ramp is approximately equal to the scale factor of the dc level sample and hold (0.5V/A). Locate the C_{RAMP} capacitor very close to the device and connect the capacitor directly to the pins of the IC (RAMP and AGND).

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 25µA of offset current provided from the emulated current source adds some fixed slope to the ramp signal. In some high output voltage, high duty cycle applications, an additional slope is required. In these applications, add a pull-up resistor between the V_{CC} and RAMP pins to increase the ramp slope compensation.

For V_{OUT} > 7.5V:

Calculate optimal slope current:

$$I_{OS} = V_{OUT} \times 5\mu A/V \quad (4)$$

For example, at V_{OUT} = 10V, I_{OS} = 50µA.

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Install a resistor from the RAMP pin to V_{CC}:

$$R_{RAMP} = \frac{V_{CC}}{[I_{OS} - 25\mu A]} \quad (5)$$

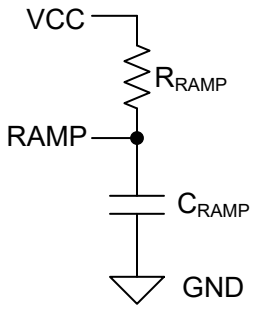


Figure 6-7. R_{RAMP} to V_{CC} for V_{OUT} > 7.5V

6.3.5 Soft-Start

The soft-start feature allows the regulator to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The internal soft-start current source, set to 10µA, gradually increases the voltage of an external soft-start capacitor connected to the SS pin. The soft-start capacitor voltage connects to the reference input of the error amplifier. Implement various sequencing and tracking schemes using external circuits that limit or clamp the voltage level of the SS pin.

In the event a fault is detected (for example, over-temperature, Vcc UVLO, SD) the soft-start capacitor discharges. When the fault condition is no longer present, a new soft-start sequence commences.

6.3.6 Current Limit

The LM25005 contains a unique current monitoring scheme for control and over-current protection. When set correctly, the emulated current sense signal provides a signal which is proportional to the buck switch current with a scale factor of 0.5V/A. The emulated ramp signal applies to the current limit comparator. If the emulated ramp signal exceeds 1.75V (3.5A) the present current cycle terminates (cycle-by-cycle current limiting). In applications with small output inductance and high input voltage, the switch current can overshoot due to the propagation delay of the current limit comparator. If an overshoot occurs, the diode current sampling circuit detects the excess inductor current during the off-time of the buck switch. If the Sample and Hold DC Level exceeds the 1.75V current limit threshold, the buck switch disables and skips pulses until the diode current sampling circuit detects the inductor current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any current overshoot.

6.4 Device Functional Modes

6.4.1 Shutdown / Standby

The LM25005 contains a dual level Shutdown (SD) circuit. When the SD pin voltage is below 0.7V, the regulator is in a low current shutdown mode. When the SD pin voltage is greater than 0.7V but less than 1.225V, the regulator is in standby mode. In standby mode, the Vcc regulator is active but the output switch is disabled. When the SD pin voltage exceeds 1.225V, the output switch enables and normal operation begins. An internal 5µA pull-up current source configures the regulator as fully operational if the SD pin is left open.

Use an external set-point voltage divider from Vin to GND to set the operational input range of the regulator. Design the divider so that the voltage at the SD pin is greater than 1.225V when Vin is in the desired operating range. Include the internal 5µA pull-up current source in calculations of the external set-point divider. Hysteresis of 0.1V is included for both the shutdown and standby thresholds. Verify that the voltage at the SD pin never exceeds 8V. When using an external set-point divider, clamping the SD pin to limit voltage at high input voltage conditions can be necessary.

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The SD pin can also be used to implement various remote enable or disable functions. Pulling the UVLO pin below the 0.7V threshold totally disables the controller. If the SD pin voltage is above 1.225V the regulator is operational.

6.4.2 Boost Pin

The LM25005 integrates an N-Channel buck switch and associated floating high voltage level shift or gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.022µF ceramic capacitor, connected with short traces between the BST pin and SW pin, is recommended. During the off-time of the buck switch, the SW pin voltage is approximately −0.5V and the bootstrap capacitor charge from Vcc through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch is forced off each cycle for 500ns to ensure that the bootstrap capacitor recharges.

Under very light load conditions or when the output voltage is pre-charged, the SW voltage does not remain low during the off-time of the buck switch. If the inductor current falls to zero and the SW pin rises, the bootstrap capacitor does not receive sufficient voltage to operate the buck switch gate driver. For these applications, connect the PRE pin to the SW pin to pre-charge the bootstrap capacitor. The internal pre-charge MOSFET and diode connected between the PRE pin and PGND turns on each cycle for 250ns just prior to the onset of a new switching cycle. If the SW pin is at a normal negative voltage level (continuous conduction mode), then no current flows through the pre-charge MOSFET or diode.

6.4.3 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165 degrees Celsius, the controller is forced into a low power reset state, disabling the output driver and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

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7 Application and Implementation

7.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.2 Application Information

7.2.1 Bias Power Dissipation Reduction

Buck regulators operating with high input voltage can dissipate an appreciable amount of power for the bias of the IC. Verify that the V_{CC} regulator steps-down the input voltage V_{IN} to a nominal V_{CC} level of 7V. The large voltage drop across the V_{CC} regulator translates into a large power dissipation within the Vcc regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. Figure 7-1 and Figure 7-2 depict two methods to bias the IC from the output voltage. In each case, the internal Vcc regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin potential is raised above the nominal 7V regulation level, which effectively disables the internal V_{CC} regulator. Verify that the voltage applied to the VCC pin never exceeds 14V and that the V_{CC} voltage is never larger than the V_{IN} voltage.

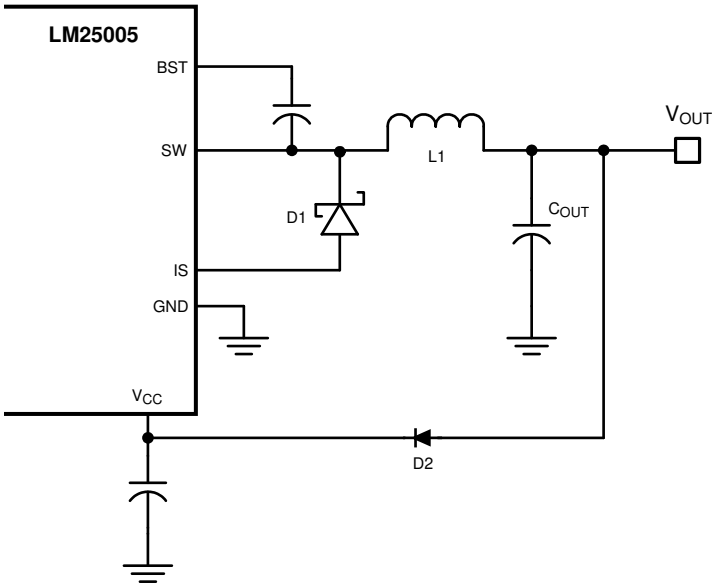


Figure 7-1. VCC Bias from VOUT for 8V < VOUT < 14V

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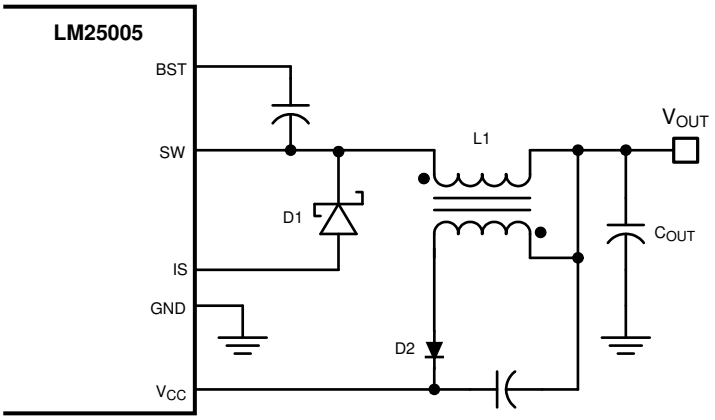


Figure 7-2. VCC Bias With Additional Winding on the Output Inductor

7.3 Typical Application

The following design procedure assists with component selection for the LM25005. Alternately, the WEBENCH® Design Tool is available to generate a complete design. With access to a comprehensive component database, the WEBENCH circuit design and selection simulation services use an iterative design procedure to create an optimized design, allowing the user to experiment with various design options.

7.3.1 Design Requirements

An example of the step-by-step procedure to generate power stage and compensation component values using the typical application setup of Figure 6-1 is given below. The circuit shown in Figure 6-1 is configured for the following specifications:

Table 7-1. Design Parameters

PARAMETER	VALUE
Input Voltage	7V to 42V
Output Voltage	5V
Minimum load current (for CCM)	250mA
Maximum load current	2.5A
Switching Frequency	300kHz

7.3.2 Detailed Design Procedure

The following sections explain the external component selection and application curves.

7.3.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the **LM25005** device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.3.2.2 External Components

The procedure for calculating the external components is illustrated with the following design example. The Bill of Materials for this design is listed in Table 7-2.

7.3.2.2.1 R3 (R_T)

R_T sets the oscillator switching frequency. Generally, higher frequency applications are smaller but have higher losses. This example uses operation at 300KHz as a reasonable compromise for both small size and high efficiency. Calculate the value of R_T for 300KHz switching frequency using Equation 6.

$$R_T = \frac{\left[\left(1 \div 300 \times 10^{3}\right) - 580 \times 10^{-9}\right]}{135 \times 10^{-12}} \quad (6)$$

R_T is the nearest standard value of 21kΩ.

7.3.2.2.2 L1

The inductor value is determined based

- Operating frequency
- Load current
- Ripple current
- Minimum input voltage ($V_{IN(min)}$)
- Maximum input voltage ($V_{IN(max)}$)

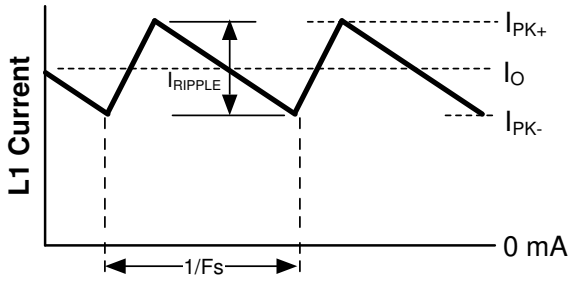


Figure 7-3. Inductor Current Waveform

To keep the circuit in continuous conduction mode (CCM), verify that the maximum ripple current I_{RIPPLE} is less than twice the minimum load current, or 0.5Ap-p. Using this value of ripple current, the value of inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT} \times \left[V_{IN(max)} - V_{OUT}\right]}{I_{RIPPLE} \times F_S \times V_{IN(max)}} \quad (7)$$

$$L1 = \frac{5V \times [42V - 5V]}{0.5A \times 300kHz \times 42V} = 29\mu H \quad (8)$$

This procedure provides a guide to select the value of L1. The nearest standard value (33µH) is used. Rate L1 for the peak current (I_{PK+}) to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. During an overload condition the peak current is limited to 3.5A nominal (4.25A maximum). The selected inductor (see Table 7-2) has a conservative 6.2A saturation current rating. For this manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30%, at 20°C.

7.3.2.2.3 C3 (C_{RAMP})

With the inductor value selected, the value of C3 (C_{RAMP}) necessary for the emulation ramp circuit is:

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$$C_{RAMP} = L \times 10^{-5} \quad (9)$$

where

- L is in Henrys (With L1 selected for 33µH the recommended value for C3 is 330pF)

7.3.2.2.4 C9, C10

The output capacitors C9 and C10 smooth the inductor ripple current and provide a source of charge for transient loading conditions. This design uses a 22µF ceramic capacitor and a 150µF SP organic capacitor. The ceramic capacitor provides ultra-low ESR to reduce the output ripple voltage and noise spikes, while the SP capacitor provides a large bulk capacitance in a small volume for transient loading conditions. An approximation for the output ripple voltage is:

$$\Delta V_{OUT} = \Delta I_L \times \left[ESR + \frac{1}{8 \times F_S \times C_{OUT}}\right] \quad (10)$$

7.3.2.2.5 D1

A Schottky-type re-circulating diode is required for all LM25005 applications. Ultra-fast diodes are not recommended and can result in damage to the IC due to reverse recovery current transients. The near-ideal reverse recovery characteristics and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications common to the LM25005. The reverse recovery characteristic determines how long the current surge lasts each cycle when the buck switch is turned on. The reverse recovery characteristics of Schottky diodes minimize the peak instantaneous power in the buck switch occurring during turn-on each cycle. The resulting switching losses of the buck switch are significantly reduced when using a Schottky diode. Select the reverse breakdown rating for the maximum V_{IN}, plus a safety margin.

The forward voltage drop has a significant impact on the conversion efficiency, especially for applications with a low output voltage. *Rated* current for diodes vary widely from various manufactures. The worst case is to assume a short circuit load condition. In this case, the diode almost continuously carries the output current. For the LM25005, this current is as high as 3.5A. Assuming a worst case 1V drop across the diode, the maximum diode power dissipation is as high as 3.5W. For the reference design, a 60V Schottky in a DPAK package is used.

7.3.2.2.6 C1, C2

The regulator supply voltage has a large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the VIN pin steps to the lower peak of the inductor current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into VIN during the on-time is the load current. Select the input capacitance for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

Select quality ceramic capacitors with a low ESR for the input filter. To allow for capacitor tolerances and voltage effects, use two 2.2µF, 100V ceramic capacitors. If step input voltage transients are expected near the maximum rating of the LM25005, complete a careful evaluation of ringing and possible spikes at the device VIN pin. Maximum rating cases can require an additional damping network or input voltage clamp.

7.3.2.2.7 C8

The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. The recommended value of C8 is no smaller than 0.1µF; verify that C8 is a good quality, low ESR, ceramic capacitor. This design uses a value of 0.47µF.

7.3.2.2.8 C7

The bootstrap capacitor between the BST and the SW pins supplies the gate current to charge the buck switch gate at turn-on. The recommended value of C7 is 0.022µF, verify that C7 is a good quality, low ESR, ceramic capacitor.

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7.3.2.2.9 C4

The capacitor at the SS pin determines the soft-start time, for example, the time for the reference voltage and the output voltage to reach the final regulated value. The time is determined using:

$$t_{ss} = \frac{C4 \times 1.225V}{10\mu A} \tag{11}$$

For this application, a C4 value of 0.01µF is used as this value corresponds to a soft-start time of 1ms.

7.3.2.2.10 R5, R6

R5 and R6 set the output voltage level, the ratio of these resistors is calculated USING:

$$R5/R6 = [V_{OUT} \div 1.225V] - 1 \tag{12}$$

For a 5V output, the R5/R6 ratio calculates to 3.082. Choose the resistors from standard value resistors, a good starting point is selection in the range of 1.0kΩ - 10kΩ. This instance uses a value of 5.11kΩ for R5 and 1.65kΩ for R6.

7.3.2.2.11 R1, R2, C12

Connect a voltage divider to the SD pin to set a minimum operating voltage $Vin_{(min)}$ for the regulator. If this feature is required, the easiest approach to select the divider resistor values is to select a value for R1 (from 10kΩ to 100kΩ is recommended), then calculate R2 from:

$$R2 = 1.225 \times \left[\frac{R1}{V_{IN(min)} + \left(5 \times 10^{-6} \times R1\right) - 1.225}\right] \tag{13}$$

Capacitor C12 provides filtering for the divider. Establish that the voltage at the SD pin never exceeds 8V. When using an external set-point divider, clamping the SD pin at high input voltage conditions can be necessary. The reference design uses the full range of the LM25005 (7V to 42V); therefore these components can be omitted. With the SD pin open circuit the LM25005 responds once the Vcc UVLO threshold is satisfied.

7.3.2.2.12 R7, C11

A snubber network across the power diode reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. In the limit, spikes beyond the rating of the LM25005 or the re-circulating diode can damage these devices. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. For the current levels typical for the LM25005a resistor value from 5Ω to 20Ω is adequate. Increasing the value of the snubber capacitor results in more damping but higher losses. Select a minimum value of C11 that provides adequate damping of the SW pin waveform at high load.

7.3.2.2.13 R4, C5, C6

R4, C5, and C6 configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R4 and C5. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM25005 is as follows:

$$\text{DC Gain}_{(MOD)} = G_{m(MOD)} \times R_{LOAD} = 2 \times R_{LOAD} \tag{14}$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD}) and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{p(MOD)} = \frac{1}{[2\pi R_{LOAD} C_{OUT}]} \tag{15}$$

For R_{LOAD} = 5Ω and C_{OUT} = 177µF, then $f_{p(MOD)}$ = 180Hz

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$$\text{DC Gain}_{(\text{MOD})} = 2 \times 5 = 10 = 20\text{dB} \quad (16)$$

For the design example of Section 6.2 the following modulator gain versus frequency characteristic is measured as shown in Figure 7-4.

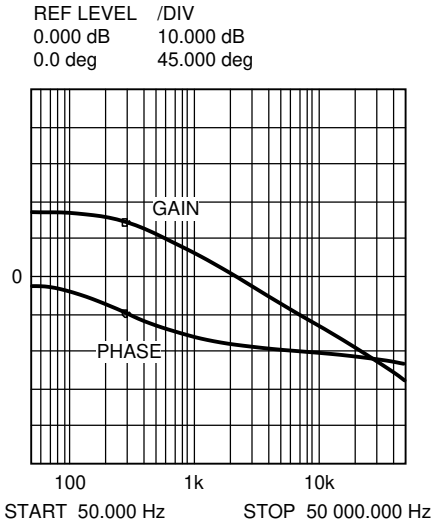


Figure 7-4. Gain and Phase of Modulator R_{LOAD} = 5Ω and C_{OUT} = 177µF

Components R4 and C5 configure the error amplifier as a type II configuration which has a pole at DC and a zero at

$$f_Z = \frac{1}{[2\pi R4C5]} \quad (17)$$

The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the loop gain. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

For the design example, the target loop bandwidth (crossover frequency) is 20kHz. Select the compensation network zero (f_Z) so that the value is at least an order of magnitude less than the target crossover frequency. This constrains the product of R4 and C5 for a desired compensation network zero 1 / (2π R4 C5) to be less than 2kHz. Increasing R4 while proportionally decreasing C5, increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C5, decreases the error amp gain. For the design example C5 is 0.01µF and R4 is 49.9kΩ. These values configure the compensation network zero at 320Hz. The error amp gain at frequencies greater than f_Z is: R4 / R5, which is approximately 10 (20dB).

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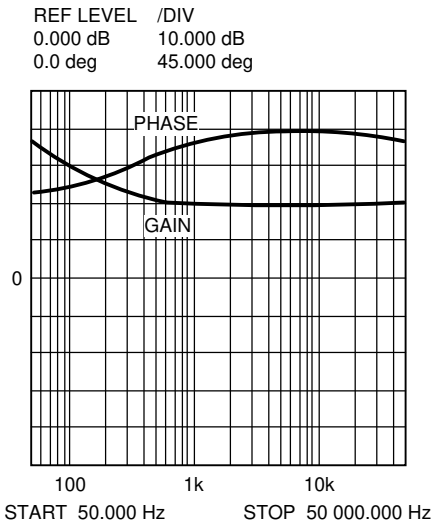


Figure 7-5. Error Amplifier Gain and Phase

The overall loop can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

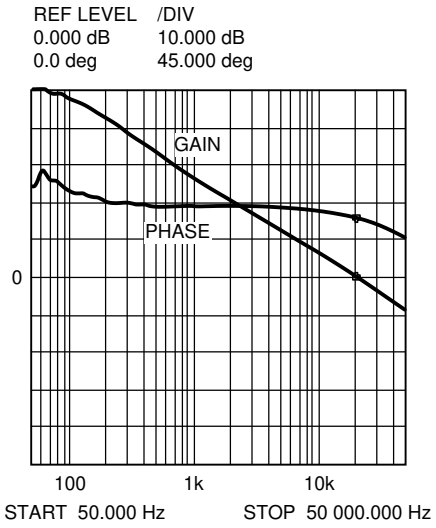


Figure 7-6. Overall Loop Gain and Phase

If a network analyzer is available, measure the modulator gain and configure the error amplifier gain for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given in this section. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. Add C6 to the compensation network to decrease noise susceptibility of the error amplifier. Provide that the value of C6 is sufficiently small as the addition of this capacitor adds a pole in the error amplifier transfer function. Establish that this pole is well beyond the loop crossover frequency. A good approximation of the location of the pole added by C6 is:

$$f_{p2} = fz \times C5/C6 \quad (18)$$

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7.3.3 Application Curves

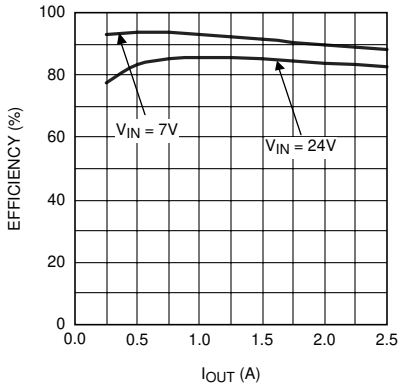


Figure 7-7. Demoboard Efficiency Vs Load Current

7.4 Power Supply Recommendations

The LM25005 converter is designed to operate from a wide input voltage range from 7V to 42V. Verify that the characteristics of the input supply are compatible with the Absolute Maximum Ratings and Recommended Operating Conditions. In addition, establish that the input supply is capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 19.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{19}$$

where

- η = efficiency

If the converter connects to an input supply through long wires or PCB traces with large impedance, special care is required to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can causes false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics.

The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range from 10µF to 47µF is typically sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, leads to instability, as well as some of the effects mentioned above. The AN-2162 Simple Success with Conducted EMI for DC-DC Converters application note provides helpful suggestions for designing an input filter for any switching regulator

7.5 Layout

7.5.1 Layout Guidelines

The circuit in the Section 6.2 serves as both a block diagram of the LM25005 and a typical application board schematic for the LM25005. In a buck regulator, there are two loops where currents switch very fast. The first loop starts from the input capacitors, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the regulator IS pins, to the diode anode, to the inductor and then out to the load. Minimizing the loop area of these two loops reduces the stray inductance and minimizes noise and possible erratic operation. A ground plane in the

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PC board is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through the topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane.

The two highest power dissipating components are the re-circulating diode and the LM25005 regulator IC. The easiest method to determine the power dissipated within the LM25005 is to measure the total conversion losses (Pin – Pout) then subtract the power losses in the Schottky diode, output inductor and snubber resistor. An approximation for the Schottky diode loss is

$$P_D = I_{OUT} \times V_{FWD} \tag{20}$$

An approximation for the output inductor power is

$$P = {I_{OUT}}^2 \times R \times 1.1 \tag{21}$$

- R = DC resistance of the inductor
- 1.1 factor = approximation for the AC losses

If using a snubber, estimate the power loss with an oscilloscope by observation of the resistor voltage drop at both turn-on and turn-off transitions. The regulator has an exposed thermal pad to aid power dissipation. Adding several vias under the device to the ground plane greatly reduces the regulator junction temperature. Selecting a diode with an exposed pad aids the power dissipation of the diode.

Table 7-2. 5V, 2.5A Demo Board Bill of Materials

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2µ, 100V
C	2	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2µ, 100V
C	3	C0805C331G1GAC	CAPACITOR, CER, KEMET	330p, 100V
C	4	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01µ, 100V
C	5	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01µ, 100V
C	6	OPEN	NOT USED	
C	7	C2012X7R2A223K	CAPACITOR, CER, TDK	0.022µ, 100V
C	8	C2012X7R1C474M	CAPACITOR, CER, TDK	0.47µ, 16V
C	9	C3225X7R1C226M	CAPACITOR, CER, TDK	22µ, 16V
C	10	EEFHE0J151R	CAPACITOR, SP, PANASONIC	150µ, 6.3V
C	11	C0805C331G1GAC	CAPACITOR, CER, KEMET	330p, 100V
C	12	OPEN	NOT USED	
D	1	CSHD6-60C	DIODE, 60V, CENTRAL	
		6CWQ10FN	DIODE, 100V, IR (D1-ALT)	
L	1	DR127-330	INDUCTOR, COOPER	33µH
R	1	OPEN	NOT USED	
R	2	OPEN	NOT USED	
R	3	CRCW08052102F	RESISTOR	21K
R	4	CRCW08054992F	RESISTOR	49.9K
R	5	CRCW08055111F	RESISTOR	5.11K
R	6	CRCW08051651F	RESISTOR	1.65K
R	7	CRCW2512100J	RESISTOR	10, 1W
U	1	LM25005	REGULATOR, TEXAS INSTRUMENTS	

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7.5.2 Layout Example

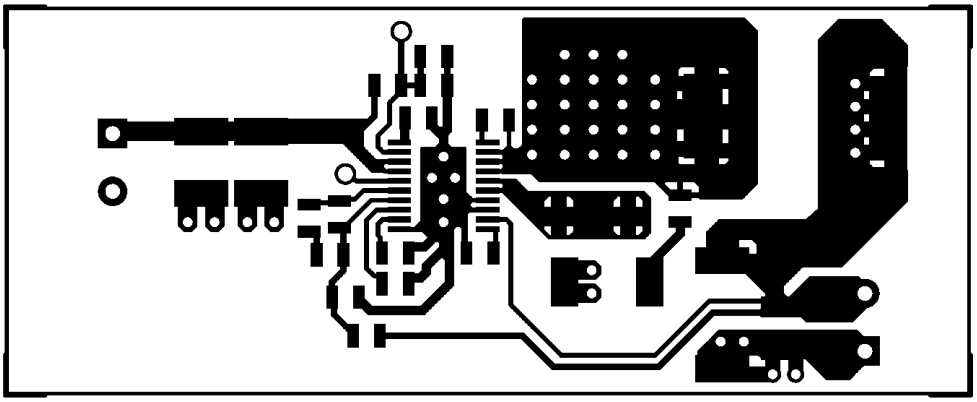


Figure 7-8. Component Side

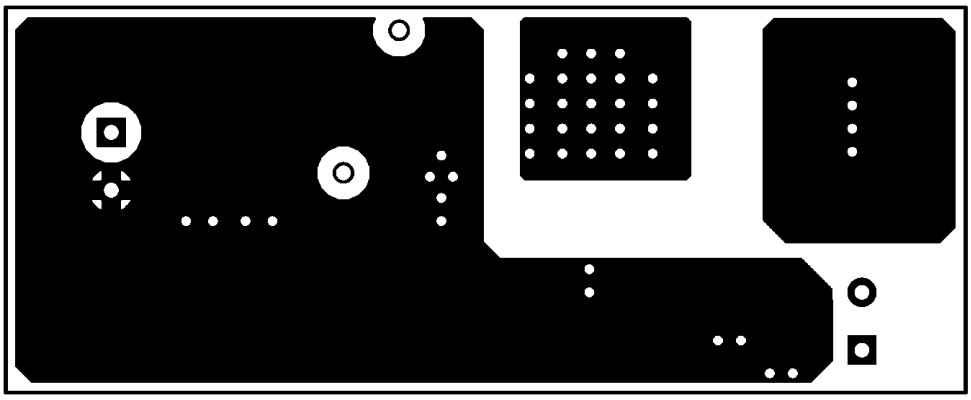


Figure 7-9. Solder Side

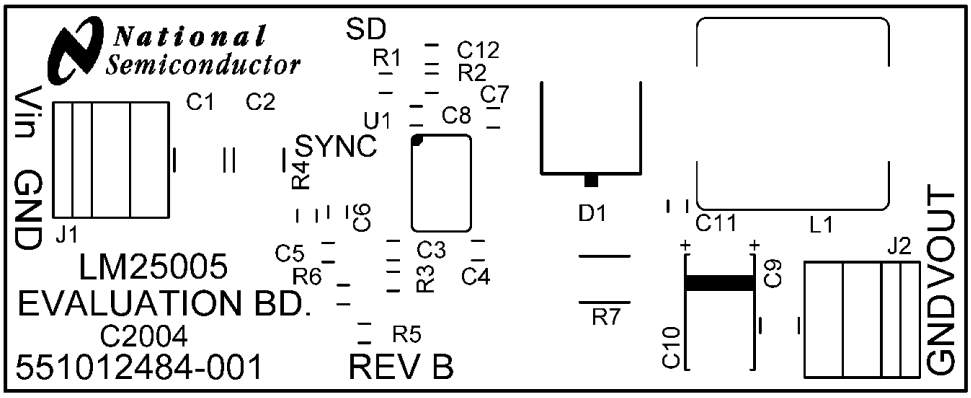


Figure 7-10. Silkscreen

7.5.3 Power Dissipation

The most significant variables that affect the power dissipated by the LM25005 are the output current, input voltage, and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The operating frequency of the LM25005 evaluation board has been designed for 300kHz.

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7.5.4 Thermal Design

As with any power conversion device, the LM25005 dissipates internal power while operating. The effect of the power dissipation is to raise the internal junction temperature of the LM25005 above ambient. The junction temperature (T_J) is a function of the ambient temperature (T_A), the power dissipation (P_D) and the effective thermal resistance of the device and PCB combination ($R_{\theta JA}$). The maximum operating junction temperature for the LM25005 is 125°C, thus establishing a limit on the maximum device power dissipation and therefore the load current at high ambient temperatures. Equation 22 and Equation 23 show the relationships between these parameters.

$$P_D = P_{OUT} \times \left[\frac{1-\eta}{\eta}\right] - V_F \times I_{OUT} \times \left[1 - D\right] - I^2_{OUT} \times R_{DCR} \times 1.5 \quad (22)$$

$$T_J = T_A + P_D \times \theta_{JA} \quad (23)$$

An approximation for the inductor power loss in Equation 22 includes a factor of 1.5 for the core losses. Also, if using a snubber, estimate the power loss by observation of the resistor voltage drop at both turnon and turnoff switching transitions.

High ambient temperatures and large values of $R_{\theta JA}$ reduce the maximum available output current. If the junction temperature exceeds 165°C, the LM25005 cycles in and out of thermal shutdown. Thermal shutdown can be a sign of inadequate heat-sinking or excessive power dissipation. Improve PCB heat-sinking by using more thermal vias, a larger board, or additional heat-spreading layers within that board.

As stated in the *Semiconductor and IC Package Thermal Metrics* application note, the values given in Thermal Information are not always valid for design purposes to estimate the thermal performance of the application.

The values reported Section 5.4 are measured under a specific set of conditions that are seldom obtained in an actual application. The effective $R_{\theta JA}$ is a critical parameter and depends on many factors, such as:

- Power dissipation
- Air temperature
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Air flow
- Adjacent component placement

The exposed pad of the LM25005 has a direct thermal connection to PGND. Verify that this pad is soldered directly to the PCB copper ground plane to provide an effective heat-sink and proper electrical connection. Use the documents listed in Section 8.2.1 as a guide for optimized thermal PCB design and estimating RθJA for a given application environment.

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.1.2 Development Support

For development support on this product, see the following:

8.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the **LM25005** device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *AN-2162 Simple Success with Conducted EMI for DC-DC Converters* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Export Control Notice

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8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added Applications section	1
• Moved Simplified Application Schematic to Description section	1
• Moved package information to Package Information table	1
• Changed section title from: Connection Diagram to: Pin Configuration and Functions	3
• Added ESD Ratings	5
• Changed from: Operating Ratings to: Recommended Operating Conditions	5
• Added Thermal Resistance Characteristics section	5
• Updated Bias Current (Iin) from: 3mA to: 2mA	6
• Updated typical shutdown current from: 50µA to: 48µA	6
• Changed BOOST UVLO Hysteresis from 0.56V to 0.8V	6
• Changed FB Bias Current from 17nA to 10nA	6
• Changed from: Typical Performance Characteristics to: Typical Characteristics	8
• Updated from: Detailed Operating Description to: Overview	10
• Moved Functional Block Diagram to Detailed Description section	11
• Added Application and Implementation section	18
• Added Application Information section	18
• Added Typical Application section	19
• Added Design Requirements section	19
• Added Detailed Design Procedure section	19
• Added Application Curves section	25
• Added Power Supply Recommendations section	25
• Changed from: PCB LAYOUT AND THERMAL CONSIDERATIONS to: Layout Guidelines	25
• Moved PCB Layout figures to Layout Example section	27

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Changes from Revision B (March 2013) to Revision C (March 2013)	Page
• Changed layout of National Data Sheet to TI format	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25005MH/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25005 MH
LM25005MH/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25005 MH
LM25005MH/NOPB.B	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25005 MH
LM25005MHX/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25005 MH
LM25005MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25005 MH
LM25005MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM25005 MH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

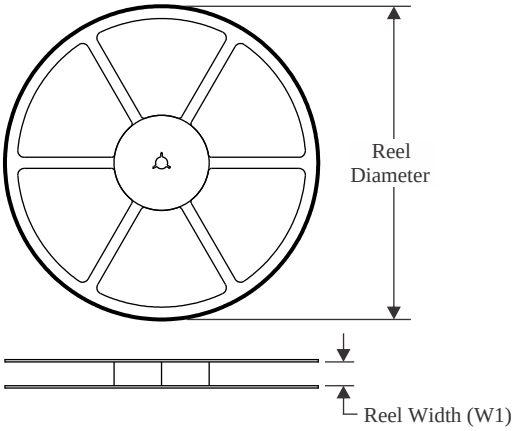
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

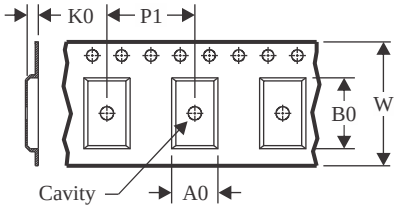
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

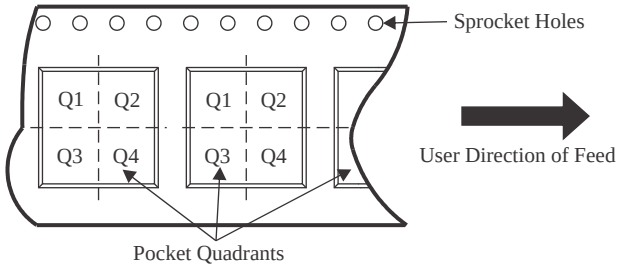


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

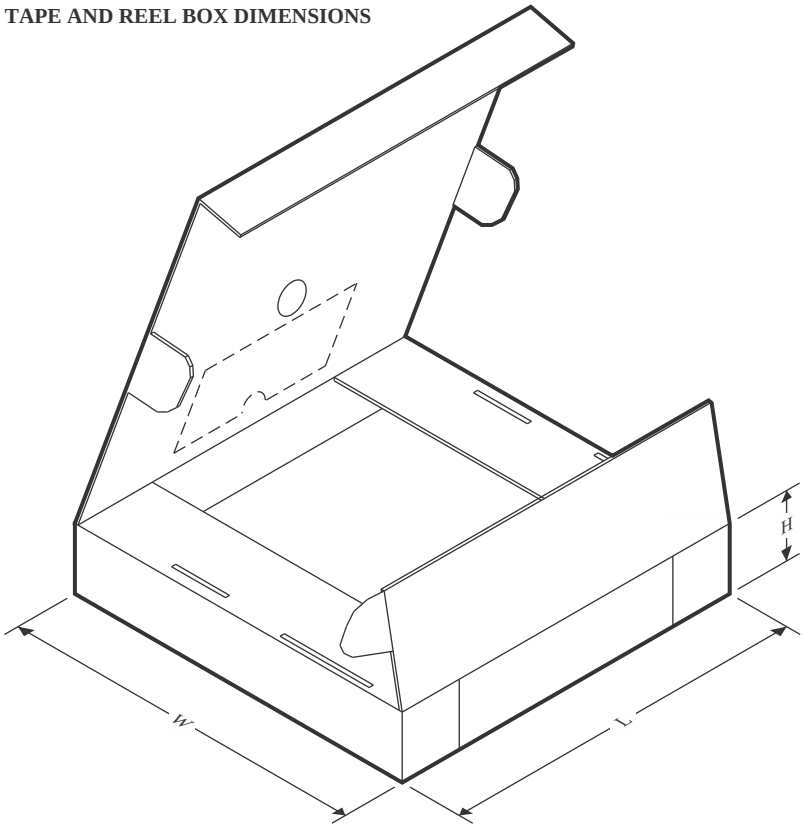
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25005MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

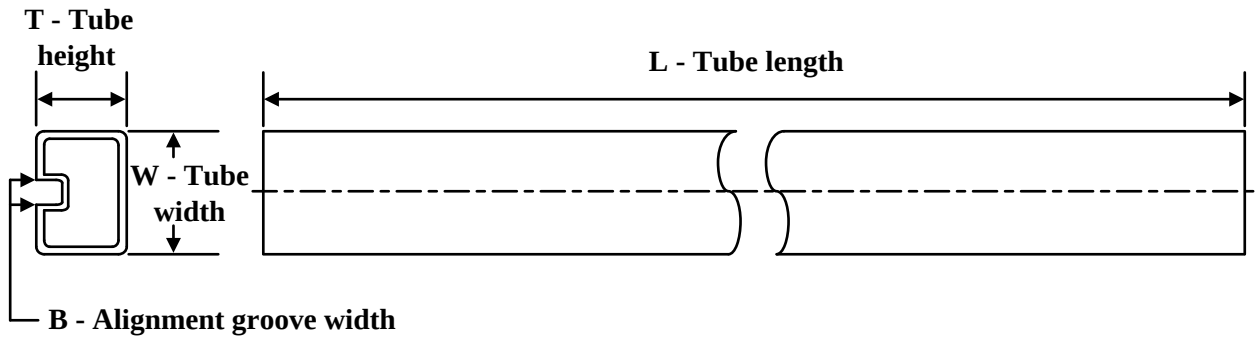
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

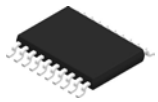
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25005MHX/NOPB	HTSSOP	PWP	20	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM25005MH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM25005MH/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM25005MH/NOPB.B	PWP	HTSSOP	20	73	495	8	2514.6	4.06

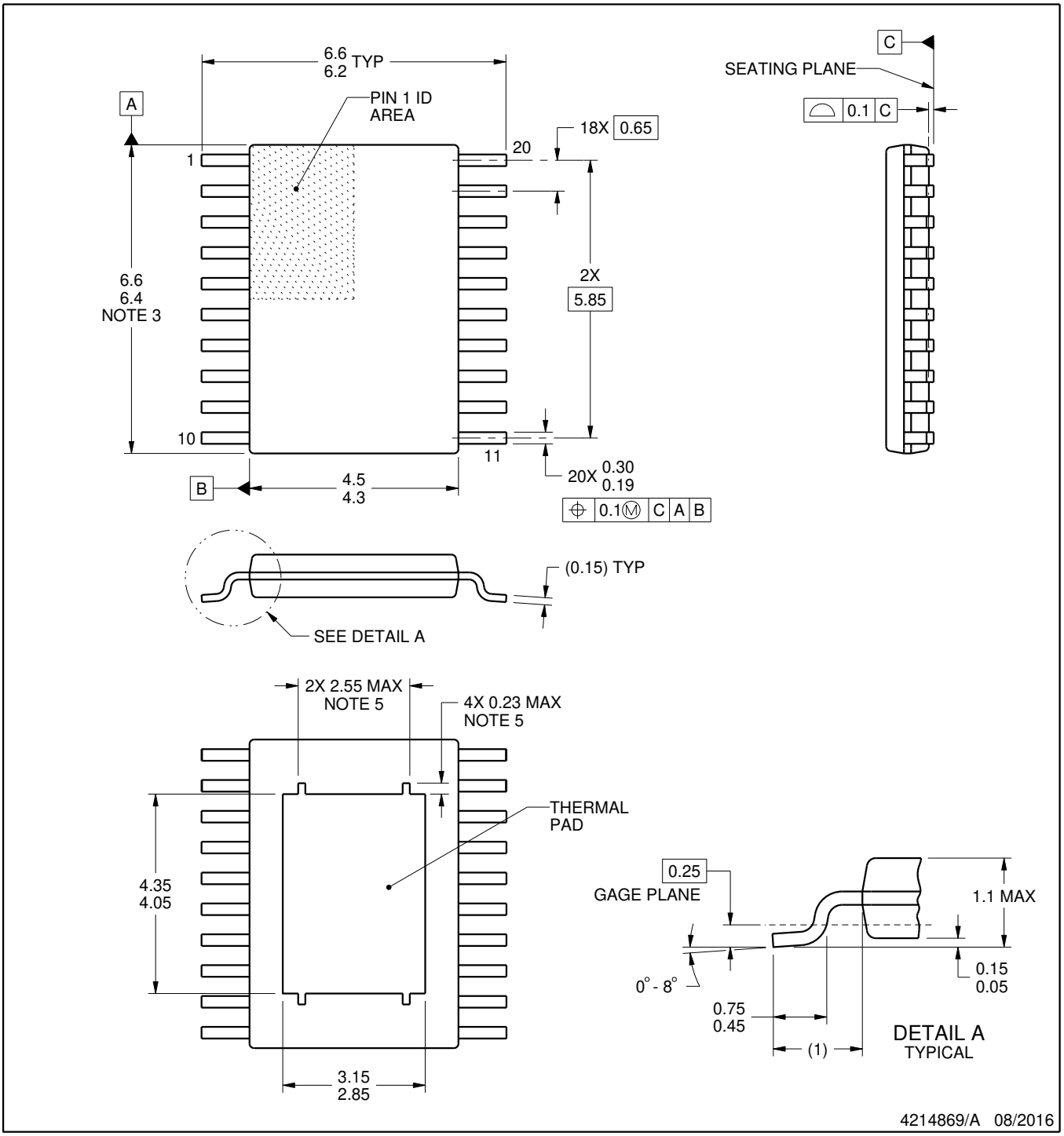


PACKAGE OUTLINE

PWP0020A

PowerPAD™ TSSOP - 1.1 mm max height

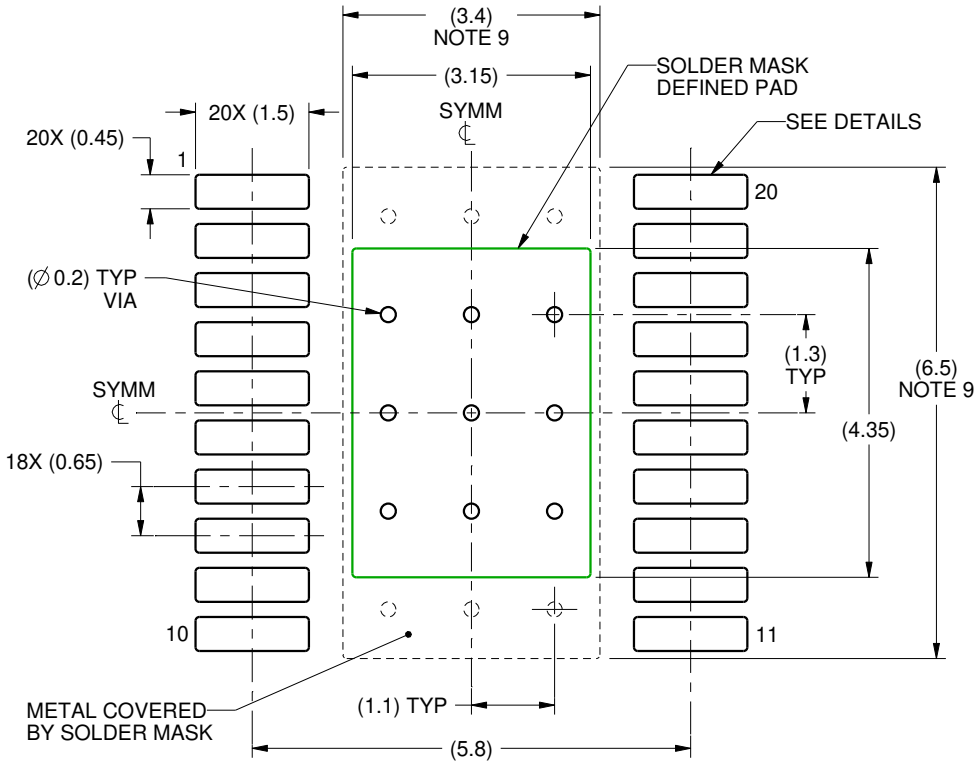
PLASTIC SMALL OUTLINE



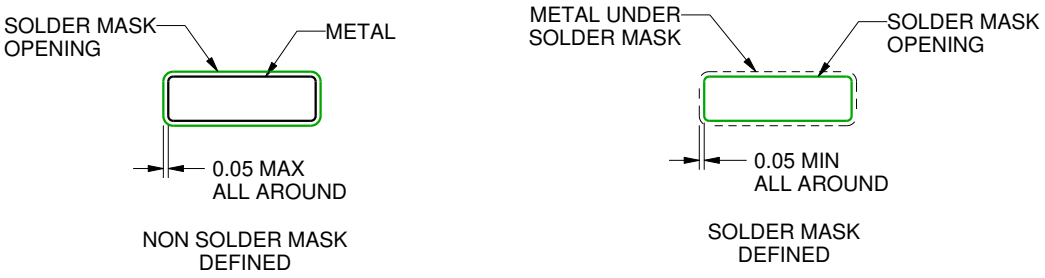
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

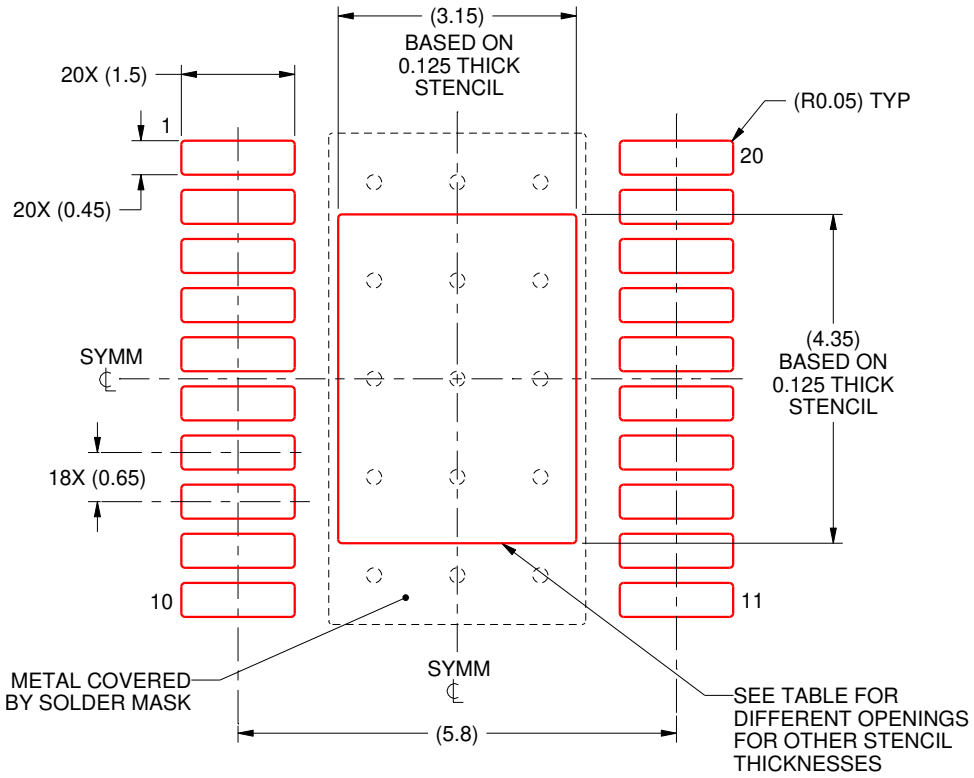


SOLDER MASK DETAILS
PADS 1-20

4214869/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.52 X 4.86
0.125	3.15 X 4.35 (SHOWN)
0.15	2.88 X 3.97
0.175	2.66 X 3.68

4214869/A 08/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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