LM2696 3A, Constant On Time Buck Regulator

Check for Samples: LM2696

FEATURES

- **Input Voltage Range of 4.5V–24V**
- **Constant On-Time**
- **No Compensation Needed**
- **Maximum Load Current of 3A**
- **Switching Frequency of 100 kHz–500 kHz**
- **Constant Frequency Across Input Range**
- **TTL Compatible Shutdown Thresholds**
- **Low Standby Current of 12 µA**
- **130 mΩ Internal MOSFET Switch**

APPLICATIONS

- **High Efficiency Step-Down Switching Regulators**
- **LCD Monitors**
- **Set-Top Boxes**

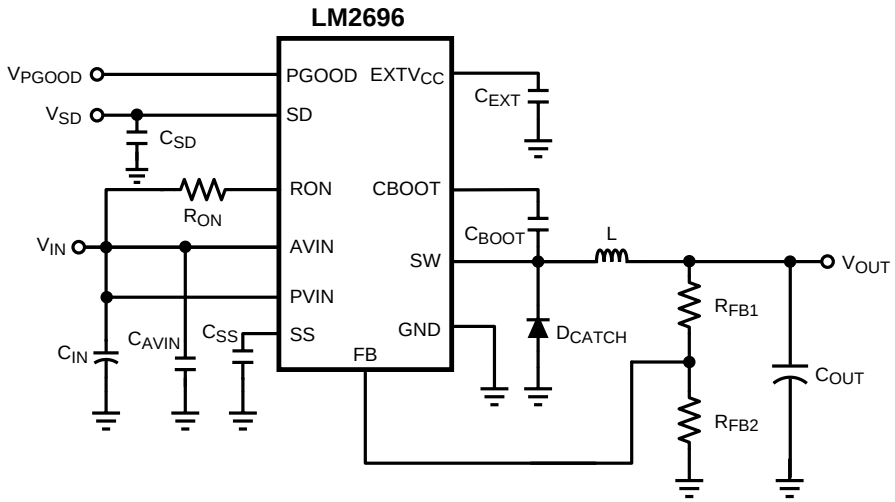
DESCRIPTION

The LM2696 is a pulse width modulation (PWM) buck regulator capable of delivering up to 3A into a load. The control loop utilizes a constant on-time control scheme with input voltage feed forward. This provides a topology that has excellent transient response without the need for compensation. The input voltage feed forward ensures that a constant switching frequency is maintained across the entire V_{IN} range.

The LM2696 is capable of switching frequencies in the range of 100 kHz to 500 kHz. Combined with an integrated 130 mΩ high side NMOS switch the LM2696 can utilize small sized external components and provide high efficiency. An internal soft-start and power-good flag are also provided to allow for simple sequencing between multiple regulators.

The LM2696 is available with an adjustable output in an exposed pad HTSSOP-16 package.

Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2005–2013, Texas Instruments Incorporated

Connection Diagram

Top View

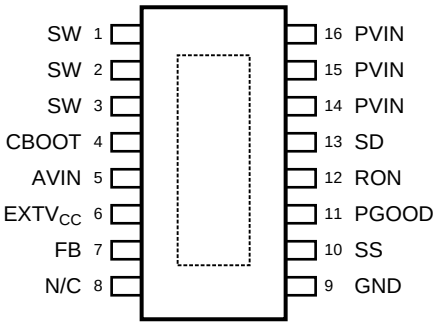


Figure 1. HTSSOP-16 Package
See Package Number PWP0016A

PIN DESCRIPTIONS

Pin #	Name	Function
1, 2, 3	SW	Switching node
4	CBOOT	Bootstrap capacitor input
5	AVIN	Analog voltage input
6	$EXTV_{CC}$	Output of internal regulator for decoupling
7	FB	Feedback signal from output
8	N/C	No connect
9	GND	Ground
10	SS	Soft-start pin
11	PGOOD	Power-good flag, open drain output
12	RON	Sets the switch on-time dependent on current
13	SD	Shutdown pin
14, 15, 16	PVIN	Power voltage input
-	Exposed Pad	Must be connected to ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2005–2013, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Voltages from the indicated pins to GND	
AVIN	−0.3V to +26V
PVIN	−0.3V to (AV_{IN}+0.3V)
CBOOT	−0.3V to +33V
CBOOT to SW	−0.3V to +7V
FB, SD, SS, PGOOD	−0.3V to +7V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Minimum ESD Rating	1.5 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Without PCB copper enhancements. The maximum power dissipation must be derated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), θ_{J-A} (junction to ambient thermal resistance) and T_A (ambient temperature). The maximum power dissipation at any temperature is: $P_{DissMAX} = (T_{JMAX} - T_A) / \theta_{J-A}$ up to the value listed in the Absolute Maximum Ratings. θ_{J-A} for HTSSOP-16 package is 38.1°C/W, T_{JMAX} = 125°C.

OPERATING RANGE

Junction Temperature	−40°C to +125°C
AVIN to GND	4.5V to 24V
PVIN	4.5V to 24V

ELECTRICAL CHARACTERISTICS

Specifications with standard typeface are for T_J = 25°C, and those in **boldface** type apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. Unless otherwise specified V_{IN} = 12V.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{FB}	Feedback Pin Voltage	V_{IN} = 4.5V to 24V I_{SW} = 0A to 3A	**1.225**	1.254	**1.282**	V
I_{CL}	Switch Current Limit	$V_{CBOOT} = V_{SW}$ + 5V	**3.6**	4.9	**6.4**	A
R_{DS_ON}	Switch On Resistance	I_{SW} = 3A		0.13	**0.22**	Ω
I_Q	Operating Quiescent Current	V_{FB} = 1.5V		1.3	**2**	mA
V_{UVLO}	AVIN Under Voltage Lockout	Rising V_{IN}	**3.9**	4.125	**4.3**	V
$V_{UVLO\ HYS}$	AVIN Under Voltage Lockout Hysteresis			60	**120**	mV
I_{SD}	Shutdown Quiescent Current	V_{SD} = 0V		12	**25**	µA
k_{ON}	Switch On-Time Constant	I_{ON} = 50 µA to 100 µA	**50**	66	**82**	µA µs
$V_{D\ ON}$	R_{ON} Voltage		**0.35**	0.65	**0.95**	V
T_{OFF_MIN}	Minimum Off Time	FB = 1.24V FB = 0V		165 12	**250** **30**	ns µs
$T_{ON\ MIN}$	Minimum On-time		**400**			ns
V_{EXTV}	$EXTV_{CC}$ Voltage		**3.30**	3.65	**4.00**	V
ΔV_{EXTV}	$EXTV_{CC}$ Load Regulation	I_{EXTV} = 0 µA to 50 µA		0.03	**0.5**	%
V_{PWRGD}	PGOOD Threshold (PGOOD Transition from Low to High)	With respect to V_{FB}	**91.5**	93.5	**95.5**	%
V_{PG_HYS}	PGOOD Hysteresis			1	**2.1**	%
I_{OL}	PGOOD Low Sink Current	V_{PGOOD} = 0.4V	**0.5**	2		mA
I_{OH}	PGOOD High Leakage Current			50		nA
I_{FB}	Feedback Pin Bias Current	V_{FB} = 1.2V		0		nA
I_{SS_SOURCE}	Soft-Start Pin Source Current	V_{SS} = 0V	**0.7**	1	**1.4**	µA

Copyright © 2005–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Specifications with standard typeface are for T_J = 25°C, and those in **boldface** type apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. Unless otherwise specified V_{IN} = 12V.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{SS\ SINK}$	Soft-Start Pin Sink Current	V_{SS} = 1.2V V_{SD} = 0V		15		mA
I_{SD}	Shutdown Pull-Up Current	V_{SD} = 0V		1	**3**	µA
V_{IH}	SD Pin Minimum High Input Level		**1.8**			V
V_{IL}	SD Pin Maximum Low Input Level				**0.6**	V
θ_{J-A}	Thermal Resistance			35.1		°C/W

Copyright © 2005–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS

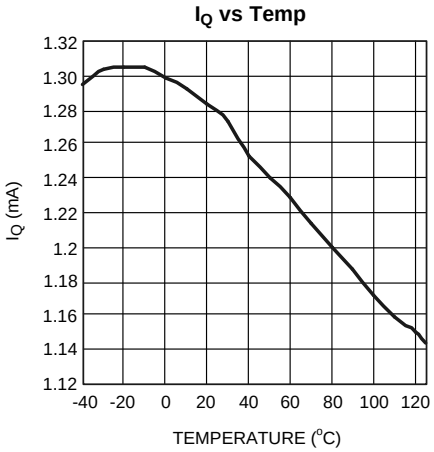


Figure 2.

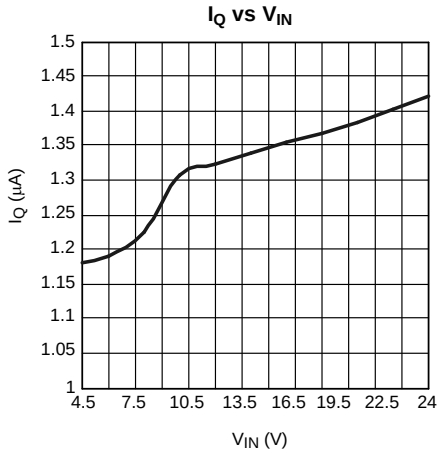


Figure 3.

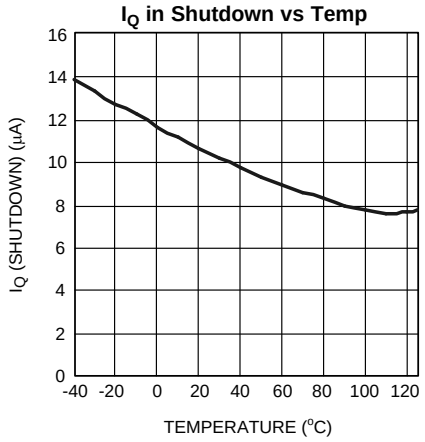


Figure 4.

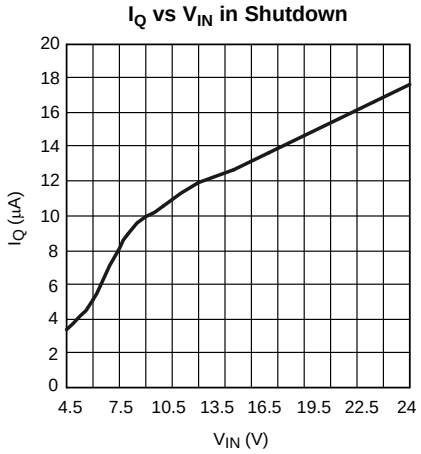


Figure 5.

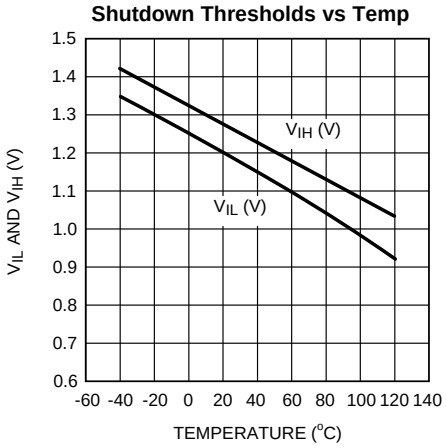


Figure 6.

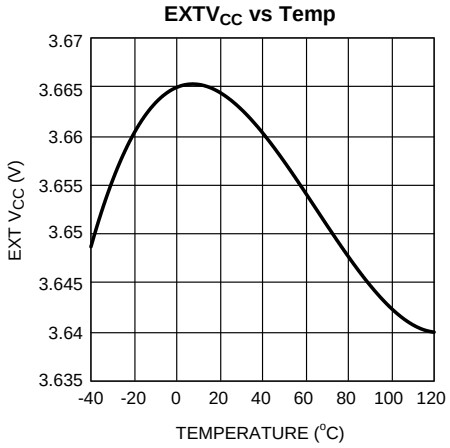


Figure 7.

Copyright © 2005–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$EXTV_{CC}$ vs V_{IN}

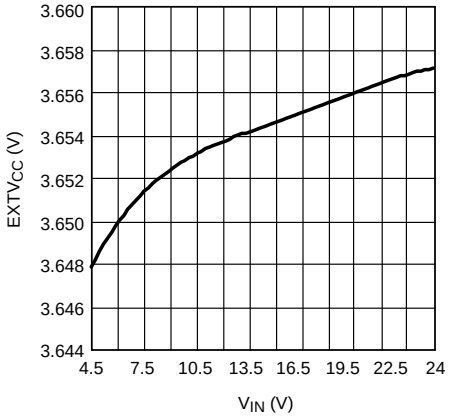


Figure 8.

$EXTV_{CC}$ vs Load Current

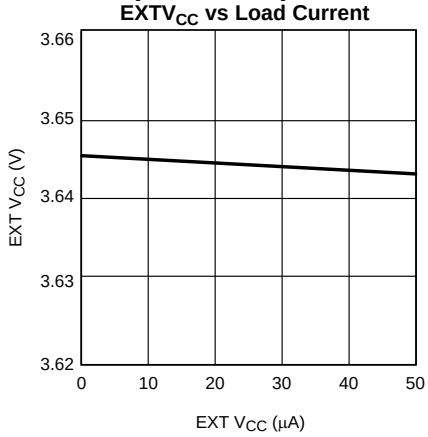


Figure 9.

Feedback Threshold Voltage vs Temp

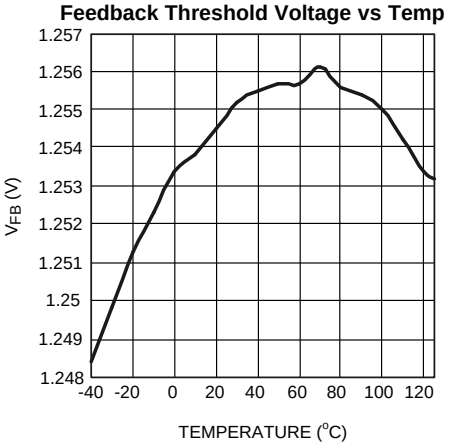


Figure 10.

k_{ON} vs Temp

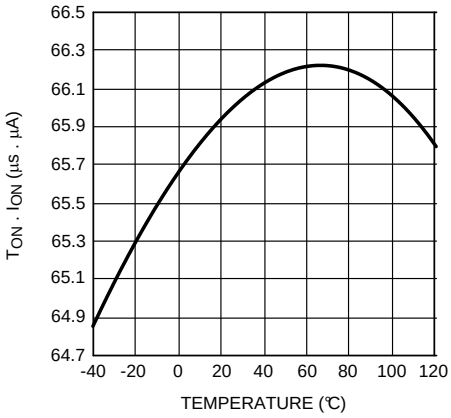


Figure 11.

Switch ON Time vs R_{ON} Pin Current

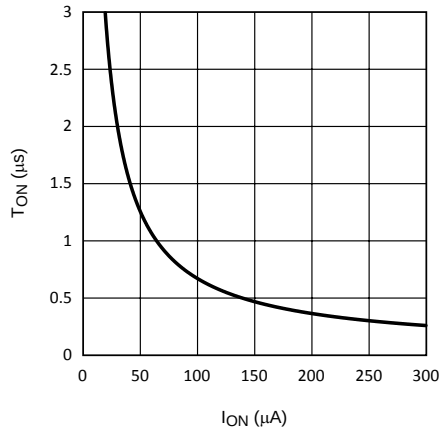


Figure 12.

Min Off-Time vs Temp

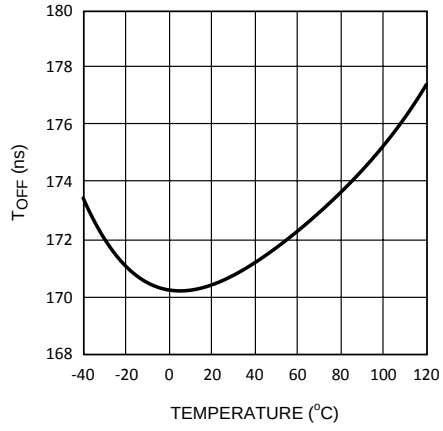


Figure 13.

Copyright © 2005–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Max and Min Duty-Cycle vs Freq
(Min T_{ON} = 400 ns, Min T_{OFF} = 200 ns)

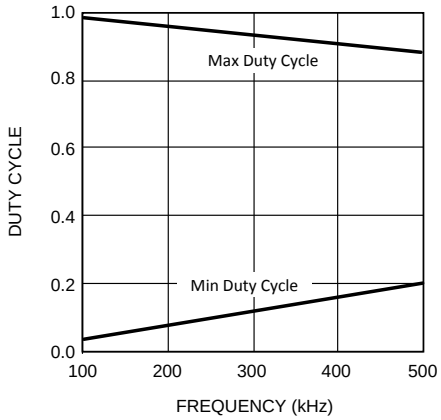


Figure 14.

FET Resistance vs Temp

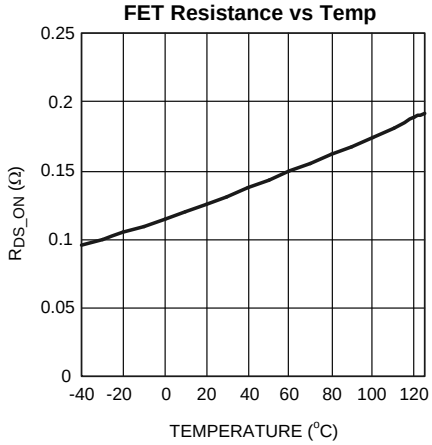


Figure 15.

R_{ON} Pin Voltage vs Temp

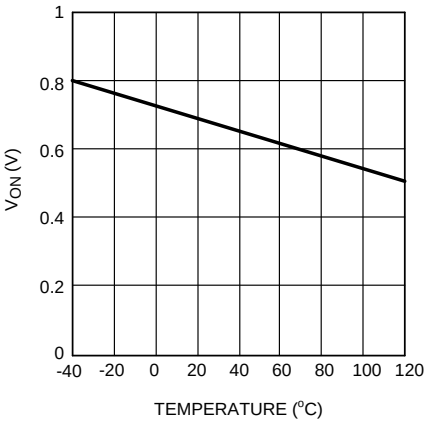


Figure 16.

Current Limit vs Temp

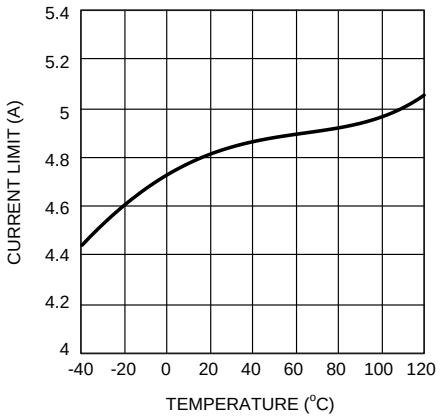
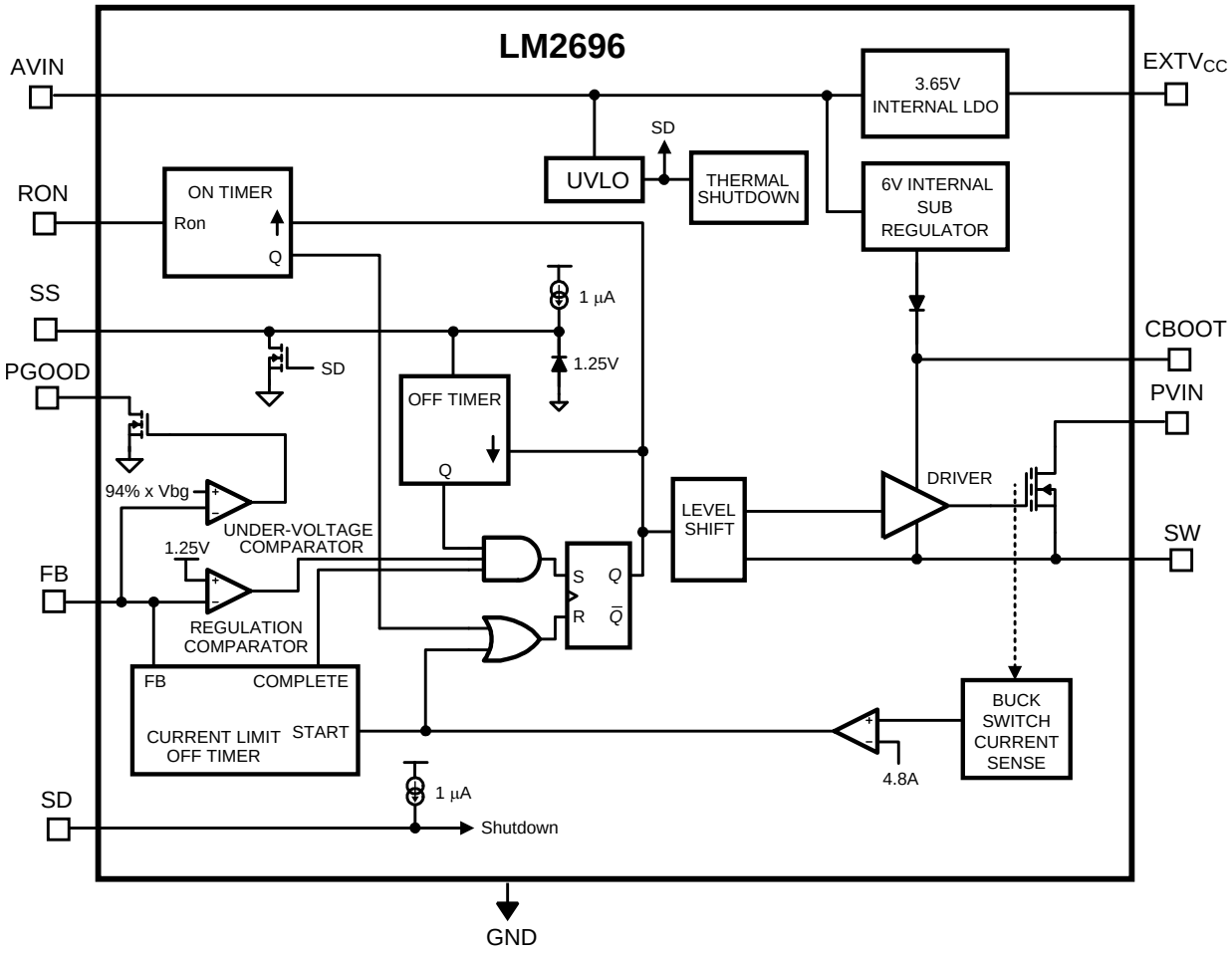


Figure 17.

Copyright © 2005–2013, Texas Instruments Incorporated

BLOCK DIAGRAM



APPLICATION INFORMATION

CONSTANT ON-TIME CONTROL OVERVIEW

The LM2696 buck DC-DC regulator is based on the constant on-time control scheme. This topology relies on a fixed switch on-time to regulate the output. The on-time can be set manually by adjusting the size of an external resistor (R_{ON}). The LM2696 automatically adjusts the on-time inversely with the input voltage (AV_{IN}) to maintain a constant frequency. In continuous conduction mode (CCM) the frequency depends only on duty cycle and on-time. This is in contrast to hysteretic regulators where the switching frequency is determined by the output inductor and capacitor. In discontinuous conduction mode (DCM), experienced at light loads, the frequency will vary according to the load. This leads to high efficiency and excellent transient response.

The on-time will remain constant for a given V_{IN} unless an over-current or over-voltage event is encountered. If these conditions are encountered the FET will turn off for a minimum pre-determined time period. This minimum T_{OFF} (250 ns) is internally set and cannot be adjusted. After the T_{OFF} period has expired the FET will remain off until the comparator trip-point has been reached. Upon passing this trip-point the FET will turn back on, and the process will repeat.

Switchers that regulate using an internal comparator to sense the output voltage for switching decisions, such as hysteretic or constant on-time, require a minimum ESR. A minimum ESR is required so that the control signal will be dominated by ripple that is in phase with the switchpin. Using a control signal dominated by voltage ripple that is in phase with the switchpin eliminates the need for compensation, thus reducing parts count and simplifying design. Alternatively, an RC feed forward scheme may be used to eliminate the need for a minimum ESR.

Copyright © 2005–2013, Texas Instruments Incorporated

INTERNAL OPERATION UNDER-VOLTAGE COMPARATOR

An internal comparator is used to monitor the feedback pin for sensing under-voltage output events. If the output voltage drops below the UVP threshold the power-good flag will fall.

ON-TIME GENERATOR SHUTDOWN

The on-time for the LM2696 is inversely proportional to the input voltage. This scheme of on-time control maintains a constant frequency over the input voltage range. The on-time can be adjusted by using an external resistor connected between the PVIN and RON pins.

CURRENT LIMIT

The LM2696 contains an intelligent current limit off-timer. If the peak current in the internal FET exceeds 4.9A the present on-time is terminated; this is a cycle-by-cycle current limit. Following the termination of the on-time, a non-resetable extended off timer is initiated. The length of the off-time is proportional to the feedback voltage. When FB = 0V the off-time is preset to 20 µs. This condition is often a result of in short circuit operation when a maximum amount of off-time is required. This amount of time ensures safe short circuit operation up to the maximum input voltage of 24V.

In cases of overload (not complete short circuit, FB > 0V) the current limit off-time is reduced. Reduction of the off-time during smaller overloads reduces the amount of fold back. This also reduces the initial startup time.

N-CHANNEL HIGH SIDE SWITCH AND DRIVER

The LM2696 utilizes an integrated N-Channel high side switch and associated floating high voltage gate driver. This gate driver circuit works in conjunction with an external bootstrap capacitor and an internal diode. The minimum off-time (165 ns) is set to ensure that the bootstrap capacitor has sufficient time to charge.

THERMAL SHUTDOWN

An internal thermal sensor is incorporated to monitor the die temperature. If the die temp exceeds 165ºC then the sensor will trip causing the part to stop switching. Soft-start will restart after the temperature falls below 155ºC.

COMPONENT SELECTION

As with any DC-DC converter, numerous trade-offs are present that allow the designer to optimize a design for efficiency, size and performance. These trade-offs are taken into consideration throughout this section.

The first calculation for any buck converter is duty cycle. Ignoring voltage drops associated with parasitic resistances and non-ideal components, the duty cycle may be expressed as:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

A duty cycle relationship that considers the voltage drop across the internal FET and voltage drop across the external catch diode may be expressed as:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{2}$$

Where

- V_D is the forward voltage of the external catch diode (D_{CATCH})
- V_{SW} is the voltage drop across the internal FET.

FREQUENCY SELECTION

Switching frequency affects the selection of the output inductor, capacitor, and overall efficiency. The trade-offs in frequency selection may be summarized as; higher switching frequencies permit use of smaller inductors possibly saving board space at the trade-off of lower efficiency. It is recommended that a nominal frequency of 300 kHz should be used in the initial stages of design and iterated if necessary.

Copyright © 2005–2013, Texas Instruments Incorporated

The switching frequency of the LM2696 is set by the resistor connected to the RON pin. This resistor controls the current flowing into the RON pin and is directly related to the on-time pulse. Connecting a resistor from this pin to PVIN allows the switching frequency to remain constant as the input voltage changes. In normal operation this pin is approximately 0.65V above GND. In shutdown, this pin becomes a high impedance node to prevent current flow.

The ON time may be expressed as:

$$T_{ON} = \frac{k_{ON} \cdot R_{ON}}{V_{IN} - V_D} 10^{-3} \ \mu s \tag{3}$$

where

- V_{IN} is the voltage at the high side of the R_{ON} resistor (typically PV_{IN})
- V_D is the diode voltage present at the RON pin (0.65V typical)
- R_{ON} is in kΩ
- k_{ON} is a constant value set internally (66 µA•µs nominal).

This equation can be re-arranged such that R_{ON} is a function of switching frequency:

$$R_{ON} = \frac{(V_{IN} - V_D) \cdot D}{k_{ON} \cdot f_{SW}} 10^{6} k\Omega \tag{4}$$

where

- f_{SW} is in kHz.

In CCM the frequency may be determined using the relationship:

$$f_{SW} = \frac{D}{T_{ON}} 10^{3} \text{ kHz} \tag{5}$$

(T_{ON} is in µs)

Which is typically used to set the switching frequency.

Under no condition should a bypass capacitor be connected to the R_{ON} pin. Doing so couples any AC perturbations into the pin and prevents proper operation.

INDUCTOR SELECTION

Selecting an inductor is a process that may require several iterations. The reason for this is that the size of the inductor influences the amount of ripple present at the output that is critical to the stability of an adaptive on-time circuit. Typically, an inductor is selected such that the maximum peak-to-peak ripple current is equal to 30% of the maximum load current. The inductor current ripple (ΔI_L) may be expressed as:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \cdot D}{L \cdot f_{SW}} \tag{6}$$

Therefore, L can be initially set to the following by applying the 30% guideline:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot D}{0.3 \cdot f_{SW} \cdot I_{OUT}} \tag{7}$$

The other features of the inductor that should be taken into account are saturation current and core material. A shielded inductor or low profile unshielded inductor is recommended to reduce EMI.

OUTPUT CAPACITOR

The output capacitor size and ESR have a direct affect on the stability of the loop. This is because the adaptive on-time control scheme works by sensing the output voltage ripple and switching appropriately. The output voltage ripple on a buck converter can be approximated by assuming that the AC inductor ripple current flows entirely into the output capacitor and the ESR of the capacitor creates the voltage ripple. This is expressed as:

$$\Delta V_{OUT} \approx \Delta I_L \cdot R_{ESR} \tag{8}$$

Copyright © 2005–2013, Texas Instruments Incorporated

To ensure stability, two constraints need to be met. These constraints are the voltage ripple at the feedback pin must be greater than some minimum value and the voltage ripple must be in phase with the switch pin.

The ripple voltage necessary at the feedback pin may be estimated using the following relationship:

$$\Delta V_{FB} > -0.057 \bullet f_{SW} + 35$$

where

- f_{SW} is in kHz
- ΔV_{FB} is in mV. (9)

This minimum ripple voltage is necessary in order for the comparator to initiate switching. The voltage ripple at the feedback pin must be in-phase with the switch. Because the ripple due to the capacitor charging and capacitor ESR are out of phase, the ripple due to capacitor ESR must dominate.

The ripple at the output may be calculated by multiplying the feedback ripple voltage by the gain seen through the feedback resistors. This gain H may be expressed as:

$$H = \frac{V_{OUT}}{V_{FB}} = \frac{V_{OUT}}{1.25V} \quad (10)$$

To simplify design and eliminate the need for high ESR output capacitors, an RC network may be used to feed forward a signal from the switchpin to the feedback (FB) pin. See the 'RIPPLE FEED FORWARD' section for more details.

Typically, the best performance is obtained using POSCAPs, SP CAPs, tantalum, Niobium Oxide, or similar chemistry type capacitors. Low ESR ceramic capacitors may be used in conjunction with the RC feed forward scheme; however, the feed forward voltage at the feedback pin must be greater than 30 mV.

RIPPLE FEED FORWARD

An RC network may be used to eliminate the need for high ESR capacitors. Such a network is connected as shown in Figure 18.

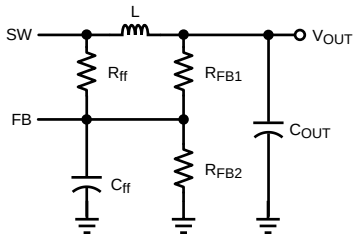


Figure 18. RC Feed Forward Network

The value of R_{ff} should be large in order to prevent any potential offset in V_{OUT}. Typically the value of R_{ff} is on the order of 1 MΩ and the value of R_{FB1} should be less than 10 kΩ. The large difference in resistor values minimizes output voltage offset errors in DCM. The value of the capacitor may be selected using the following relationship:

$$C_{ff_MAX} = \frac{(V_{IN_MIN} - V_{FB}) \times T_{ON_MIN}}{0.03V \times R_{ff}} \text{ pF}$$

where

- on-time (T_{ON_MIN}) is in µs
- resistance (R_{ff}) is in MΩ. (11)

FEEDBACK RESISTORS

The feedback resistors are used to scale the output voltage to the internal reference value such that the loop can be regulated. The feedback resistors should not be made arbitrarily large as this creates a high impedance node at the feedback pin that is more susceptible to noise. Typically, R_{FB2} is on the order of 1 kΩ. To calculate the value of R_{FB1}, one may use the relationship:

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (12)$$

Where

- V_{FB} is the internal reference voltage that can be found in the ELECTRICAL CHARACTERISTICS table (1.254V typical).

The output voltage value can be set in a precise manner by taking into account the fact that the reference voltage is regulating the bottom of the output ripple as opposed to the average value. This relationship is shown in Figure 19.

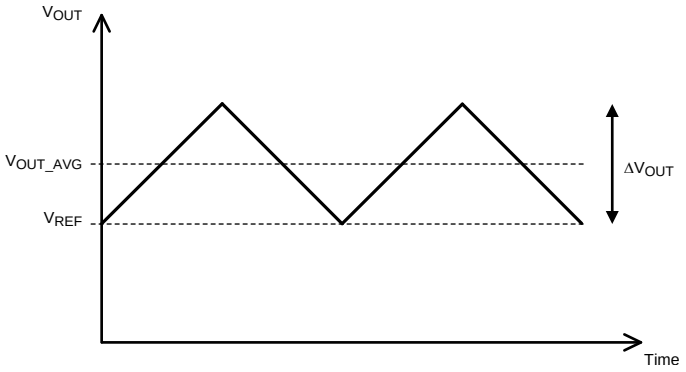


Figure 19. Average and Ripple Output Voltages

It can be seen that the average output voltage is higher than the gained up reference by exactly half the output voltage ripple. The output voltage may then be appended according to the voltage ripple. The appended V_{OUT} term may be expressed using the relationship:

$$V_{OUT} = V_{OUT_AVG} - \frac{1}{2} \Delta V_{OUT} = V_{OUT_AVG} - \frac{1}{2} \Delta I_L \bullet R_{ESR} \quad (13)$$

One should note that for high output voltages (>5V), a load of approximately 15 mA may be required for the output voltage to reach the desired value.

INPUT CAPACITOR

Because PV_{IN} is the power rail from which the output voltage is derived, the input capacitor is typically selected according to the load current. In general, package size and ESR determine the current capacity of a capacitor. If these criteria are met, there should be enough capacitance to prevent impedance interactions with the source. In general, it is recommended to use a low ESR, high capacitance electrolytic and ceramic capacitor in parallel. Using two capacitors in parallel ensures adequate capacitance and low ESR over the operating range. The Sanyo MV-WX series electrolytic capacitors and a ceramic capacitor with X5R or X7R dielectric are an excellent combination. To calculate the input capacitor RMS, one may use the following relationship:

$$I_{CIN_RMS} = I_{OUT} \sqrt{D \left(1 - D + \frac{\Delta I_L^2}{12 \bullet I_{OUT}^2} \right)} \quad (14)$$

that can be approximated by,

$$I_{CIN_RMS} = I_{OUT} \sqrt{D(1 - D)} \quad (15)$$

Typical values are 470 µF for the electrolytic capacitor and 0.1 µF for the ceramic capacitor.

Copyright © 2005–2013, Texas Instruments Incorporated

AV_{IN} CAPACITOR

AV_{IN} is the analog bias rail of the device. It should be bypassed externally with a small (1 µF) ceramic capacitor to prevent unwanted noise from entering the device. In a shutdown state the current needed by AV_{IN} will drop to approximately 12 µA, providing a low power sleep state.

In most cases of operation, AV_{IN} is connected to PV_{IN}; however, it is possible to have split rail operation where AV_{IN} is at a higher voltage than PV_{IN}. AV_{IN} should never be lower than PV_{IN}. Splitting the rails allows the power conversion to occur from a lower rail than the AV_{IN} operating range.

SOFT-START CAPACITOR

The SS capacitor is used to slowly ramp the reference from 0V to its final value of 1.25V (during shutdown this pin will be discharged to 0V). This controlled startup ability eliminates large in-rush currents in an attempt to charge up the output capacitor. By changing the value of this capacitor, the duration of the startup may be changed accordingly. The startup time may be calculated using the following relationship:

$$t_{SS} = \frac{1.25V \bullet C_{SS}}{I_{SS}} \quad (16)$$

Where

- I_{SS} is the soft-start pin source current (1 µA typical) that may be found in the ELECTRICAL CHARACTERISTICS table.

While the C_{SS} capacitor can be sized to meet the startup requirements, there are limitations to its size. If the capacitor is too small, the soft-start will have little effect as the reference voltage is rising faster than the output capacitor can be charged causing the part to go into current limit. Therefore a minimum soft-start time should be taken into account. This can be determined by:

$$t_{SS_MIN} = \frac{C_{OUT} V_{OUT}}{3A} \quad (17)$$

While C_{OUT} and V_{OUT} control the slew rate of the output voltage, the total amount of time the LM2696 takes to startup is dependent on two other terms. See the " Startup" section for more information.

$EXTV_{CC}$ CAPACITOR

External V_{CC} is a 3.65V rail generated by an internal sub-regulator that powers the parts internal circuitry. This rail should be bypassed with a 1 µF ceramic capacitor (X5R or equivalent dielectric). Although $EXTV_{CC}$ is for internal use, it can be used as an external rail for extremely light loads (<50 µA). If $EXTV_{CC}$ is accidentally shorted to GND the part is protected by a 5 mA current limit. This rail also has an under-voltage lockout that will prevent the part from switching if the $EXTV_{CC}$ voltage drops.

SHUTDOWN

The state of the shutdown pin enables the device or places it in a sleep state. This pin has an internal pull-up and may be left floating or connected to a high logic level. Connecting this pin to GND will shutdown the part. Shutting down the part will prevent the part from switching and reduce the quiescent current drawn by the part. This pin must be bypassed with a 1 nF ceramic capacitor (X5R or Y5V) to ensure proper logic thresholds.

CBOOT CAPACITOR

The purpose of an external bootstrap capacitor is to turn the FET on by using the SW node as a pedestal. This allows the voltage on the CBOOT pin to be greater than V_{IN}. Whenever the catch diode is conducting and the SW node is at GND, an internal diode will conduct that charges the CBOOT capacitor to approximately 4V. When the SW node rises, the CBOOT pin will rise to approximately 4V above the SW node. For optimal performance, a 0.1 µF ceramic capacitor (X5R or equivalent dielectric) should be used.

Copyright © 2005–2013, Texas Instruments Incorporated

PGOOD RESISTOR

The PGOOD resistor is used to pull the PGOOD pin high whenever a steady state operating range is achieved. This resistor needs to be sized to prevent excessive current from flowing into the PGOOD pin whenever the open drain FET is turned on. The recommendation is to use a 10 kΩ–100 kΩ resistor. This range of values is a compromise between rise time and power dissipation.

CATCH DIODE

The catch or freewheeling diode acts as the bottom switch in a non-synchronous buck switcher. Because of this, the diode has to handle the full output current whenever the FET is not conducting. Therefore, it must be sized appropriately to handle the current. The average current through the diode can be calculated by the equation:

$$I_{D_AVG} = I_{OUT} \bullet (1–D) \quad (18)$$

Care should also be taken to ensure that the reverse voltage rating of the diode is adequate. Whenever the FET is conducting the voltage across the diode will be approximately equal to V_{IN}. It is recommended to have a reverse rating that is equal to 120% of V_{IN} to ensure adequate guard banding against any ringing that could occur on the switch node.

Selection of the catch diode is critical to overall switcher performance. To obtain the optimal performance, a Schottky diode should be used due to their low forward voltage drop and fast recovery.

BYPASS CAPACITOR

A bypass capacitor must be used on the AV_{IN} line to help decouple any noise that could interfere with the analog circuitry. Typically, a small (1 µF) ceramic capacitor is placed as close as possible to the AVIN pin.

EXTERNAL OPERATION STARTUP

The total startup time, from the initial V_{IN} rise to the time V_{OUT} reaches its nominal value is determined by three separate steps. Upon the rise of V_{IN}, the first step to occur is that the $EXTV_{CC}$ voltage has to reach its nominal output voltage of 3.65V before the internal circuitry is active. This time is dictated by the output capacitance (1 µF) and the current limit of the regulator (5 mA typical), which will always be on the order of 730 µs. Upon reaching its steady state value, an internal delay of 200 µs will occur to ensure stable operation. Upon completion the LM2696 will begin switching and the output will rise. The rise time of the output will be governed by the soft-start capacitor. To highlight these three steps a timing diagram please refer to Figure 20.

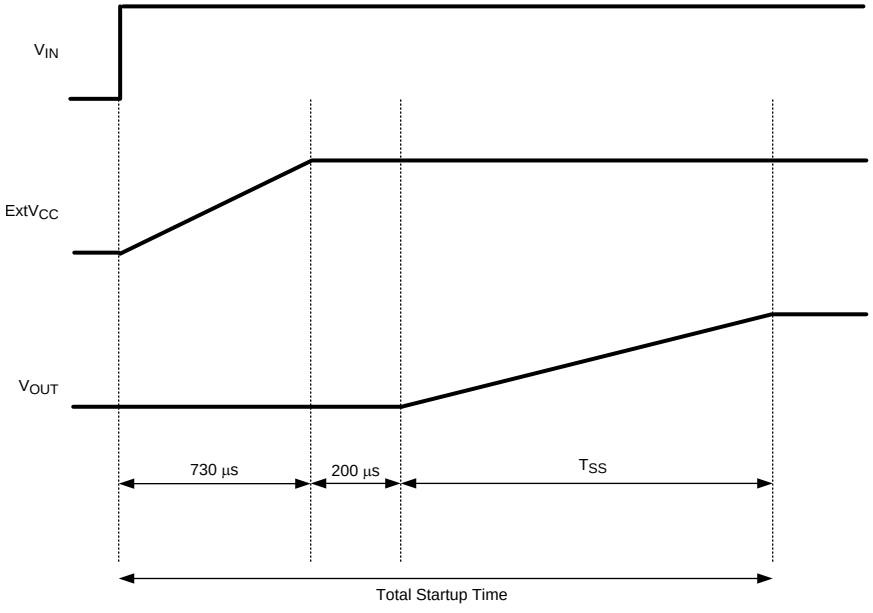


Figure 20. Startup Timing Diagram

Copyright © 2005–2013, Texas Instruments Incorporated

UNDER- & OVER-VOLTAGE CONDITIONS

The LM2696 has a built in under-voltage comparator that controls PGOOD. Whenever the output voltage drops below the set threshold, the PGOOD open drain FET will turn on pulling the pin to ground. For an over-voltage event, there is no separate comparator to control PGOOD. However, the loop responds to prevent this event from occurring because the error comparator is essentially sensing an OVP event. If the output is above the feedback threshold then the part will not switch back on; therefore, the worst-case condition is one on-time pulse.

CURRENT LIMIT

The LM2696 utilizes a peak-detect current limit that senses the current through the FET when conducting and will immediately terminate the on-pulse whenever the peak current exceeds the threshold (4.9A typical). In addition to terminating the present on-pulse, it enforces a mandatory off-time that is related to the feedback voltage.

If current limit trips and the feedback voltage is close to its nominal value of 1.25V, the off-time imposed will be relatively short. This is to prevent the output from dropping or any fold back from occurring if a momentary short occurred because of a transient or load glitch. If a short circuit were present, the off-time would extend to approximately 12 µs. This ensures that the inductor current will reach a low value (approximately 0A) before the next switching cycle occurs. The extended off-time prevents runaway conditions caused by hard shorts and high side blanking times.

If the part is in an over current condition, the output voltage will begin to drop as shown in Figure 21. If the output voltage is dropping and the current is below the current limit threshold, (I_1), the part will assert a pulse (t_2) after a minimum off-time (t_1). This is in an attempt to raise the output voltage.

If the part is in an over current condition and the output voltage is below the regulation value (V_L) as shown in Figure 21, the part will assert a pulse of minimal width (t_4) and extend the off-time (t_5). In the event that the voltage is below the regulation value (V_L) and the current is below the current limit value, the part will assert two (or more) pulses separated by some minimal off-time (t_1).

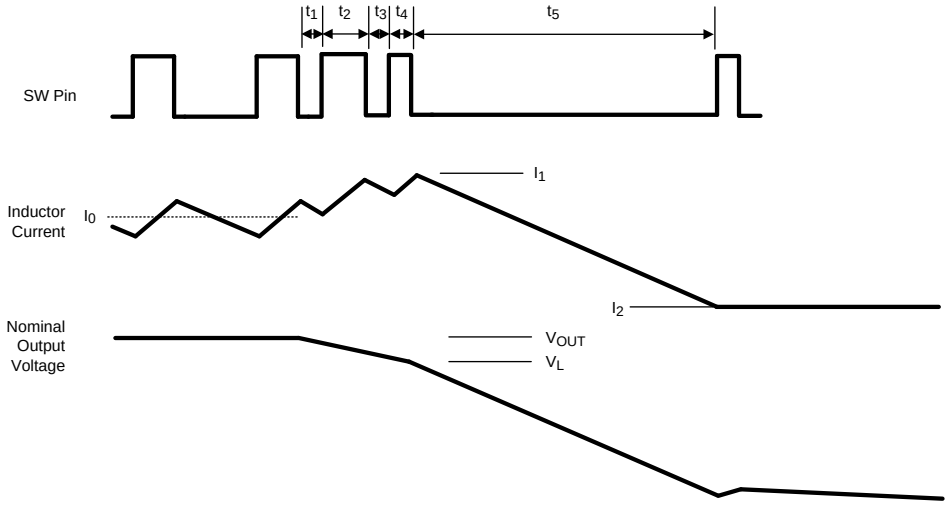


Figure 21. Fault Condition Timing

Legend:

t_1: Min off-time (165 ns typical)

t_2: On-time (set by the user)

t_3: Min off-time (165 ns typical)

t_4: Blanking time (165 ns typical)

t_5: Extended off-time (12 µs typical)

V_L: UVP threshold

Copyright © 2005–2013, Texas Instruments Incorporated

The last benefit of this scheme is when the short circuit is removed, and full load is re-applied, the part will automatically recover into the load. The variation in the off-time removes the constraints of other frequency fold back systems where the load would typically have to be reduced.

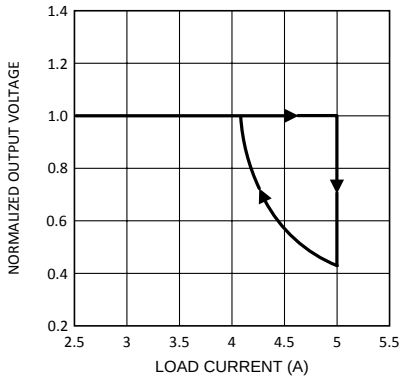


Figure 22. Normalized Output Voltage Versus Load Current

MODES OF OPERATION

Since the LM2696 utilizes a catch diode, whenever the load current is reduced to a point where the inductor ripple is greater than two times the load current, the part will enter discontinuous operation. This is because the diode does not permit the inductor current to reverse direction. The point at which this occurs is the critical conduction boundary and can be calculated by the following equation:

$$I_{BOUNDARY} = \frac{(V_{IN} - V_{OUT}) \cdot D}{2 \cdot L \cdot f_{SW}} \quad (19)$$

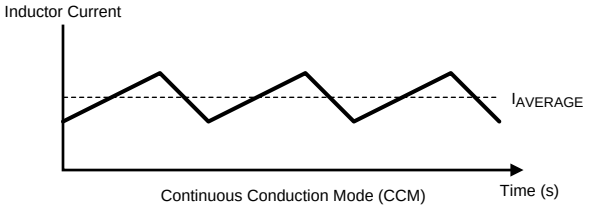
One advantage of the adaptive on-time control scheme is that during discontinuous conduction mode the frequency will gradually decrease as the load current decreases. In DCM the switching frequency may be determined using the relationship:

$$f_{SW} = \frac{2 \cdot L \cdot V_{OUT} \cdot I_{OUT}}{T_{ON}^2 \cdot V_{IN} \cdot (V_{IN} - V_{OUT})} \quad (20)$$

It can be seen that there will always be some minimum switching frequency. The minimum switching frequency is determined by the parameters above and the minimum load presented by the feedback resistors. If there is some minimum frequency of operation the feedback resistors may be sized accordingly.

The adaptive on-time control scheme is effectively a pulse-skipping mode, but since it is not tied directly to an internal clock, its pulse will only occur when needed. This is in contrast to schemes that synchronize to a reference clock frequency. The constant on-time pulse-skipping/DCM mode minimizes output voltage ripple and maximizes efficiency.

Several diagrams are shown in Figure 23 illustrating continuous conduction mode (CCM), discontinuous conduction mode (DCM), and the boundary condition.



Copyright © 2005–2013, Texas Instruments Incorporated

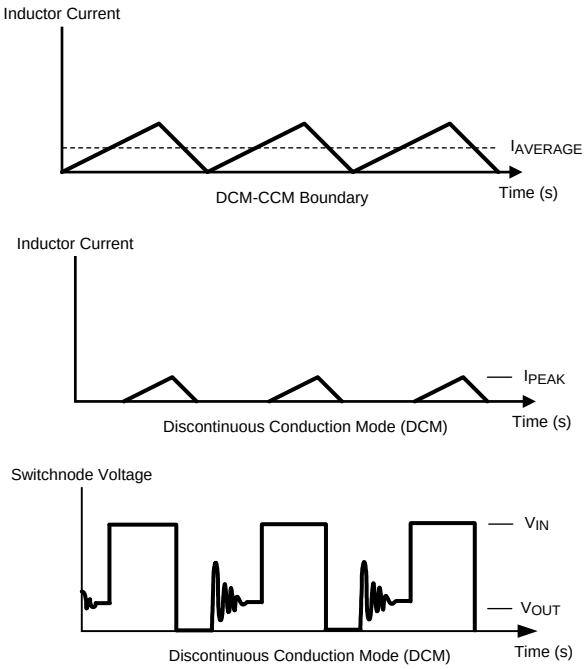


Figure 23. Modes of Operation

It can be seen that in DCM, whenever the inductor runs dry the SW node will become high impedance. Ringing will occur as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the SW node.

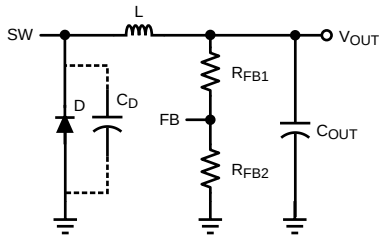


Figure 24. Parasitic Tank Circuit at the Switchpin

LINE REGULATION

The LM2696 regulates to the lowest point of the output voltage (V_L in Figure 25). This is to say that the output voltage may be represented by a waveform that is some average voltage with ripple. The LM2696 will regulate to the trough of the ripple.

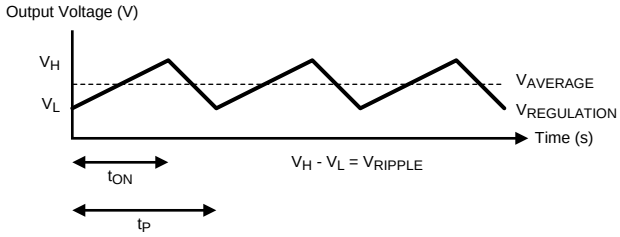


Figure 25. Average Output Voltage and Regulation Point

Copyright © 2005–2013, Texas Instruments Incorporated

The output voltage is given by the following relationship:

$$V_{OUT} = V_L = V_{AVERAGE} - \frac{1}{2} V_{RIPPLE} = V_{AVERAGE} - \frac{1}{2} \Delta I_L \bullet R_{ESR} \quad (21)$$

as discussed in the FEEDBACK RESISTORS section of this document.

TRANSIENT RESPONSE

Constant on-time architectures have inherently excellent transient line and load response. This is because the control loop is extremely fast. Any change in the line or load conditions will result in a nearly instantaneous response in the PWM off time.

If one considers the switcher response to be nearly cycle-by-cycle, and amount of energy contained in a single PWM pulse, there will be very little change in the output for a given change in the line or load.

EFFICIENCY

The constant on-time architecture features high efficiency even at light loads. The ability to achieve high efficiency at light loads is due to the fact that the off-time will become necessarily long at light loads. Having extended the off-time, there is little mechanism for loss during this interval.

The efficiency is easily estimated using the following relationships:

Power loss due to FET:

$P_{FET} = P_C + P_{GC} + P_{SW}$

Where

- $P_C = D \bullet (I_{OUT}^2 \bullet R_{DS_ON})$
- $P_{GC} = AV_{IN} + V_{GS} \bullet Q_{GS} \bullet f_{SW}$
- $P_{SW} = 0.5 \bullet V_{IN} \cdot I_{OUT} \bullet (t_r + t_f) \bullet f_{SW}$ (22)

Typical values are:

$\mathbf{R_{DS_ON}}$ = 130 mΩ

V_{GS} = 4V
Q_{GS} = 13.3 nC
t_r= 3.8 ns
t_f= 4.5 ns Power loss due to catch diode:

$P_D = (1\text{-}D) \bullet (I_{OUT} \bullet V_f)$ (23)

Power loss due to DCR and ESR:

$P_{DCR} = I_{OUT}^2 \bullet R_{DCR}$ (24)

$P_{ESR_OUTPUT} = I_{RIPPLE}^2/\sqrt{12} \bullet R_{ESR_OUTPUT}$ (25)

$P_{ESR_INPUT} = I_{OUT}^2(D(1\text{-}D)) \bullet R_{ESR_INPUT}$ (26)

Power loss due to Controller:

$P_{CONT} = V_{IN} \bullet I_Q$ (27)

I_Q is typically 1.3 mA (28)

The efficiency may be calculated as shown below:

Total power loss = $P_{FET} + P_D + P_{DCR} + P_{ESR_OUTPUT} + P_{ESR_INPUT} + P_{CONT}$ (29)

Power Out = $I_{OUT} \bullet V_{OUT}$ (30)

$$\text{Efficiency} = \frac{\text{Power_Out}}{\text{Power_Out} + \text{Total_Power_Loss}} \quad (31)$$

Copyright © 2005–2013, Texas Instruments Incorporated

PRE-BIAS LOAD STARTUP

Should the LM2696 start into a pre-biased load the output will not be pulled low. This is because the part is asynchronous and cannot sink current. The part will respond to a pre-biased load by simply enabling PWM high or extending the off-time until regulation is achieved. This is to say that if the output voltage is greater than the regulation voltage the off-time will extend until the voltage discharges through the feedback resistors. If the load voltage is greater than the regulation voltage, a series of pulses will charge the output capacitor to its regulation voltage.

THERMAL CONSIDERATIONS

The thermal characteristics of the LM2696 are specified using the parameter θ_{JA}, which relates the junction temperature to the ambient temperature. While the value of θ_{JA} is specific to a given set of test parameters (including board thickness, number of layers, orientation, etc), it provides the user with a common point of reference.

To obtain an estimate of a devices junction temperature, one may use the following relationship:

$$T_J = P_{IN} (1\text{-Efficiency}) \times \theta_{JA} + T_A$$

Where

- T_J is the junction temperature in ºC
- P_{IN} is the input power in Watts ($P_{IN} = V_{IN} \cdot I_{IN}$)
- θ_{JA} is the thermal coefficient of the LM2696
- T_A is the ambient temperature in ºC

(32)

LAYOUT CONSIDERATIONS

The LM2696 regulation and under-voltage comparators are very fast and will respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The components at pins 5, 6, 7, 12 and 13 should be as physically close as possible to the IC, thereby minimizing noise pickup in the PC traces. If the internal dissipation of the LM2696 produces excessive junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the HTSSOP-16 package can be soldered to a ground plane on the PC board, and that plane should extend out from beneath the IC to help dissipate the heat. Use of several vias beneath the part is also an effective method of conducting heat. Additionally, the use of wide PC board traces, where possible, can also help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures. Traces in the power plane (Figure 26) should be short and wide to minimize the trace impedance; they should also occupy the smallest area that is reasonable to minimize EMI. Sizing the power plane traces is a tradeoff between current capacity, inductance, and thermal dissipation. For more information on layout considerations, please refer to TI Application Note AN-1229.

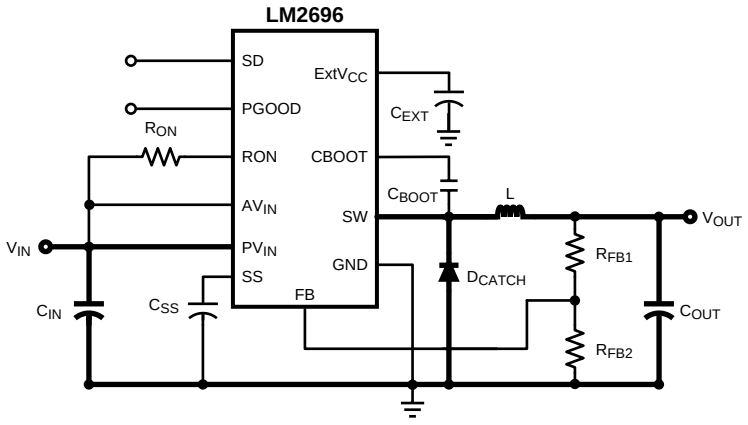


Figure 26. Bold Traces Are In The Power Plane

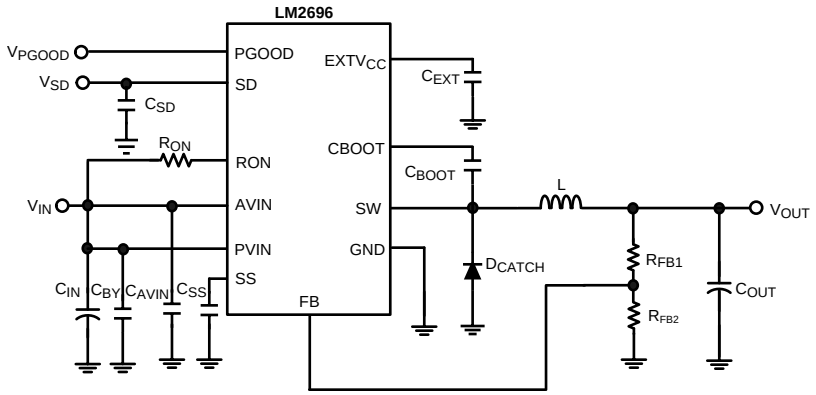


Figure 27. 5V-to-2.5V Voltage Applications Circuit

Table 1. Bill of Materials(1)

Designator	Function	Description	Vendor	Part Number
C_{IN}	Input Cap	470 µF	Sanyo	10MV470WX
C_{BY}	Bypass Cap	0.1 µF	Vishay	VJ0805Y104KXAM
C_{SS}	Soft-Start Cap	0.01 µF	Vishay	VJ080JY103KXX
C_{EXT}	$EXTV_{CC}$	1 µF	Vishay	VJ0805Y105JXACW1BC
C_{BOOT}	Boot	0.1 µF	Vishay	VJ0805Y104KXAM
C_{AVIN}	Analog V_{IN}	1 µF	Vishay	VJ0805Y105JXACW1BC
C_{OUT}	Output Cap	47 µF	AVX	TPSW476M010R0150
C_{SD}	Shutdown Cap	1 nF	Vishay	VJ0805Y102KXXA
R_{FB1}	High Side FB Res	1 kΩ	Vishay	CRCW08051001F
R_{FB2}	Low Side RB Res	1 kΩ	Vishay	CRCW08051001F
R_{ON}	On Time Res	143 kΩ	Vishay	CRCW08051433F
D_{CATCH}	Boot Diode	40V @ 3A Diode	Central Semi	CMSH3-40M-NST
L	Output Inductor	6.8 uH, 4.9A ISAT	Coilcraft	MSS1260-682MX

(1) (Figure 27: Medium Voltage Board, 5V-to-2.5V conversion, f_{sw} = 300 kHz)

Copyright © 2005–2013, Texas Instruments Incorporated

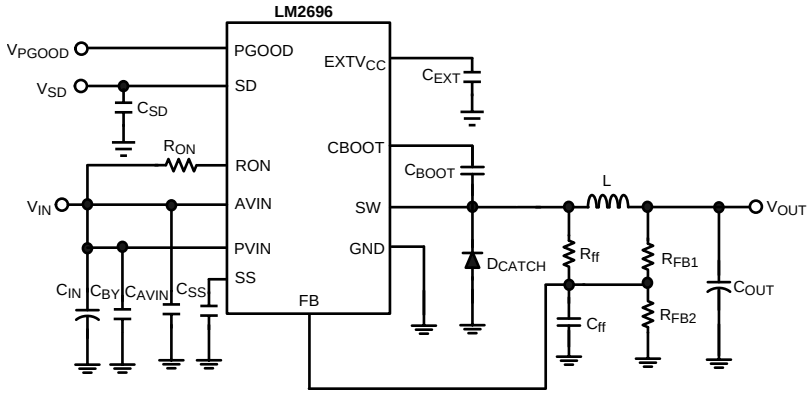


Figure 28. 12V-to 3.3V Voltage Applications Circuit

Table 2. Bill of Materials(1)

Designator	Function	Description	Vendor	Part Number
C_{IN}	Input Cap	560 µF	Sanyo	35MV560WX
C_{BY}	Bypass Cap	0.1 µF	Vishay	VJ0805Y104KXAM
C_{SS}	Soft-Start Cap	0.01 µF	Vishay	VJ080JY103KXX
C_{EXT}	$EXTV_{CC}$	1 µF	Vishay	VJ0805Y105JXACW1BC
C_{BOOT}	Boot	0.1 µF	Vishay	VJ0805Y104KXAM
C_{AVIN}	Analog V_{IN}	1 µF	Vishay	VJ0805Y105JXACW1BC
C_{OUT}	Output Cap	100 µF	Sanyo	6SVPC100M
C_{SD}	Shutdown Cap	1 nF	Vishay	VJ0805Y102KXXA
C_{ff}	Feedforward Cap	560 pF	Vishay	VJ0805A561KXXA
R_{ff}	Feedforward Res	1 MΩ	Vishay	CRCW08051004F
R_{FB1}	High Side FB Res	1.62 kΩ	Vishay	CRCW08051621F
R_{FB2}	Low Side RB Res	1 kΩ	Vishay	CRCW08051001F
R_{ON}	On Time Res	143 kΩ	Vishay	CRCW08051433F
D_{CATCH}	Boot Diode	40V @ 3A Diode	Central Semi	CMSH3-40M-NST
L	Output Inductor	10 uH, 5.4A ISAT	Coilcraft	MSS1278-103MX

(1) (Figure 28: Medium Voltage Board, 12V-to-3.3V conversion, f_{sw} = 300 kHz)

Copyright © 2005–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	21

Copyright © 2005–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2696MXA/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2696 MXA
LM2696MXA/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2696 MXA
LM2696MXA/NOPB.B	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2696 MXA
LM2696MXAX/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2696 MXA
LM2696MXAX/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2696 MXA
LM2696MXAX/NOPB.B	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2696 MXA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

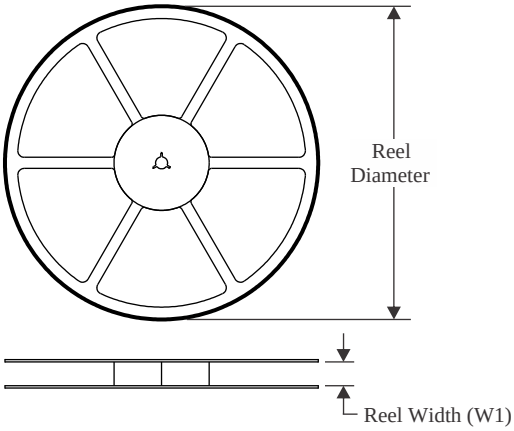
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

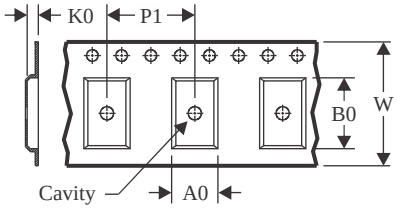
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

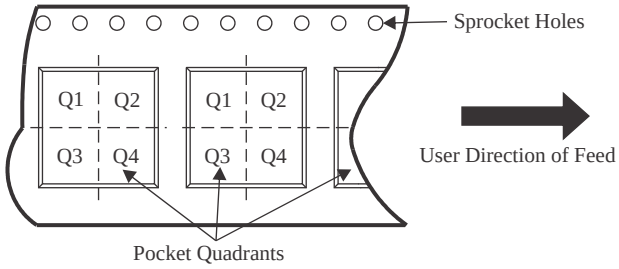


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

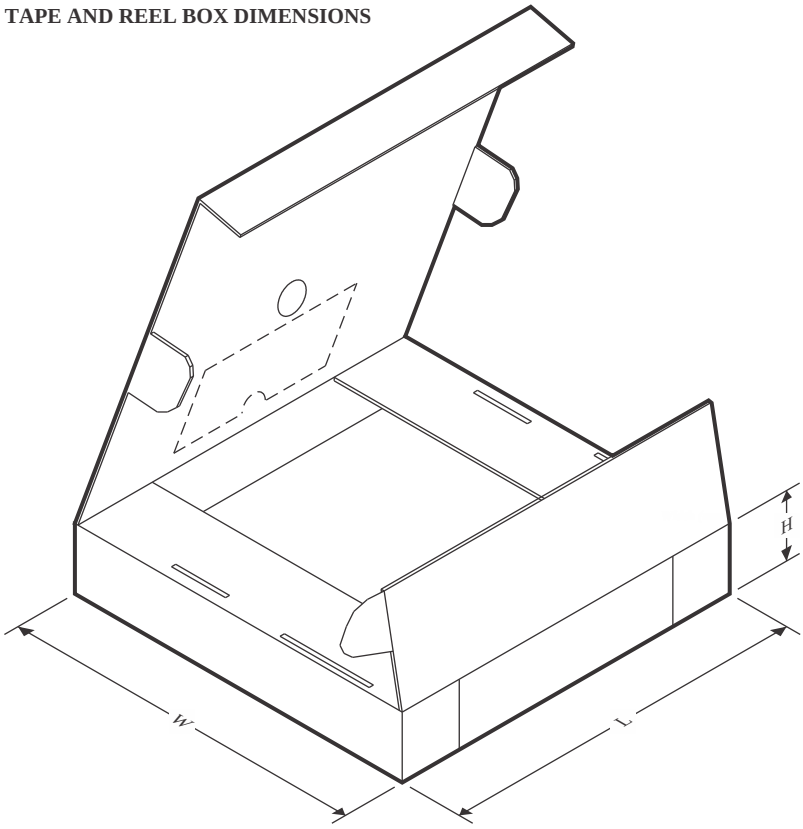
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2696MXAX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

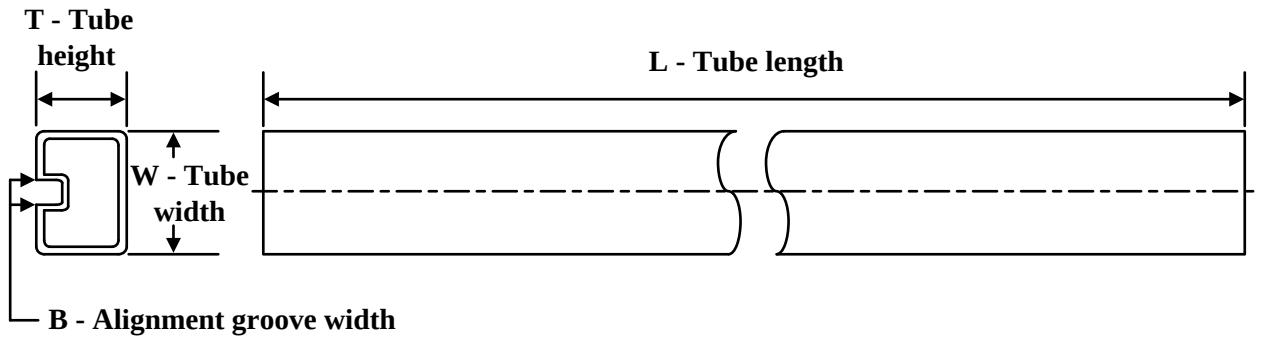
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2696MXAX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2696MXA/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM2696MXA/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM2696MXA/NOPB.B	PWP	HTSSOP	16	92	495	8	2514.6	4.06

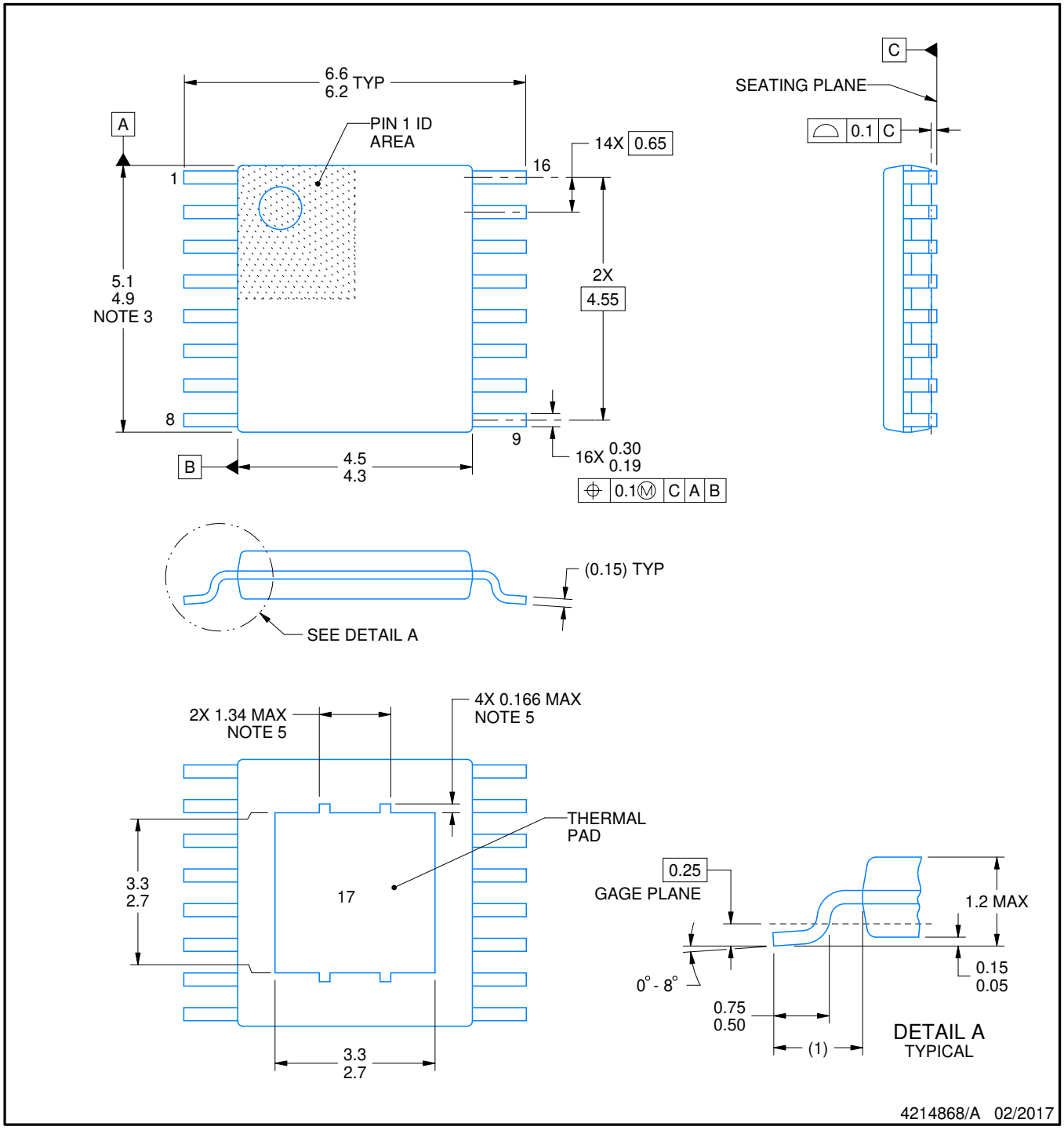


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

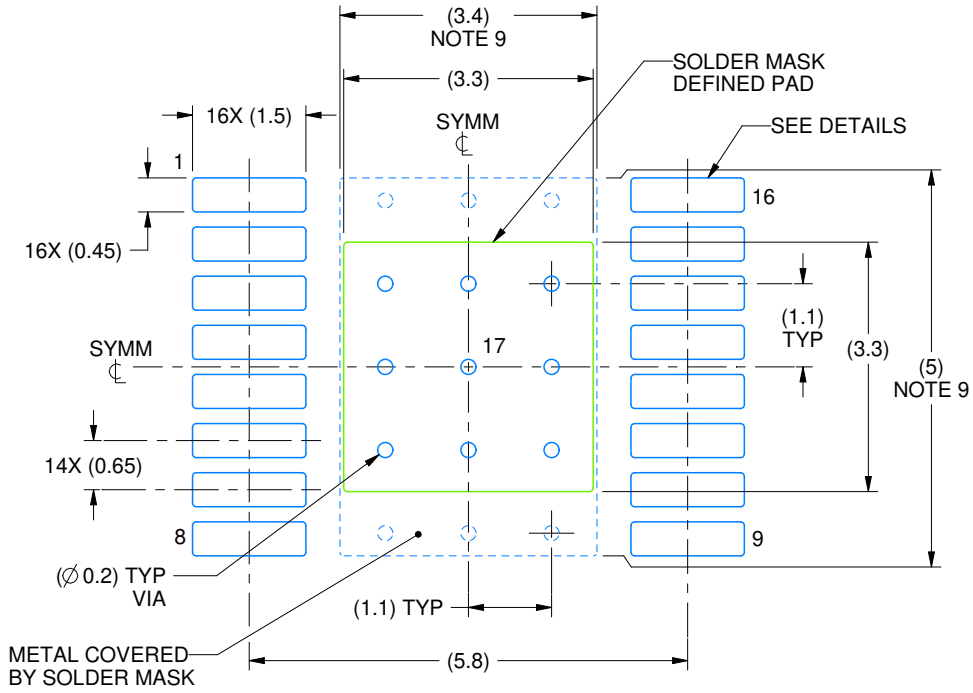
PLASTIC SMALL OUTLINE



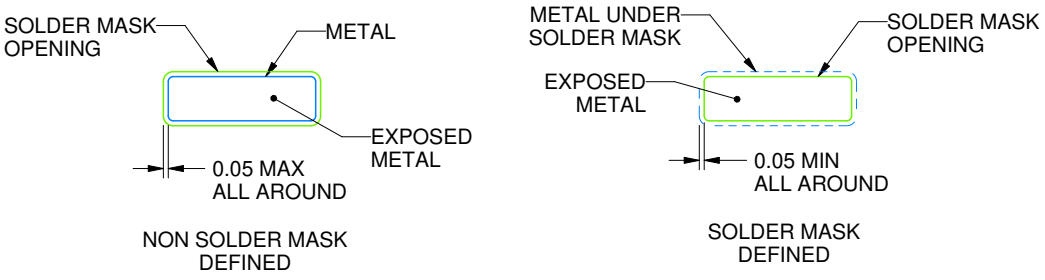
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

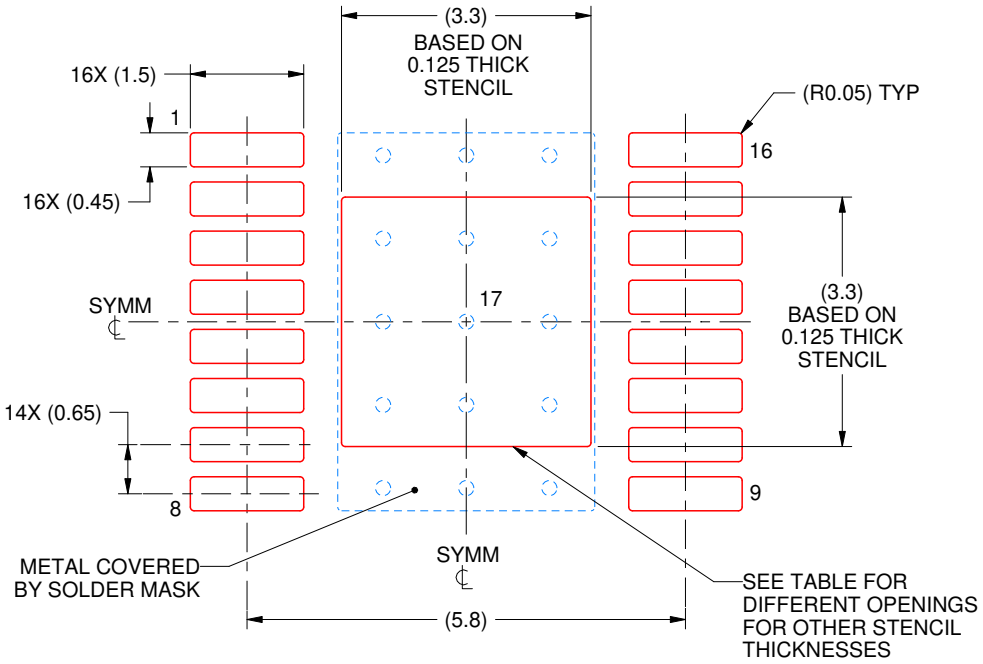


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025