LM2830/-Q1 High-Frequency 1.0-A Load Step-Down DC-DC Regulator

1 Features

- LM2830Z-Q1 and LM2830X-Q1 in the SOT-23 Package are Automotive-Grade Products that are AEC-Q100 Grade 1 Qualified (–40°C to +125°C Operating Junction Temperature)
- Space-Saving SOT-23 Package
- Input Voltage Range of 3.0 V to 5.5 V
- Output Voltage Range of 0.6 V to 4.5 V
- 1.0-A Output Current
- High Switching Frequencies
  - 1.6 MHz (LM2830X)
  - 3.0 MHz (LM2830Z)
- 130-mΩ PMOS Switch
- 0.6-V, 2% Internal Voltage Reference
- Internal Soft-Start
- Current Mode, PWM Operation
- Thermal Shutdown
- Overvoltage Protection

2 Applications

- Local 5-V to Vcore Step-Down Converters
- Core Power in HDDs
- Set-Top Boxes
- USB Powered Devices
- DSL Modems
- Automotive

3 Description

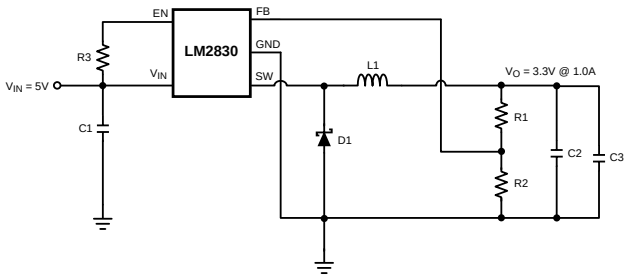
The LM2830 regulator is a monolithic, high-frequency, PWM step-down DC-DC converter in a 5-pin SOT-23 and a 6-Pin WSON package. The device provides all the active functions to provide local DC-DC conversion with fast transient response and accurate regulation in the smallest possible PCB area. With a minimum of external components, the LM2830 regulator is easy to use. The ability to drive 1.0-A loads with an internal 130-mΩ PMOS switch using state-of-the-art 0.5-µm BiCMOS technology results in the best power density available. The world-class control circuitry allows on-times as low as 30 ns, thus supporting exceptionally high frequency conversion over the entire 3-V to 5.5-V input operating range down to the minimum output voltage of 0.6 V. Switching frequency is internally set to 1.6 MHz, or 3.0 MHz, allowing the use of extremely small surface-mount inductors and chip capacitors. Even though the operating frequency is high, efficiencies up to 93% are easy to achieve. External shutdown is included, featuring an ultra-low standby current of 30 nA. The LM2830 regulator uses current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output overvoltage protection.

Device Information[1]

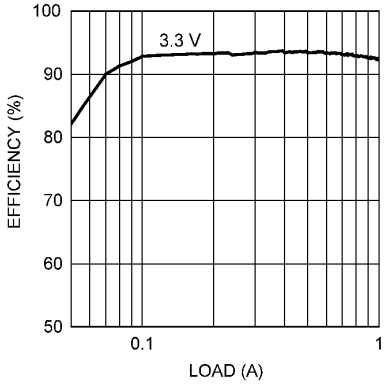
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2830	SOT (5)	2.90 mm × 1.60 mm
	WSON (6)	3.00 mm × 3.00 mm
LM2830-Q1	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

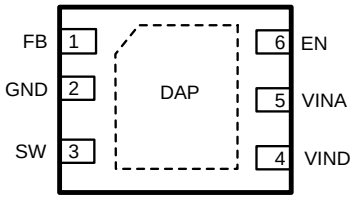
Changes from Revision C (April 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 23

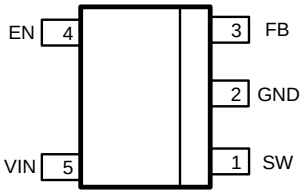
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5 Pin Configuration and Functions

WSON Package
6-Pin
Top View



SOT Package
5-Pins
Top View



Pin Functions (5-Pin SOT)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
SW	1	O	Output switch. Connect to the inductor and catch diode.
GND	2	G	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
FB	3	I	Feedback pin. Connect to external resistor divider to set output voltage.
EN	4	I	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than VIN + 0.3 V.
VIN	5	I/P	Input supply voltage.

(1) I: Input Pin, O: Output Pin, P: Power Pin, G: Ground Pin

Pin Functions (6-Pin WSON)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback pin. Connect to external resistor divider to set output voltage.
GND	2	G	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
SW	3	O	Output switch. Connect to the inductor and catch diode.
VIND	4	I/P	Power Input supply.
VINA	5	I/P	Control circuitry supply voltage. Connect VINA to VIND on PC board.
EN	6	I	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than VINA + 0.3V.
Die Attach Pad	–	–	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.

(1) I: Input Pin, O: Output Pin, P: Power Pin, G: Ground Pin

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6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
VIN	–0.5	7	V
FB Voltage	–0.5	3	V
EN Voltage	–0.5	7	V
SW Voltage	–0.5	7	V
Junction Temperature[3]		150	°C
T_{stg} Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Thermal shutdown will occur if the junction temperature exceeds the maximum junction temperature of the device.

6.2 ESD Ratings: LM2830

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM2830-Q1

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
	Charged device model (CDM), per AEC Q100-011	WSON corner pins (1, 3, 4, and 6)	±1000	
		SOT-23 corner pins (1, 3, 4, and 5)	±1000	
		Other pins	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
VIN	3		5.5	V
Junction Temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC[1]		LM2830, LM2830-Q1	LM2830	UNIT
		DBV	NGG	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.2	53.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.9	51.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	27.3	28.2	
ψ_{JT}	Junction-to-top characterization parameter	1.8	0.6	
ψ_{JB}	Junction-to-board characterization parameter	26.8	28.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	8.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.6 Electrical Characteristics

VIN = 5 V unless otherwise indicated. Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback Voltage	WSON and SOT-23 Package	0.588	0.600	0.612	V
$\Delta V_{FB}/V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3 V to 5 V		0.02		%/V
I_B	Feedback Input Bias Current			0.1	100	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.73	2.90	V
		V_{IN} Falling	1.85	2.3		
	UVLO Hysteresis			0.43		
F_{SW}	Switching Frequency	LM2830-X	1.2	1.6	1.95	MHz
		LM2830-Z	2.25	3.0	3.75	
D_{MAX}	Maximum Duty Cycle	LM2830-X	86%	94%		
		LM2830-Z	82%	90%		
D_{MIN}	Minimum Duty Cycle	LM2830-X		5%		
		LM2830-Z		7%		
$R_{DS(ON)}$	Switch On Resistance	WSON Package		150		mΩ
		SOT-23 Package		130	195	
I_{CL}	Switch Current Limit	V_{IN} = 3.3 V	1.2	1.75		A
V_{EN_TH}	Shutdown Threshold Voltage				0.4	V
	Enable Threshold Voltage		1.8			
I_{SW}	Switch Leakage			100		nA
I_{EN}	Enable Pin Current	Sink/Source		100		nA
I_Q	Quiescent Current (switching)	LM2830X V_{FB} = 0.55		3.3	5	mA
		LM2830Z V_{FB} = 0.55		4.3	6.5	mA
	Quiescent Current (shutdown)	All Options V_{EN} = 0 V		30		nA
T_{SD}	Thermal Shutdown Temperature			165		°C

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6.7 Typical Characteristics

All curves taken at VIN = 5.0 V with configuration in typical application circuit shown in *Application Information* section of this data sheet. T_J = 25°C, unless otherwise specified.

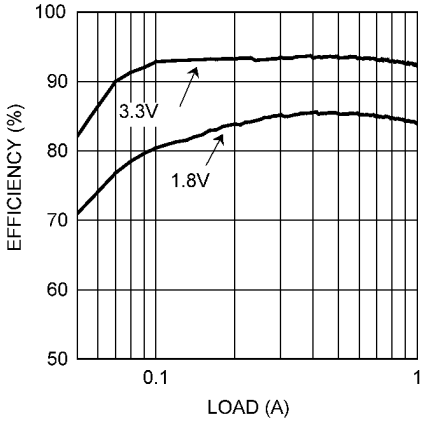


Figure 1. η vs Load "X" Vin = 5 V, Vo = 1.8 V and 3.3 V

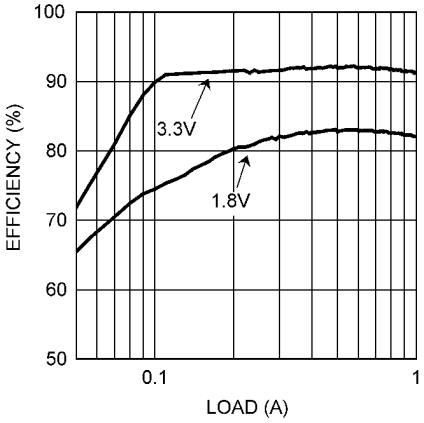


Figure 2. η vs Load "Z" Vin = 5 V, Vo = 3.3 V and 1.8 V

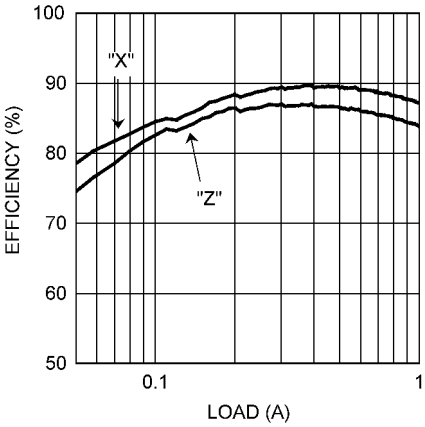


Figure 3. η vs Load "X and Z" Vin = 3.3 V, Vo = 1.8 V

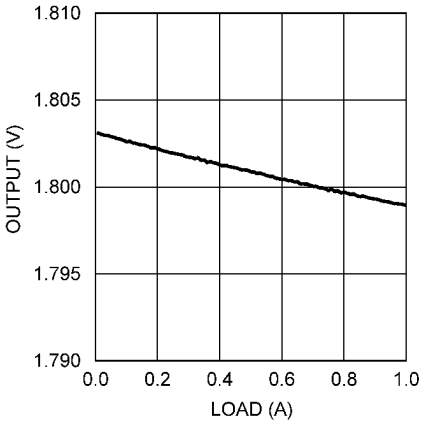


Figure 4. Load Regulation Vin = 3.3 V, Vo = 1.8 V (All Options)

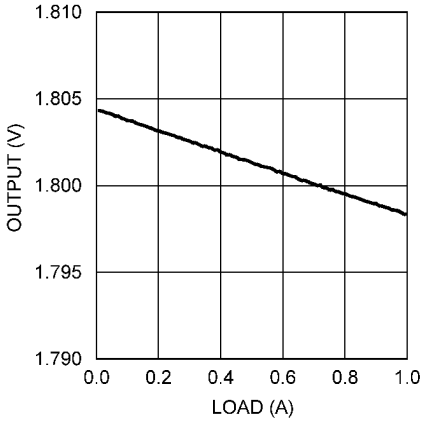


Figure 5. Load Regulation Vin = 5 V, Vo = 1.8 V (All Options)

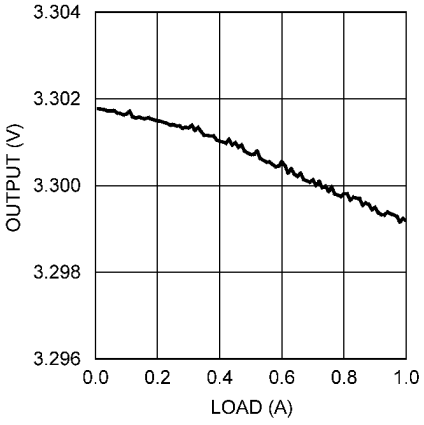


Figure 6. Load Regulation Vin = 5 V, Vo = 3.3 V (All Options)

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Typical Characteristics (continued)

All curves taken at VIN = 5.0 V with configuration in typical application circuit shown in *Application Information* section of this data sheet. T_J = 25°C, unless otherwise specified.

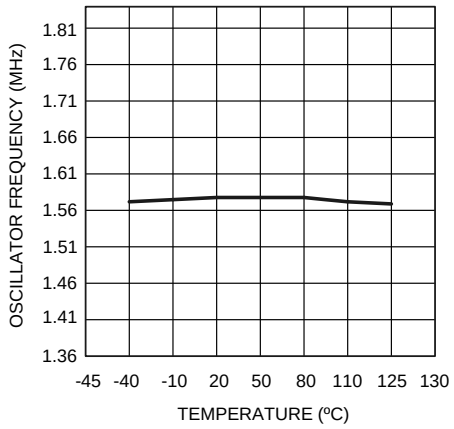


Figure 7. Oscillator Frequency vs Temperature - "X"

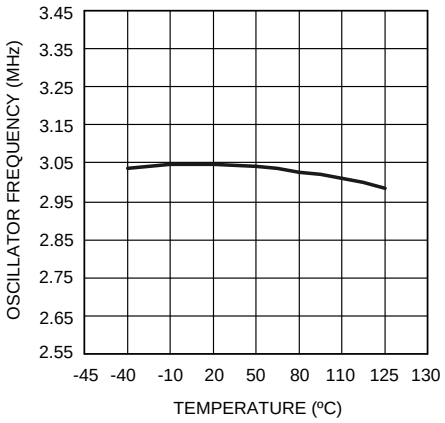


Figure 8. Oscillator Frequency vs Temperature - "Z"

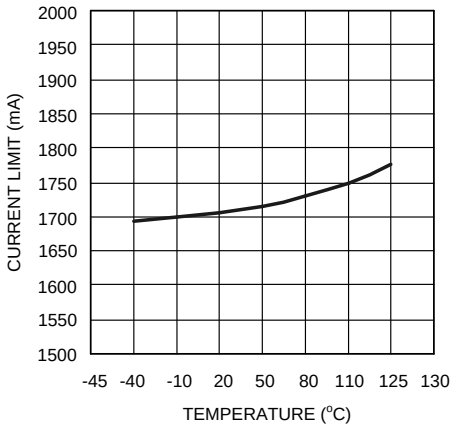


Figure 9. Current Limit vs Temperature Vin = 3.3 V

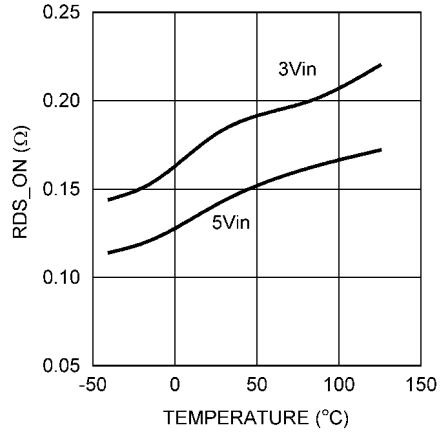


Figure 10. RDSON vs Temperature (WSON Package)

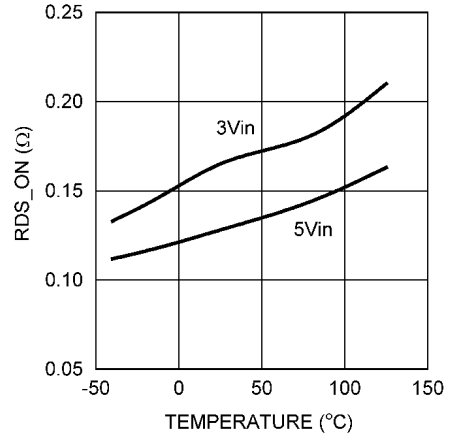


Figure 11. RDSON vs Temperature (SOT-23 Package)

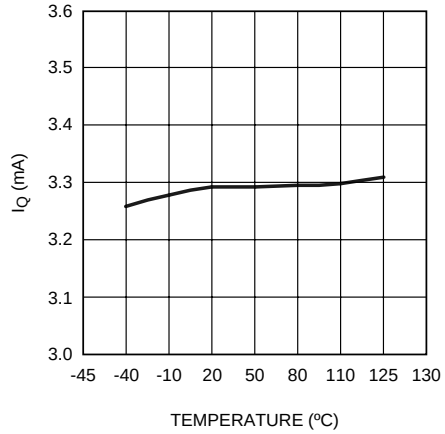


Figure 12. LM2830X I_Q (Quiescent Current)

Typical Characteristics (continued)

All curves taken at VIN = 5.0 V with configuration in typical application circuit shown in *Application Information* section of this data sheet. T_J = 25°C, unless otherwise specified.

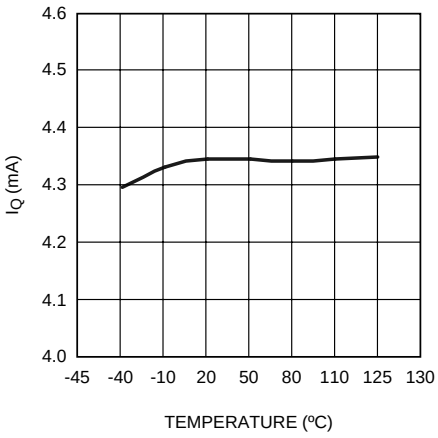


Figure 13. LM2830Z I_Q (Quiescent Current)

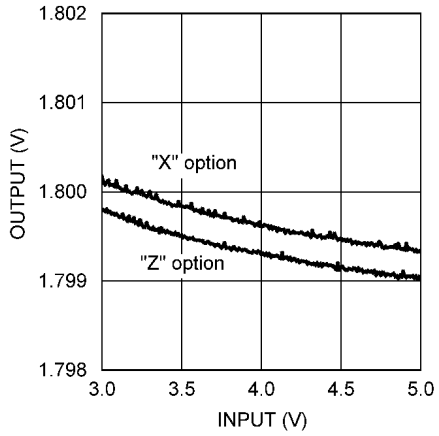


Figure 14. Line Regulation Vo = 1.8 V, Io = 500 mA

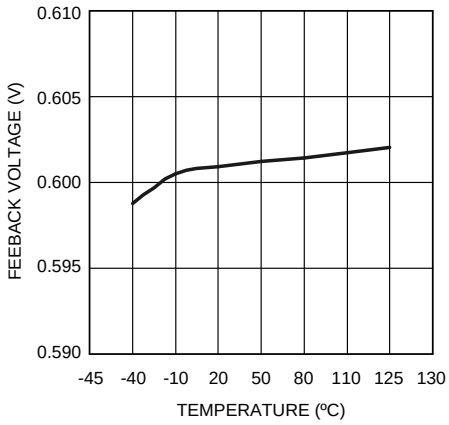


Figure 15. V_{FB} vs Temperature

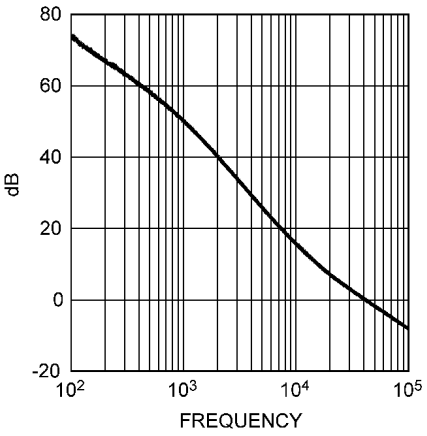


Figure 16. Gain vs Frequency (Vin = 5 V, Vo = 1.2 V at 1 A)

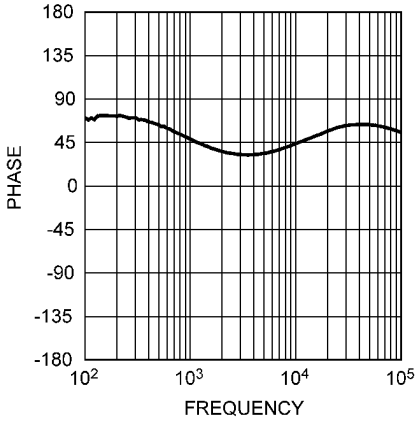


Figure 17. Phase Plot vs Frequency (Vin = 5 V, Vo = 1.2 V at 1 A)

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7 Detailed Description

7.1 Overview

The LM2830 device is a constant frequency PWM buck regulator IC that delivers a 1.0-A load current. The regulator has a preset switching frequency of 1.6 MHz or 3.0 MHz. This high frequency allows the LM2830 device to operate with small surface-mount capacitors and inductors, resulting in a DC-DC converter that requires a minimum amount of board space. The LM2830 device is internally compensated, so it is simple to use and requires few external components. The LM2830 device uses current-mode control to regulate the output voltage.

The following operating description of the LM2830 device will refer to the Simplified Block Diagram (*Functional Block Diagram*) and to the waveforms in Figure 18. The LM2830 device supplies a regulated output voltage by switching the internal PMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal PMOS control switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through the Schottky catch diode, which forces the SW pin to swing below ground by the forward voltage (V_D) of the Schottky catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

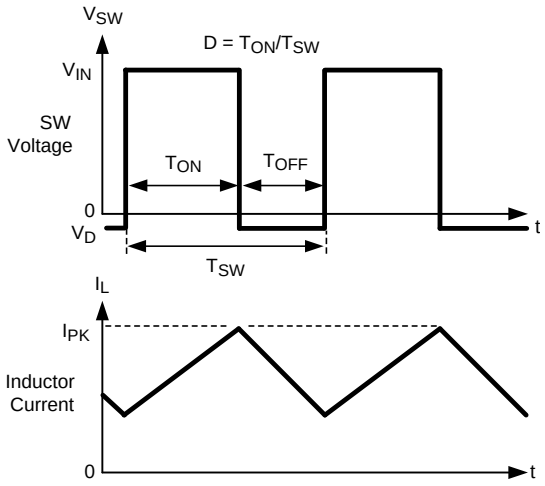
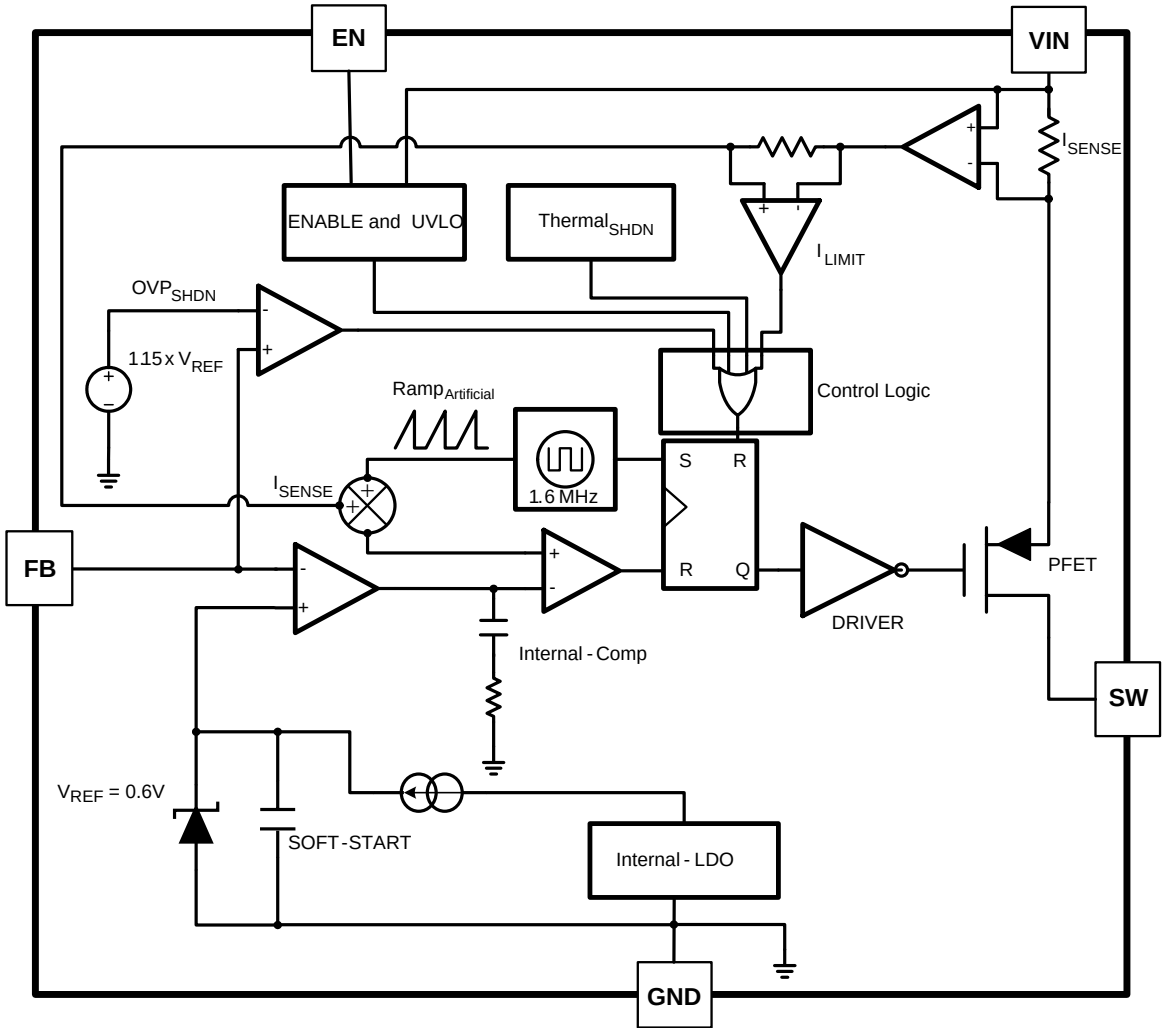


Figure 18. Typical Waveforms

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft-Start

This function forces V_{OUT} to increase at a controlled rate during start up. During soft-start, the error reference voltage of the amplifier ramps from 0 V to its nominal value of 0.6 V in approximately 600 µs. This forces the regulator output to ramp up in a controlled fashion, which helps reduce inrush current.

7.3.2 Output Overvoltage Protection

The overvoltage comparator compares the FB pin voltage to a voltage that is 15% higher than the internal reference V_{REF}. Once the FB pin voltage goes 15% above the internal reference, the internal PMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

7.3.3 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LM2830 device from operating until the input voltage exceeds 2.73 V (typical). The UVLO threshold has approximately 430 mV of hysteresis, so the part will operate until V_{IN} drops below 2.3V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is nonmonotonic.

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Feature Description (continued)

7.3.4 Current Limit

The LM2830 device uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 1.75 A (typical), and turns off the switch until the next switching cycle begins.

7.3.5 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 150°C.

7.4 Device Functional Modes

In normal operational mode, the device will regulate output voltage to the value set with resistive divider.

In addition, this device has an enable (EN) pin that lets the user turn the device on and off by driving this pin high and low. Default setup is that this pin is connected to V_{IN} through pull up resistor (typically 100 kΩ). When enable pin is low the device is in shutdown mode consuming typically only 30 nA, making it ideal for applications where low power consumption is desirable.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device operates with input voltage in the range of 3.3 V to 5.5 V and provide regulated output voltage up to 1 A of continuous DC load. This device is optimized for high efficiency operation with minimum number of external components. Also, high switching frequency allows use of small surface-mount components enabling very small solution size. For component selection, see *Detailed Design Procedure*.

8.2 Typical Applications

8.2.1 LM2830X Design Vo = 1.2 V at 1.0A

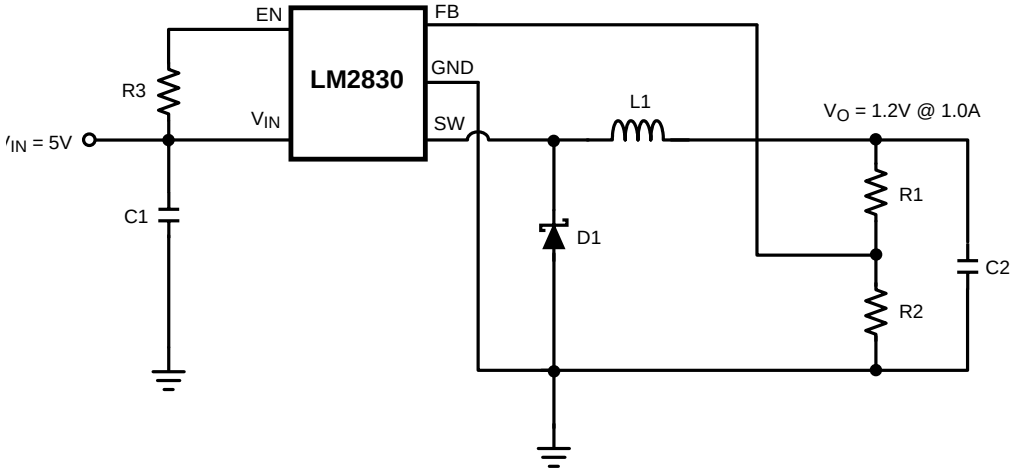


Figure 19. LM2830X (1.6 MHz): Vin = 5 V, Vo = 1.2 V at 1.0-A Schematic

8.2.1.1 Design Requirements

This device must be able to operate at any voltage within input voltage range.

Load Current must be defined to properly size the inductor, input and output capacitors. Inductor should be able to handle full expected load current as well as the peak current generated during load transients and start up. Inrush current at startup will depend on the output capacitor selection. More details are provided in *Detailed Design Procedure*.

Device has an enable (EN) pin that is used to enable and disable the device. This pin is active high and should not be left floating in application.

8.2.1.2 Detailed Design Procedure

Table 1. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	1.0-A Buck Regulator	TI	LM2830X
C1, Input Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C2, Output Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
D1, Catch Diode	0.3 V_f Schottky 1.5 A, 30 V_R	TOSHIBA	CRS08

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Typical Applications (continued)

Table 1. Bill of Materials (continued)

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
L1	3.3 µH, 1.3 A	Coilcraft	ME3220-332
R2	15.0 kΩ, 1%	Vishay	CRCW08051502F
R1	15.0 kΩ, 1%	Vishay	CRCW08051502F
R3	100 kΩ, 1%	Vishay	CRCW08051003F

8.2.1.2.1 Inductor Selection

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal PMOS must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{2}$$

V_{SW} can be approximated by:

$$V_{SW} = I_{OUT} \times R_{DSON} \tag{3}$$

The diode forward drop (V_D) can range from 0.3 V to 0.7 V depending on the quality of the diode. The lower the V_D, the higher the operating efficiency of the converter. The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value will decrease the output ripple current.

One must ensure that the minimum current limit (1.2 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L \tag{4}$$

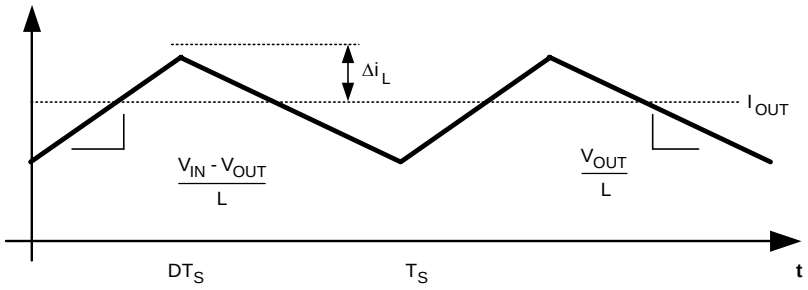


Figure 20. Inductor Current

$$\frac{V_{IN} - V_{OUT}}{L} = \frac{2\Delta i_L}{DT_S} \tag{5}$$

In general,

$$\Delta i_L = 0.1 \times (I_{OUT}) \rightarrow 0.2 \times (I_{OUT}) \tag{6}$$

If Δi_L = 20% of 1 A, the peak current in the inductor will be 1.2 A. The minimum ensured current limit over all operating conditions is 1.2 A. One can either reduce Δi_L, or make the engineering judgment that zero margin will be safe enough. The typical current limit is 1.75 A.

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The LM2830 device operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the *Output Capacitor* for more details on calculating output voltage ripple. Now that the ripple current is determined, the inductance is calculated by:

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) \times (V_{IN} - V_{OUT})$$

where

- $T_s = 1/f_s$ (7)

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, it is necessary to specify the peak current of the inductor only required maximum output current. For example, if the designed maximum output current is 1.0 A and the peak current is 1.25 A, then the inductor should be specified with a saturation current limit of > 1.25 A. There is no need to specify the saturation or peak current of the inductor at the 1.75-A typical switch current limit. The difference in inductor size is a factor of 5. Because of the operating frequency of the LM2830 device, ferrite based inductors are preferred to minimize core losses. This presents little restriction because the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (R_{DCR}) will provide better operating efficiency.

8.2.1.2.2 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and ESL (Equivalent Series Inductance). The recommended input capacitance is 22 µF. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS_IN} \sqrt{D\left[I_{OUT}{}^2\,(1\text{-}D) + \frac{\Delta i^2}{3}\right]} \tag{8}$$

Neglecting inductor ripple simplifies the above equation to:

$$I_{RMS_IN} = I_{OUT} \times \sqrt{D(1 - D)} \tag{9}$$

From Equation 9, it can be shown that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle D is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and a 0805 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LM2830 device, leaded capacitors may have an ESL so large that the resulting impedance (2πfL) will be higher than that required to provide stable operation. As a result, surface-mount capacitors are strongly recommended.

Sanyo POSCAP, Tantalum or Niobium, Panasonic SP, and multilayer ceramic capacitors (MLCC) are all good choices for both input and output capacitors and have very low ESL. For MLCCs it is recommended to use X7R or X5R type capacitors due to their tolerance and temperature characteristics. Consult the capacitor manufacturer data sheets to see how rated capacitance varies over operating conditions.

8.2.1.2.3 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \tag{10}$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LM2830 device, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic

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capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Because the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum of 22 µF of output capacitance. Capacitance often, but not always, can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types.

8.2.1.2.4 Catch Diode

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode should be chosen so that its current rating is greater than:

$$I_{D1} = I_{OUT} \times (1\text{-}D) \tag{11}$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward voltage drop.

8.2.1.2.5 Output Voltage

The output voltage is set using Equation 12, where R2 is connected between the FB pin and GND, and R1 is connected between V_O and the FB pin. A good value for R2 is 10 kΩ. When designing a unity gain converter (Vo = 0.6 V), R1 should be between 0 Ω and 100 Ω, and R2 should be equal or greater than 10 kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \tag{12}$$

$$V_{REF} = 0.60\ V \tag{13}$$

8.2.1.2.6 Calculating Efficiency, and Junction Temperature

The complete LM2830 DC-DC converter efficiency can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{14}$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \tag{15}$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter: switching and conduction. Conduction losses usually dominate at higher output loads, whereas switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{16}$$

V_{SW} is the voltage drop across the internal PFET when it is on, and is equal to:

$$V_{SW} = I_{OUT} \times R_{DSON} \tag{17}$$

V_D is the forward voltage drop across the Schottky catch diode. It can be obtained from the diode manufacturer's Electrical Characteristics section. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_D + V_{DCR}}{V_{IN} + V_D + V_{DCR} - V_{SW}} \tag{18}$$

The conduction losses in the free-wheeling Schottky diode are calculated as follows:

$$P_{DIODE} = V_D \times I_{OUT} \times (1\text{-}D) \tag{19}$$

Often this is the single most significant power loss in the circuit. Care should be taken to choose a Schottky diode that has a low forward voltage drop.

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Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (20)$$

The conduction loss of the LC2830 device is mainly associated with the internal PFET:

$$P_{COND} = (I_{OUT}^2 \times D)\left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON} \quad (21)$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to:

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D \quad (22)$$

Switching losses are also associated with the internal PFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows:

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{RISE}) \quad (23)$$

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{FALL}) \quad (24)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (25)$$

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (26)$$

I_Q is the quiescent operating current, and is typically around 3.3 mA for the 1.6-MHz frequency option.

Table 2 lists typical application power losses.

Table 2. Power Loss Tabulation

Design Parameter	Value	Design Parameter	Value
V_{IN}	5.0 V		
V_{OUT}	3.3 V	P_{OUT}	3.3 W
I_{OUT}	1.0A		
V_D	0.45 V	P_{DIODE}	150 mW
F_{SW}	1.6 MHz		
I_Q	3.3 mA	P_Q	17 mW
T_{RISE}	4 nS	P_{SWR}	6 mW
T_{FALL}	4 nS	P_{SWF}	6 mW
$R_{DS(ON)}$	150 mΩ	P_{COND}	100 mW
IND_{DCR}	70 mΩ	P_{IND}	70 mW
D	0.667	P_{LOSS}	345 mW
η	88%	$P_{INTERNAL}$	125 mW

$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q = P_{LOSS} \quad (27)$$

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q = P_{INTERNAL} \quad (28)$$

$$P_{INTERNAL} = 125mW \quad (29)$$

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8.2.1.3 Application Curves

Figure 21 and Figure 22 show start-up waveforms.

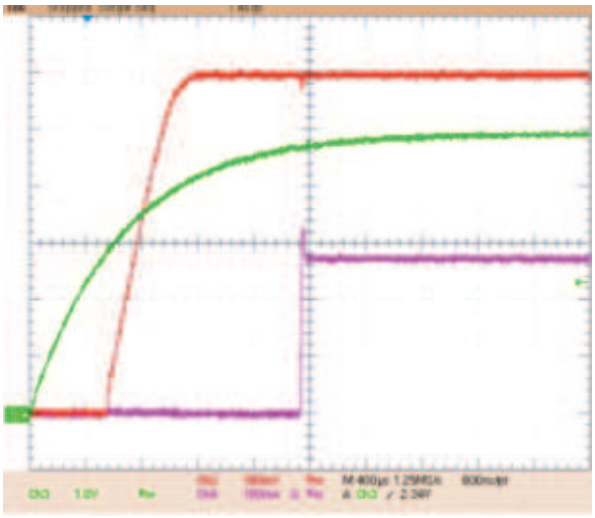


Figure 21. V_{IN} = 5.0 V, V_{OUT} = 0.6 V, I_{load} = 250 mA at 25°C

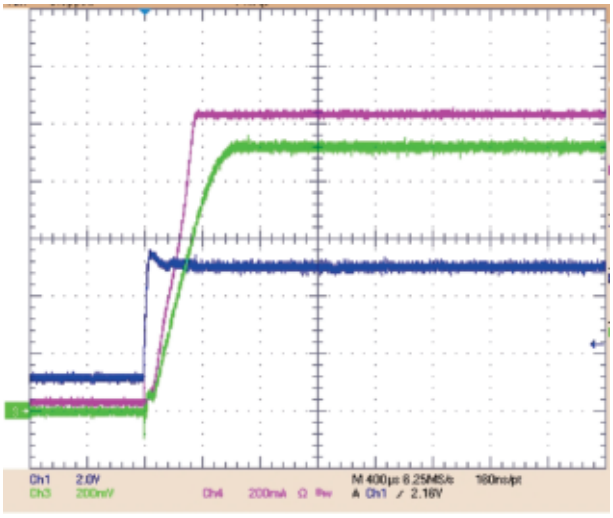


Figure 22. V_{IN} = 5.0 V, V_{OUT} = 0.9 V, I_{load} = 1 A at –40°C

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8.2.2 LM2830X Design Vo = 0.6 V at 1.0-A

Figure 23 shows typical application circuit for step-down solution from V_{IN}=5 to V_{OUT}=0.6 V, 1.0-A load current.

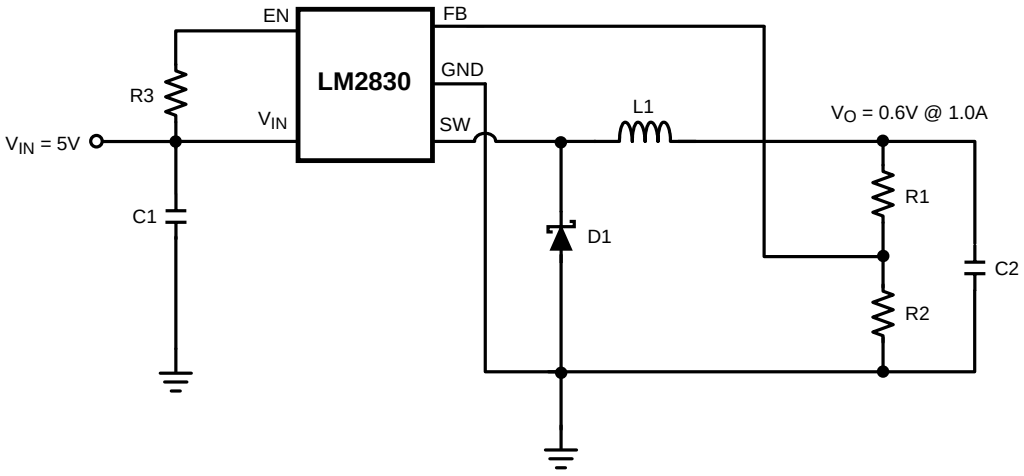


Figure 23. LM2830X (1.6 MHz): Vin = 5 V, Vo = 0.6 V at 1.0-A Schematic

Table 3. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	1.0-A Buck Regulator	TI	LM2830X
C1, Input Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C2, Output Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
D1, Catch Diode	0.3 V_f Schottky 1.5 A, 30 V_R	TOSHIBA	CRS08
L1	3.3 µH, 1.3 A	Coilcraft	ME3220-332
R2	10.0 kΩ, 1%	Vishay	CRCW08051000F
R1	0 Ω		
R3	100 kΩ, 1%	Vishay	CRCW08051003F

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8.2.3 LM2830X Design Vo = 3.3 V at 1.0-A

Figure 24 shows typical application circuit for step down solution from V_{IN}=5 to V_{OUT}=3.3 V, 1.0-A load current.

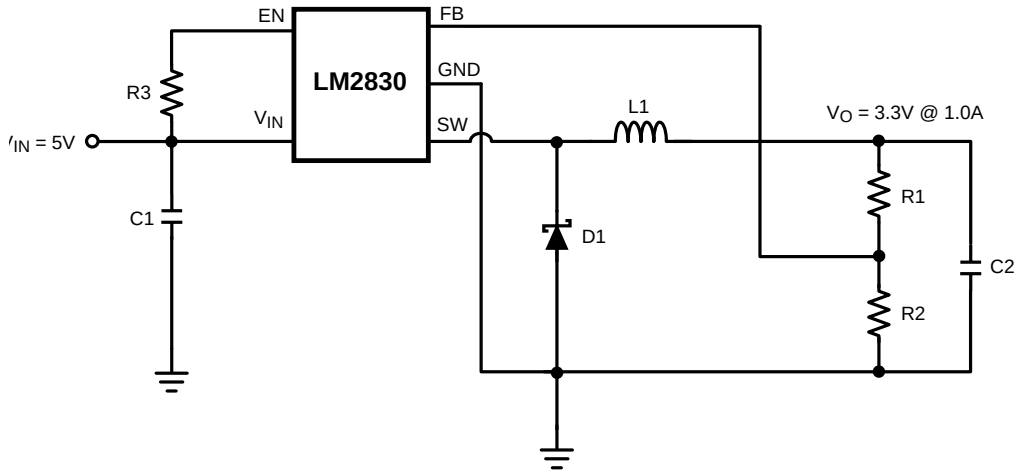


Figure 24. LM2830X (1.6 MHz): Vin = 5 V, Vo = 3.3 V at 1.0-A Schematic

Table 4. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	1.0-A Buck Regulator	TI	LM2830X
C1, Input Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C2, Output Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
D1, Catch Diode	0.3 V_f Schottky 1.5 A, 30 V_R	TOSHIBA	CRS08
L1	2.2 µH, 1.8 A	Coilcraft	ME3220-222
R2	10.0 kΩ, 1%	Vishay	CRCW08051002F
R1	45.3 kΩ, 1%	Vishay	CRCW08054532F
R3	100 kΩ, 1%	Vishay	CRCW08051003F

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8.2.4 LM2830Z Design Vo = 3.3 V at 1.0-A

Figure 25 shows typical application circuit for step down solution from V_{IN}=5 to V_{OUT}=3.3 V, 1.0-A load current when using device version with higher switching frequency.

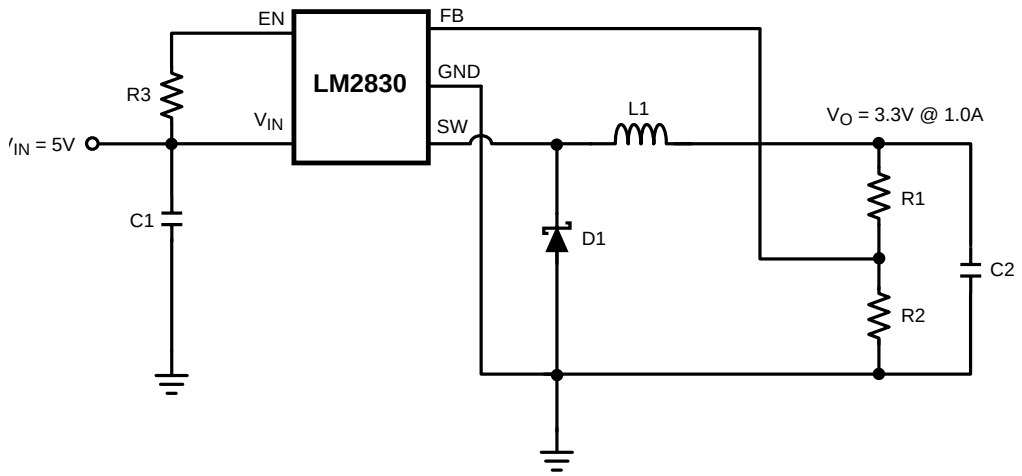


Figure 25. LM2830Z (3 MHz): Vin = 5 V, Vo = 3.3 V at 1.0-A Schematic

Table 5. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	1.0-A Buck Regulator	TI	LM2830Z
C1, Input Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C2, Output Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
D1, Catch Diode	0.3 V_f Schottky 1.5 A, 30V_R	TOSHIBA	CRS08
L1	1.6 µH, 2.0 A	TDK	VLCF4018T-1R6N1R7-2
R2	10.0 kΩ, 1%	Vishay	CRCW08051002F
R1	45.3 kΩ, 1%	Vishay	CRCW08054532F
R3	100 kΩ, 1%	Vishay	CRCW08051003F

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8.2.5 LM2830Z Design Vo = 1.2 V at 1.0-A

Figure 26 shows a typical application circuit for step down solution from V_{IN}=5 to V_{OUT}=1.2 V, 1.0-A load current when using device version with higher switching frequency.

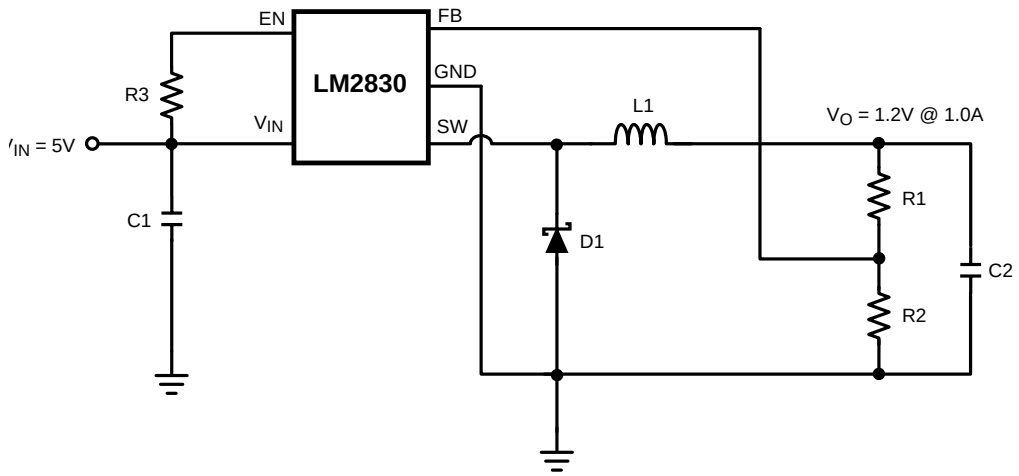


Figure 26. LM2830Z (3 MHz): Vin = 5 V, Vo = 1.2 V at 1.0-A Schematic

Table 6. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	1.0-A Buck Regulator	TI	LM2830Z
C1, Input Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C2, Output Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
D1, Catch Diode	0.3V_f Schottky 1.5 A, 30V_R	TOSHIBA	CRS08
L1	1.6 µH, 2.0 A	TDK	VLCF4018T-1R6N1R7-2
R2	10.0 kΩ, 1%	Vishay	CRCW08051002F
R1	10.0 kΩ, 1%	Vishay	CRCW08051002F
R3	100 kΩ, 1%	Vishay	CRCW08051003F

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8.2.6 LM2830X Dual Converters With Delayed Enabled Design

Figure 27 shows proposed solution with two LM2830 devices. Output of device on top (3.3-V output) is used to control the enable pin of the lower device, thus ensuring that the second device (1.2-V output) can not turn on before the output of first device (3.3-V in this example) reaches steady state. Additionally, small POR supervisory (LP3470) circuit is used to monitor enable voltage for lower device. The RESET pin on POR circuit is open drain and requires typically 20-kΩ pullup resistor to the monitored voltage.

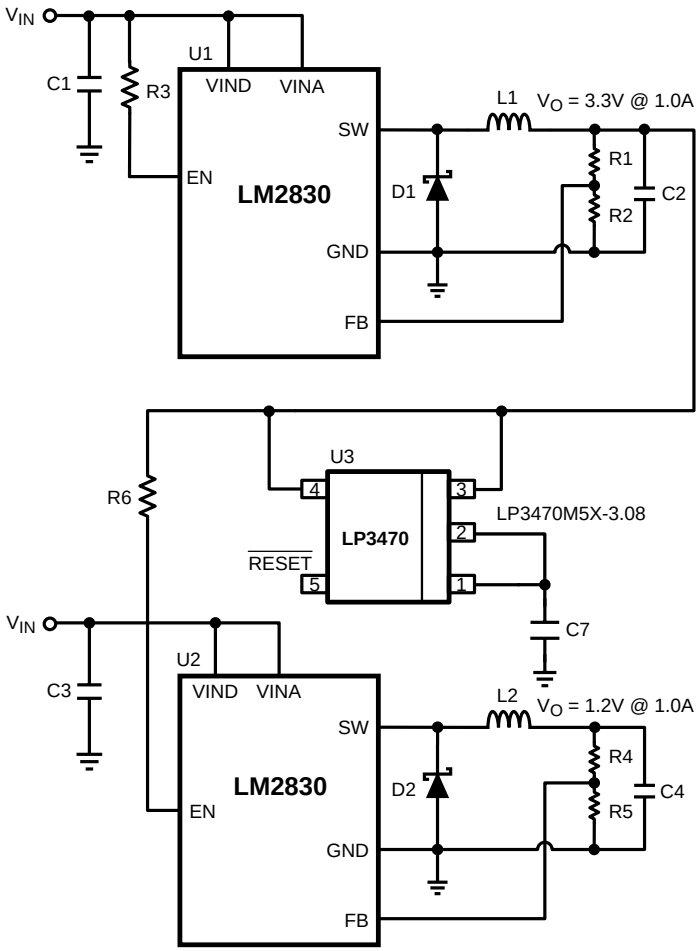


Figure 27. LM2830X (1.6 MHz): Vin = 5 V, Vo = 1.2 V at 1.0 A and 3.3 V at 1.0-A Schematic

Table 7. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1, U2	1.0-A Buck Regulator	TI	LM2830X
U3	Power on Reset	TI	LP3470M5X-3.08
C1, C3 Input Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C2, C4 Output Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C7	Trr delay capacitor	TDK	
D1, D2 Catch Diode	0.3 V_f Schottky 1.5 A, 30 V_R	TOSHIBA	CRS08
L1, L2	3.3 µH, 1.3 A	Coilcraft	ME3220-332
R2, R4, R5	10.0 kΩ, 1%	Vishay	CRCW08051002F
R1, R6	45.3 kΩ, 1%	Vishay	CRCW08054532F
R3	100 kΩ, 1%	Vishay	CRCW08051003F

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8.2.7 LM2830X Buck Converter and Voltage Double Circuit With LDO Follower

Figure 28 shows an example where the LM2830 device is used to provide regulated output voltage (3.3 V) as well as input voltage for an LDO, effectively providing solution with two output voltages.

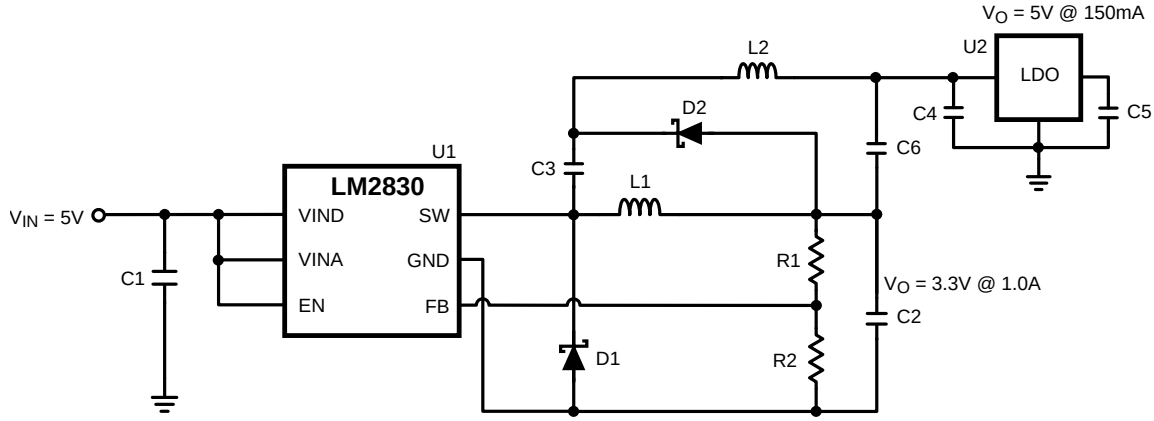


Figure 28. LM2830X (1.6 MHz): Vin = 5 V, Vo = 3.3 V at 1.0 A and LP2986-5.0 at 150-mA Schematic

Table 8. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	1.0-A Buck Regulator	TI	LM2830X
U2	200-mA LDO	TI	LP2986-5.0
C1, Input Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C2, Output Cap	22 µF, 6.3 V, X5R	TDK	C3216X5ROJ226M
C3 – C6	2.2 µF, 6.3 V, X5R	TDK	C1608X5R0J225M
D1, Catch Diode	0.3 V_f Schottky 1.5 A, 30 V_R	TOSHIBA	CRS08
D2	0.4 V_f Schottky 20 V_R, 500 mA	ON Semi	MBR0520
L2	10 µH, 800 mA	CoilCraft	ME3220-103
L1	3.3 µH, 2.2 A	TDK	VLCF5020T-3R3N2R0-1
R2	45.3 kΩ, 1%	Vishay	CRCW08054532F
R1	10.0 kΩ, 1%	Vishay	CRCW08051002F

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9 Power Supply Recommendations

The LM2830 is designed to operate from an input voltage supply range between 3.0 V and 5.5 V. This input supply should be able to withstand the maximum input current and maintain a voltage above 3.0 V. If the input supply is located farther away (more than a few inches) from the LM2830, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor and the catch diode D1. These ground ends should be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. Next in importance is the location of the GND connection of the output capacitor, which should be near the GND connections of CIN and D1.

There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island.

The FB pin is a high-impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of R1 placed as close as possible to the GND of the IC. The V_{OUT} trace to R2 should be routed away from the inductor and any other traces that are switching.

High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components should also be placed as close as possible to the IC. See Application Note AN-1229 SNVA054 for further considerations and the LM2830 demo board as an example of a four-layer layout.

10.2 Layout Example

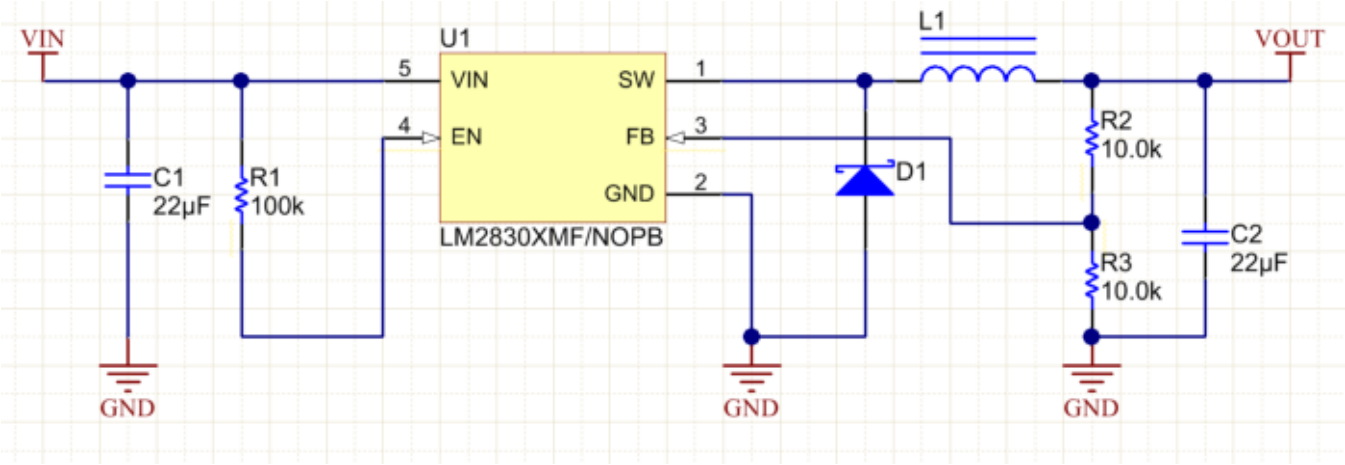


Figure 29. Example Schematic

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Layout Example (continued)

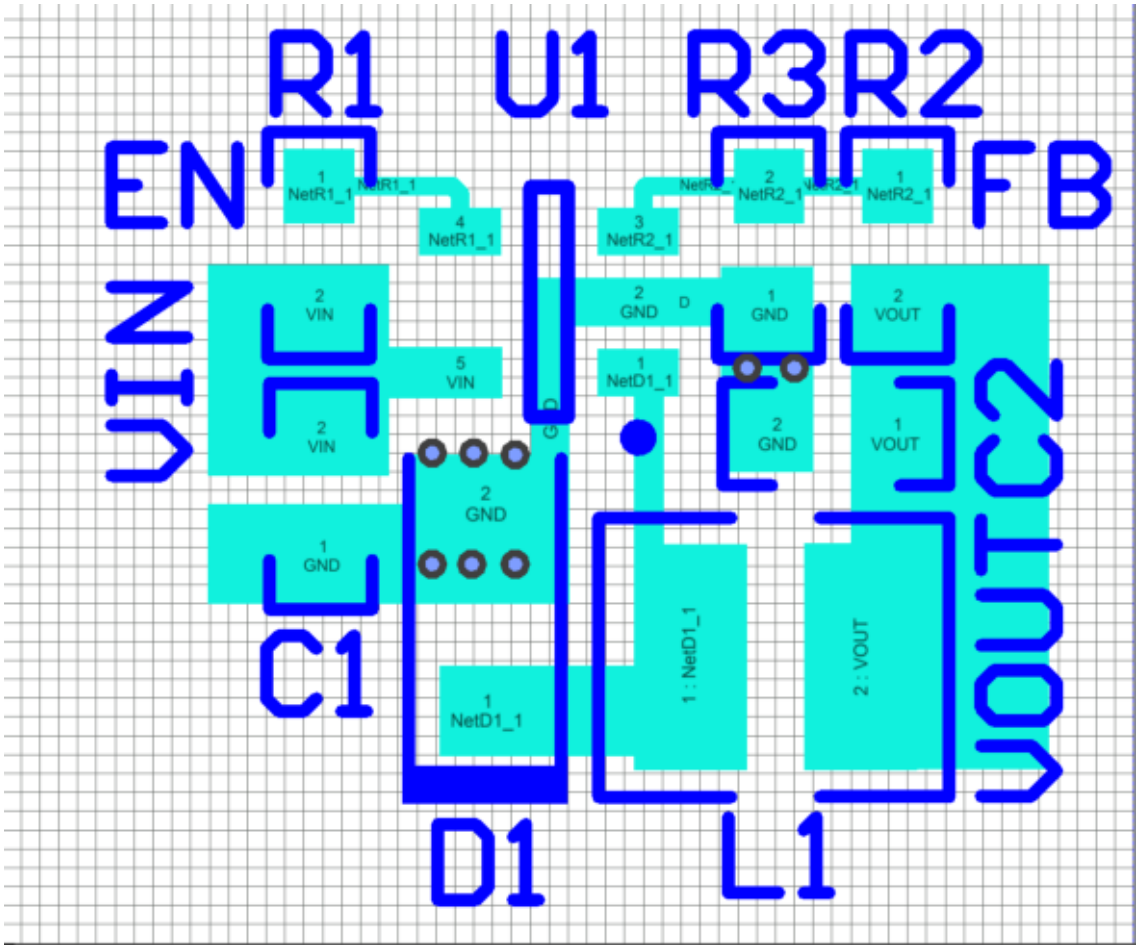


Figure 30. PCB Layout Example

10.3 Thermal Considerations

The PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB can greatly effect $R_{\theta JA}$. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Four to six thermal vias should be placed under the exposed pad to the ground plane if the WSON package is used.

Thermal impedance also depends on the thermal properties of the application operating conditions (Vin, Vo, Io etc), and the surrounding circuitry.

Silicon Junction Temperature Determination Method 1:

To accurately measure the silicon temperature for a given application, two methods can be used. The first method requires the user to know the thermal impedance of the silicon junction to top case temperature.

Some clarification needs to be made before we go any further.

$R_{\theta JC}$ is the thermal impedance from all six sides of an IC package to silicon junction.

$R_{\Phi JC}$ is the thermal impedance from top case to the silicon junction.

In this data sheet we will use $R_{\Phi JC}$ so that it allows the user to measure top case temperature with a small thermocouple attached to the top case.

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Thermal Considerations (continued)

$R_{\Phi JC}$ is approximately 30°C/Watt for the 6-pin WSON package with the exposed pad. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature, which can be empirically measured on the bench we have:

$$R_{\Phi JC} = \frac{T_J - T_C}{\text{Power}} \tag{30}$$

Therefore:

$$T_j = (R_{\Phi JC} \times P_{LOSS}) + T_C \tag{31}$$

From the previous example:

$$T_j = (R_{\Phi JC} \times P_{INTERNAL}) + T_C \tag{32}$$

$$T_j = 30°C/W \times 0.189W + T_C \tag{33}$$

The second method can give a very accurate silicon junction temperature.

The first step is to determine $R_{\theta JA}$ of the application. The LM2830 device has over-temperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of about 15°C. Once the silicon temperature has decreased to approximately 150°C, the device will start to switch again. Knowing this, the $R_{\theta JA}$ for any application can be characterized during the early stages of the design one may calculate the $R_{\theta JA}$ by placing the PCB circuit into a thermal chamber. Raise the ambient temperature in the given working application until the circuit enters thermal shutdown. If the SW-pin is monitored, it will be obvious when the internal PFET stops switching, indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above methods, the junction temperature, and the ambient temperature $R_{\theta JA}$ can be determined.

$$R_{\theta JA} = \frac{165° - Ta}{P_{INTERNAL}} \tag{34}$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

An example of calculating $R_{\theta JA}$ for an application using the Texas Instruments LM2830 WSON demonstration board is shown below.

The four layer PCB is constructed using FR4 with ½ oz copper traces. The copper ground plane is on the bottom layer. The ground plane is accessed by two vias. The board measures 3-cm × 3-cm. It was placed in an oven with no forced airflow. The ambient temperature was raised to 144°C, and at that temperature, the device went into thermal shutdown.

From the previous example:

$$P_{INTERNAL} = 189mW \tag{35}$$

$$R_{\theta JA} = \frac{165^oC - 144^oC}{189\ mW} = 111^o\ C/W \tag{36}$$

If the junction temperature was to be kept below 125°C, then the ambient temperature could not go above 109°C

$$T_j - (R_{\theta JA} \times P_{LOSS}) = T_A \tag{37}$$

$$125°C - (111°C/W \times 189mW) = 104°C \tag{38}$$

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10.4 WSON Package

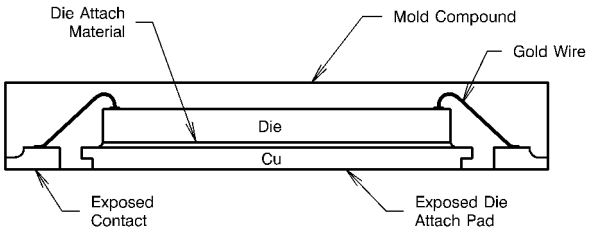


Figure 31. Internal WSON Connection

For certain high-power applications, the PCB land may be modified to a "dog bone" shape (see Figure 32). By increasing the size of ground plane, and adding thermal vias, the $R_{\theta JA}$ for the application can be reduced.

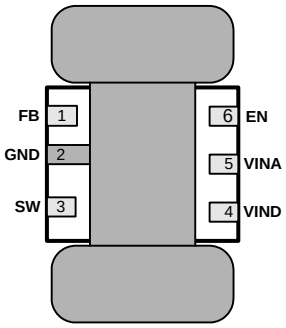


Figure 32. 6-Lead WSON PCB "Dog Bone" Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Thermal Definitions

T_J Chip junction temperature

T_A Ambient temperature

$R_{\theta JC}$ Thermal resistance from chip junction to device case

$R_{\theta JA}$ Thermal resistance from chip junction to ambient air

Heat in the LM2830 device due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs. conductor).

Heat Transfer goes as:

Silicon → package → lead frame → PCB

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_\theta = \frac{\Delta T}{\text{Power}} \tag{39}$$

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{\text{Power}} \tag{40}$$

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2830	Click here	Click here	Click here	Click here	Click here
LM2830-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2830XMF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SKTB
LM2830XMF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SKTB
LM2830XMFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SKTB
LM2830XMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SKTB
LM2830XQMF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUFB
LM2830XQMF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUFB
LM2830XQMFE/NOPB	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUFB
LM2830XQMFE/NOPB.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUFB
LM2830XQMFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUFB
LM2830XQMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUFB
LM2830ZMF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SKXB
LM2830ZMF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SKXB
LM2830ZQMF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SURB
LM2830ZQMF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SURB
LM2830ZQMFE/NOPB	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SURB
LM2830ZQMFE/NOPB.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SURB
LM2830ZQMFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SURB
LM2830ZQMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SURB
LM2830ZSD/NOPB	Active	Production	WSON (NGG) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L192B
LM2830ZSD/NOPB.A	Active	Production	WSON (NGG) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L192B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM2830, LM2830-Q1 :

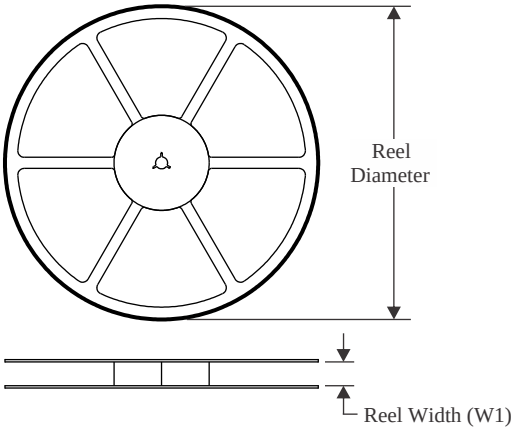
- Catalog : LM2830
- Automotive : LM2830-Q1

NOTE: Qualified Version Definitions:

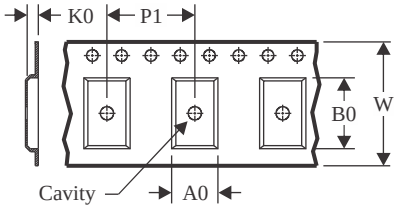
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

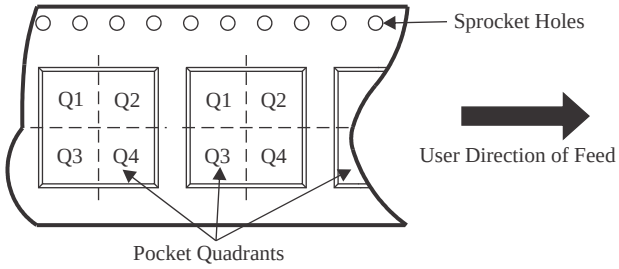


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

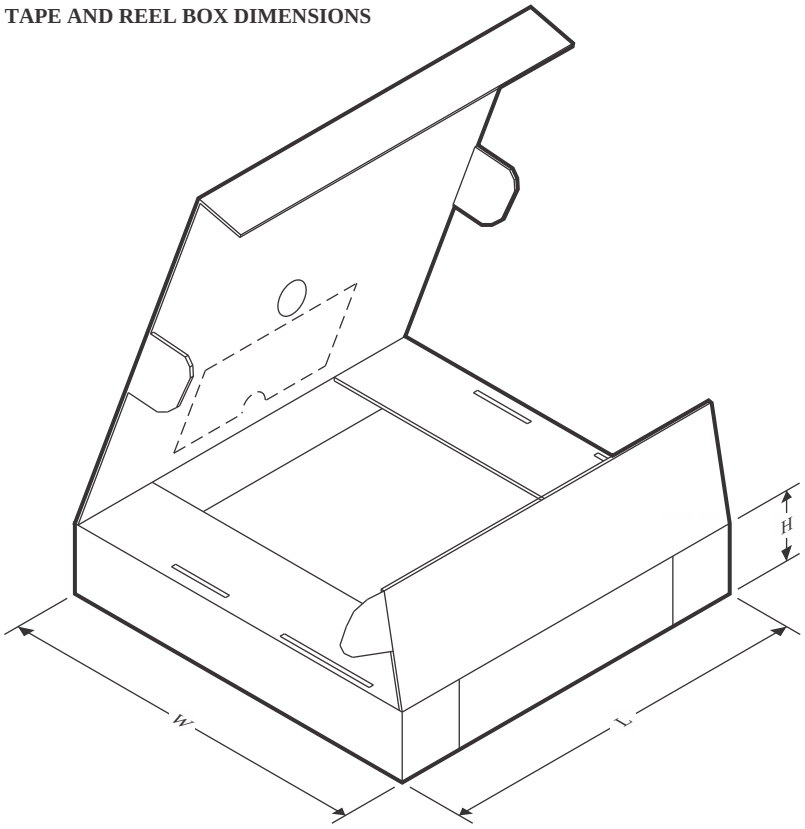
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2830XMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830XMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830XQMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830XQMFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830XQMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830ZMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830ZQMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830ZQMFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830ZQMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2830ZSD/NOPB	WSON	NGG	6	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1

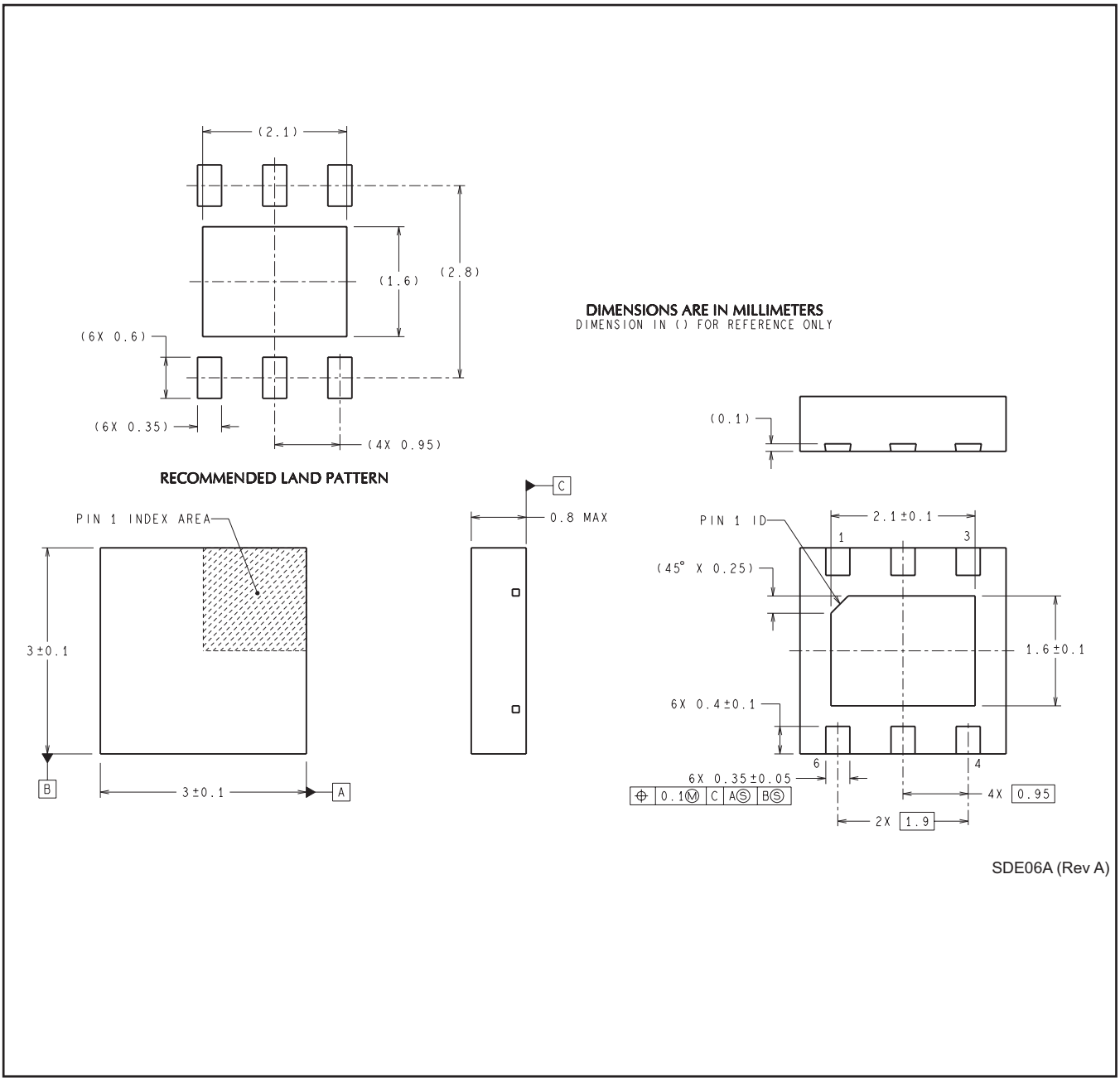
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2830XMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2830XMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2830XQMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2830XQMFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LM2830XQMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2830ZMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2830ZQMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2830ZQMFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LM2830ZQMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2830ZSD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0

NGG0006A



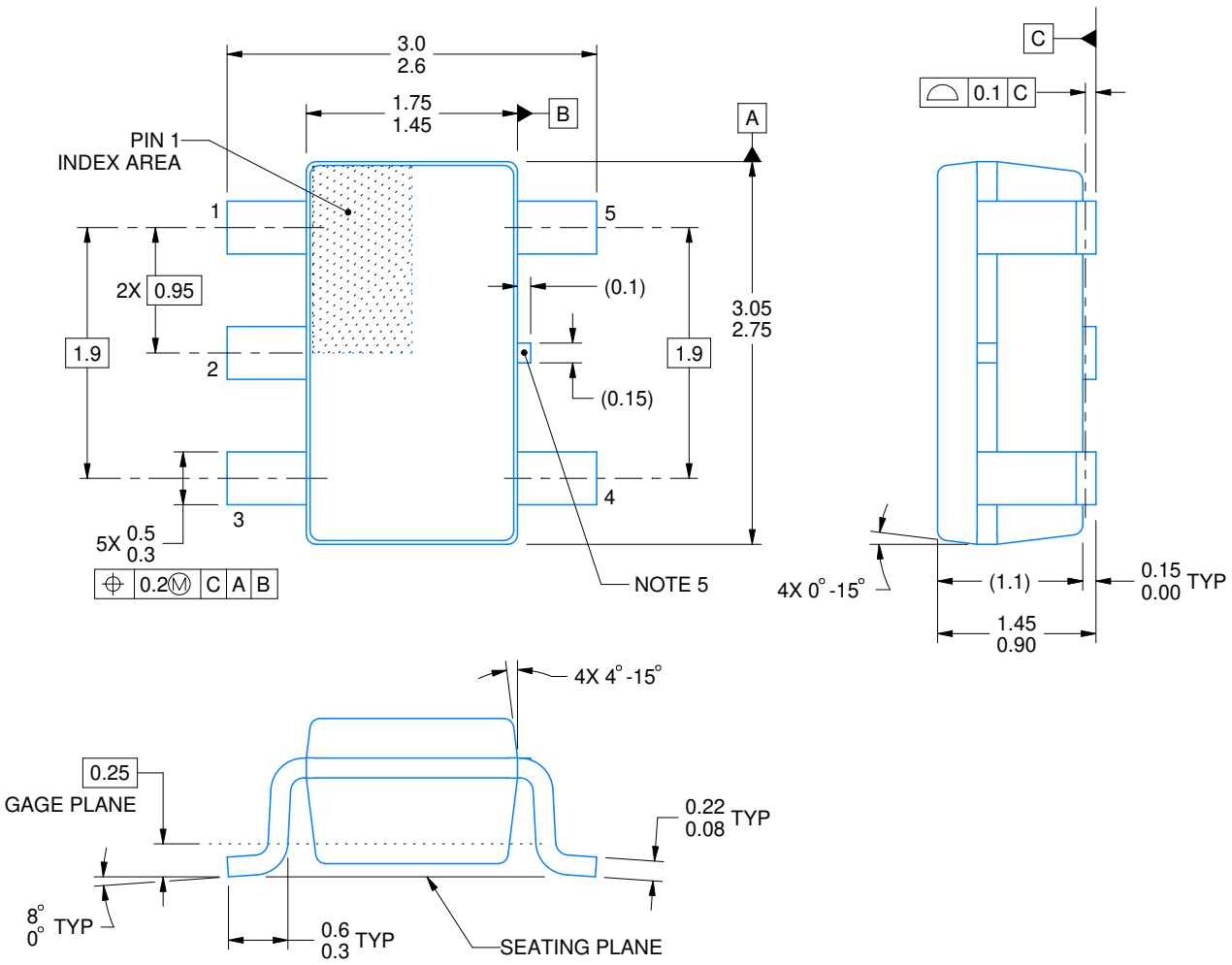
SDE06A (Rev A)

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

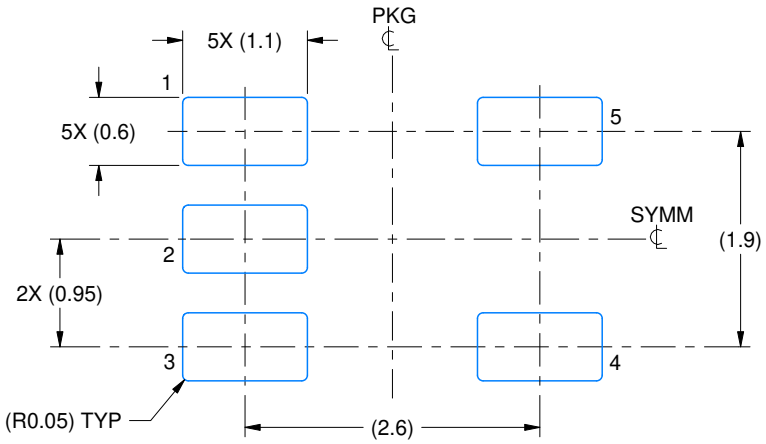
SMALL OUTLINE TRANSISTOR



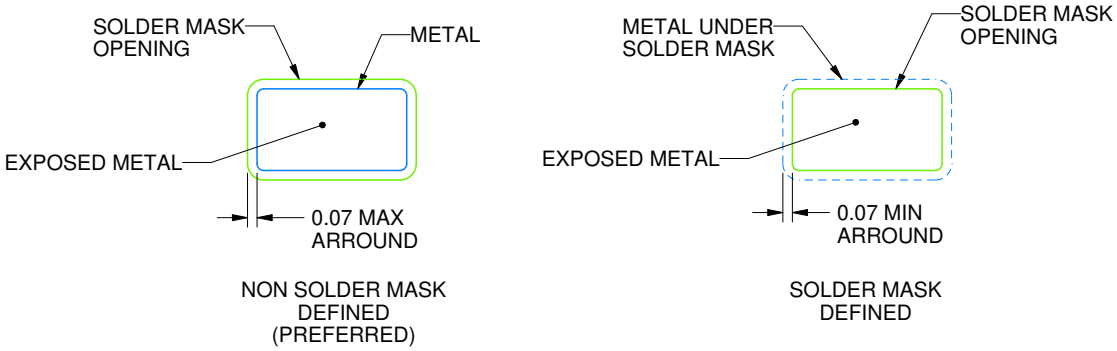
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

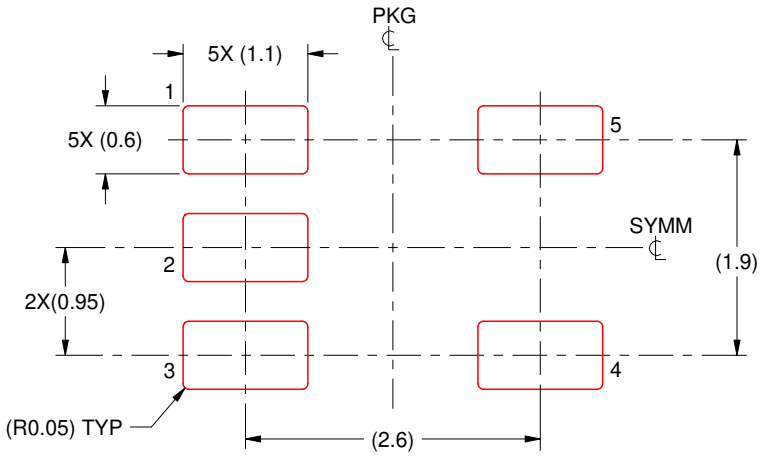


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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