LM3102 Synchronous 1-MHz, 2.5-A Step-Down Voltage Regulator

1 Features

- Low Component Count and Small Solution Size
- Stable With Ceramic and Other Low-ESR Capacitors
- No Loop Compensation Required
- High Efficiency at a Light Load by DCM Operation
- Prebias Start-Up
- Ultra-Fast Transient Response
- Programmable Soft-Start
- Programmable Switching Frequency up to 1 MHz
- Valley Current Limit
- Output Overvoltage Protection
- Precision Internal Reference for an Adjustable Output Voltage Down to 0.8 V
- Thermal Shutdown
- Key Specifications
  - Input Voltage Range 4.5 V to 42 V
  - 2.5-A Output Current
  - 0.8 V, ±1.5% Reference
  - Integrated Dual N-Channel Main and Synchronous MOSFETs
  - Thermally Enhanced HTSSOP-20 Package

2 Applications

- 5-VDC, 12-VDC, 24-VDC, 12-VAC, and 24-VAC Systems
- Embedded Systems and Industrial Control
- Automotive Telematics and Body Electronics
- Point of Load Regulators
- Storage Systems
- Broadband Infrastructure
- Direct Conversion from 2-, 3-, and 4-Cell Lithium Batteries Systems

3 Description

The LM3102 Synchronously Rectified Buck Converter features all required functions to implement a highly efficient and cost-effective buck regulator. The device can supply 2.5 A to loads with an output voltage as low as 0.8 V. Dual N-channel synchronous MOSFET switches allow a low component count, thus reducing complexity and minimizing board size.

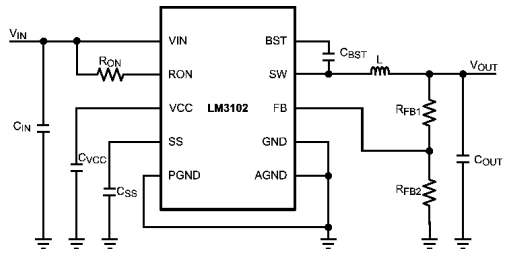
Different from most other COT regulators, the LM3102 does not rely on output capacitor ESR for stability, and is designed to work exceptionally well with ceramic and other very low-ESR output capacitors. The device requires no loop compensation, results in a fast load transient response and simple circuit implementation. The operating frequency remains nearly constant with line variations due to the inverse relationship between the input voltage and the ON-time. The operating frequency can be externally programmed up to 1 MHz. Protection features include V_{CC} undervoltage lockout (UVLO), output overvoltage protection, thermal shutdown, and gate drive UVLO. The LM3102 is available in the thermally enhanced HTSSOP-20 package, and LM3102 is also available in a DSBGA low-profile chip-scale package with reduced output current.

Device Information[1]

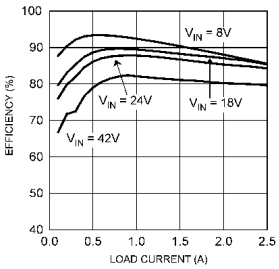
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3102	DSBGA (28)	3.645 mm × 2.45 mm
LM3102	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Load Current (V_{OUT} = 3.3 V)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

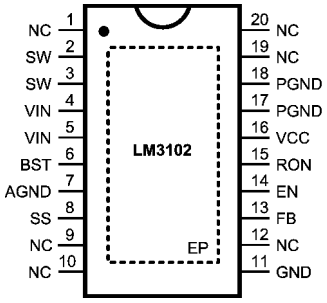
Changes from Revision H (June 2015) to Revision I	Page
• Changed LM3102 and LM3102-Q1 to Stand Alone data sheets	1

Changes from Revision G (January 2012) to Revision H	Page
• Updated the LM3102Q part number to LM3102-Q1	1
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

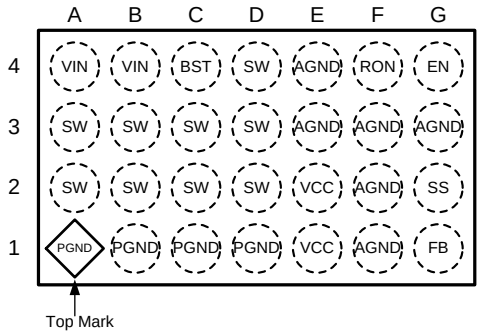
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5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP
Top View



YPA Package
28–Ball DSBGA
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	PIN NO.	BALL NO.		
N/C	1	—	—	No Connection
	9			
	10			
	12			
	19			
	20			
SW	2	A2	Power	Switching Node
		A3		
		B2		
		B3		
		C2		
	3	C3		
		D2		
		D3		
		D4		
VIN	4	A4	Power	Input supply voltage
	5	B4		
BST	6	C4	Power	Connection for bootstrap capacitor
AGND	7	E3	Ground	Analog Ground
		E4		
		F1		
		F2		
		F3		
		G3		
SS	8	G2	Analog	Soft-Start
GND	11	—	Ground	Ground
FB	13	G1	Analog	Feedback
EN	14	G4	Analog	Enable
RON	15	F4	Analog	ON-time Control
VCC	16	E1	Power	Start-up regulator Output
		E2		

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Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	PIN NO.	BALL NO.		
PGND	17	A1	Ground	Power Ground
		B1		
	18	C1		
		D1		
EP	EP	—	Ground	Exposed Pad

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN, RON to AGND	–0.3	43.5	V
SW to AGND	–0.3	43.5	V
SW to AGND (Transient)		–2 (< 100 ns)	V
VIN to SW	–0.3	43.5	V
BST to SW	–0.3	7	V
All Other Inputs to AGND	–0.3	7	V
Junction Temperature, T_J		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage Range (VIN)	4.5	42	V
Junction Temperature Range (T_J)	−40	125	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Ratings* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		LM3102 PWP (HTSSOP) 20 PINS	LM3102 YPA (DSBGA) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30	50	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.5	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Specifications with standard type are for T_J = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18 V, V_{OUT} = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
START-UP REGULATOR, V_{CC}							
V_{CC}	V_{CC} output voltage	C_{CC} = 680 nF, no load			6		V
			over the full Operating Junction Temperature (T_J) range	5		7.2	
$V_{IN} - V_{CC}$	$V_{IN} - V_{CC}$ dropout voltage	I_{CC} = 2 mA			50		mV
			over the full Operating Junction Temperature (T_J) range			200	
		I_{CC} = 20 mA			350		
			over the full Operating Junction Temperature (T_J) range			570	
I_{VCCL}	V_{CC} current limit(1)	V_{CC} = 0 V			65		mA
			over the full Operating Junction Temperature (T_J) range	40			
$V_{CC-UVLO}$	V_{CC} undervoltage lockout threshold (UVLO)	V_{IN} increasing			3.75		V
			over the full Operating Junction Temperature (T_J) range	3.6		3.9	
$V_{CC-UVLO-HYS}$	V_{CC} UVLO hysteresis	V_{IN} decreasing – HTSSOP package			130		mV
$V_{CC-UVLO-HYS}$	V_{CC} UVLO hysteresis	V_{IN} decreasing – DSBGA package			150		mV
$t_{VCC-UVLO-D}$	V_{CC} UVLO filter delay				3		µs
I_{IN}	I_{IN} operating current	No switching, V_{FB} = 1 V			0.7		mA
			over the full Operating Junction Temperature (T_J) range			1	
I_{IN-SD}	I_{IN} operating current, Device shutdown	V_{EN} = 0 V			25		µA
			over the full Operating Junction Temperature (T_J) range			40	
SWITCHING CHARACTERISTICS							
$R_{DS-UP-ON}$	Main MOSFET $R_{DS(on)}$				0.18		Ω
		over the full Operating Junction Temperature (T_J) range				0.375	
$R_{DS-DN-ON}$	Syn. MOSFET $R_{DS(on)}$				0.11		Ω
		over the full Operating Junction Temperature (T_J) range				0.225	
V_{G-UVLO}	Gate drive voltage UVLO	V_{BST} - V_{SW} increasing			3.3		V
			over the full Operating Junction Temperature (T_J) range			4	
SOFT-START							
I_{SS}	SS pin source current	V_{SS} = 0.5 V			8		µA
			over the full Operating Junction Temperature (T_J) range	6		10	

(1) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

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Electrical Characteristics (continued)

Specifications with standard type are for T_J = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18 V, V_{OUT} = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT LIMIT							
I_{CL}	Syn. MOSFET current limit threshold	LM3102			2.7		A
I_{CL}	Syn. MOSFET current limit threshold	LM3102TLX–1			1.5		A
ON/OFF TIMER							
t_{on}	ON timer pulse width	V_{IN} = 10 V, R_{ON} = 100 kΩ			1.38		µs
		V_{IN} = 30 V, R_{ON} = 100 kΩ			0.47		
t_{on-MIN}	ON timer minimum pulse width				150		ns
t_{off}	OFF timer pulse width				260		ns
ENABLE INPUT							
V_{EN}	EN Pin input threshold	V_{EN} rising			1.18		V
			over the full Operating Junction Temperature (T_J) range	1.13		1.23	
V_{EN-HYS}	Enable threshold hysteresis	V_{EN} falling			90		mV
REGULATION AND OVERVOLTAGE COMPARATOR							
V_{FB}	In-regulation feedback voltage	V_{SS} ≥ 0.8 V T_J = −40°C to +125°C			0.8		V
			over the full Operating Junction Temperature (T_J) range	0.784		0.816	
		V_{SS} ≥ 0.8 V T_J = 0°C to +125°C	over the full Operating Junction Temperature (T_J) range	0.788		0.812	
V_{FB-OV}	Feedback overvoltage threshold				0.92		V
		over the full Operating Junction Temperature (T_J) range		0.888		0.945	
I_{FB}					5		nA
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown temperature	T_J rising			165		°C
T_{SD-HYS}	Thermal shutdown temperature hysteresis	T_J falling			20		°C

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6.6 Typical Characteristics

All curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V shown in this data sheet. T_A = 25°C, unless otherwise specified.

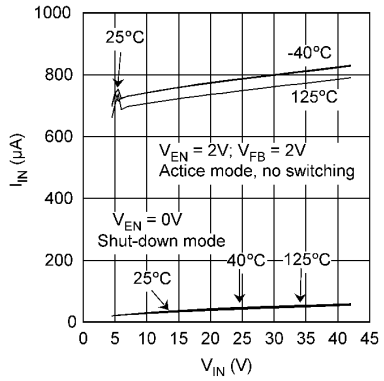


Figure 1. Quiescent Current, I_{IN} vs V_{IN}

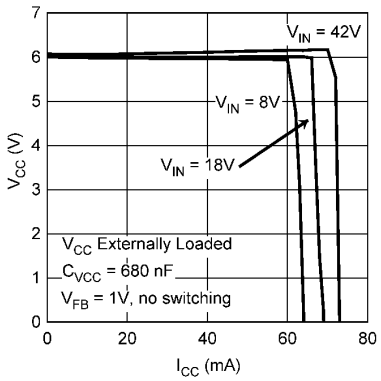


Figure 2. V_{CC} vs I_{CC}

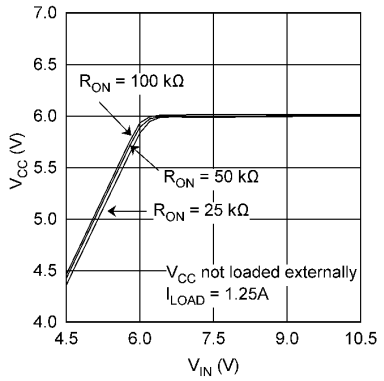


Figure 3. V_{CC} vs V_{IN}

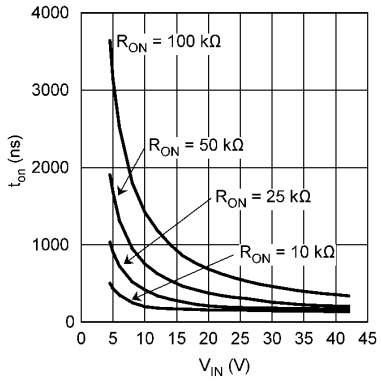


Figure 4. t_{on} vs V_{IN}

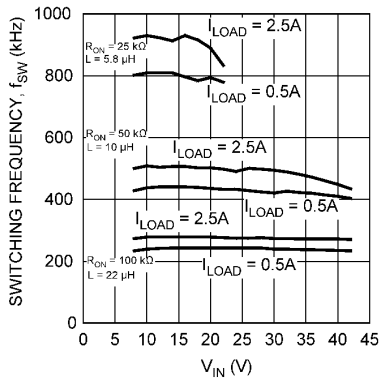


Figure 5. Switching Frequency, f_{SW} vs V_{IN}

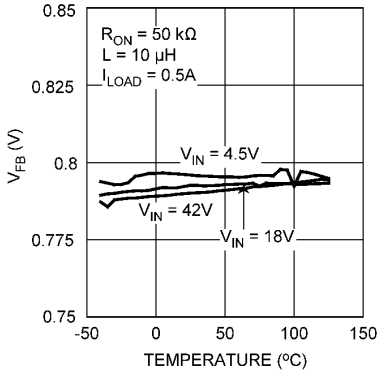


Figure 6. V_{FB} vs Temperature

Typical Characteristics (continued)

All curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V shown in this data sheet. T_A = 25°C, unless otherwise specified.

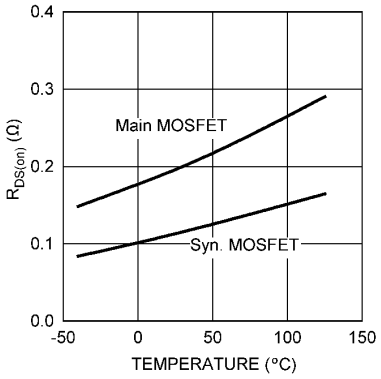


Figure 7. $R_{DS(on)}$ vs Temperature

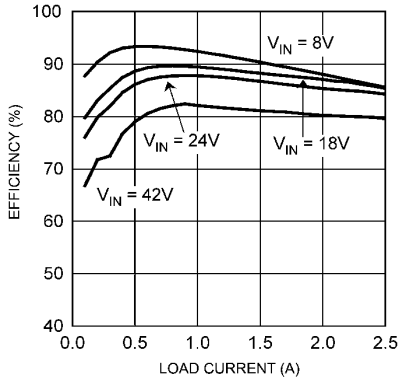


Figure 8. Efficiency vs Load Current (V_{OUT} = 3.3 V)

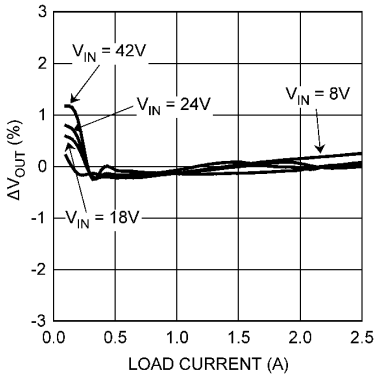


Figure 9. V_{OUT} Regulation vs Load Current (V_{OUT} = 3.3 V)

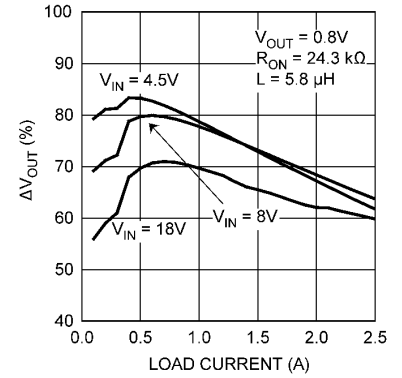


Figure 10. Efficiency vs Load Current (V_{OUT} = 0.8 V)

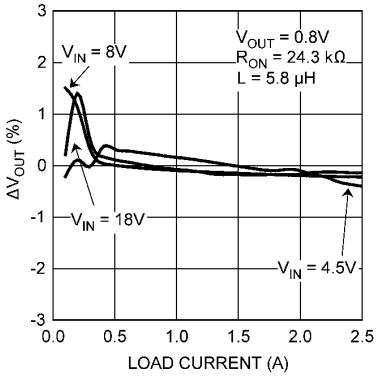


Figure 11. V_{OUT} Regulation vs Load Current (V_{OUT} = 0.8 V)

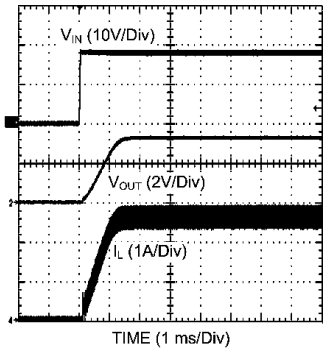


Figure 12. Power Up (V_{OUT} = 3.3 V, 2.5 A Loaded)

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Typical Characteristics (continued)

All curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V shown in this data sheet. T_A = 25°C, unless otherwise specified.

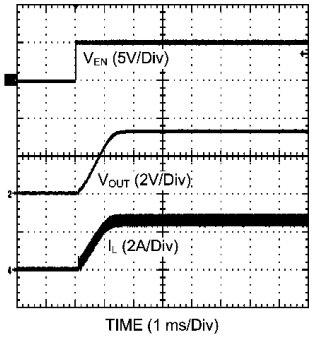


Figure 13. Enable Transient (V_{OUT} = 3.3 V, 2.5 A Loaded)

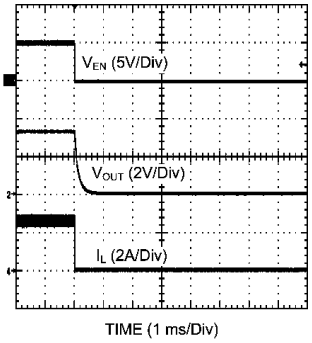


Figure 14. Shutdown Transient (V_{OUT} = 3.3 V, 2.5 A Loaded)

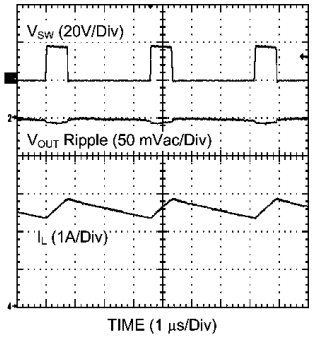


Figure 15. Continuous Mode Operation (V_{OUT} = 3.3 V, 2.5 A Loaded)

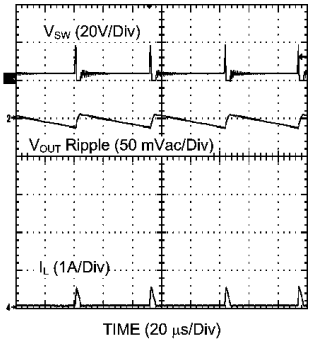


Figure 16. Discontinuous Mode Operation (V_{OUT} = 3.3 V, 0.025 A Loaded)

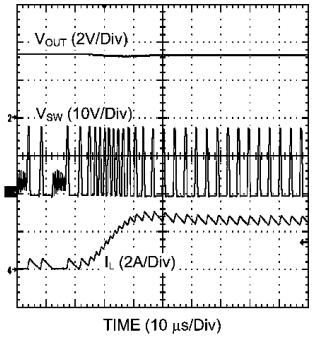


Figure 17. DCM to CCM Transition (V_{OUT} = 3.3 V, 0.15-A - 2.5-A Load)

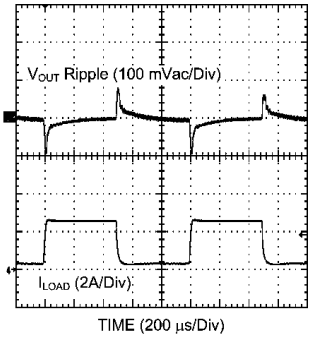


Figure 18. Load Transient (V_{OUT} = 3.3 V, 0.25-A - 2.5-A Load, Current Slew Rate: 2.5 A/µs)

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Typical Characteristics (continued)

All curves are taken at V_{IN} = 18 V with the configuration in the typical application circuit for V_{OUT} = 3.3 V shown in this data sheet. T_A = 25°C, unless otherwise specified.

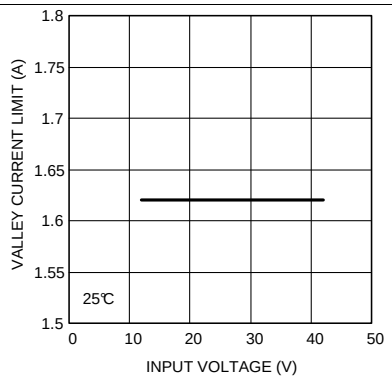


Figure 19. DSBGA Valley Current Limit V_{OUT} = 5 V at 25°C

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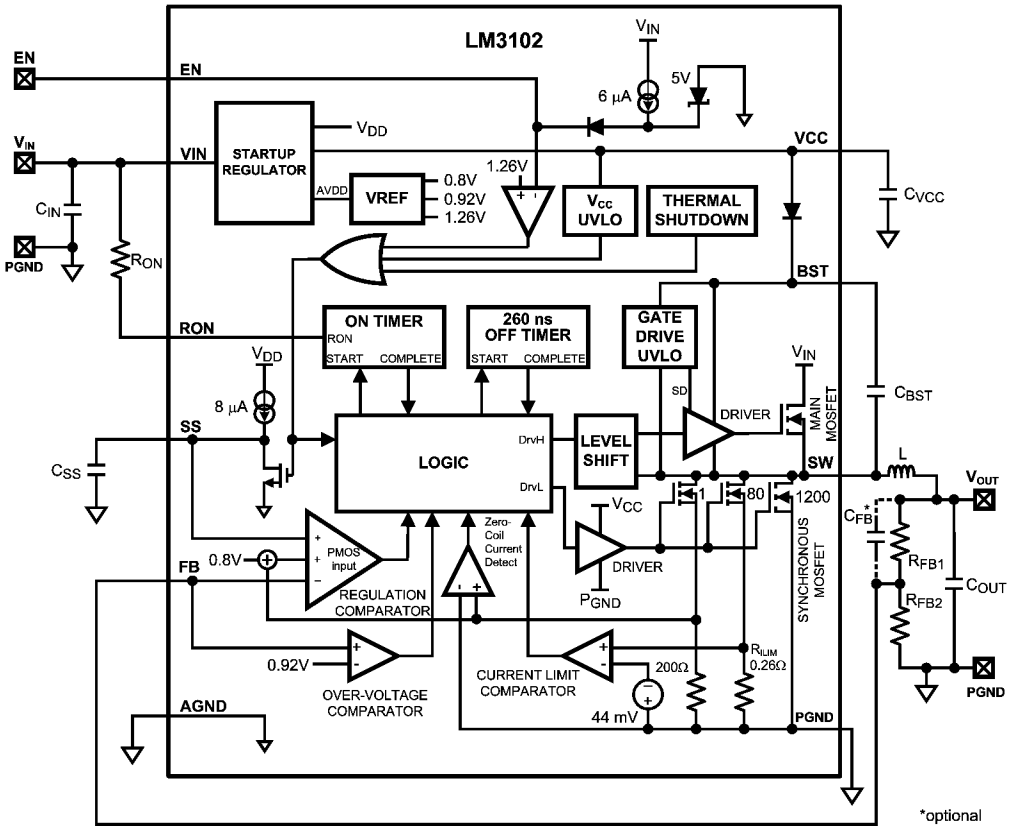
7 Detailed Description

7.1 Overview

The LM3102 Step-Down Switching Regulator features all required functions to implement a cost-effective, efficient buck power converter capable of supplying 2.5 A to a load. It contains Dual N-channel main and synchronous MOSFETs. The Constant ON-Time (COT) regulation scheme requires no loop compensation, results in fast load transient response and simple circuit implementation. The regulator can function properly even with an all ceramic output capacitor network, and does not rely on the ESR of the output capacitor for stability. The operating frequency remains constant with line variations due to the inverse relationship between the input voltage and the ON-time. The valley current limit detection circuit, with the limit set internally at 2.7 A, inhibits the main MOSFET until the inductor current level subsides.

The LM3102 can be applied in numerous applications and can operate efficiently for inputs as high as 42 V. Protection features include output overvoltage protection, thermal shutdown, V_{CC} UVLO, gate drive UVLO. The LM3102 is available in the thermally enhanced HTSSOP-20 package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 COT Control Circuit Overview

COT control is based on a comparator and a one-shot ON-timer, with the output voltage feedback (feeding to the FB pin) compared with an internal reference of 0.8 V. If the voltage of the FB pin is below the reference, the main MOSFET is turned on for a fixed ON-time determined by a programming resistor R_{ON} and the input voltage V_{IN}, upon which the ON-time varies inversely. Following the ON-time, the main MOSFET remains off for a minimum of 260 ns. Then, if the voltage of the FB pin is below the reference, the main MOSFET is turned on again for another ON-time period. The switching will continue to achieve regulation.

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Feature Description (continued)

The regulator will operate in the discontinuous conduction mode (DCM) at a light load, and the continuous conduction mode (CCM) with a heavy load. In the DCM, the current through the inductor starts at zero and ramps up to a peak during the ON-time, and then ramps back to zero before the end of the OFF-time. It remains zero and the load current is supplied entirely by the output capacitor. The next ON-time period starts when the voltage at the FB pin falls below the internal reference. The operating frequency in the DCM is lower and varies larger with the load current as compared with the CCM. Conversion efficiency is maintained because conduction loss and switching loss are reduced with the reduction in the load and the switching frequency, respectively. The operating frequency in the DCM can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT} (V_{IN} - 1) \times L \times 1.18 \times 10^{20} \times I_{OUT}}{(V_{IN} - V_{OUT}) \times R_{ON}^2} \quad (1)$$

In the continuous conduction mode (CCM), the current flows through the inductor in the entire switching cycle, and never reaches zero during the OFF-time. The operating frequency remains relatively constant with load and line variations. The CCM operating frequency can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT}}{1.3 \times 10^{-10} \times R_{ON}} \quad (2)$$

The output voltage is set by two external resistors R_{FB1} and R_{FB2}. The regulated output voltage is

$$V_{OUT} = 0.8V \times (R_{FB1} + R_{FB2})/R_{FB2} \quad (3)$$

7.3.2 Start-Up Regulator (V_{CC})

A startup regulator is integrated within the LM3102. The input pin VIN can be connected directly to a line voltage up to 42 V. The V_{CC} output regulates at 6 V, and is current limited to 65 mA. Upon power up, the regulator sources current into an external capacitor C_{VCC}, which is connected to the VCC pin. For stability, C_{VCC} must be at least 680 nF. When the voltage on the VCC pin is higher than the UVLO threshold of 3.75 V, the main MOSFET is enabled and the SS pin is released to allow the soft-start capacitor C_{SS} to charge.

The minimum input voltage is determined by the dropout voltage of the regulator and the V_{CC} UVLO falling threshold (≅3.7 V). If V_{IN} is less than ≅4.0 V, the regulator shuts off and V_{CC} goes to zero.

7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to a 0.8-V internal reference. In normal operation (the output voltage is regulated), an ON-time period is initiated when the voltage at the FB pin falls below 0.8 V. The main MOSFET stays on for the ON-time, causing the output voltage and consequently the voltage of the FB pin to rise above 0.8 V. After the ON-time period, the main MOSFET stays off until the voltage of the FB pin falls below 0.8 V again. Bias current at the FB pin is nominally 5 nA.

7.3.4 Zero Coil Current Detect

The current of the synchronous MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operation, which improves the efficiency at a light load.

7.3.5 Overvoltage Comparator

The voltage at the FB pin is compared to a 0.92-V internal reference. If the voltage rises above 0.92 V, the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage or the output load changes suddenly. Once the OVP is activated, the main MOSFET remains off until the voltage at the FB pin falls below 0.92 V. The synchronous MOSFET will stay on to discharge the inductor until the inductor current reduces to zero, and then switch off.

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Feature Description (continued)

7.3.6 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the re-circulating current through the synchronous MOSFET. Referring to the *Functional Block Diagram*, when the main MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 2.7 A, the current limit comparator toggles, and as a result disabling the start of the next ON-time period. The next switching cycle starts when the re-circulating current falls back below 2.7 A (and the voltage at the FB pin is below 0.8V). The inductor current is monitored during the ON-time of the synchronous MOSFET. As long as the inductor current exceeds 2.7 A, the main MOSFET will remain inhibited to achieve current limit. The operating frequency is lower during current limit due to a longer OFF-time.

Figure 20 illustrates an inductor current waveform. On average, the output current I_{OUT} is the same as the inductor current I_L, which is the average of the rippled inductor current. In case of current limit (the current limit portion of Figure 20), the next ON-time will not initiate until that the current drops below 2.7 A (assume the voltage at the FB pin is lower than 0.8 V). During each ON-time the current ramps up an amount equal to:

$$I_{LR} = \frac{(V_{IN} - V_{OUT}) \times t_{on}}{L} \quad (4)$$

During current limit, the LM3102 operates in a constant current mode with an average output current $I_{OUT(CL)}$ equal to 2.7 A + I_{LR} / 2.

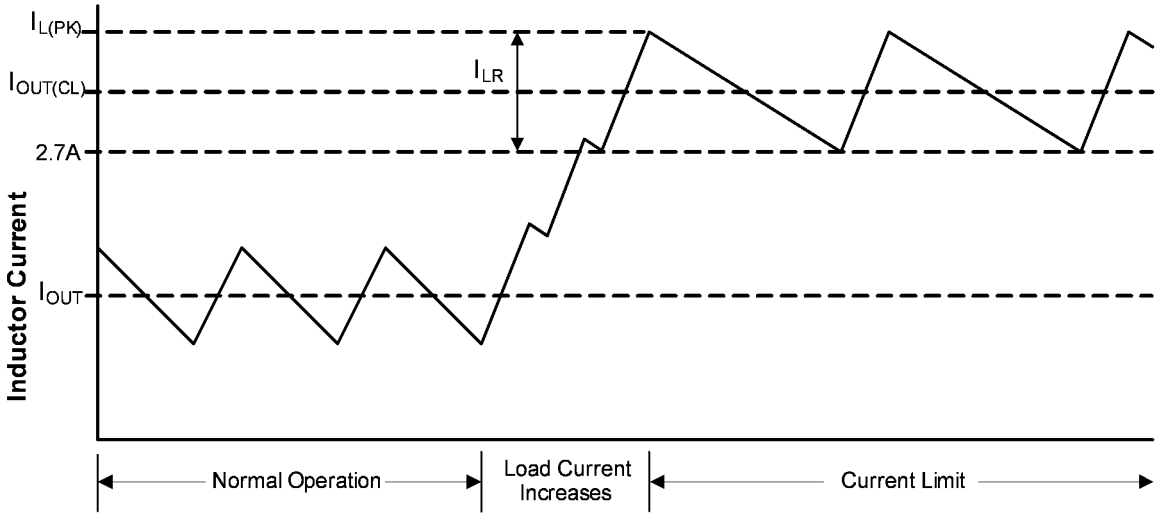


Figure 20. Inductor Current - Current Limit Operation

7.3.7 N-Channel MOSFET and Driver

The LM3102 integrates an N-channel main MOSFET and an associated floating high voltage main MOSFET gate driver. The gate drive circuit works in conjunction with an external bootstrap capacitor C_{BST} and an internal high voltage diode. C_{BST} connecting between the BST and SW pins powers the main MOSFET gate driver during the main MOSFET ON-time. During each OFF-time, the voltage of the SW pin falls to approximately –1 V, and C_{BST} charges from V_{CC} through the internal diode. The minimum OFF-time of 260 ns provides enough time for charging C_{BST} in each cycle.

7.3.8 Soft-Start

The soft-start feature allows the converter to gradually reach a steady-state operating point, thereby reducing startup stresses and current surges. Upon turnon, after V_{CC} reaches the undervoltage threshold, an 8-µA internal current source charges up an external capacitor C_{SS} connecting to the SS pin. The ramping voltage at the SS pin (and the non-inverting input of the regulation comparator as well) ramps up the output voltage V_{OUT} in a controlled manner.

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Feature Description (continued)

An internal switch grounds the SS pin if any of the following three cases happens: (i) V_{CC} is below the UVLO threshold; (ii) a thermal shutdown occurs; or (iii) the EN pin is grounded. Alternatively, the output voltage can be shut off by connecting the SS pin to ground using an external switch. Releasing the switch allows the SS pin to ramp up and the output voltage to return to normal. The shutdown configuration is shown in Figure 21.

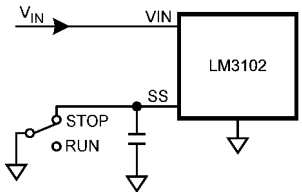


Figure 21. Alternate Shutdown Implementation

7.3.9 Thermal Protection

The junction temperature of the LM3102 should not exceed the maximum limit. Thermal protection is implemented by an internal Thermal Shutdown circuit, which activates (typically) at 165°C to make the controller enter a low power reset state by disabling the main MOSFET, disabling the ON-timer, and grounding the SS pin. Thermal protection helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C), the SS pin is released and normal operation resumes.

7.3.10 Thermal Derating

The LM3102 can supply 2.5 A below an ambient temperature of 100°C. Under worst-case operation, with either input voltage up to 42 V, operating frequency up to 1 MHz, or voltage of the RON pin below the absolute maximum of 7 V, the LM3102 can deliver a minimum of 1.9-A output current without thermal shutdown with a PCB ground plane copper area of 40 cm^2, 2 oz/Cu. Figure 22 shows a thermal derating curve for the minimum output current without thermal shutdown against ambient temperature up to 125°C. Obtaining 2.5-A output current is possible by increasing the PCB ground plane area, or reducing the input voltage or operating frequency.

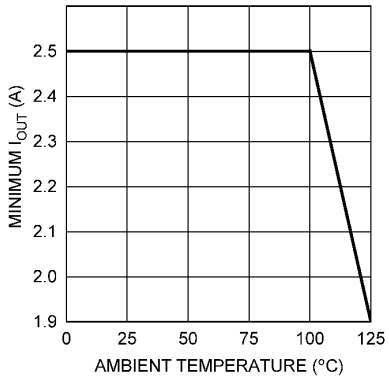


Figure 22. Thermal Derating Curve

7.4 Device Functional Modes

7.4.1 ON-Time Timer, Shutdown

The ON-time of the LM3102 main MOSFET is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{on} = \frac{1.3 \times 10^{-10} \times R_{ON}}{V_{IN}} \quad (5)$$

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Device Functional Modes (continued)

The inverse relationship of t_{on} and V_{IN} gives a nearly constant frequency as V_{IN} is varied. R_{ON} should be selected such that the ON-time at maximum V_{IN} is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for t_{on}. This limits the maximum operating frequency, which is governed by Equation 6:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \times 150\ ns} \quad (6)$$

The LM3102 can be remotely shutdown by pulling the voltage of the EN pin below 1 V. In this shutdown mode, the SS pin is internally grounded, the ON-timer is disabled, and bias currents are reduced. Releasing the EN pin allows normal operation to resume because the EN pin is internally pulled up.

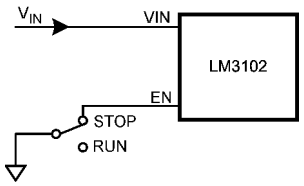


Figure 23. Shutdown Implementation

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3102 is a step-down DC-to-DC controller. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2.5 A. The following design procedure can be used to select components for the LM3102. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH® software uses iterative design procedure and accesses comprehensive databases of components. For more details, go to www.ti.com.

8.2 Typical Application

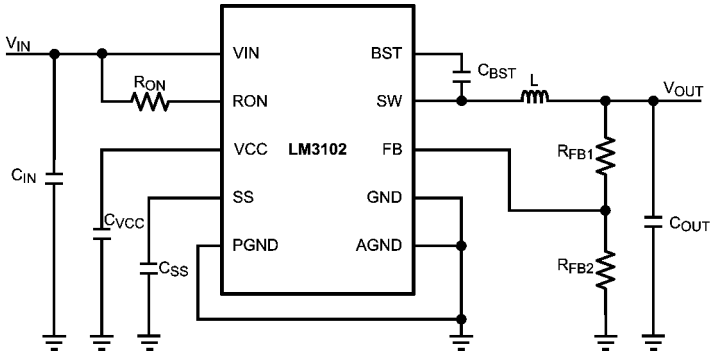


Figure 24. Typical Application Schematic

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = 8 V to 42 V
- V_{OUT} = 3.3 V
- I_{OUT} = 2.5 A

Refer to *Detailed Design Procedure* for more information on operational guidelines and limits.

8.2.2 Detailed Design Procedure

8.2.2.1 Design Steps for the LM3102 Application

The LM3102 is fully supported by WEBENCH which offers the following: component selection, electrical simulation, thermal simulation, as well as the build-it prototype board for a reduction in design time. The following list of steps can be used to manually design the LM3102 application.

1. Program V_O with divider resistor selection.
2. Program turnon time with soft-start capacitor selection.
3. Select C_O.
4. Select C_{IN}.
5. Set operating frequency with R_{ON}.
6. Determine thermal dissipation.
7. Lay out PCB for required thermal performance.

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Typical Application (continued)

8.2.2.2 External Components

The following guidelines can be used to select external components.

R_{FB1} and R_{FB2}: These resistors should be chosen from standard values in the range of 1.0 kΩ to 10 kΩ, satisfying the following ratio:

$$R_{FB1}/R_{FB2} = (V_{OUT}/0.8\ V) - 1 \quad (7)$$

For V_{OUT} = 0.8 V, the FB pin can be connected to the output directly with a pre-load resistor drawing more than 20 µA. It is because the converter operation needs a minimum inductor current ripple to maintain good regulation when no load is connected.

R_{ON}: Equation 2 can be used to select R_{ON} if a desired operating frequency is selected. But the minimum value of R_{ON} is determined by the minimum ON-time. It can be calculated as follows:

$$R_{ON} \geq \frac{V_{IN(MAX)} \times 150\ ns}{1.3 \times 10^{-10}} \quad (8)$$

If R_{ON} calculated from Equation 2 is smaller than the minimum value determined in Equation 8, a lower frequency should be selected to recalculate R_{ON} by Equation 2. Alternatively, $V_{IN(MAX)}$ can also be limited to keep the frequency unchanged. The relationship of $V_{IN(MAX)}$ and R_{ON} is shown in Figure 25.

On the other hand, the minimum OFF-time of 260 ns can limit the maximum duty ratio. Larger R_{ON} should be selected in any application requiring large duty ratio.

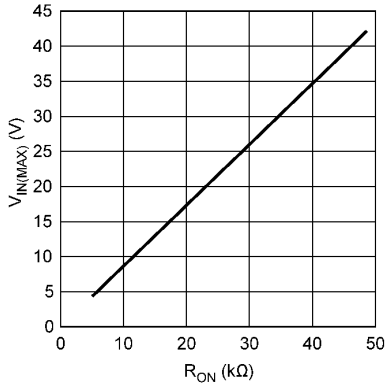


Figure 25. Maximum V_{IN} for Selected R_{ON}

L: The main parameter affected by the inductor is the amplitude of inductor current ripple (I_{LR}). Once I_{LR} is selected, L can be determined by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{LR} \times f_{SW} \times V_{IN}}$$

where

- V_{IN} is the maximum input voltage
- f_{SW} is determined from Equation 2

(9)

If the output current I_{OUT} is determined, by assuming that $I_{OUT} = I_L$, the higher and lower peak of I_{LR} can be determined. Beware that the higher peak of I_{LR} should not be larger than the saturation current of the inductor and current limits of the main and synchronous MOSFETs. Also, the lower peak of I_{LR} must be positive if CCM operation is required.

Figure 26 and Figure 27 show curves on inductor selection for various V_{OUT} and R_{ON}. For small R_{ON}, according to (8), V_{IN} is limited. Some curves are therefore limited as shown in the figures.

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Typical Application (continued)

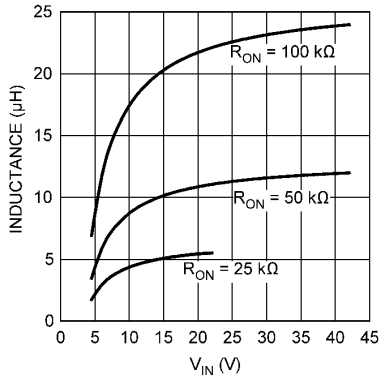


Figure 26. Inductor Selection for V_{OUT} = 3.3 V

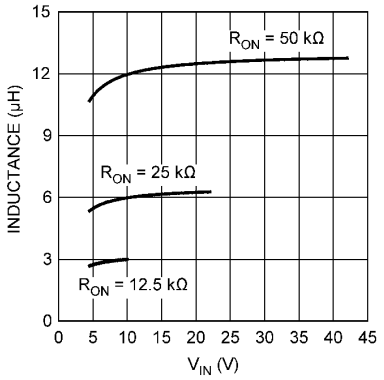


Figure 27. Inductor Selection for V_{OUT} = 0.8 V

C_{VCC}: The capacitor on the V_{CC} output provides not only noise filtering and stability, but also prevents false triggering of the V_{CC} UVLO at the main MOSFET on/off transitions. C_{VCC} should be no smaller than 680 nF for stability, and should be a good quality, low-ESR, ceramic capacitor.

C_{OUT} and C_{OUT3}: C_{OUT} should generally be no smaller than 10 µF. Experimentation is usually necessary to determine the minimum value for C_{OUT}, as the nature of the load may require a larger value. A load which creates significant transients requires a larger C_{OUT} than a fixed load.

C_{OUT3} is a small value ceramic capacitor located close to the LM3102 to further suppress high frequency noise at V_{OUT}. A 100-nF capacitor is recommended.

C_{IN} and C_{IN3}: The function of C_{IN} is to supply most of the main MOSFET current during the ON-time, and limit the voltage ripple at the VIN pin, assuming that the voltage source connecting to the VIN pin has finite output impedance. If the voltage source's dynamic impedance is high (effectively a current source), C_{IN} supplies the average input current, but not the ripple current.

At the maximum load current, when the main MOSFET turns on, the current to the VIN pin suddenly increases from zero to the lower peak of the inductor's ripple current and ramps up to the higher peak value. It then drops to zero at turnoff. The average current during the ON-time is the load current. For a worst case calculation, C_{IN} must be capable of supplying this average load current during the maximum ON-time. C_{IN} is calculated from:

$$C_{IN} = \frac{I_{OUT} \times t_{on}}{\Delta V_{IN}}$$

where

- I_{OUT} is the load current
- t_{on} is the maximum ON-time
- ΔV_{IN} is the allowable ripple voltage at V_{IN} (10)

The purpose of C_{IN3} is to help avoid transients and ringing due to long lead inductance at the VIN pin. A low ESR 0.1-µF ceramic chip capacitor located close to the LM3102 is recommended.

C_{BST}: A 33-nF, high-quality ceramic capacitor with low ESR is recommended for C_{BST} because it supplies a surge current to charge the main MOSFET gate driver at turnon. Low ESR also helps ensure a complete recharge during each OFF-time.

C_{SS}: The capacitor at the SS pin determines the soft-start time, that is, the time for the reference voltage at the regulation comparator and the output voltage to reach their final value. The time is determined from the following equation:

$$t_{SS} = \frac{C_{SS} \times 0.8V}{8\ \mu A} \quad (11)$$

C_{FB}: If the output voltage is higher than 1.6 V, C_{FB} is needed in the Discontinuous Conduction Mode to reduce the output ripple. The recommended value for C_{FB} is 10 nF.

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Typical Application (continued)

8.2.3 Application Curve

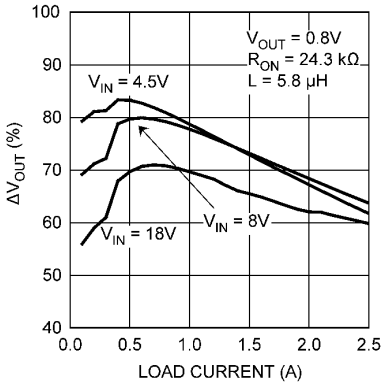


Figure 28. Efficiency vs Load Current (V_{OUT} = 0.8 V)

8.3 System Examples

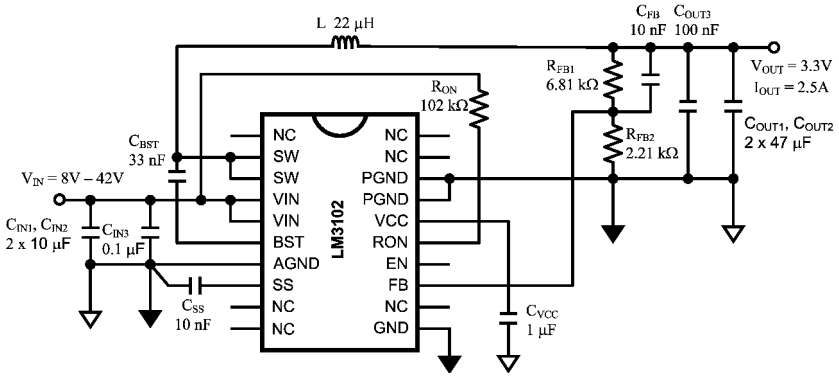


Figure 29. Typical Application Schematic for V_{OUT} = 3.3 V

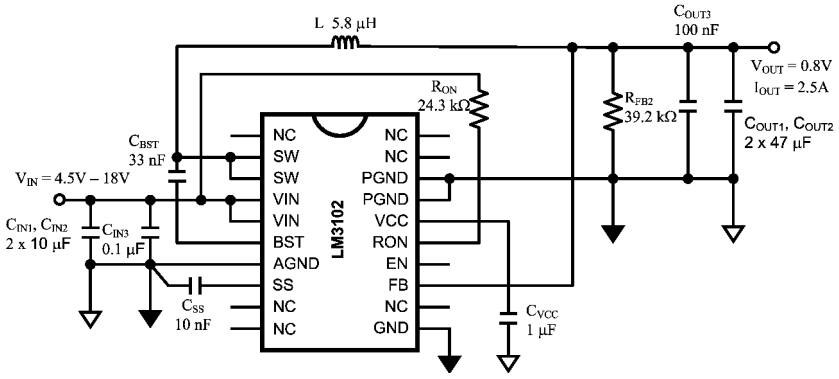


Figure 30. Typical Application Schematic for V_{OUT} = 0.8 V

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9 Power Supply Recommendations

The LM3102 device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LM3102 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LM3102, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

The LM3102 regulation, overvoltage, and current limit comparators are very fast so they will respond to short duration noise pulses. Layout is therefore critical for optimum performance. It must be as neat and compact as possible, and all external components must be as close to their associated pins of the LM3102 as possible.

Refer to *Layout Example*, the loop formed by C_{IN}, the main and synchronous MOSFET internal to the LM3102, and the PGND pin should be as small as possible. The connection from the PGND pin to C_{IN} should be as short and direct as possible. Vias should be added to connect the ground of C_{IN} to a ground plane, located as close to the capacitor as possible. The bootstrap capacitor C_{BST} should be connected as close to the SW and BST pins as possible, and the connecting traces should be thick. The feedback resistors and capacitor R_{FB1}, R_{FB2}, and C_{FB} should be close to the FB pin.

A long trace running from V_{OUT} to R_{FB1} is generally acceptable because this is a low-impedance node. Ground R_{FB2} directly to the AGND pin (pin 7). The output capacitor C_{OUT} should be connected close to the load and tied directly to the ground plane. The inductor L should be connected close to the SW pin with as short a trace as possible to reduce the potential for EMI (electromagnetic interference) generation.

If it is expected that the internal dissipation of the LM3102 will produce excessive junction temperature during normal operation, making good use of the PCB ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the LM3102 IC package can be soldered to the ground plane, which should extend out from beneath the LM3102 to help dissipate heat.

The exposed pad is internally connected to the LM3102 IC substrate. Additionally the use of thick traces, where possible, can help conduct heat away from the LM3102. Using numerous vias to connect the die attached pad to the ground plane is a good practice. Judicious positioning of the PCB within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

10.2 Layout Example

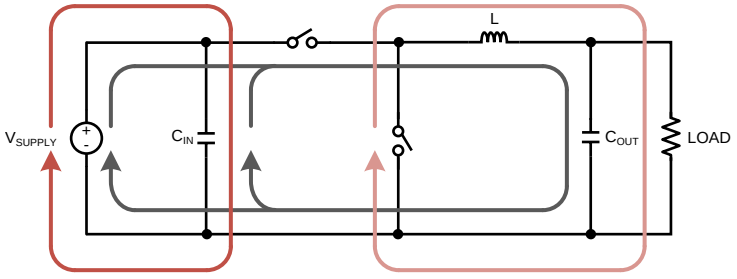


Figure 31. Minimize Area of Current Loops in Buck Regulators

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Layout Example (continued)

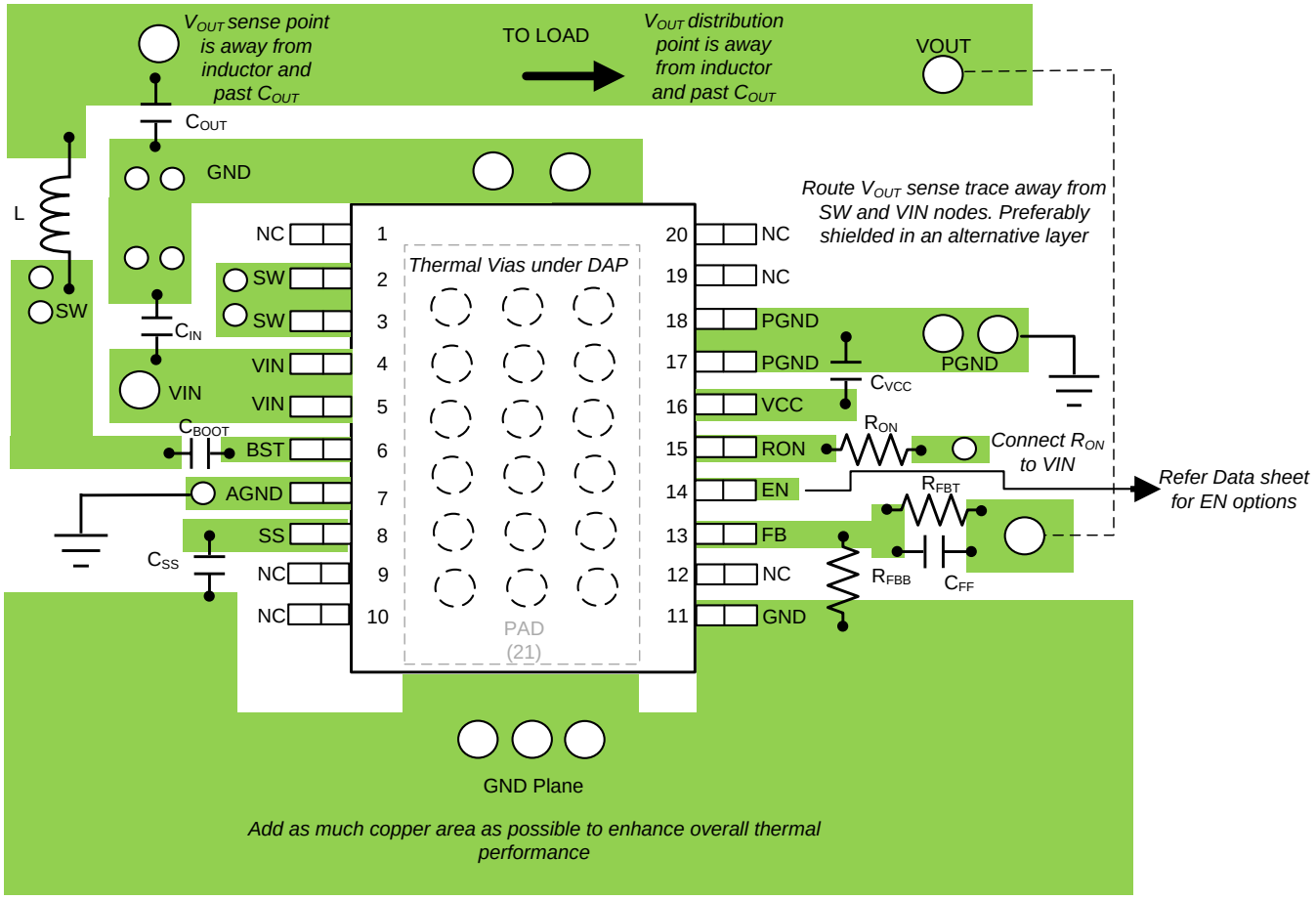


Figure 32. PCB Layout Example - Top View

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3102MH/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3102 MH
LM3102MH/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3102 MH
LM3102MH/NOPB.B	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3102 MH
LM3102MHX/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3102 MH
LM3102MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3102 MH
LM3102MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3102 MH
LM3102TL-1/NOPB	Active	Production	DSBGA (YPA) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3102
LM3102TL-1/NOPB.A	Active	Production	DSBGA (YPA) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3102
LM3102TL-1/NOPB.B	Active	Production	DSBGA (YPA) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3102
LM3102TLX-1/NOPB	Active	Production	DSBGA (YPA) | 28	1000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3102
LM3102TLX-1/NOPB.A	Active	Production	DSBGA (YPA) | 28	1000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3102
LM3102TLX-1/NOPB.B	Active	Production	DSBGA (YPA) | 28	1000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3102

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM3102 :

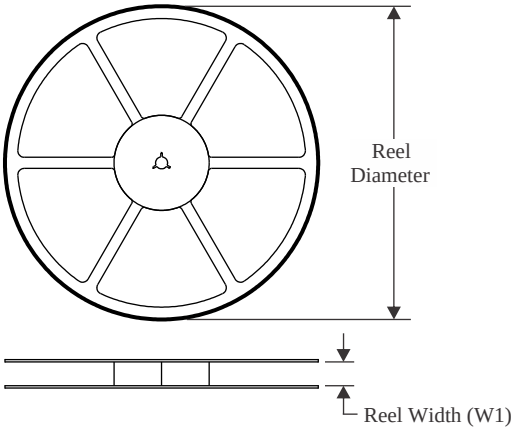
- Automotive : LM3102-Q1

NOTE: Qualified Version Definitions:

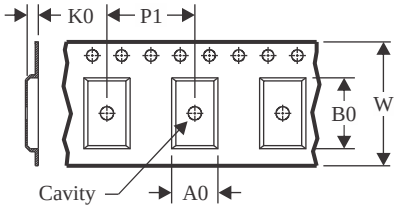
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

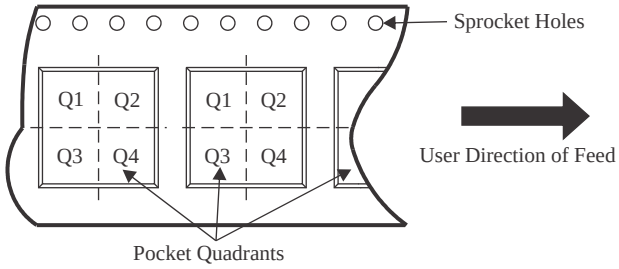


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

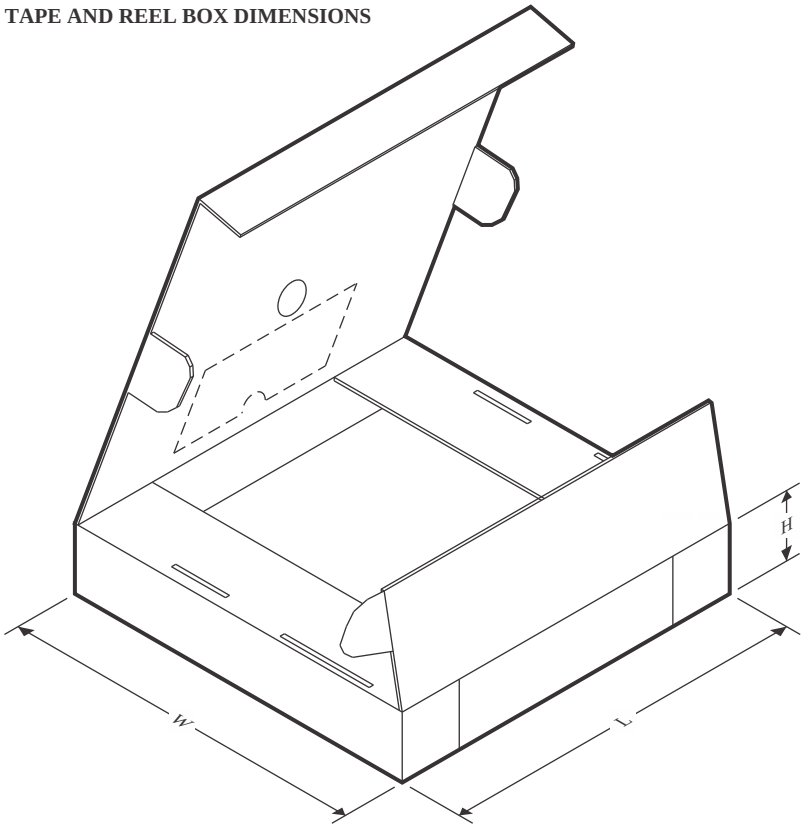
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3102MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM3102TL-1/NOPB	DSBGA	YPA	28	250	177.8	12.4	2.64	3.84	0.76	8.0	12.0	Q1
LM3102TLX-1/NOPB	DSBGA	YPA	28	1000	177.8	12.4	2.64	3.84	0.76	8.0	12.0	Q1

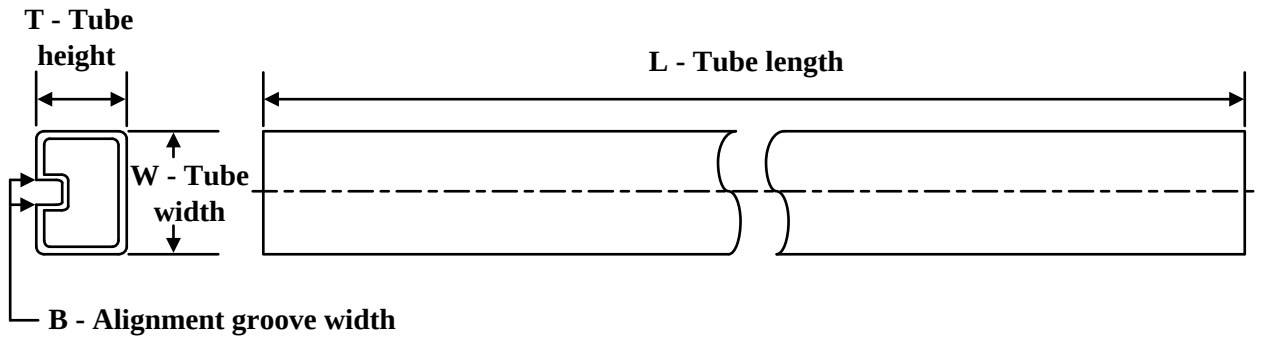
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3102MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM3102TL-1/NOPB	DSBGA	YPA	28	250	208.0	191.0	35.0
LM3102TLX-1/NOPB	DSBGA	YPA	28	1000	208.0	191.0	35.0

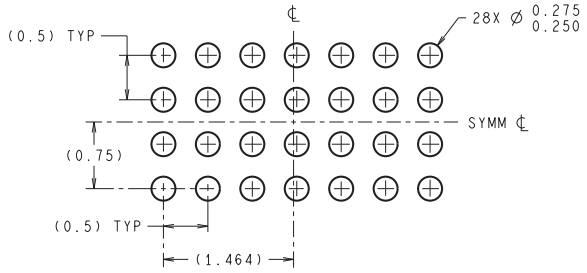
TUBE



*All dimensions are nominal

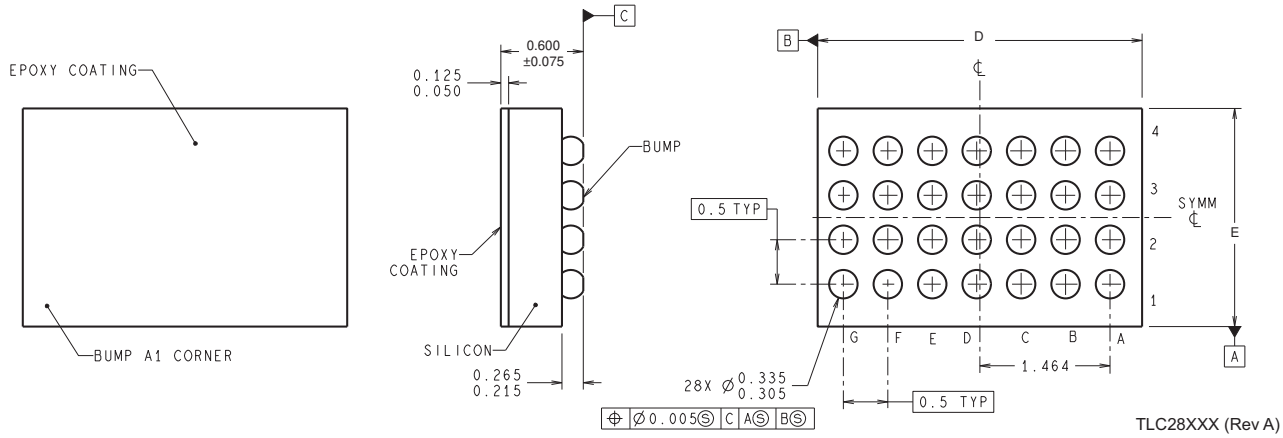
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3102MH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM3102MH/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM3102MH/NOPB.B	PWP	HTSSOP	20	73	495	8	2514.6	4.06

YPA0028



LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

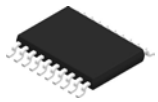


D: Max = 3.676 mm, Min =3.615 mm

E: Max = 2.48 mm, Min = 2.419 mm

4215064/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

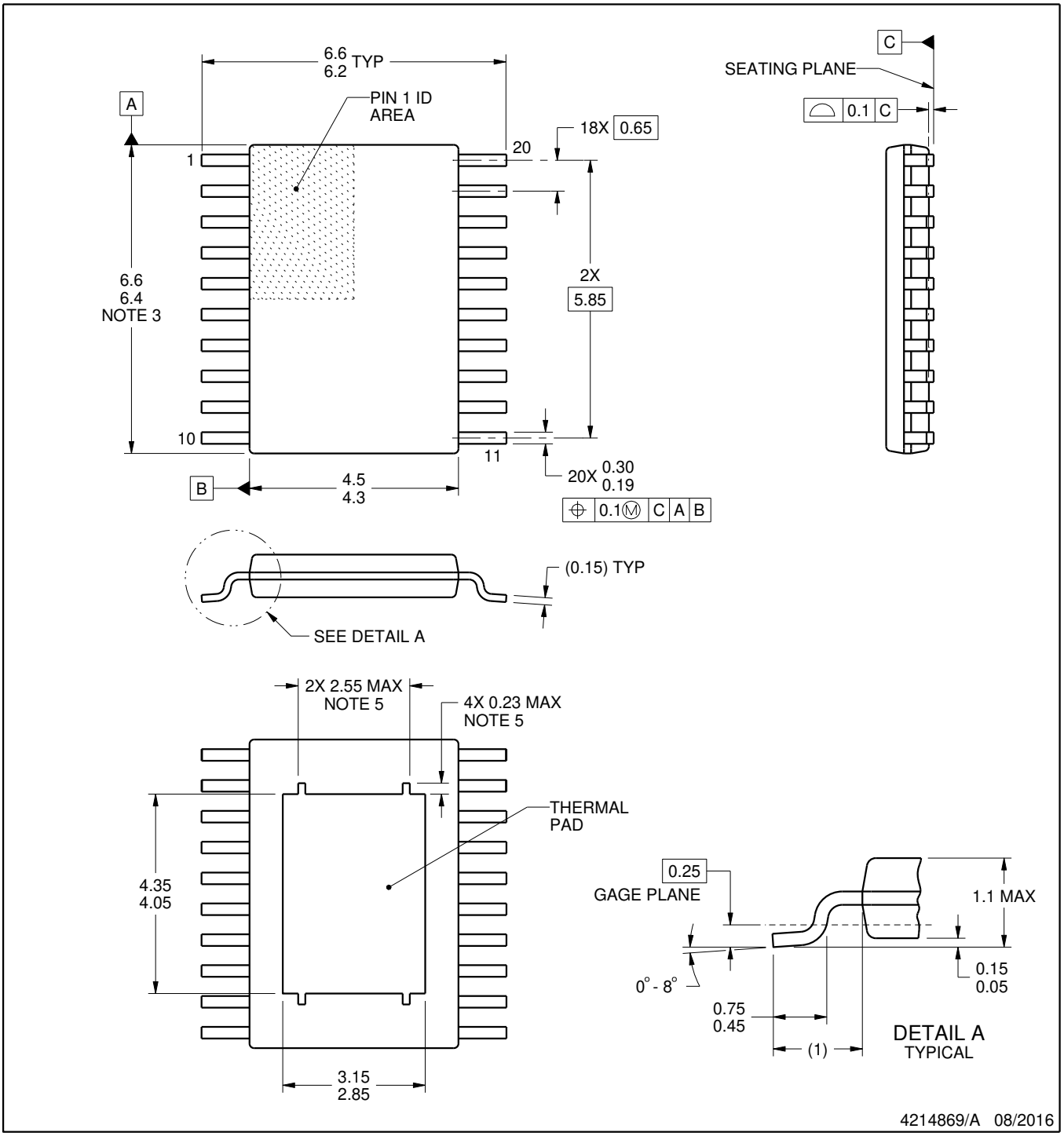


PACKAGE OUTLINE

PWP0020A

PowerPAD™ TSSOP - 1.1 mm max height

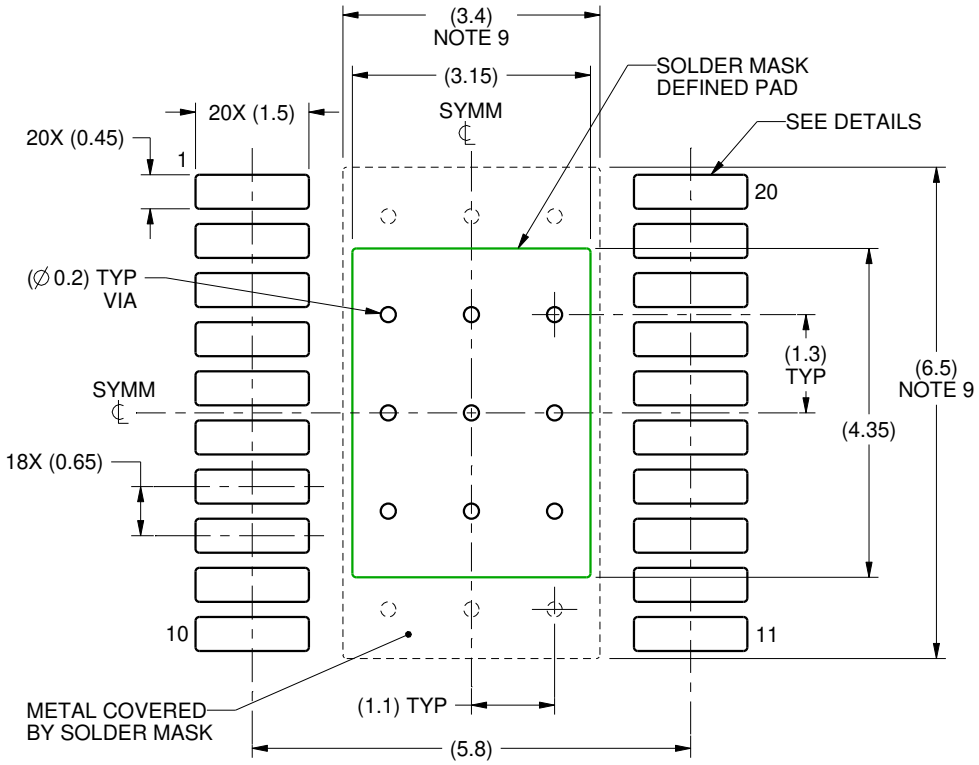
PLASTIC SMALL OUTLINE



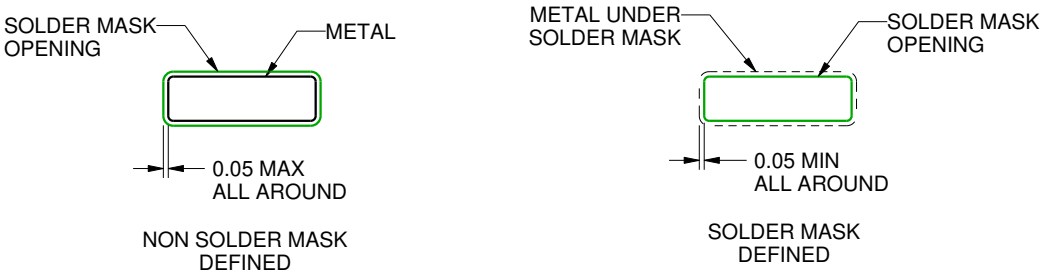
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

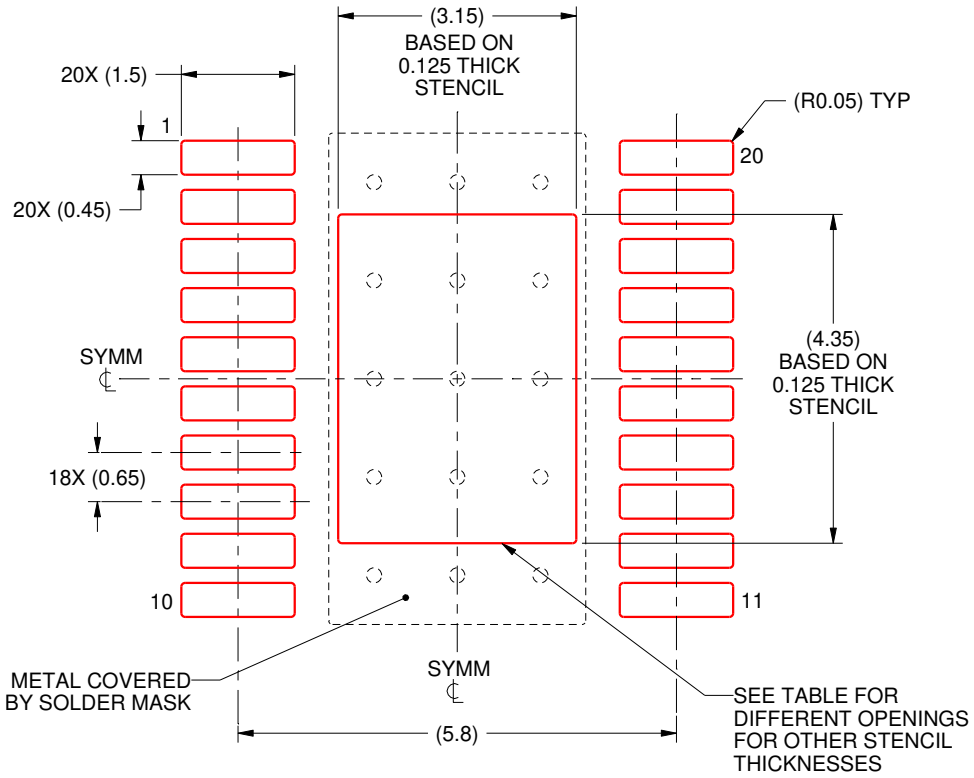


SOLDER MASK DETAILS
PADS 1-20

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.52 X 4.86
0.125	3.15 X 4.35 (SHOWN)
0.15	2.88 X 3.97
0.175	2.66 X 3.68

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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