LM3405A 1.6-MHz, 1-A Constant Current Buck LED Driver With Internal Compensation in Tiny SOT and MSOP-PowerPAD™ Packages

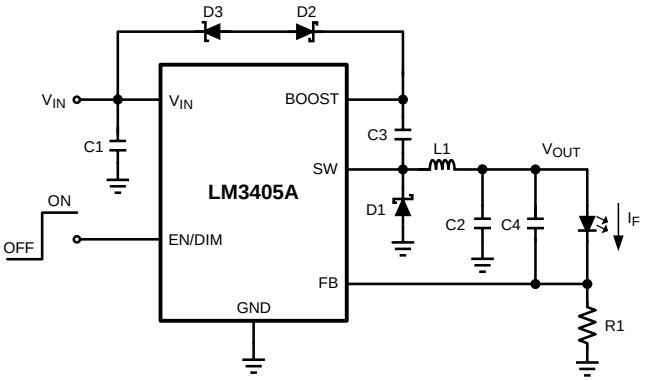
1 Features

- V_{IN} Operating Range of 3 V to 22 V
- Drives up to 5 High-Brightness LEDs in Series at 1 A
- Thin SOT-6 and MSOP-PowerPAD™-8 Packages
- 1.6-MHz Switching Frequency
- EN/DIM Input for Enabling and PWM Dimming of LEDs
- 300-mΩ NMOS Switch
- 40-nA Shutdown Current at V_{IN} = 5 V
- Internally Compensated Current-mode Control
- Cycle-by-Cycle Current Limit
- Input Voltage UVLO
- Overcurrent Protection
- Thermal Shutdown

2 Applications

- LED Drivers
- Constant Current Sources
- Industrial Lighting
- LED Flashlights
- LED Lightbulbs

Typical Application Circuit



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3 Description

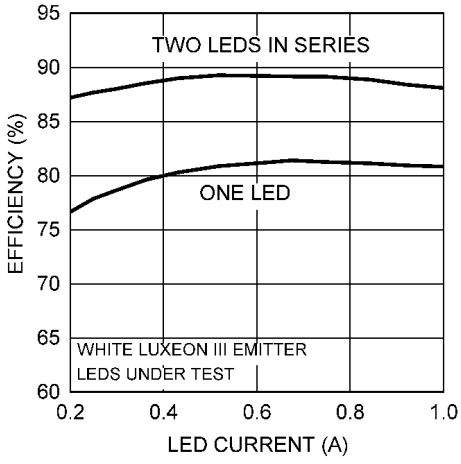
The LM3405A is a 1-A constant current buck LED driver designed to provide a simple, high efficiency solution for driving high power LEDs. With a 0.205-V reference voltage feedback control to minimize power dissipation, an external resistor sets the current as needed for driving various types of LEDs. Switching frequency is internally set to 1.6 MHz, allowing small surface mount inductors and capacitors to be used. The LM3405A uses current-mode control and internal compensation offering ease of use and predictable, high performance regulation over a wide range of operating conditions. With a maximum input voltage of 22 V, the device can drive up to 5 High-Brightness LEDs in series at 1-A forward current, with the single LED forward voltage of approximately 3.7 V. Additional features include user accessible EN/DIM pin for enabling and PWM dimming of LEDs, thermal shutdown, cycle-by-cycle current limit and overcurrent protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3405A	SOT (6)	2.90 mm × 1.60 mm
	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs LED Current (V_{IN} = 12 V)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed $R_{\theta JA}$ for SOT package from 118°C/W to 182.9°C/W ... 5
- Changed $R_{\theta JA}$ for MSOP package from 73°C/W to 55.3°C/W ... 5

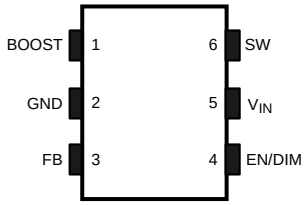
Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 23

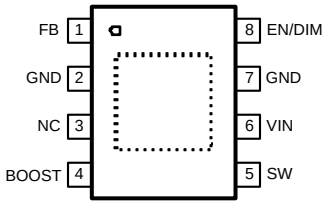
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5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



DGN Package
8-Pin MSOP-PowerPAD™
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT	MSOP-PowerPAD		
BOOST	1	4	O	Boost voltage that drives the NMOS output switch. A bootstrap capacitor is connected between the BOOST and SW pins.
GND	2	2, 7	—	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
FB	3	1	I	Feedback pin. Connect FB to the LED string cathode and an external resistor to ground to set the LED current.
EN/DIM	4	8	I	Enable control input. Logic high enables operation. Toggling this pin with a periodic logic square wave of varying duty cycle at different frequencies controls the brightness of LEDs. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
VIN	5	6	I	Input supply voltage. Connect a bypass capacitor locally from this pin to GND.
SW	6	5	O	Switch pin. Connect this pin to the inductor, catch diode, and bootstrap capacitor.
NC	—	3	—	No connection.
DAP	N/A	—	—	Attach to power ground pin (GND).

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}	–0.5	24	V
SW voltage	–0.5	24	V
Boost voltage	–0.5	30	V
Boost to SW voltage	–0.5	6	V
FB voltage	–0.5	3	V
EN/DIM voltage	–0.5	(V_{IN} + 0.3)	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
LM3405A IN SOT PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
LM3405A IN MSOP-PowerPAD PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}		3	22	V
EN/DIM voltage		0	(V_{IN} + 0.3)	V
Boost to SW voltage		2.5	5.5	V
Junction temperature		–40	125	°C
I_{LED}	SOT package		400	mA
	MSOP-PowerPAD package		1	A

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6.4 Thermal Information

THERMAL METRIC(1)		LM3405A		UNIT
		DDC (SOT)	DGN (MSOP-PowerPAD)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.9	55.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.4	62.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.1	38.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.7	38.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

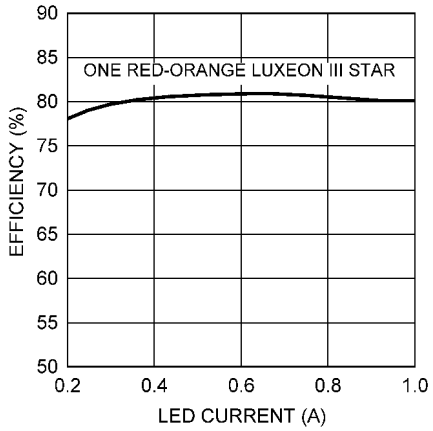
Unless otherwise specified, V_{IN} = 12 V. TYP values are for T_J = 25°C only; MIN/MAX limits apply over the junction temperature (T_J) range of –40°C to 125°C. Typical values represent the most likely parametric norm, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage		0.188	0.205	0.22	V
$\Delta V_{FB}/(\Delta V_{IN} x V_{FB})$	Feedback voltage line regulation	V_{IN} = 3 V to 22 V		0.01		%/V
I_{FB}	Feedback input bias current	Sink/source		10	250	nA
UVLO	Undervoltage lockout	V_{IN} Rising		2.74	2.95	V
		V_{IN} Falling	1.9	2.3		V
	UVLO Hysteresis			0.44		V
f_{SW}	Switching frequency		1.2	1.6	1.9	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0 V	85%	94%		
$R_{DS(ON)}$	Switch ON resistance	SOT (V_{BOOST} - V_{SW} = 3 V)		300	600	mΩ
		MSOP-PowerPAD (V_{BOOST} - V_{SW} = 3 V)		360	700	
I_{CL}	Switch current limit	V_{BOOST} - V_{SW} = 3 V, V_{IN} = 3 V	1.2	2	2.8	A
I_Q	Quiescent current	Switching, V_{FB} = 0.195 V		1.8	2.8	mA
	Quiescent current (shutdown)	$V_{EN/DIM}$ = 0 V		0.3		µA
V_{EN/DIM_TH}	Enable threshold voltage	$V_{EN/DIM}$ Rising	1.8			V
	Shutdown threshold voltage	$V_{EN/DIM}$ Falling			0.4	V
$I_{EN/DIM}$	EN/DIM pin current	Sink/Source		0.01		µA
I_{SW}	Switch leakage	V_{IN} = 22 V		0.1		µA

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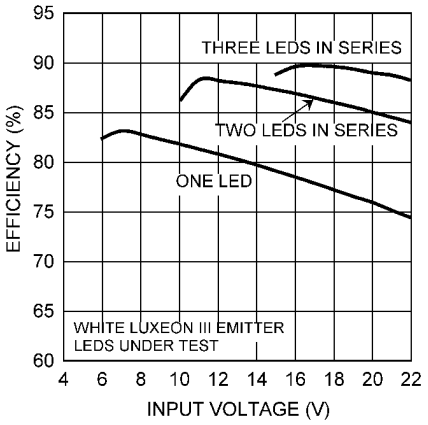
6.6 Typical Characteristics

Unless otherwise specified, V_{IN} = 12 V, $V_{BOOST} - V_{SW}$ = 5 V and T_A = 25°C.



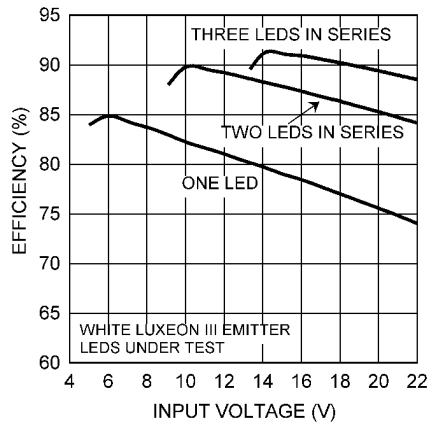
V_{IN} = 5 V

Figure 1. Efficiency vs LED Current



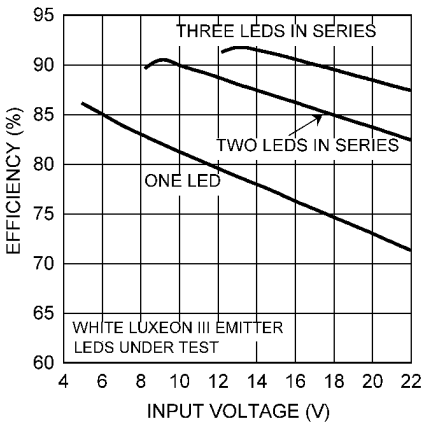
I_F = 1 A

Figure 2. Efficiency vs Input Voltage



I_F = 0.7 A

Figure 3. Efficiency vs Input Voltage



I_F = 0.35 A

Figure 4. Efficiency vs Input Voltage

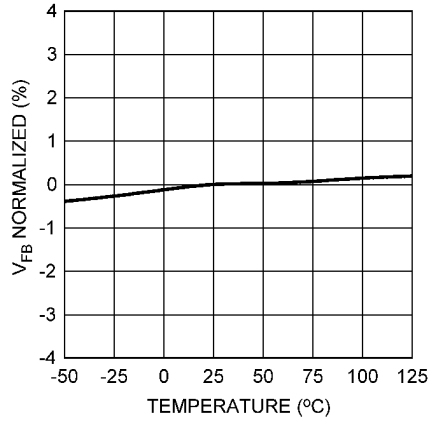


Figure 5. V_{FB} vs Temperature

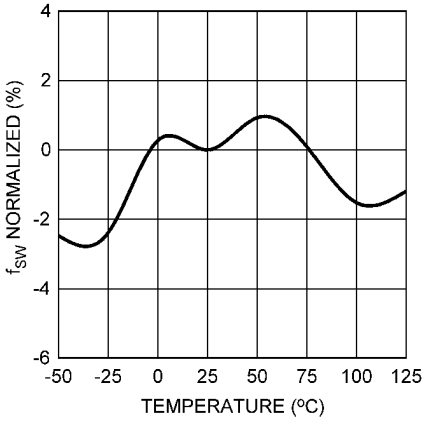


Figure 6. Oscillator Frequency vs Temperature

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Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, $V_{BOOST} - V_{SW}$ = 5 V and T_A = 25°C.

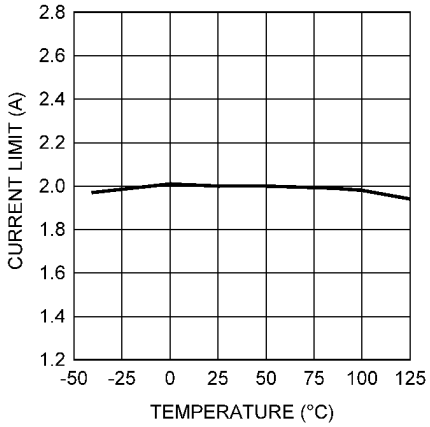
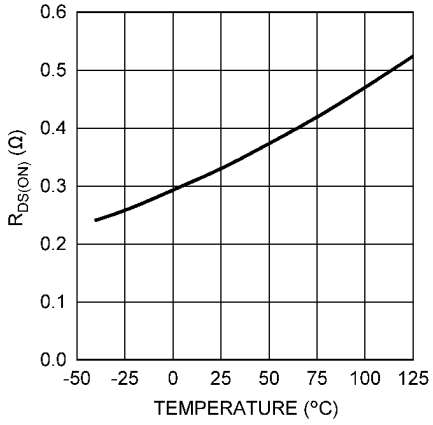


Figure 7. Current Limit vs Temperature



V_{BOOST} - V_{SW} = 3 V

Figure 8. SOT $R_{DS(ON)}$ vs Temperature

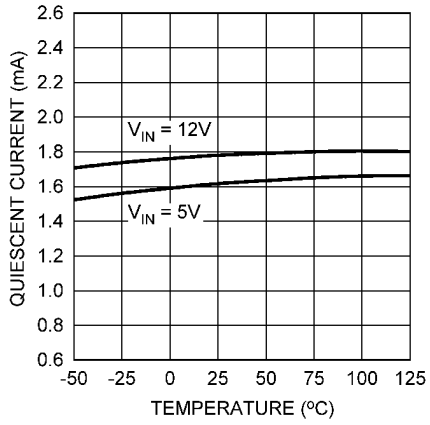
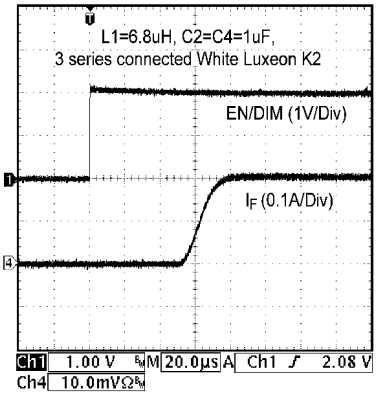


Figure 9. Quiescent Current vs Temperature



V_{IN} = 15 V I_F = 0.2 A

Figure 10. Start-Up Response to EN/DIM Signal

7 Detailed Description

7.1 Overview

The LM3405A is a PWM, current-mode controlled buck switching regulator designed to provide a simple, high efficiency solution for driving LEDs with a preset switching frequency of 1.6MHz. This high frequency allows the LM3405A to operate with small surface mount capacitors and inductors, resulting in LED drivers that need only a minimum amount of board space. The LM3405A is internally compensated, simple to use, and requires few external components.

The following description of operation of the LM3405A refers to the *Typical Application Circuit* and to the waveforms in Figure 11. The LM3405A supplies a regulated output current by switching the internal NMOS power switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS power switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the internal power switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through the catch diode D1, which forces the SW pin to swing below ground by the forward voltage (V_{D1}) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output current (I_F) through the LED, by forcing FB pin voltage to be equal to V_{REF} (0.205 V).

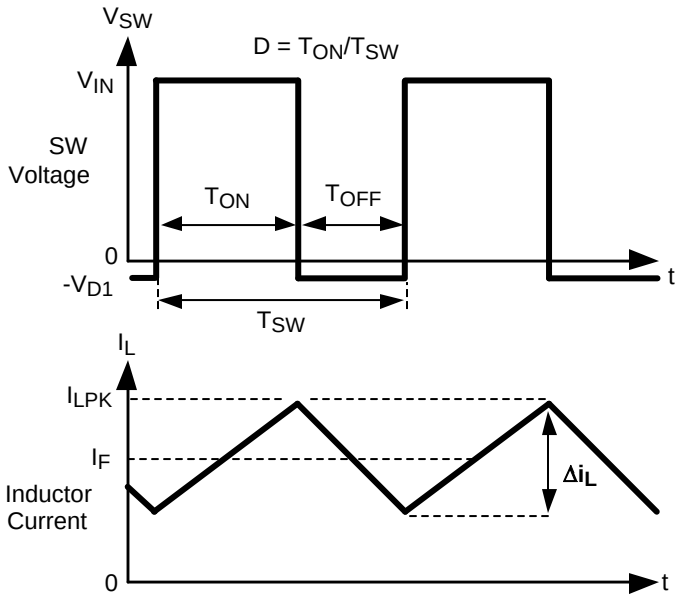
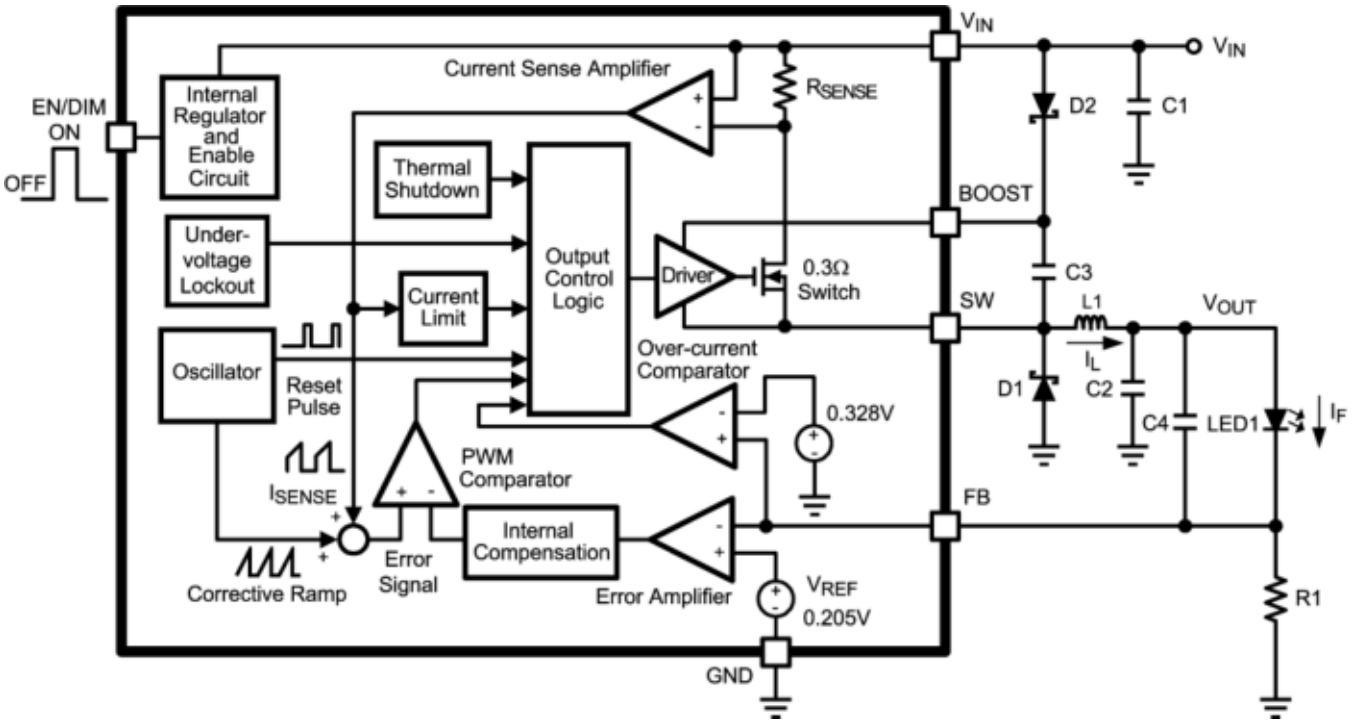


Figure 11. SW Pin Voltage and Inductor Current Waveforms of LM3405A

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Boost Function

Capacitor C3 and diode D2 in the *Functional Block Diagram* are used to generate a voltage V_{BOOST}. The voltage across C3, V_{BOOST} - V_{SW}, is the gate drive voltage to the internal NMOS power switch. To properly drive the internal NMOS switch during its on-time, V_{BOOST} needs to be at least 2.5-V greater than V_{SW}. A large value of V_{BOOST} - V_{SW} is recommended to achieve better efficiency by minimizing both the internal switch ON resistance ($R_{DS(ON)}$), and the switch rise and fall times. However, V_{BOOST} - V_{SW} should not exceed the maximum operating limit of 5.5 V.

When the LM3405A starts up, internal circuitry from V_{IN} supplies a 20-mA current to the BOOST pin, flowing out of the BOOST pin into C3. This current charges C3 to a voltage sufficient to turn the switch on. The BOOST pin will continue to source current to C3 until the voltage at the feedback pin is greater than 123 mV.

There are various methods to derive V_{BOOST}:

1. From the input voltage (V_{IN})
2. From the output voltage (V_{OUT})
3. From a shunt or series Zener diode
4. From an external distributed voltage rail (V_{EXT})

The first method is shown in the *Functional Block Diagram*. Capacitor C3 is charged via diode D2 by V_{IN}. During a normal switching cycle, when the internal NMOS power switch is off (T_{OFF}) (see Figure 11), V_{BOOST} equals V_{IN} minus the forward voltage of D2 (V_{D2}), during which the current in the inductor (L1) forward biases the catch diode D1 (V_{D1}). Therefore the gate drive voltage stored across C3 is:

$$V_{BOOST} - V_{SW} = V_{IN} - V_{D2} + V_{D1} \quad (1)$$

When the NMOS switch turns on (T_{ON}), the switch pin rises to:

$$V_{SW} = V_{IN} – (R_{DS(ON)} \times I_L) \quad (2)$$

Feature Description (continued)

Since the voltage across C3 remains unchanged, V_{BOOST} is forced to rise thus reverse biasing D2. The voltage at V_{BOOST} is then:

$$V_{BOOST} = 2V_{IN} – (R_{DS(ON)} \times I_L) – V_{D2} + V_{D1} \quad (3)$$

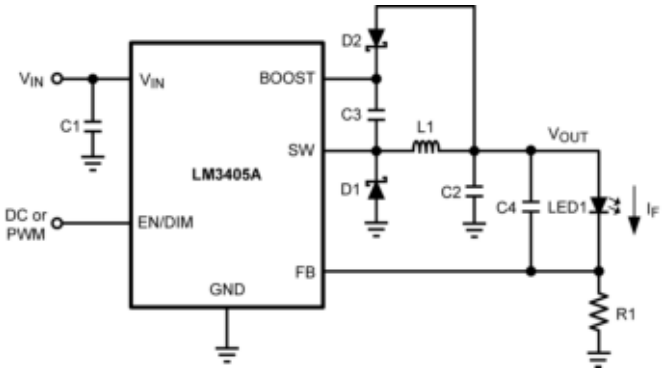
Depending on the quality of the diodes D1 and D2, the gate drive voltage in this method can be slightly less or larger than the input voltage V_{IN}. For best performance, ensure that the variation of the input supply does not cause the gate drive voltage to fall outside the recommended range:

$$2.5V < V_{IN} - V_{D2} + V_{D1} < 5.5\ V \quad (4)$$

The second method for deriving the boost voltage is to connect D2 to the output as shown in Figure 12. The gate drive voltage in this configuration is:

$$V_{BOOST} - V_{SW} = V_{OUT} – V_{D2} + V_{D1} \quad (5)$$

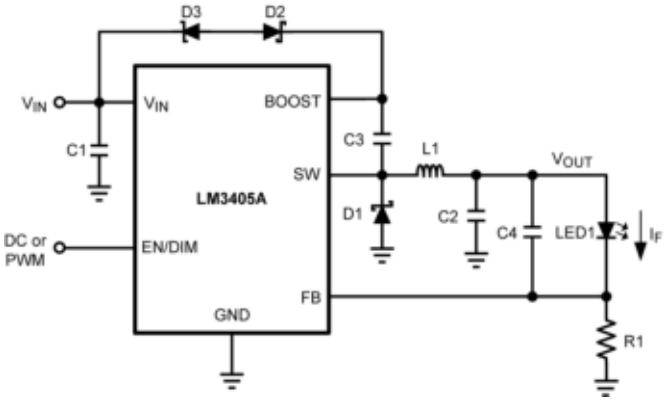
Since the gate drive voltage needs to be in the range of 2.5 V to 5.5 V, the output voltage V_{OUT} should be limited to a certain range. For the calculation of V_{OUT}, see *Output Voltage*.



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Figure 12. V_{BOOST} Derived from V_{OUT}

The third method can be used in the applications where both V_{IN} and V_{OUT} are greater than 5.5 V. In these cases, C3 cannot be charged directly from these voltages; instead C3 can be charged from V_{IN} or V_{OUT} minus a Zener voltage (V_{D3}) by placing a Zener diode D3 in series with D2 as shown in Figure 13. When using a series Zener diode from the input, the gate drive voltage is $V_{IN} - V_{D3} - V_{D2} + V_{D1}$.



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Figure 13. V_{BOOST} Derived from V_{IN} Through a Series Zener

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Feature Description (continued)

An alternate method is to place the zener diode D3 in a shunt configuration as shown in Figure 14. A small 350 mW to 500 mW, 5.1-V Zener in a SOT or SOD package can be used for this purpose. A small ceramic capacitor such as a 6.3 V, 0.1-µF capacitor (C5) should be placed in parallel with the Zener diode. When the internal NMOS switch turns on, a pulse of current is drawn to charge the internal NMOS gate capacitance. The 0.1-µF parallel shunt capacitor ensures that the V_{BOOST} voltage is maintained during this time. Resistor R2 should be chosen to provide enough RMS current to the zener diode and to the BOOST pin. A recommended choice for the zener current (I_{ZENER}) is 1 mA. The current I_{BOOST} into the BOOST pin supplies the gate current of the NMOS power switch. It reaches a maximum of around 3.6 mA at the highest gate drive voltage of 5.5 V over the LM3405A operating range.

For the worst case I_{BOOST}, increase the current by 50%. In that case, the maximum boost current will be:

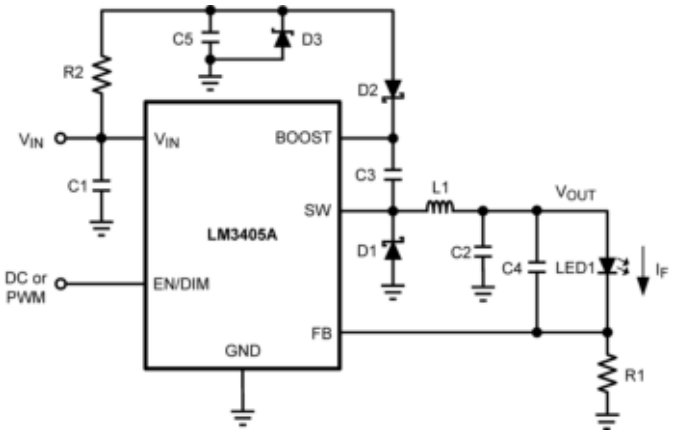
$$I_{BOOST\text{-}MAX} = 1.5 \times 3.6\ mA = 5.4\ mA \quad (6)$$

R2 will then be given by:

$$R2 = (V_{IN} - V_{ZENER}) / (I_{BOOST_MAX} + I_{ZENER}) \quad (7)$$

For example, let V_{IN} = 12 V, V_{ZENER} = 5V, I_{ZENER} = 1 mA, then:

$$R2 = (12\ V - 5\ V) / (5.4\ mA + 1\ mA) = 1.09\ k\Omega \quad (8)$$



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Figure 14. V_{BOOST} Derived from V_{IN} Through a Shunt Zener

The fourth method can be used in an application which has an external low voltage rail, V_{EXT}. C3 can be charged through D2 from V_{EXT}, independent of V_{IN} and V_{OUT} voltage levels. Again for best performance, ensure that the gate drive voltage, $V_{EXT} - V_{D2} + V_{D1}$, falls in the range of 2.5 V to 5.5 V.

7.3.2 Setting the LED Current

LM3405A is a constant current buck regulator. The LEDs are connected between V_{OUT} and the FB pin as shown in the
Typical Application Circuit. The FB pin is at 0.205V in regulation and therefore the LED current I_F is set by V_{FB} and resistor R1 from FB to ground by the following equation:

$$I_F = V_{FB} / R1 \quad (9)$$

I_F should not exceed the 1-A current capability of LM3405A and therefore R1 minimum must be approximately 0.2 Ω. I_F should also be kept above 200 mA for stable operation, and therefore R1 maximum must be approximately 1 Ω. If average LED currents less than 200 mA are desired, the EN/DIM pin can be used for PWM dimming. See *LED PWM Dimming*.

7.3.3 Output Voltage

The output voltage is primarily determined by the number of LEDs (n) connected from V_{OUT} to FB pin and therefore V_{OUT} can be written as:

$$V_{OUT} = ((n \times V_F) + V_{FB})$$

Feature Description (continued)

where

- V_F is the forward voltage of one LED at the set LED current level (see LED manufacturer data sheet for forward characteristics curve) (10)

7.3.4 Enable Mode / Shutdown Mode

The LM3405A has both enable and shutdown modes that are controlled by the EN/DIM pin. Connecting a voltage source greater than 1.8 V to the EN/DIM pin enables the operation of LM3405A, while reducing this voltage below 0.4 V places the part in a low quiescent current (0.3 µA typical) shutdown mode. There is no internal pullup on EN/DIM pin, therefore an external signal is required to initiate switching. Do not allow this pin to float or rise to 0.3 V above V_{IN}. It should be noted that when the EN/DIM pin voltage rises above 1.8 V while the input voltage is greater than UVLO, there is a finite delay before switching starts. During this delay the LM3405A will go through a power on reset state after which the internal soft-start process commences. The soft-start process limits the inrush current and brings up the LED current (I_F) in a smooth and controlled fashion. The total combined duration of the power on reset delay, soft-start delay and the delay to fully establish the LED current is in the order of 100 µs (see Figure 19).

The simplest way to enable the operation of LM3405A is to connect the EN/DIM pin to V_{IN} which allows self start-up of LM3405A whenever the input voltage is applied. However, when an input voltage of slow rise time is used to power the application and if both the input voltage and the output voltage are not fully established before the soft-start time elapses, the control circuit will command maximum duty cycle operation of the internal power switch to bring up the output voltage rapidly. When the feedback pin voltage exceeds 0.205 V, the duty cycle will have to reduce from the maximum value accordingly, to maintain regulation. It takes a finite amount of time for this reduction of duty cycle and this will result in a spike in LED current for a short duration as shown in Figure 15. In applications where this LED current overshoot is undesirable, EN/DIM pin voltage can be separately applied and delayed such that V_{IN} is fully established before the EN/DIM pin voltage reaches the enable threshold. The effect of delaying EN/DIM with respect to V_{IN} on the LED current is shown in Figure 16. For a fast rising input voltage (200 µs for example), there is no need to delay the EN/DIM signal since soft-start can smoothly bring up the LED current as shown in Figure 17.

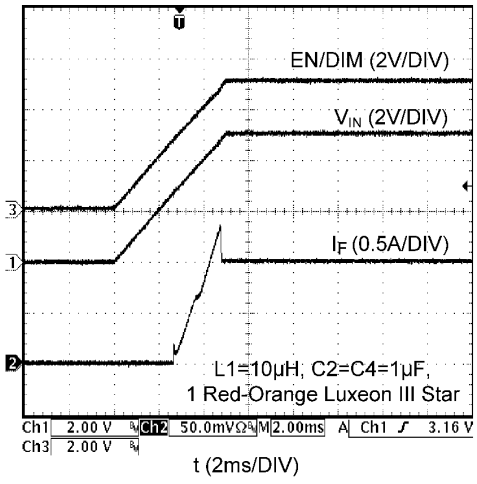


Figure 15. Start-Up Response to V_{IN} With 5-ms Rise Time

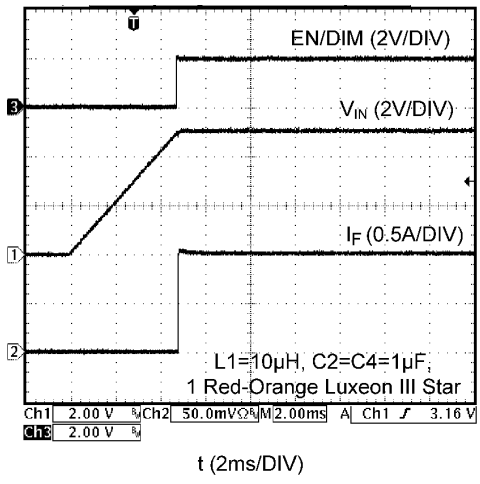


Figure 16. Start-Up Response to V_{IN} With EN/DIM Delayed

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Feature Description (continued)

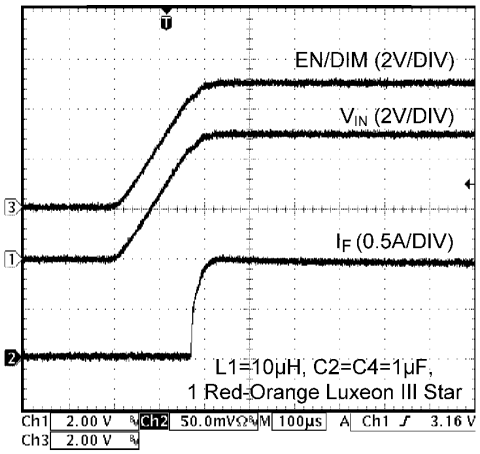


Figure 17. Start-Up Response to V_{IN} With 200-µs Rise Time

7.3.5 LED PWM Dimming

The LED brightness can be controlled by applying a periodic pulse signal to the EN/DIM pin and varying its frequency and/or duty cycle. This so-called PWM dimming method controls the average light output by pulsing the LED current between the set value and zero. A logic high level at the EN/DIM pin turns on the LED current whereas a logic low level turns off the LED current. Figure 18 shows a typical LED current waveform in PWM dimming mode. As explained in the previous section, there is approximately a 100-µs delay from the EN/DIM signal going high to fully establishing the LED current as shown in Figure 19. This 100-µs delay sets a maximum frequency limit for the driving signal that can be applied to the EN/DIM pin for PWM dimming. Figure 20 shows the average LED current versus duty cycle of PWM dimming signal for various frequencies. The applicable frequency range to drive LM3405A for PWM dimming is from 100 Hz to 5 kHz. The dimming ratio reduces drastically when the applied PWM dimming frequency is greater than 5 kHz.

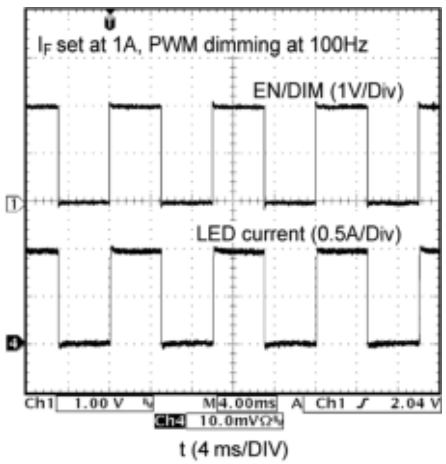


Figure 18. PWM Dimming of LEDs Using the EN/DIM Pin

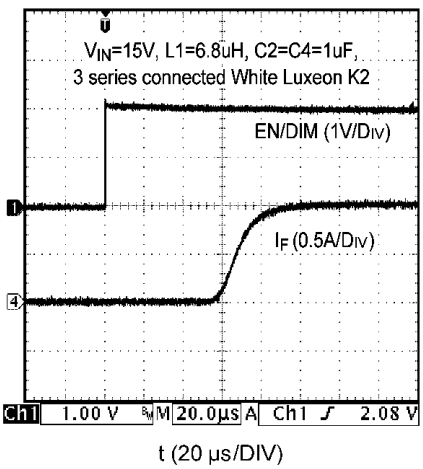


Figure 19. Start-Up Response to EN/DIM With I_F = 1 A

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Feature Description (continued)

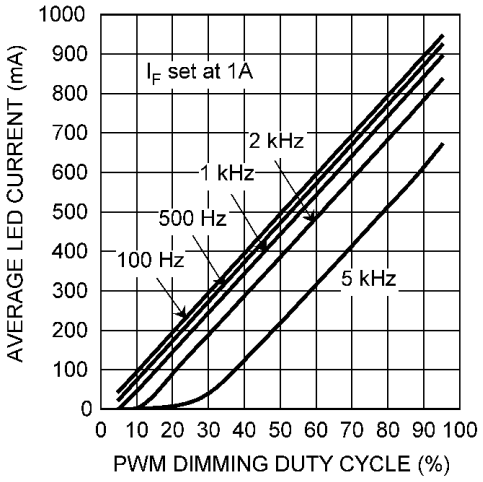


Figure 20. Average LED Current vs Duty Cycle of PWM Dimming Signal at EN/DIM Pin

7.3.6 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LM3405A from operating until the input voltage exceeds 2.74 V (typical). The UVLO threshold has approximately 440 mV of hysteresis, so the part will operate until V_{IN} drops below 2.3 V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

7.3.7 Current Limit

The LM3405A uses cycle-by-cycle current limit to protect the internal power switch. During each switching cycle, a current limit comparator detects if the power switch current exceeds 2 A (typical), and turns off the switch until the next switching cycle begins.

7.3.8 Overcurrent Protection

The LM3405A has a built-in overcurrent comparator that compares the FB pin voltage to a threshold voltage that is 60% higher than the internal reference V_{REF}. Once the FB pin voltage exceeds this threshold level (typically 328 mV), the internal NMOS power switch is turned off, which allows the feedback voltage to decrease towards regulation. This threshold provides an upper limit for the LED current. LED current overshoot is limited to 328 mV/R1 by this comparator during transients.

7.4 Device Functional Modes

7.4.1 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal power switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the power switch does not turn on until the junction temperature drops below approximately 150°C.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Inductor (L1)

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \tag{11}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal NMOS must be included to calculate a more accurate duty cycle. Calculate D by using Equation 12:

$$D = \frac{V_{OUT} + V_{D1}}{V_{IN} + V_{D1} - V_{SW}} \tag{12}$$

V_{SW} can be approximated by Equation 13:

$$V_{SW} = I_F \times R_{DS(ON)} \tag{13}$$

The diode forward drop (V_{D1}) can range from 0.3 V to 0.7 V depending on the quality of the diode. The lower V_{D1} is, the higher the operating efficiency of the converter.

The inductor value determines the output ripple current (Δi_L, as defined in Figure 11). Lower inductor values decrease the size of the inductor, but increases the output ripple current. An increase in the inductor value will decrease the output ripple current. The ratio of ripple current to LED current is optimized when it is set between 0.3 and 0.4 at 1A LED current. This ratio r is defined as:

$$r = \frac{\Delta i_L}{I_F} \tag{14}$$

One must also ensure that the minimum current limit (1.2 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated as:

$$I_{LPK} = I_F + \Delta i_L/2 \tag{15}$$

When the designed maximum output current is reduced, the ratio r can be increased. At a current of 0.2 A, r can be made as high as 0.7. The ripple ratio can be increased at lighter loads because the net ripple is actually quite low, and if r remains constant the inductor value can be made quite large. An equation empirically developed for the maximum ripple ratio at any current below 2 A is:

$$r = 0.387 \times I_{OUT}^{-0.3667} \tag{16}$$

Note that this is just a guideline.

The LM3405A operates at a high frequency allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing LED current ripple. See the output capacitor and feed-forward capacitor sections for more details on LED current ripple.

Now that the ripple current or ripple ratio is determined, the inductance is calculated by Equation 17:

$$L = \frac{V_{OUT} + V_{D1}}{I_F \times r \times f_{SW}} \times (1\text{-}D) \tag{17}$$

where

- f_{SW} is the switching frequency
- I_F is the LED current

Application Information (continued)

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the operating frequency of the LM3405A, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety of ferrite based inductors is huge. Lastly, inductors with lower series resistance (DCR) will provide better operating efficiency. For recommended inductor selection, refer to Circuit Examples and Recommended Inductance Range in Table 1.

Table 1. Recommended Inductance Range

I_F	INDUCTANCE RANGE AND INDUCTOR CURRENT RIPPLE			
1 A	6.8 µH-15 µH			
	Inductance	6.8 µH	10 µH	15 µH
	$\Delta i_L / I_F$ (1)	51%	36%	24%
0.6 A	10 µH-22 µH			
	Inductance	10 µH	15 µH	22 µH
	$\Delta i_L / I_F$ (1)	58%	39%	26%
0.2 A	15 µH-27 µH			
	Inductance	15 µH	22 µH	27 µH
	$\Delta i_L / I_F$ (1)	116%	79%	65%

(1) Maximum over full range of V_{IN} and V_{OUT}.

8.1.2 Input Capacitor (C1)

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage rating, RMS current rating, and ESL (Equivalent Series Inductance). The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS-IN} = I_F \times \sqrt{D \times \left(1 - D + \frac{r^2}{12}\right)} \quad (18)$$

It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle D, is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and an 0805 ceramic chip capacitor will have very low ESL. At the operating frequency of the LM3405A, certain capacitors may have an ESL so large that the resulting inductive impedance ($2\pi fL$) will be higher than that required to provide stable operation. It is strongly recommended to use ceramic capacitors due to their low ESR and low ESL. A 10µF multilayer ceramic capacitor (MLCC) is a good choice for most applications. In cases where large capacitance is required, use surface mount capacitors such as Tantalum capacitors and place at least a 1µF ceramic capacitor close to the V_{IN} pin. For MLCCs it is recommended to use X7R or X5R dielectrics. Consult capacitor manufacturer datasheet to see how rated capacitance varies over operating conditions.

8.1.3 Output Capacitor (C2)

The output capacitor is selected based upon the desired reduction in LED current ripple. A 1µF ceramic capacitor results in very low LED current ripple for most applications. Due to the high switching frequency, the 1µF capacitor alone (without feed-forward capacitor C4) can filter more than 90% of the inductor current ripple for most applications where the sum of LED dynamic resistance and R1 is larger than 1Ω. Since the internal compensation is tailored for small output capacitance with very low ESR, it is strongly recommended to use a ceramic capacitor with capacitance less than 3.3µF.

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Given the availability and quality of MLCCs and the expected output voltage of designs using the LM3405A, there is really no need to review other capacitor technologies. A benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through the parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise. In cases where large capacitance is required, use Electrolytic or Tantalum capacitors with large ESR, and verify the loop performance on the bench. Like the input capacitor, multilayer ceramic capacitors are recommended X7R or X5R. Again, verify actual capacitance at the desired operating voltage and temperature.

Check the RMS current rating of the capacitor. The maximum RMS current rating of the capacitor is:

$$I_{RMS\text{-}OUT} = I_F \times \frac{r}{\sqrt{12}} \tag{19}$$

One may select a 1206 size ceramic capacitor for C2 since its current rating is typically higher than 1A, more than enough for the requirement.

8.1.4 Feed-Forward Capacitor (C4)

The feed-forward capacitor (designated as C4) connected in parallel with the LED string is required to provide multiple benefits to the LED driver design. It greatly improves the large signal transient response and suppresses LED current overshoot that may otherwise occur during PWM dimming; it also helps to shape the rise and fall times of the LED current pulse during PWM dimming thus reducing EMI emission; it reduces LED current ripple by bypassing some of inductor ripple from flowing through the LED. For most applications, a 1-µF ceramic capacitor is sufficient. In fact, the combination of a 1µF feed-forward ceramic capacitor and a 1µF output ceramic capacitor leads to less than 1% current ripple flowing through the LED. Lower and higher C4 values can be used, but bench validation is required to ensure the performance meets the application requirement.

Figure 21 shows a typical LED current waveform during PWM dimming without feed-forward capacitor. At the beginning of each PWM cycle, overshoot can be seen in the LED current. Adding a 1µF feed-forward capacitor can totally remove the overshoot as shown in Figure 22.

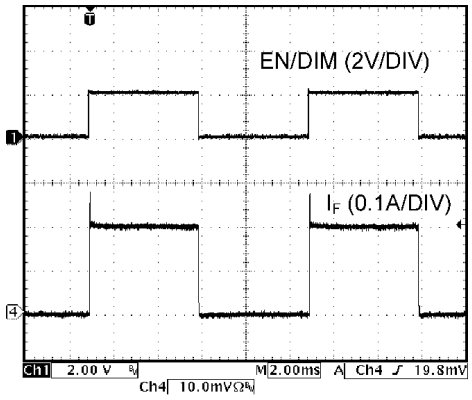


Figure 21. PWM Dimming Without Feed-Forward Capacitor

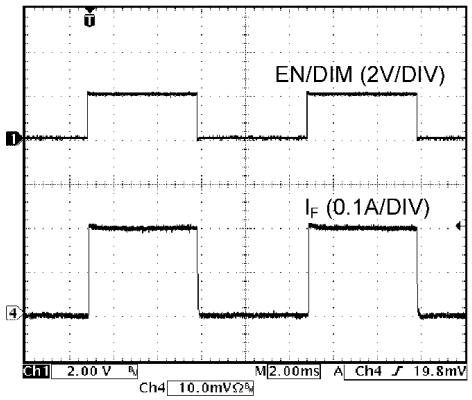


Figure 22. PWM Dimming With a 1-µF Feed-Forward Capacitor

8.1.5 Catch Diode (D1)

The catch diode (D1) conducts during the switch off-time. A Schottky diode is required for its fast switching time and low forward voltage drop. The catch diode should be chosen such that its current rating is greater than:

$$I_{D1} = I_F \times (1\text{-}D) \tag{20}$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward voltage drop.

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8.1.6 Boost Diode (D2)

A standard diode such as the 1N4148 type is recommended. For V_{BOOST} circuits derived from voltages less than 3.3V, a small-signal Schottky diode is recommended for better efficiency. A good choice is the BAT54 small signal diode.

8.1.7 Boost Capacitor (C3)

A 0.01µF ceramic capacitor with a voltage rating of at least 6.3V is sufficient. The X7R and X5R MLCCs provide the best performance.

8.1.8 Power Loss Estimation

The main power loss in LM3405A includes three basic types of loss in the internal power switch: conduction loss, switching loss, and gate charge loss. In addition, there is loss associated with the power required for the internal circuitry of IC.

The conduction loss is calculated as:

$$P_{COND} = \left(I_F^2 \times D\right) \times \left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_F}\right)^2\right) \times R_{DS(ON)} \quad (21)$$

If the inductor ripple current is fairly small (for example, less than 40%) , the conduction loss can be simplified to:

$$P_{COND} = I_F^2 \times R_{DS(ON)} \times D \quad (22)$$

The switching loss occurs during the switch on and off transition periods, where voltage and current overlap resulting in power loss. The simplest means to determine this loss is to empirically measure the rise and fall times (10% to 90%) of the voltage at the switch pin.

Switching power loss is calculated as follows:

$$P_{SW} = 0.5 \times V_{IN} \times I_F \times f_{SW} \times (T_{RISE} + T_{FALL}) \quad (23)$$

The gate charge loss is associated with the gate charge Q_G required to drive the switch:

$$P_G = f_{SW} \times V_{IN} \times Q_G \quad (24)$$

The power loss required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (25)$$

I_Q is the quiescent operating current, and is typically around 1.8mA for the LM3405A.

The total power loss in the IC is:

$$P_{INTERNAL} = P_{COND} + P_{SW} + P_G + P_Q \quad (26)$$

An example of power losses for a typical application is shown in Table 2:

Table 2. Power Loss Tabulation

CONDITIONS		POWER LOSS	
V_{IN}	12 V		
V_{OUT}	3.9 V		
I_{OUT}	1 A		
V_{D1}	0.45 V		
$R_{DS(ON)}$	300 mΩ	P_{COND}	108 mW
f_{SW}	1.6 MHz		
T_{RISE}	18 ns	P_{SW}	288 mW
T_{FALL}	12 ns		
I_Q	1.8 mA	P_Q	22 mW
Q_G	1.4 nC	P_G	27 mW
D is calculated to be 0.36			

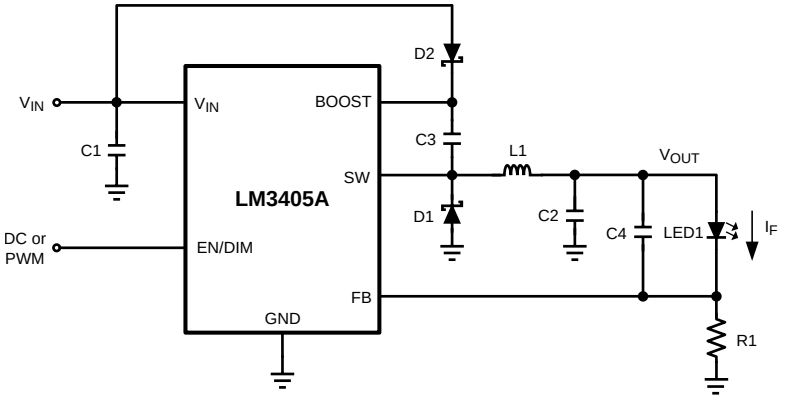
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$$\Sigma \left(P_{COND} + P_{SW} + P_Q + P_G \right) = P_{INTERNAL} \quad (27)$$

$$P_{INTERNAL} = 445mW \quad (28)$$

8.2 Typical Applications

8.2.1 V_{BOOST} Derived from V_{IN} (V_{IN} = 5 V, I_F = 1 A)



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Figure 23. V_{BOOST} Derived from V_{IN} (V_{IN} = 5 V, I_F = 1 A) Diagram

8.2.1.1 Design Requirements

- Input Voltage: V_{IN} = 5 V ± 10%
- LED Current: I_F = 1 A
- LED Forward Voltage: V_{LED} = 3.4 V
- Output Voltage: VOUT = 3.4 V + 0.2 V = 3.6 V
- Ripple Ratio: r < 0.6
- PWM Dimmable

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Calculate Duty Cycle (D)

Calculate the nominal duty cycle for calculations and ensure the maximum duty cycle will not be exceeded in the application using Equation 29:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{3.6V}{5V} = 0.72 \quad (29)$$

Using the same equation D_{MAX} can be calculated for the minimum input voltage of 4.5 V. The duty cycle at 4.5 V is 0.8 which is less than the minimum D_{MAX} of 0.85 specified in *Electrical Characteristics*.

8.2.1.2.2 Choose Capacitor Values (C1, C2, C3, and C4)

Low input voltage applications and PWM dimming applications generally require more input capacitance so the higher value of **C1 = 10 µF** is chosen for best performance. The other capacitor values chosen are the recommended values of **C2 = C4 = 1 µF** and **C3 = 0.01 µF**. All capacitors chosen are X5R or X7R dielectric ceramic capacitors of sufficient voltage rating.

8.2.1.2.3 Set the Nominal LED Current (R1)

The nominal LED current at 100% PWM dimming duty cycle is set by the resistor R1. R1 can be calculated using Equation 30:

$$R1 = \frac{V_{FB}}{I_F} = \frac{0.205V}{1A} = 0.205\Omega \quad (30)$$

Typical Applications (continued)

The standard value of **R1 = 0.2Ω** is chosen. R1 should have a power rating of at least 1/4 W.

8.2.1.2.4 Choose Diodes (D1 and D2)

For the boost diode, D2, choose a low current diode with a voltage rating greater than the input voltage to give some margin. D2 should also be a schottky to minimize the forward voltage drop. For this example a schottky diode of **D2 = 100 mA, 30 V** is chosen. The catch diode, D1, should be a schottky diode and should have a voltage rating greater than the input voltage and a current rating greater than the average current. The average current in D1 can be calculated with Equation 31:

$$I_{D1} = I_F \times (1 - D) = 1A \times (1 - 0.72) = 0.28A \quad (31)$$

For this example **D1 = 1 A, 10 V** is chosen.

8.2.1.2.5 Calculate the Inductor Value (L1)

The inductor value is chosen for a given ripple ratio (r). To calculate L1 the forward voltage of D1 is required. In this case the chosen diode has a forward voltage drop of V_F = 0.37 V. Given the desired ripple ratio L1 is calculated as:

$$L = \frac{V_{OUT} + V_{D1}}{I_F \times r \times f_{SW}} = \frac{3.6V + 0.37V}{1A \times 0.6 \times 1.6MHz} = 4.14\mu H \quad (32)$$

The next larger standard value of **L1 = 4.7 µH** is chosen. A ripple ratio of 0.6 translates to a Δi_L of 600 mA and a peak inductor current of 1.3 A ($I_F + \Delta i_L/2$). Choose an inductor with a saturation current rating of greater than 1.3 A.

Table 3. Bill of Materials for Figure 23

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A LED Driver	LM3405A	Texas Instruments
C1, Input Cap	10 µF, 6.3 V, X5R	C3216X5R0J106M	TDK
C2, Output Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
C3, Boost Cap	0.01 µF, 16 V, X7R	0805YC103KAT2A	AVX
C4, Feedforward Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
D1, Catch Diode	Schottky, 0.37 V at 1A, V_R = 10 V	MBRM110LT1G	ON Semiconductor
D2, Boost Diode	Schottky, 0.36 V at 15 mA	CMDSH-3	Central Semiconductor
L1	4.7 µH, 1.6 A	SLF6028T-4R7M1R6	TDK
R1	0.2 Ω, 0.5 W, 1%	WSL2010R2000FEA	Vishay
LED1	1.5 A, White LED	LXK2-PW14	Lumileds

8.2.1.3 Application Curve

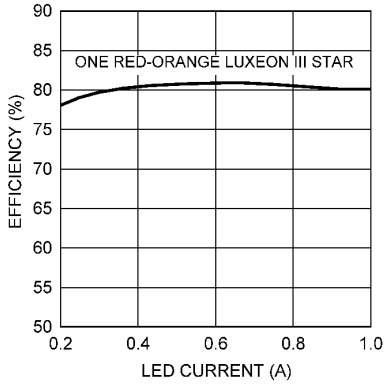
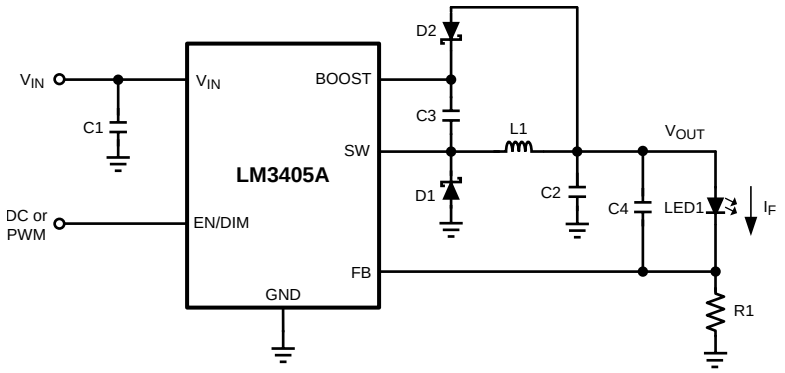


Figure 24. Efficiency vs Input Voltage

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8.3 System Examples

8.3.1 V_{BOOST} Derived from V_{OUT} (V_{IN} = 12 V, I_F = 1 A)



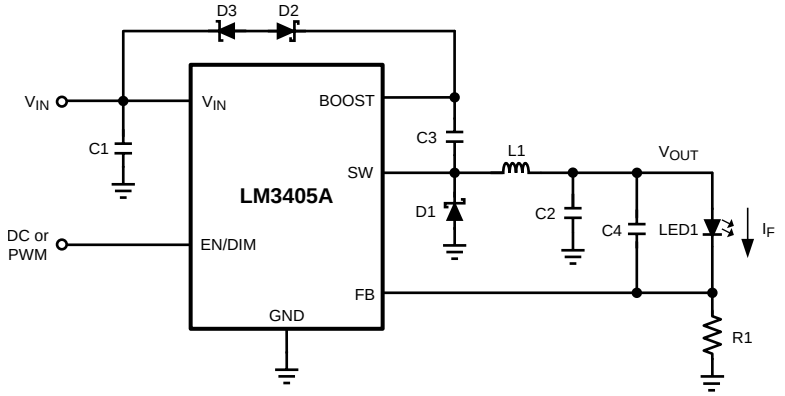
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Figure 25. V_{BOOST} Derived from V_{OUT} (V_{IN} = 12 V, I_F = 1 A) Diagram

Table 4. Bill of Materials for Figure 25

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A LED Driver	LM3405A	Texas Instruments
C1, Input Cap	10 µF, 25 V, X5R	ECJ-3YB1E106K	Panasonic
C2, Output Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
C3, Boost Cap	0.01 µF, 16 V, X7R	0805YC103KAT2A	AVX
C4, Feedforward Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
D1, Catch Diode	Schottky, 0.5 V at 1 A, V_R = 30 V	SS13	Vishay
D2, Boost Diode	Schottky, 0.36 V at 15 mA	CMDSH-3	Central Semiconductor
L1	4.7 µH, 1.6 A	SLF6028T-4R7M1R6	TDK
R1	0.2 Ω, 0.5 W, 1%	WSL2010R2000FEA	Vishay
LED1	1.5 A, White LED	LXK2-PW14	Lumileds

8.3.2 V_{BOOST} Derived from V_{IN} through a Series Zener Diode (D3) (V_{IN} = 15 V, I_F = 1 A)



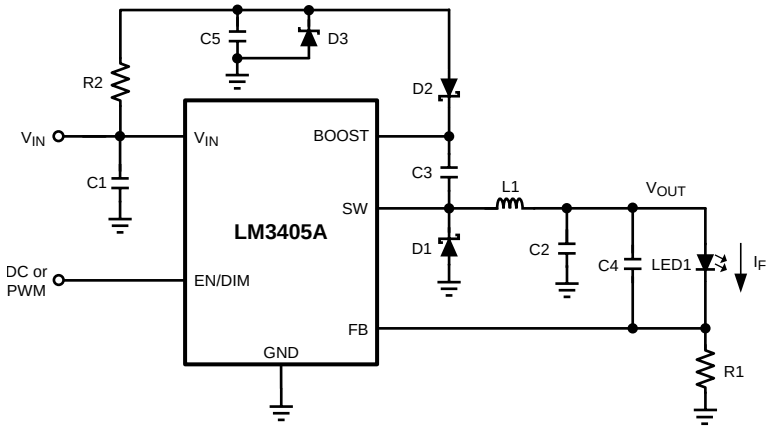
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Figure 26. V_{BOOST} Derived from V_{IN} through a Series Zener Diode (D3) (V_{IN} = 15 V, I_F = 1 A) Diagram

Table 5. Bill of Materials for Figure 26

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A LED Driver	LM3405A	Texas Instruments
C1, Input Cap	10 µF, 25 V, X5R	ECJ-3YB1E106K	Panasonic
C2, Output Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
C3, Boost Cap	0.01 µF, 16 V, X7R	0805YC103KAT2A	AVX
C4, Feedforward Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
D1, Catch Diode	Schottky, 0.5 V at 1A, V_R = 30 V	SS13	Vishay
D2, Boost Diode	Schottky, 0.36 V at 15 mA	CMDSH-3	Central Semiconductor
D3, Zener Diode	11 V, 350 mW, SOT-23	BZX84C11	Fairchild
L1	6.8 µH, 1.5 A	SLF6028T-6R8M1R5	TDK
R1	0.2 Ω, 0.5 W, 1%	WSL2010R2000FEA	Vishay
LED1	1.5 A, White LED	LXK2-PW14	Lumileds

8.3.3 V_{BOOST} Derived from V_{IN} through a Shunt Zener Diode (D3) (V_{IN} = 18 V, I_F = 1 A)



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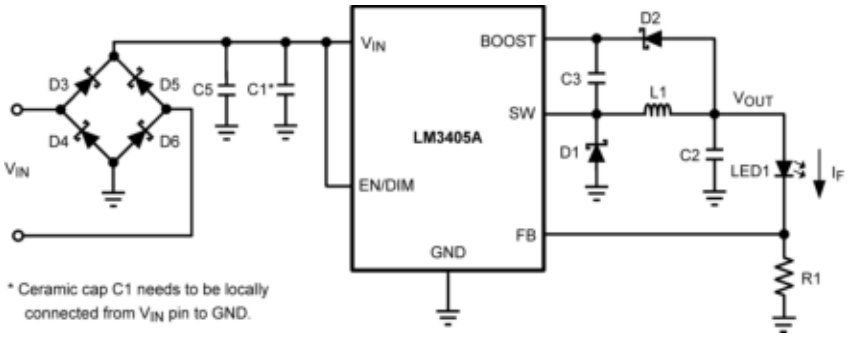
Figure 27. V_{BOOST} Derived From V_{IN} Through a Shunt Zener Diode (D3) (V_{IN} = 18 V, I_F = 1 A) Diagram

Table 6. Bill of Materials for Figure 27

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A LED Driver	LM3405A	Texas Instruments
C1, Input Cap	10 µF, 25 V, X5R	ECJ-3YB1E106K	Panasonic
C2, Output Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
C3, Boost Cap	0.01 µF, 16 V, X7R	0805YC103KAT2A	AVX
C4, Feedforward Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
C5, Shunt Cap	0.1 µF, 16 V, X7R	GRM219R71C104KA01D	Murata
D1, Catch Diode	Schottky, 0.5 V at 1 A, V_R = 30 V	SS13	Vishay
D2, Boost Diode	Schottky, 0.36 V at 15 mA	CMDSH-3	Central Semiconductor
D3, Zener Diode	4.7 V, 35 0mW, SOT-23	BZX84C4 V7	Fairchild
L1	6.8 µH, 1.5 A	SLF6028T-6R8M1R5	TDK
R1	0.2 Ω, 0.5 W, 1%	WSL2010R2000FEA	Vishay
R2	1.91 kΩ, 1%	CRCW08051K91FKEA	Vishay
LED1	1.5 A, White LED	LXK2-PW14	Lumileds

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8.3.4 LED MR16 Lamp Application (V_{IN} = 12-V AC, I_F = 0.75 A)



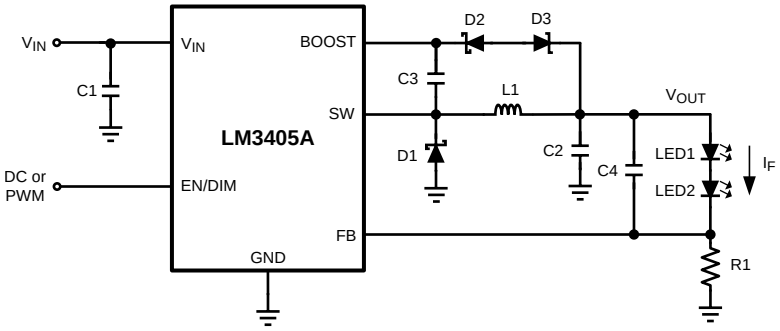
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Figure 28. LED MR16 Lamp Application (V_{IN} = 12-V AC, I_F = 0.75 A) Diagram

Table 7. Bill of Materials for Figure 28

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A LED Driver	LM3405A	Texas Instruments
C1, Input Cap	10 µF, 25 V, X5R	ECJ-3YB1E106K	Panasonic
C2, Output Cap	1 µF, 10 V, X7R	GRM319R71A105KC01D	Murata
C3, Boost Cap	0.01 µF, 16 V, X7R	0805YC103KAT2A	AVX
C5, Input Cap	220 µF, 25 V, electrolytic	ECE-A1EN221U	Panasonic
D1, Catch Diode	Schottky, 0.5 V at 1 A, V_R = 30 V	SS13	Vishay
D2, Boost Diode	Schottky, 0.36 V at 15 mA	CMDSH-3	Central Semiconductor
D3, Rectifier Diode	Schottky, 0.385 V at 500 mA	CMHSH5-2L	Central Semiconductor
D4, Rectifier Diode	Schottky, 0.385 V at 500 mA	CMHSH5-2L	Central Semiconductor
D5, Rectifier Diode	Schottky, 0.385 V at 500 mA	CMHSH5-2L	Central Semiconductor
D6, Rectifier Diode	Schottky, 0.385 V at 500 mA	CMHSH5-2L	Central Semiconductor
L1	6.8 µH, 1.5 A	SLF6028T-6R8M1R5	TDK
R1	0.27 Ω, 0.33 W, 1%	ERJ8BQFR27	Panasonic
LED1	1 A, White LED	LXHL-PW09	Lumileds

8.3.5 V_{BOOST} Derived from V_{OUT} through a Series Zener Diode (D3) (V_{IN} = 18 V, I_F = 1 A)



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Figure 29. V_{BOOST} Derived from V_{OUT} Through a Series Zener Diode (D3) (V_{IN} = 18 V, I_F = 1 A) Diagram

Table 8. Bill of Materials for Figure 29

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A LED Driver	LM3405A	Texas Instruments
C1, Input Cap	10 µF, 25 V, X5R	ECJ-3YB1E106K	Panasonic
C2, Output Cap	1 µF, 16 V, X7R	GRM319R71A105KC01D	Murata
C3, Boost Cap	0.01 µF, 16 V, X7R	0805YC103KAT2A	AVX
C4, Feedforward Cap	1 µF, 16 V, X7R	GRM319R71A105KC01D	Murata
D1, Catch Diode	Schottky, 0.5 V at 1 A, V_R = 30 V	SS13	Vishay
D2, Boost Diode	Schottky, 0.36 V at 15 mA	CMDSH-3	Central Semiconductor
D3, Zener Diode	3.6 V, 350 mW, SOT-23	BZX84C3V6	Fairchild
L1	6.8 µH, 1.5 A	SLF6028T-6R8M1R5	TDK
R1	0.2 Ω, 0.5 W, 1%	WSL2010R2000FEA	Vishay
LED1	1.5 A, White LED	LXK2-PW14	Lumileds
LED2	1.5 A, White LED	LXK2-PW14	Lumileds

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9 Power Supply Recommendations

Any DC output power supply may be used provided it has a high enough voltage and current rating required for the particular application.

10 Layout

10.1 Layout Guidelines

When planning the layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration when completing the layout is the close coupling of the GND connections of the input capacitor C1 and the catch diode D1. These ground ends should be close to one another and be connected to the GND plane with at least two vias. Place these components as close to the IC as possible. The next consideration is the location of the GND connection of the output capacitor C2, which should be near the GND connections of C1 and D1.

There should be a continuous ground plane on the bottom layer of a two-layer board.

The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup that causes inaccurate regulation. The LED current setting resistor R1 should be placed as close as possible to the IC, with the GND of R1 placed as close as possible to the GND of the IC. The V_{OUT} trace to LED anode should be routed away from the inductor and any other traces that are switching.

High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components should also be placed as close as possible to the IC. See *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* (SNVA054) for further considerations and the LM3405A demo board as an example of a four-layer layout.

10.2 Layout Example

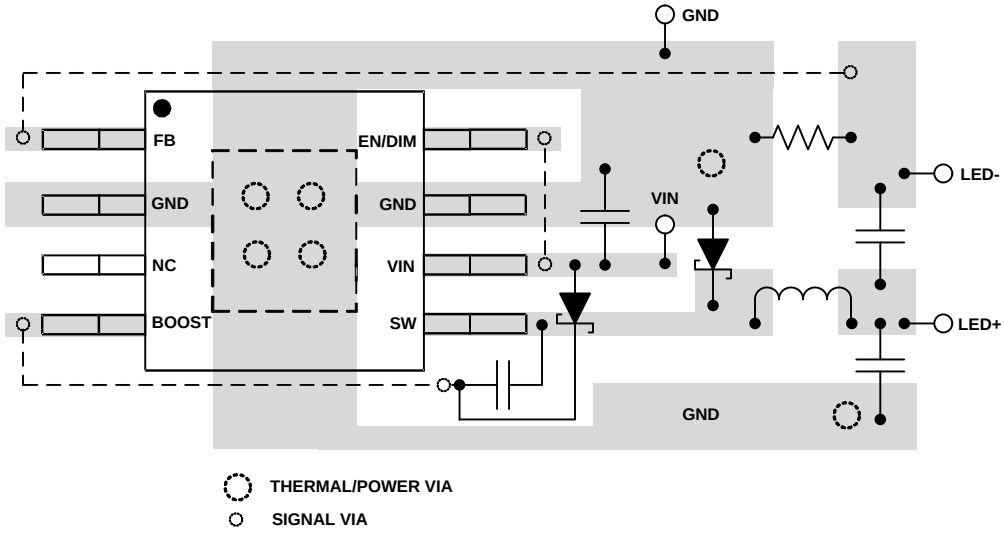


Figure 30. Layout Example (MSOP-PowerPAD Package, Schematic in Figure 23)

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* (SNVA054)
- *AN-1644 Powering and Dimming High-Brightness LEDs with the LM3405 Constant-Current Buck Regulator* (SNVA247)
- *AN-1656 Design Challenges of Switching LED Drivers* (SNVA253)
- *AN-1685 LM3405A Demo Board* (SNVA271)
- *AN-1899 LM3405A VSSOP Evaluation Board* (SNVA370)
- *AN-1982 Small, Wide Input Voltage Range LM2842 Keeps LEDs Cool* (SNVA402)
- *LM3405A Reference Design for MR16 LED Bulb, 600mA* (SNVU101)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3405AXMK/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSEB
LM3405AXMK/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSEB
LM3405AXMKE/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSEB
LM3405AXMKE/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSEB
LM3405AXMKX/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSEB
LM3405AXMKX/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSEB
LM3405AXMY/NOPB	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	SVSA
LM3405AXMY/NOPB.A	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVSA
LM3405AXMYX/NOPB	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	SVSA
LM3405AXMYX/NOPB.A	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVSA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

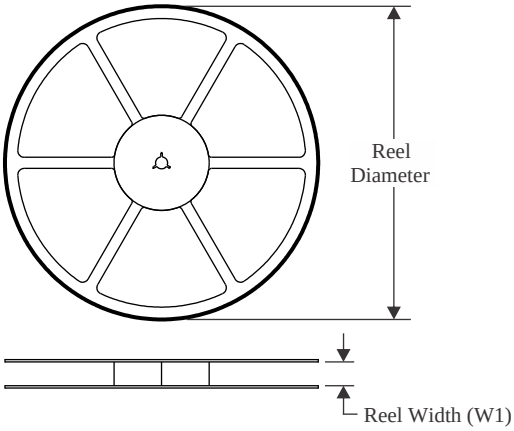
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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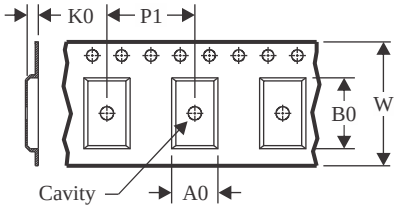
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

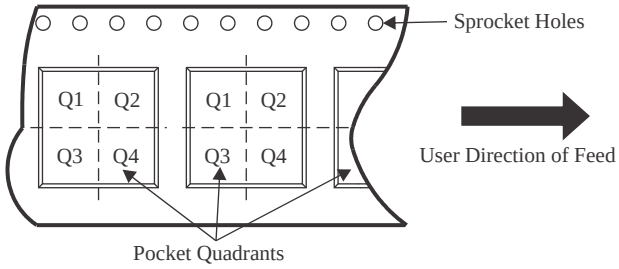


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

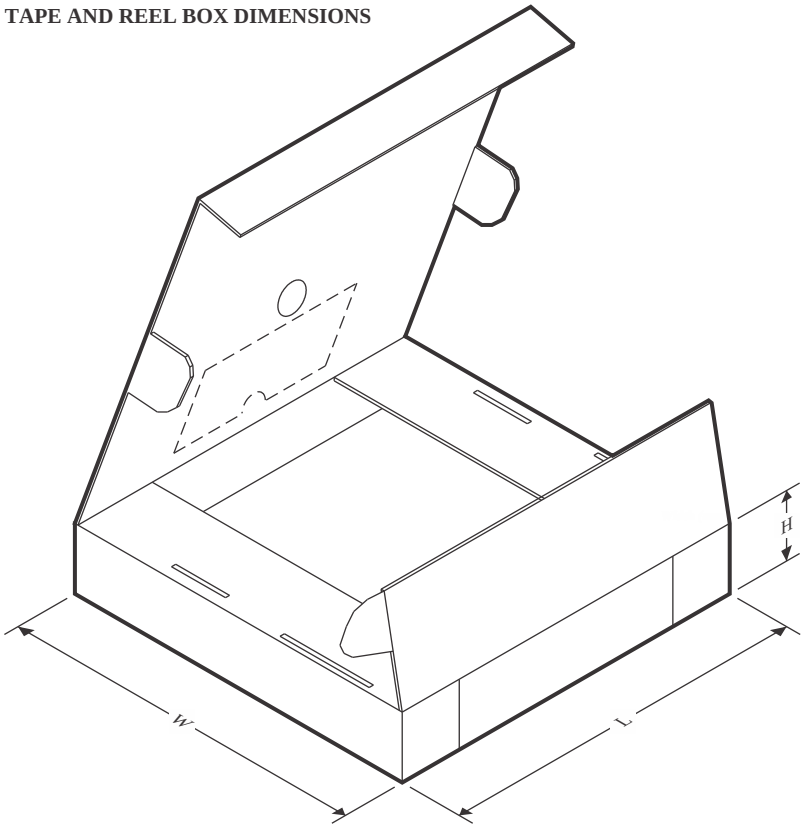
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3405AXMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3405AXMKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3405AXMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3405AXMY/NOPB	HVSSOP	DGN	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3405AXMYX/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

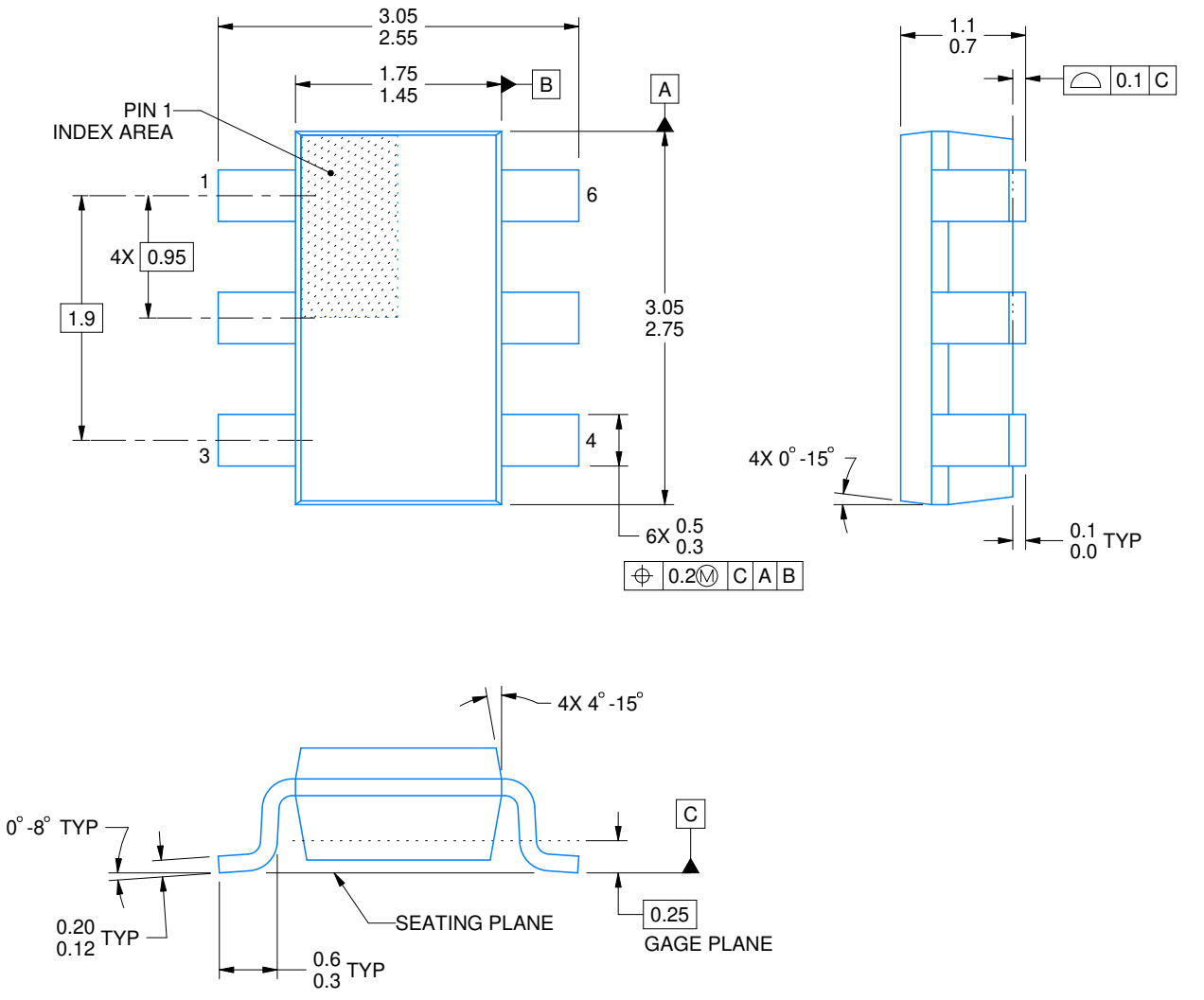
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3405AXMK/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LM3405AXMKE/NOPB	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LM3405AXMKX/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LM3405AXMY/NOPB	HVSSOP	DGN	8	1000	208.0	191.0	35.0
LM3405AXMYX/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

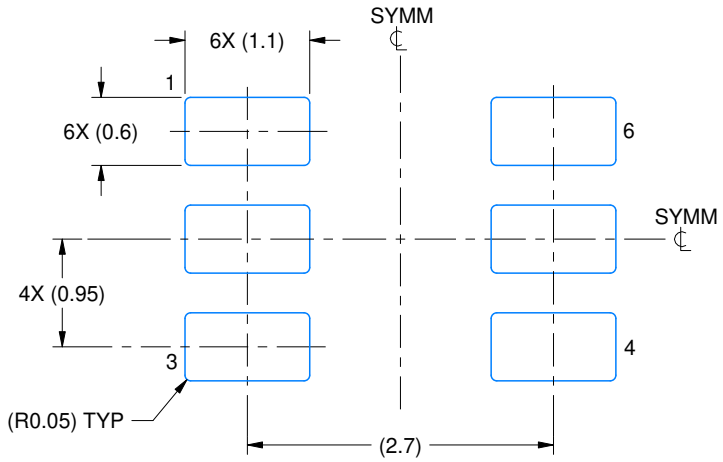
SMALL OUTLINE TRANSISTOR



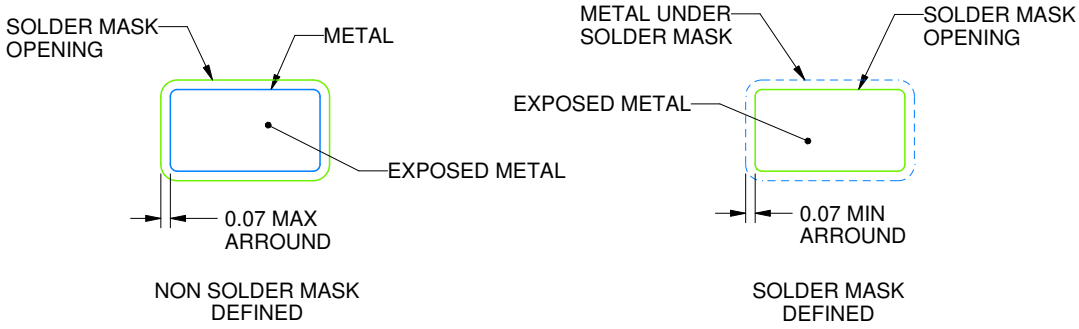
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

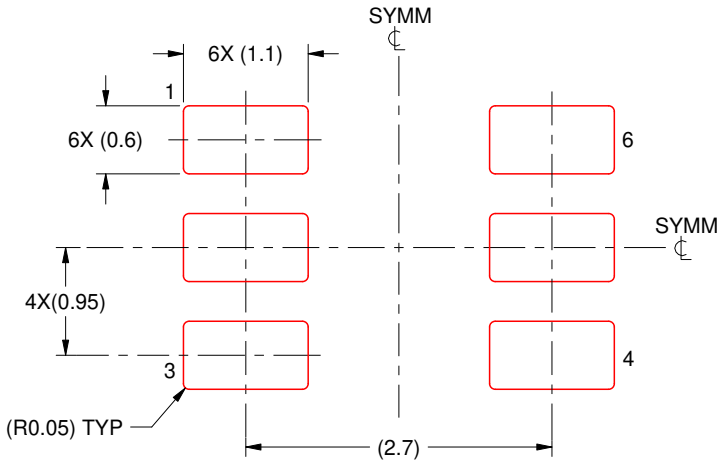


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

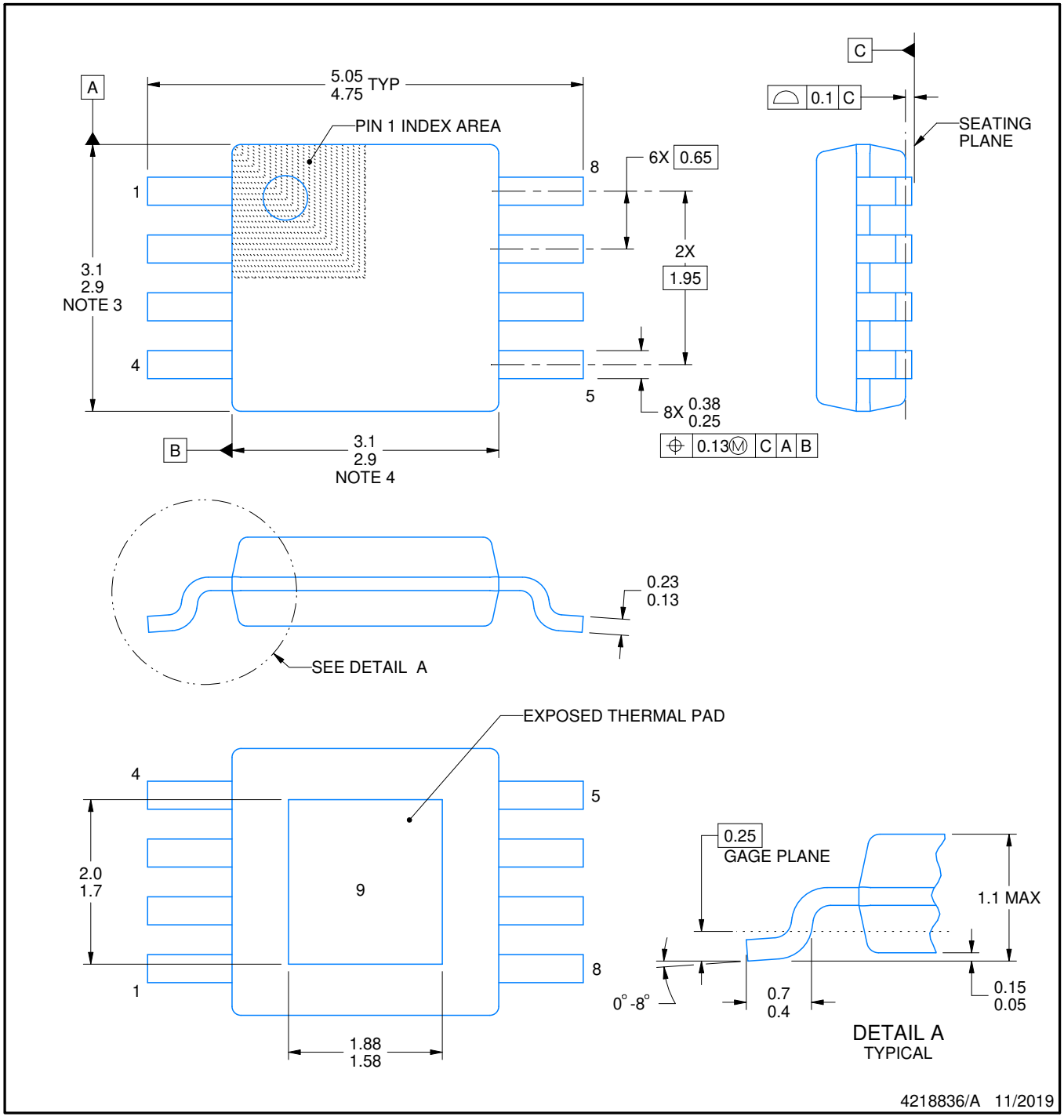
PACKAGE OUTLINE

DGN0008A



PowerPAD™ VSSOP - 1.1 mm max height

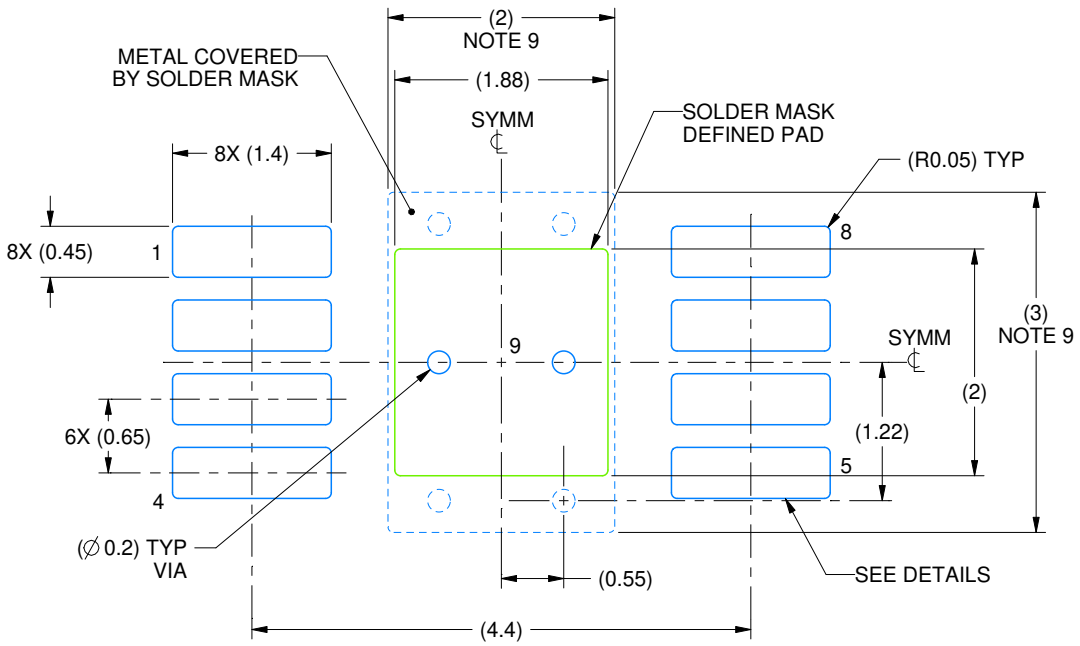
SMALL OUTLINE PACKAGE



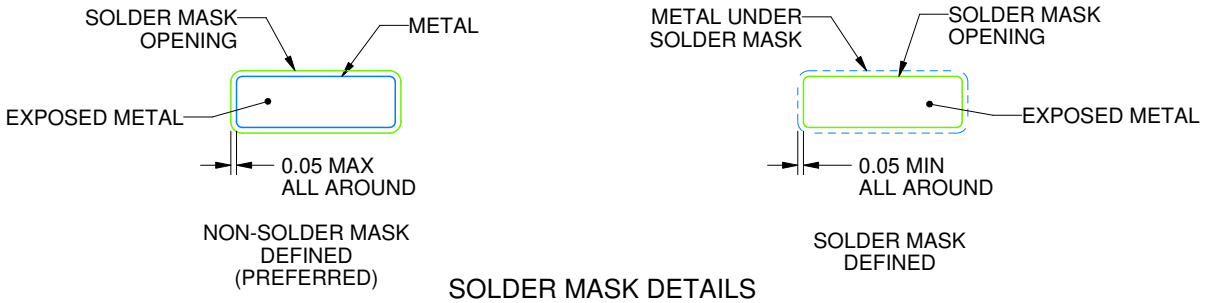
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

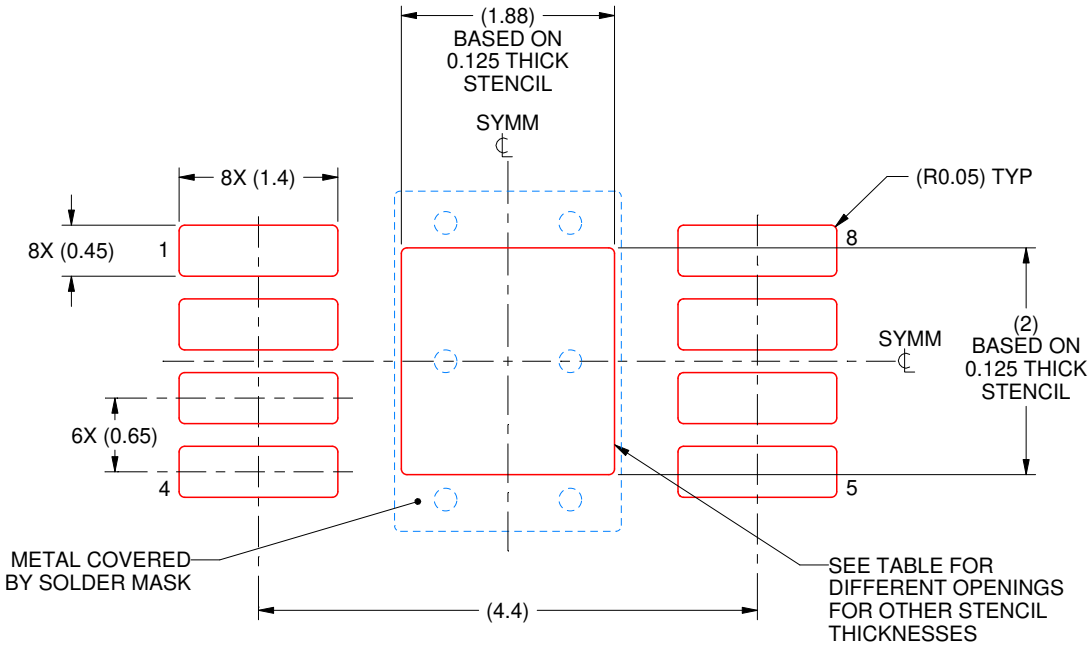


SOLDER MASK DETAILS

4218836/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

4218836/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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