LM342x N -Channel Controllers for Constant-Current LED Drivers

1 Features

- V_{IN} Range From 4.5 V to 75 V
- High-Side Adjustable Current Sense
- 2-Ω, 1-A Peak MOSFET Gate Driver
- Input Undervoltage and Output Overvoltage Protection
- PWM and Analog Dimming
- Cycle-by-Cycle Current Limit
- Programmable Switching Frequency
- Zero Current Shutdown and Thermal Shutdown
- LED Output Status Flag (LM3423 and LM3423-Q0 Only)
- Fault Status Flag and Timer(LM3423 and LM3423-Q0 Only)

2 Applications

- LED Drivers: Buck, Boost, Buck-Boost, and SEPIC
- Indoor and Outdoor Area SSL
- Automotive
- General Illumination
- Constant-Current Regulators

3 Description

The LM3421 and LM3423 family of devices are versatile high voltage N-channel MOSFET controllers for LED drivers. They can be easily configured in buck, boost, buck-boost and SEPIC topologies. This flexibility, along with an input voltage rating of 75 V, makes the these controllers ideal for illuminating LEDs in a large family of applications.

Adjustable high-side current sense voltage allows for tight regulation of the LED current with the highest efficiency possible. The LM3421 and LM3423 devices use predictive off-time (PRO) control, which is a combination of peak current-mode control and a predictive off-timer. This method of control eases the design of loop compensation while providing inherent input voltage feed-forward compensation.

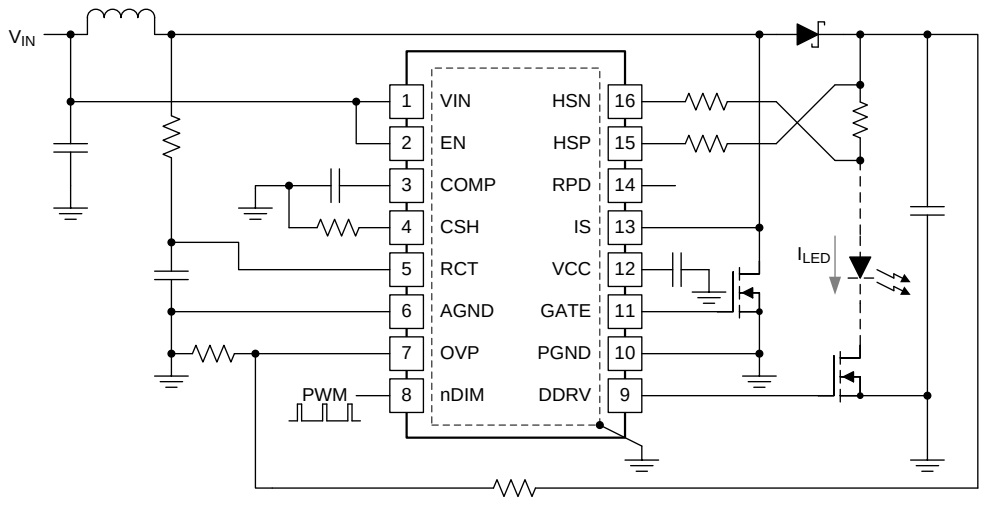
The LM3421 and LM3423 devices include a high-voltage start-up regulator that operates over a wide input range of 4.5 V to 75 V. The internal PWM controller is designed for adjustable switching frequencies of up to 2 MHz, thus enabling compact solutions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3421	HTSSOP (16)	5.00 mm × 4.40 mm
LM3423	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Boost Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2015) to Revision G — **Page**

- Deleted references to automotive grade (LM342x-Q1 and LM342x-Q0) devices, now available in data sheet SNVSB95 ... 1
- Corrected typographic error in Table 1 ... 3
- Changed *EN pulldown resistance* specification minimum value from: 0.45 MΩ to: 0.245 MΩ *Electrical Characteristics* table. ... 7
- Changed *EN pulldown resistance* specification maximum value from: 1.3 MΩ to: 2.85 MΩ in *Electrical Characteristics* table. ... 7

Changes from Revision E (April 2013) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (May 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 64

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5 Device Comparison

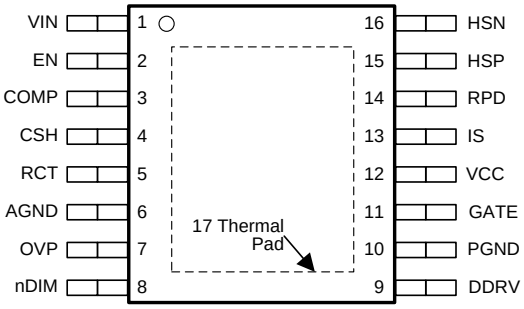
Table 1. Device Comparison

DEVICE	FLAG FEATURES		QUALIFACTION	TEMPERATURE RANGE, T_A
	LED OUTPUT	FAULT STATUS		
LM3421-Q0	No	No	AEC-Q100 Grade 0	–40°C to +150°C
LM3421-Q1	No	No	AEC-Q100 Grade 1	–40°C to +125°C
LM3423-Q0	Yes	Yes	AEC-Q100 Grade 0	–40°C to +150°C
LM3423-Q1	Yes	Yes	AEC-Q100 Grade 1	–40°C to +125°C
LM3421	No	No	Commercial Grade	–40°C to +125°C
LM3423	Yes	Yes	Commercial Grade	–40°C to +125°C

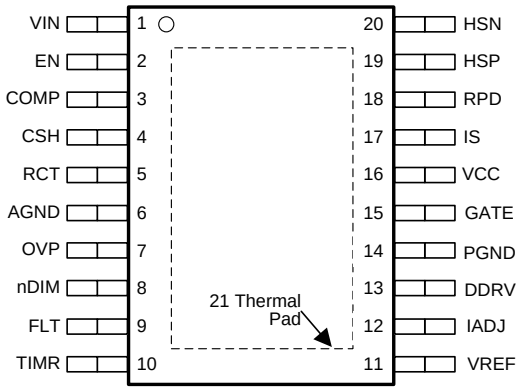
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6 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP
Top View



PWP Package
20-Pin HTSSOP
Top View



Pin Functions

PIN			I/O(1)	FUNCTION
NAME	LM3423	LM3421		
AGND	6	6	G	Analog ground. Connect to PGND through the DAP copper pad to provide ground return for CSH, COMP, RCT, and TIMR.
COMP	3	3	I	Compensation. Connect a capacitor to AGND to set the compensation.
CSH	4	4	I	Current sense high. Connect a resistor to AGND to set the signal current. For analog dimming, connect a controlled current source or a potentiometer to AGND as detailed in the *Analog Dimming* section.
DDRV	13	9	O	Dim gate drive output. Connect to the gate of the dimming MOSFET.
DPOL	12	—	I	Dim polarity. Connect to AGND if dimming with a series P-channel MOSFET or leave open when dimming with series N-channel MOSFET.
EN	2	2	I	Enable. Connect to AGND for zero current shutdown or apply more than 2.4 V to enable device.
FLT	9	—	I	Fault flag. Connect to pullup resistor from VIN and N-channel MOSFET open-drain output is high when a fault condition is latched by the timer.
GATE	15	11	O	Main gate drive output. Connect to the gate of the main switching MOSFET.
HSN	20	16	I	LED current sense negative. Connect through a series resistor to the negative side of the LED current sense resistor.
HSP	19	15	I	LED current sense positive. Connect through a series resistor to the positive side of the LED current sense resistor.
IS	17	13	I	Main switch current sense. Connect to the drain of the main N-channel MOSFET switch for R_{DS-ON} sensing or to a sense resistor installed in the source of the same device.
LRDY	11	—	O	LED ready flag. Connect to pullup resistor from VIN and N-channel MOSFET open-drain output pulls down when the LED current is not in regulation.
nDIM	8	8	I	Dimming input and undervoltage protection. Connect a PWM signal for dimming as detailed in the *PWM Dimming* section and/or a resistor divider from V_{IN} to program input undervoltage lockout (UVLO). Turnon threshold is 1.24 V and hysteresis for turnoff is provided by a 23-µA current source.
OVP	7	7	I	Overvoltage protection. Connect to a resistor divider from V_O to program output overvoltage lockout (OVLO). Turnoff threshold is 1.24 V and hysteresis for turnon is provided by 23-µA current source.
PGND	14	10	G	Power ground. Connect to AGND through the DAP copper pad to provide ground return for GATE and DDRV.
RCT	5	5	I	Resistor capacitor timing. External RC network sets the predictive off-time and thus the switching frequency.

(1) G = Ground, I = Input, O = Output

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Pin Functions (continued)

PIN			I/O(1)	FUNCTION
NAME	LM3423	LM3421		
RPD	18	14	I	Resistor pulldown. Connect the low side of all external resistor dividers (V_{IN} UVLO, OVP) to implement zero-current shutdown.
TIMR	10	—	I	Fault timer. Connect a capacitor to AGND to set the time delay before a sensed fault condition is latched.
V_{IN}	1	1	I	Input voltage. Bypass with 100-nF capacitor to AGND as close to the device as possible in the printed-circuit-board layout.
V_{CC}	16	12	I	Internal regulator output. Bypass with 2.2-µF to 3.3-µF ceramic capacitor to PGND.
Thermal PAD			G	Thermal PAD on bottom of IC. Star ground, connecting AGND and PGND.
DAP	DAP (21)	DAP (17)	G	Star ground, connecting AGND and PGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN}, EN, RPD, nDIM	–0.3	76	V
	–1 continuous		mA
OVP, HSP, HSN, LRDY, FLT, DPOL	–0.3	76	V
	–100 continuous		µA
RCT	–0.3	76	V
	–1 continuous	5 continuous	mA
IS	–0.3	76	V
	–2 for 100 ns		
	–1 continuous		mA
V_{CC}	–0.3	8	V
TIMR	–0.3	7	V
	–100 continuous	100 continuous	µA
COMP, CSH	–0.3	6	V
	–200 continuous	200 continuous	µA
GATE, DDRV	–0.3	V_{CC}	V
	–2.5 for 100 ns	V_{CC}+ 2.5 for 100 ns	
	–1 continuous	1 continuous	mA
PGND	–0.3	0.3	V
	–2.5 for 100 ns	2.5 for 100 ns	
Continuous power dissipation	Internally Limited		
Maximum junction temperature	Internally Limited		
Maximum lead temperature (solder and reflow) (3)		260	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Refer to http://www.ti.com/packaging for more detailed information and mounting techniques.

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7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Operating junction temperature, T_J	LM3421 , LM3423	−40	125	°C
Input voltage, V_{IN}		4.5	75	V

7.4 Thermal Information

THERMAL METRIC (1)		LM3421 PWP (HTSSOP) 16 PINS	LM3423 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	36.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.1	21.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.8	18	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.6	17.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{IN} = 14, −40°C ≤ T_J ≤ 125°C unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
START-UP REGULATOR							
V_{CCREG}	V_{CC} regulation	I_{CC} = 0 mA		6.3		7.35	V
		I_{CC} = 0 mA, T_A = 25°C			6.9		
I_{CCLIM}	V_{CC} current limit	V_{CC} = 0 V		20			mA
		V_{CC} = 0 V, T_A = 25°C			25		
I_Q	Quiescent Current	V_{EN} = 3 V, Static				3	mA
		V_{EN} = 3 V, Static, T_A = 25°C			2		
I_{SD}	Shutdown current	V_{EN} = 0 V				1	µA
		V_{EN} = 0 V, T_A = 25°C			0.1		
V_{CC} SUPPLY							
V_{CCUV}	V_{CC} UVLO Threshold	V_{CC} Increasing				4.5	V
		V_{CC} Increasing, T_A = 25°C			4.17		
		V_{CC} Decreasing		3.7			
		V_{CC} Decreasing, T_A = 25°C			4.08		
V_{CCHYS}	V_{CC} UVLO Hysteresis	T_A = 25°C			0.1		V
ENABLE THRESHOLDS							
EN_{ST}	EN start-up threshold	V_{EN} Increasing				2.4	V
		V_{EN} Increasing, T_A = 25°C			1.75		
EN_{ST}	EN start-up threshold	V_{EN} Decreasing		0.8			V
		V_{EN} Decreasing, T_A = 25°C			1.63		
EN_{STHYS}	EN start-up hysteresis	T_A = 25°C			0.1		V
R_{EN}	EN pulldown resistance	V_{EN} = 1 V		0.245		2.85	MΩ
		V_{EN} = 1 V, T_A = 25°C			0.82		
CSH THRESHOLDS							
	CSH high fault	CSH Increasing, T_A = 25°C			1.6		V
	CSH low condition on LRDY Pin	CSH increasing, T_A = 25°C	LM3423		1		V
OV THRESHOLDS							
OVP_{CB}	OVP OVLO threshold	OVP Increasing		1.185		1.285	V
		OVP Increasing, T_A = 25°C			1.24		
OVP_{HYS}	OVP hysteresis source current	OVP Active (high)		20		25	µA
		OVP Active (high), T_A = 25°C			23		

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Electrical Characteristics (continued)

V_{IN} = 14, −40°C ≤ T_J ≤ 125°C unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DPOL THRESHOLDS						
$DPOL_{THRSH}$	DPOL logic threshold	DPOL Increasing	2		2.6	V
		DPOL Increasing, T_A = 25°C		2.3		
R_{DPOL}	DPOL pullup resistance				1200	kΩ
		T_A = 25°C		500		
FAULT TIMER						
V_{FLTTH}	Fault threshold		1.185		1.29	V
		T_A = 25°C		1.24		
I_{FLT}	FAULT pin source current		10		13	µA
		T_A = 25°C		11.5		
ERROR AMPLIFIER						
V_{REF}	CSH reference voltage	w/r/t to AGND	1.21		1.26	V
		w/r/t to AGND, T_J = 25°C		1.235		
	Error amplifier input bias current	T_J = 25°C	–0.6	0	0.6	µA
	COMP sink or source current		22		35	µA
		T_J = 25°C		30		
	Transconductance	T_J = 25°C		100		µA/V
	Linear input range	(1), T_J = 25°C		±125		mV
	Transconductance bandwidth	–6dB Unloaded Response (1), MIN = T_J = 25°C	0.5	1		MHz
OFF TIMER						
$t_{OFF(min)}$	Minimum OFF-time	RCT = 1 V through 1 kΩ			75	ns
		RCT = 1 V through 1 kΩ, T_J = 25°C		35		
R_{RCT}	RCT reset pulldown resistance				120	Ω
		T_J = 25°C		36		
V_{RCT}	V_{IN}/25 reference voltage	V_{IN} = 14 V	540		585	mV
		V_{IN} = 14 V, T_J = 25°C		565		
f	Continuous conduction switching frequency	2.2 nF > C_T > 470 pF, T_J = 25°C		(See (2))		Hz
PWM COMPARATOR						
	COMP-to-PWM offset voltage		700		900	mV
		T_J = 25°C		800		
CURRENT LIMIT (IS)						
I_{LIM}	Current limit threshold		215		275	mV
		T_J = 25°C		245		
	Current limit delay-to-output				75	ns
		T_J = 25°C		35		
t_{LEB}	Leading edge blanking (LEB) time		115		325	ns
		T_J = 25°C		210		
HIGH SIDE TRANSCONDUCTANCE AMPLIFIER						
	Input bias current	T_J = 25°C		11.5		µA
g_M	Transconductance		20			mA/V
		T_J = 25°C		119		

(1) Specified by design. Not production tested.
(2) f = 25/(C_T × R_T)

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Electrical Characteristics (continued)

V_{IN} = 14, −40°C ≤ T_J ≤ 125°C unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input offset current		–1.5		1.5	µA
		T_J = 25°C		0		
	Input offset voltage		–7		7	mV
		T_J = 25°C		0		
$g_{M(BW)}$	Transconductance bandwidth	I_{CSH} = 100 µA(1), T_J = 25°C	250	500		kHz
GATE DRIVER (GATE)						
$R_{SRC(GATE)}$	GATE sourcing resistance	GATE = High			6	Ω
		GATE = High, T_J = 25°C		2		
$R_{SNK(GATE)}$	GATE sinking resistance	GATE = Low			4.5	Ω
		GATE = Low, T_J = 25°C		1.3		
DIM DRIVER (DIM, DDRV)						
$nDIM_{VTH}$	nDIM / UVLO threshold		1.185		1.285	V
		T_J = 25°C		1.24		
$nDIM_{HYS}$	nDIM hysteresis current		20		25	µA
		T_J = 25°C		23		
$R_{SRC(DDRV)}$	DDRV sourcing resistance	DDRV = High			30	Ω
		DDRV = High, T_J = 25°C		13.5		
$R_{SNK(DDRV)}$	DDRV sinking resistance	DDRV = Low			10	Ω
		DDRV = Low, T_J = 25°C		3.5		

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Electrical Characteristics (continued)

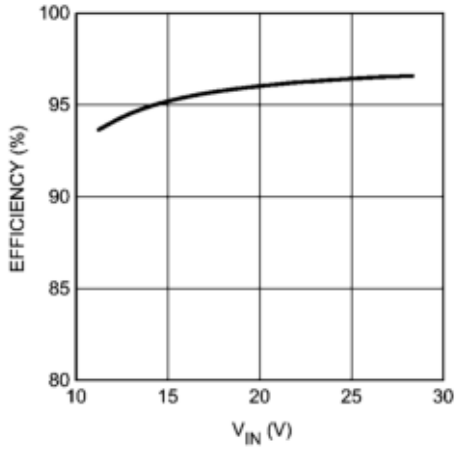
V_{IN} = 14, −40°C ≤ T_J ≤ 125°C unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULLDOWN N-CHANNEL MOSFETS						
R_{RPD}	RPD pulldown resistance				300	Ω
		T_J = 25°C		145		
R_{FLT}	FLT pulldown resistance				300	Ω
		T_J = 25°C		145		
R_{LRDY}	LRDY pulldown resistance				300	Ω
		T_J = 25°C		135		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold(1)	T_J = 25°C		165		°C
T_{HYS}	Thermal shutdown hysteresis(1)	T_J = 25°C		25		°C

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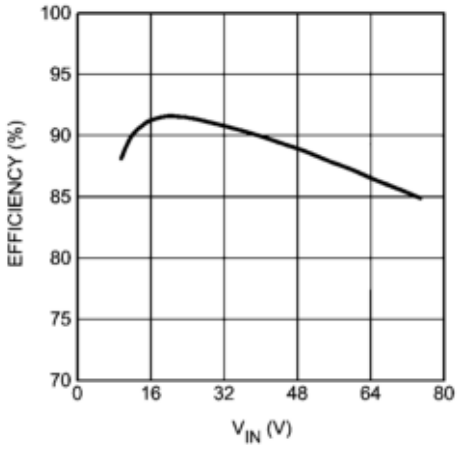
7.6 Typical Characteristics

T_A= 25°C, V_{IN} = 14 V unless otherwise specified



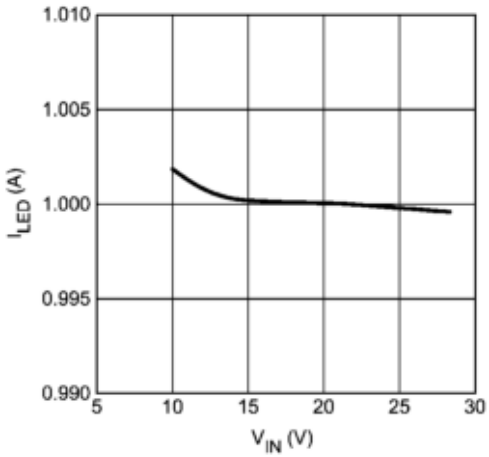
V_O = 32 V (9 LEDs)

Figure 1. Boost Efficiency vs. Input Voltage



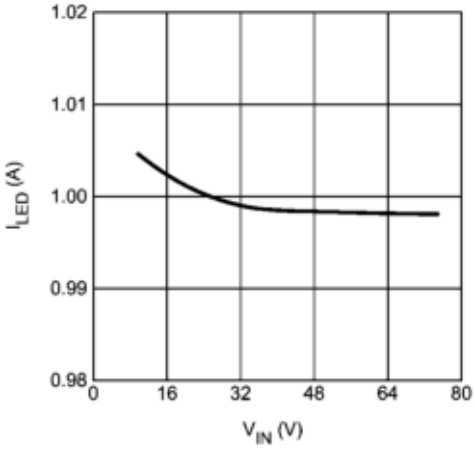
V_O = 21 V (6 LEDs)

Figure 2. Buck-Boost Efficiency vs. Input Voltage



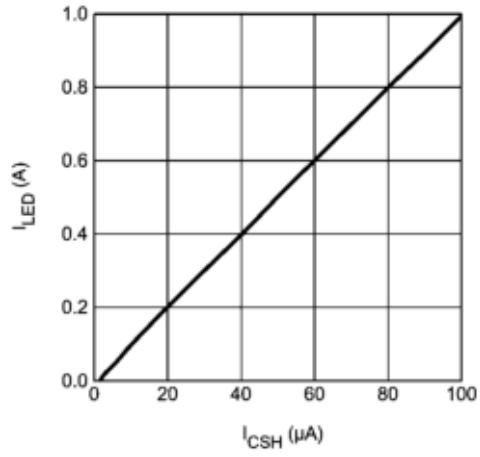
V_O = 32V (9 LEDs)

Figure 3. Boost LED Current vs. Input Voltage



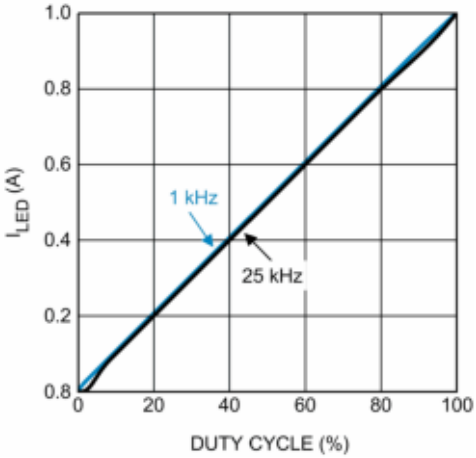
V_O = 21 V (6 LEDs)

Figure 4. Buck-Boost LED Current vs. Input Voltage



V_O = 21 V (6 LEDs), V_{IN} = 24 V

Figure 5. Analog Dimming



V_O = 32 V (9 LEDs), V_{IN} = 24 V

Figure 6. PWM Dimming

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Typical Characteristics (continued)

T_A= 25°C, V_{IN} = 14 V unless otherwise specified

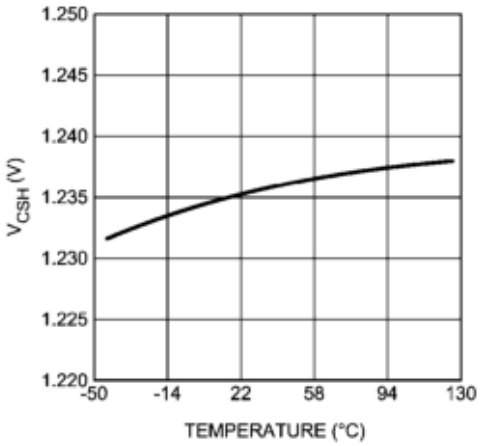


Figure 7. V_{CSH} vs Junction Temperature

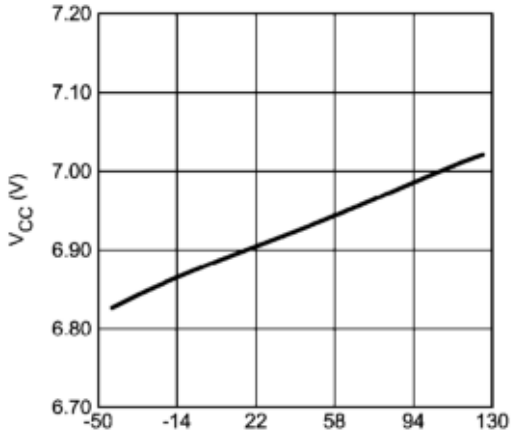


Figure 8. V_{CC} vs Junction Temperature

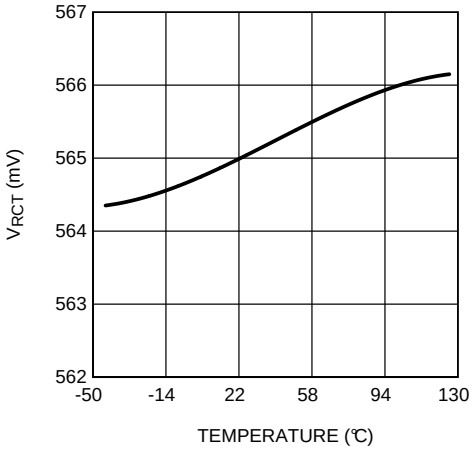


Figure 9. V_{RCT} vs Junction Temperature

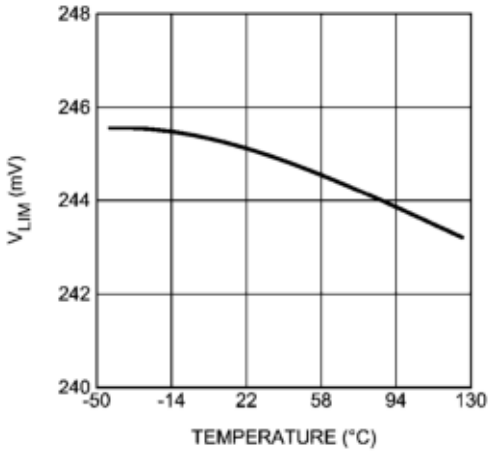


Figure 10. V_{LIM} vs Junction Temperature

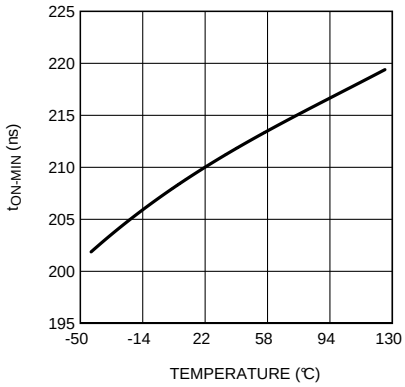


Figure 11. $t_{ON(min)}$ vs Junction Temperature

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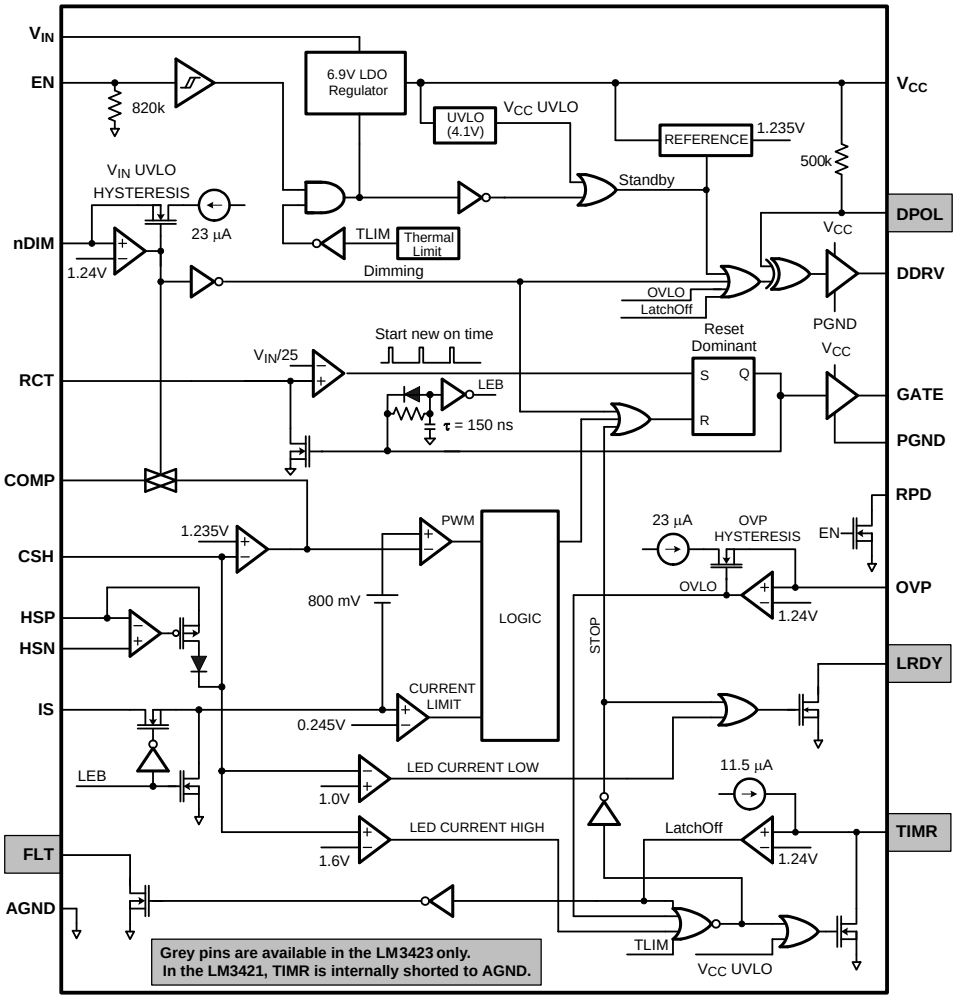
8 Detailed Description

8.1 Overview

The LM3421 and LM3423 are N-channel MOSFET (N-channel FET) controllers for buck, boost and buck-boost current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency.

The devices use a Predictive Off-time (PRO) control architecture that allows the regulator to be operated using minimal external control loop compensation, while providing an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current and the output enable and disable function with external dimming FET driver allows for fast PWM dimming of the LED load. The maximum attainable LED current is not internally limited because the device is a controller. Instead, current is a function of the system operating point, component choices, and switching frequency that allows the device to easily provide constant currents up to 5 A. This controller contains all the features necessary to implement a high-efficiency versatile LED driver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Current Regulators

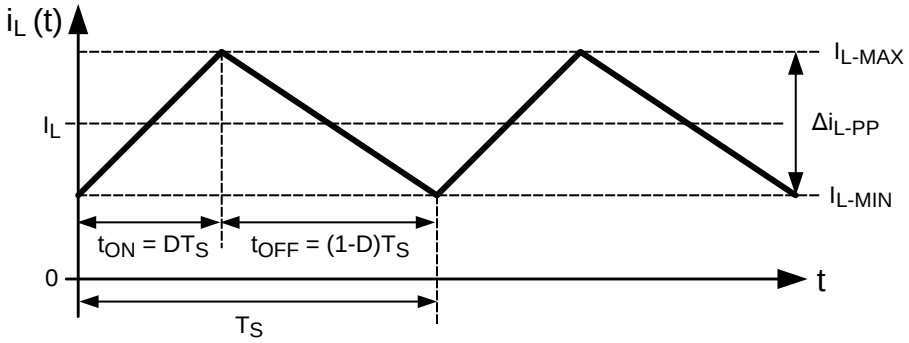


Figure 12. Ideal CCM Regulator Inductor Current $i_L(t)$

Current regulators can create three basic topologies: buck, boost, or buck-boost. All three topologies in their most basic form contain a main switching MOSFET, a recirculating diode, an inductor and capacitors. The controller is designed to drive a ground referenced N-channel FET which is perfect for a standard boost regulator. However, buck and buck-boost regulators usually have a high-side switch. When driving an LED load, a ground referenced load is often not necessary, therefore a ground referenced switch drives a floating load instead. The controller can then be used to drive all three basic topologies as shown in the *Basic Topology Schematics* section. Other topologies such as the SEPIC and flyback converter (both derivatives of the buck-boost) can be implemented as well.

Looking at the buck-boost design, the basic operation of a current regulator can be analyzed. During the time that the N-channel FET (Q1) is turned on (t_{ON}), the input voltage source stores energy in the inductor (L1) while the output capacitor (C_O) provides energy to the LED load. When Q1 is turned off (t_{OFF}), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both C_O and the LED load. Figure 12 shows the inductor current ($i_L(t)$) waveform for a regulator operating in CCM.

The average output LED current (I_{LED}) is proportional to the average inductor current (I_L) , therefore if I_L is tightly controlled, I_{LED} is well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate I_L and ultimately I_{LED}. For any current regulator, D is a function of the conversion ratio:

Buck

$$D = \frac{V_O}{V_{IN}} \tag{1}$$

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \tag{2}$$

Buck-boost

$$D = \frac{V_O}{V_O + V_{IN}} \tag{3}$$

8.3.2 Predictive Off-Time (PRO) Control

PRO control is used by the device to control I_{LED}. It is a combination of average peak current control and a one-shot off-timer that varies with input voltage. The LM3421 and LM3423 use peak current control to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MOSFET path or the MOSFET $R_{DS\text{-}ON}$ for both cycle-by-cycle current limit and input voltage feed forward. D is indirectly controlled by changes in both t_{OFF} and t_{ON}, which vary depending on the operating point.

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Feature Description (continued)

Even though the off-time control is quasi-hysteretic, the input voltage proportionality in the off-timer creates an essentially constant switching frequency over the entire operating range for boost and buck-boost topologies. The buck topology can be designed to give constant ripple over either input voltage or output voltage, however switching frequency is only constant at a specific operating point .

This type of control minimizes the control loop compensation necessary in many switching regulators, simplifying the design process. The averaging mechanism in the peak detection control loop provides extremely accurate LED current regulation over the entire operating range.

PRO control was designed to mitigate *current mode instability* (also called *sub-harmonic oscillation*) found in standard peak current mode control when operating near or above 50% duty cycles. When using standard peak current mode control with a fixed switching frequency, this condition is present, regardless of the topology. However, using a constant off-time approach, current mode instability cannot occur, enabling easier design and control.

Predictive off-time advantages:

- There is no current mode instability at any duty cycle.
- Higher duty cycles or voltage transformation ratios are possible, especially in the boost regulator.

The only disadvantage is that synchronization to an external reference frequency is generally not available.

8.3.3 Average LED Current

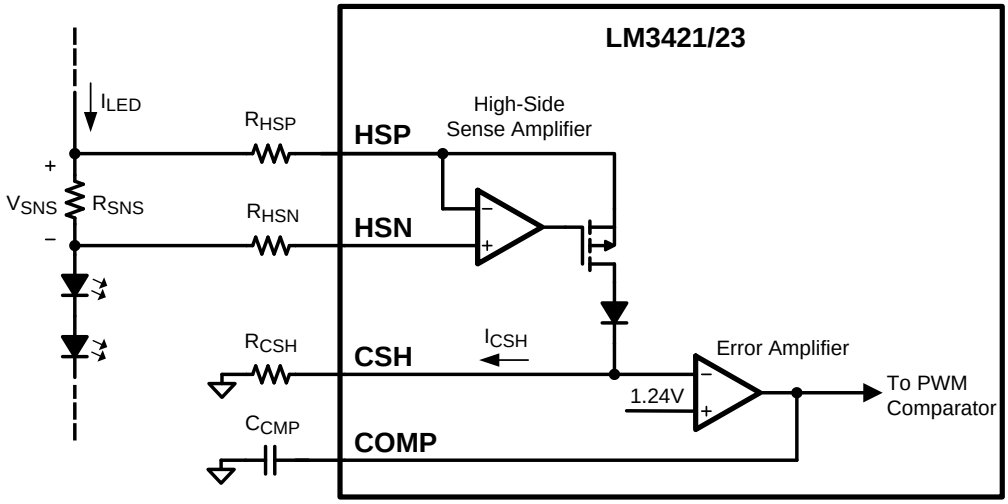


Figure 13. LED Current Sense Circuitry

The LM3421 and LM3423 use an external current sense resistor (R_{SNS}) placed in series with the LED load to convert the LED current (I_{LED}) into a voltage (V_{SNS}) as shown in Figure 13. The HSP and HSN pins are the inputs to the high-side sense amplifier which are forced to be equal potential (V_{HSP}=V_{HSN}) through negative feedback. Because of this, the V_{SNS} voltage is forced across R_{HSP} to generate the signal current (I_{CSH}) which flows out of the CSH pin and through the R_{CSH} resistor. The error amplifier regulates the CSH pin to 1.24 V, therefore I_{CSH} can be calculated using Equation 4.

$$I_{CSH} = \frac{V_{SNS}}{R_{HSP}} \tag{4}$$

This application regulates V_{SNS} as described in Equation 5.

$$V_{SNS} = 1.24V \times \frac{R_{HSP}}{R_{CSH}} \tag{5}$$

Calculate I_{LED} using Equation 6.

Feature Description (continued)

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \frac{1.24V}{R_{SNS}} \times \frac{R_{HSP}}{R_{CSH}} \quad (6)$$

The selection of the three resistors (R_{SNS}, R_{CSH}, and R_{HSP}) is not arbitrary. For matching and noise performance, the suggested signal current I_{CSH} is approximately 100 µA. This current does not flow in the LEDs and does not affect either the off-state LED current or the regulated LED current. I_{CSH} can be above or below this value, but the high-side amplifier offset characteristics may be affected slightly. In addition, to minimize the effect of the high-side amplifier voltage offset on LED current accuracy, the minimum V_{SNS} is suggested to be 50 mV. Place a resistor ($R_{HSN} = R_{HSP}$) in series with the HSN pin to cancel out the effects of the input bias current (approximately 10 µA) of both inputs of the high-side sense amplifier.

The sense resistor (R_{SNS}) can be placed anywhere in the series string of LEDs as long as the voltage at the HSN and HSP pins (V_{HSP} and V_{HSN}) satisfies the following conditions.

$$V_{HSP} < 76V$$
$$V_{HSN} > 3.5V \quad (7)$$

Typically, for a buck-boost configuration, R_{SNS} is placed at the bottom of the string (LED-) which allows for greater flexibility of input and output voltage. However, if there is substantial input voltage ripple allowed, it can help to place R_{SNS} at the top of the string (LED+) which limits the output voltage of the string to:

$$V_O = 76V - V_{IN} \quad (8)$$

The CSH pin can also be used as a low-side current sense input regulated to 1.24 V. The high-side sense amplifier is disabled if HSP and HSN are tied to AGND (or $V_{HSN} > V_{HSP}$) .

8.3.4 Analog Dimming

The CSH pin can be used to analog dim the LED current by adjusting the current sense voltage (V_{SNS}). There are several different methods to adjust V_{SNS} using the CSH pin:

1. External variable resistance: Adjust a potentiometer placed in series with R_{CSH} to vary V_{SNS}.
2. External variable current source: Source current (0 µA to I_{CSH}) into the CSH pin to adjust V_{SNS}.

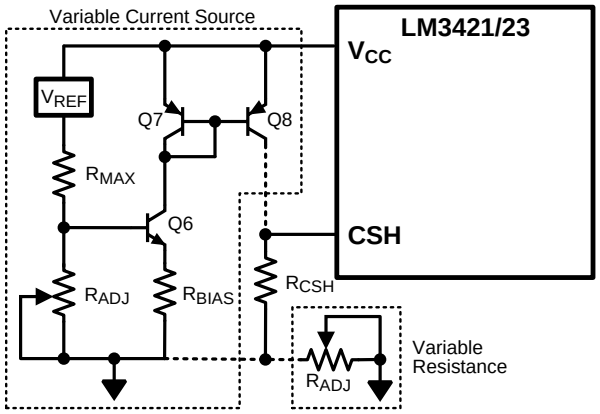


Figure 14. Analog Dimming Circuitry

In general, analog dimming applications require a lower switching frequency to minimize the effect of the leading edge blanking circuit. As the LED current is reduced, the output voltage and the duty cycle decreases. Eventually, the minimum on-time is reached. The lower the switching frequency, the wider the linear dimming range. Figure 14 shows how both CSH methods are physically implemented.

Method 1 uses an external potentiometer in the CSH path which is a simple addition to the existing circuitry. However, the LEDs cannot dim completely because there is always some resistance causing signal current to flow. This method is also susceptible to noise coupling at the CSH pin because the potentiometer increases the size of the signal current loop.

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Feature Description (continued)

Method 2 provides a complete dimming range and better noise performance, though it is more complex. It consists of a PNP current mirror and a bias network consisting of an NPN, 2 resistors and a potentiometer (R_{ADJ}), where R_{ADJ} controls the amount of current sourced into the CSH pin. A higher resistance value sources more current into the CSH pin, causing less regulated signal current through R_{HSP}, effectively dimming the LEDs. V_{REF} should be a precise external voltage reference, while Q7 and Q8 should be a dual pair PNP for best matching and performance. The additional current (I_{ADD}) sourced into the CSH pin can be calculated using Equation 9.

$$I_{ADD} = \frac{\left(\frac{R_{ADJ} \times V_{REF}}{R_{ADJ} + R_{MAX}}\right) - V_{BE\text{-}Q6}}{R_{BIAS}} \quad (9)$$

The corresponding LED current (I_{LED}) for a specific I_{ADD} is:

$$I_{LED} = (I_{CSH} - I_{ADD}) \times \left(\frac{R_{HSP}}{R_{SNS}}\right) \quad (10)$$

8.3.5 Current Sense and Current Limit

The LM3421 and LM3423 achieve peak current mode control using a comparator that monitors the main MOSFET (Q1) transistor current, comparing it with the COMP pin voltage as shown in Figure 15. The controller incorporates a cycle-by-cycle overcurrent protection function. Aredundant internal current sense comparator provides the current limit functionality . If the voltage at the current sense comparator input (IS pin) exceeds 245 mV (typical), the on cycle is immediately terminated. The IS input pin has an internal N-channel MOSFET which pulls it down at the conclusion of every cycle. The discharge device remains on for an additional 210 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. The leading edge blanking (LEB) determines the minimum achievable on-time ($t_{ON\text{-}MIN}$).

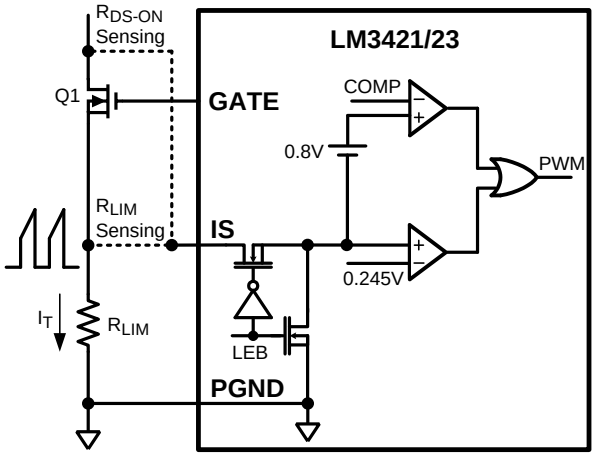


Figure 15. Current Sense / Current Limit Circuitry

There are two possible methods to sense the transistor current. The $R_{DS\text{-}ON}$ of the main power MOSFET can be used as the current sense resistance because the IS pin was designed to withstand the high voltages present on the drain when the MOSFET is in the off state. Alternatively, a sense resistor located in the source of the MOSFET may be used for current sensing; however, TI suggests a low inductance (ESL) type. The cycle-by-cycle current limit (I_{LIM}) can be calculated using either method as the limiting resistance (R_{LIM}):

$$I_{LIM} = \frac{245\ mV}{R_{LIM}} \quad (11)$$

Feature Description (continued)

8.3.6 Overcurrent Protection

The LM3421 and LM3423 controllers have a secondary method of overcurrent protection. Switching action is disabled whenever the current in the LEDs is more than 30% above the regulation set point. The dimming MOSFET switch driver (DDRV) is not disabled however as this would immediately remove the fault condition and cause oscillatory behavior.

8.3.7 Zero Current Shutdown

The LM3421 and LM3423 controllers implement zero current shutdown through the EN and RPD pins. When pulled low, the EN pin places the devices into near-zero current state, where only the leakage currents occurs at the pins (typical 0.1 µA). The applications circuits frequently have resistor dividers to set UVLO, OVLO, or other similar functions. The RPD pin is an open-drain N-channel MOSFET that is enabled only when the device is enabled. Tying the bottom of all resistor dividers to the RPD pin as shown in Figure 16 allows them to float during shutdown, thus removing their current paths and providing true application-wide zero current shutdown.

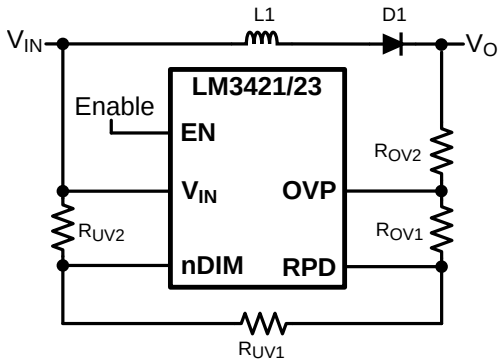


Figure 16. Zero Current Shutdown Circuit

8.3.8 Control Loop Compensation

The control loop is modeled as most typical current mode controllers. Using a first order approximation, the uncompensated loop can be modeled as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance. There is also a high-frequency pole in the model; however, it is near the switching frequency and plays no part in the compensation design process. Therefore, it is neglected. Because ceramic capacitance is recommended for use with LED drivers, due to long lifetimes and high ripple current rating, the ESR of the output capacitor can also be neglected in the loop analysis. The DC gain of the uncompensated loop depends on internal controller gains and the external sensing network.

This section describes a buck-boost regulator as an example case.

Use Equation 12 to calculate the uncompensated loop gain for a buck-boost regulator.

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \tag{12}$$

Where the uncompensated DC loop gain of the system is calculated using Equation 13.

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \tag{13}$$

And the output pole (ω_{P1}) is approximated using Equation 14.

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \tag{14}$$

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Feature Description (continued)

And the right half plane zero (ω_{Z1}) is:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \quad (15)$$

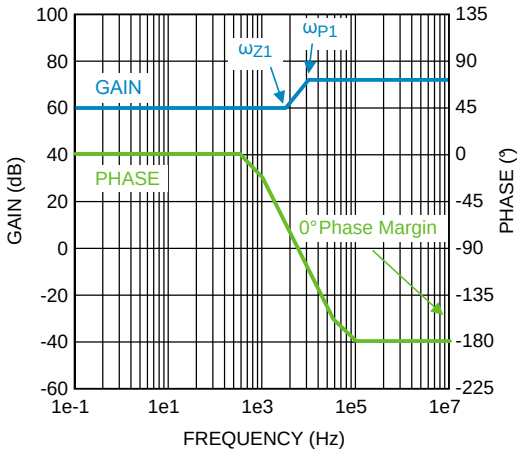


Figure 17. Uncompensated Loop Gain Frequency Response

Figure 17 shows the uncompensated loop gain in a worst-case scenario when the RHP zero is below the output pole. This occurs at high duty cycles when the regulator is trying to boost the output voltage significantly. The RHP zero adds 20dB/decade of gain while losing 45°/decade of phase, which places the crossover frequency (when the gain is zero dB) extremely high because the gain only starts falling again due to the high-frequency pole (not shown in Figure 17). The phase is below –180° at the crossover frequency, which means there is no phase margin (180° + phase at crossover frequency) causing system instability. Even if the output pole is below the RHP zero, the phase reaches –180° before the crossover frequency in most cases yielding instability.

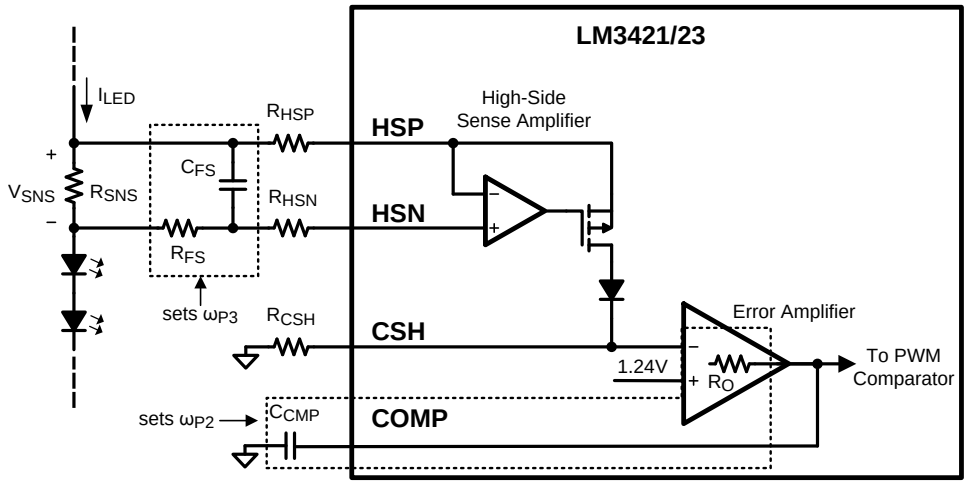


Figure 18. Compensation Circuitry

Feature Description (continued)

To mitigate this problem, a compensator should be designed to give adequate phase margin (above 45°) at the crossover frequency. A simple compensator using a single capacitor at the COMP pin (C_{CMP}) adds a dominant pole to the system, which ensures adequate phase margin if placed low enough. At high duty cycles (as shown in Figure 17), the RHP zero places extreme limits on the achievable bandwidth with this type of compensation. However, because an LED driver is essentially free of output transients (except catastrophic failures open or short), the dominant pole approach, even with reduced bandwidth, is usually the best approach. The dominant compensation pole (ω_{P2}) is determined by C_{CMP} and the output resistance (R_O) of the error amplifier (typically 5 MΩ) as demonstrated in Equation 16.

$$\omega_{P2} = \frac{1}{5 \times 10^6 \times C_{CMP}} \tag{16}$$

It may also be necessary to add one final pole at least one decade above the crossover frequency to attenuate switching noise and, in some cases, provide better gain margin. This pole can be placed across R_{SNS} to filter the ESL of the sense resistor at the same time. Figure 18 shows how the compensation is physically implemented in the system.

The high-frequency pole (ω_{P3}) can be calculated using Equation 17.

$$\omega_{P3} = \frac{1}{R_{FS} \times C_{FS}} \tag{17}$$

The total system transfer function becomes:

$$T = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \tag{18}$$

The resulting compensated loop gain frequency response shown in Figure 19 indicates that the system has adequate phase margin (above 45°) if the dominant compensation pole is placed low enough, ensuring stability.

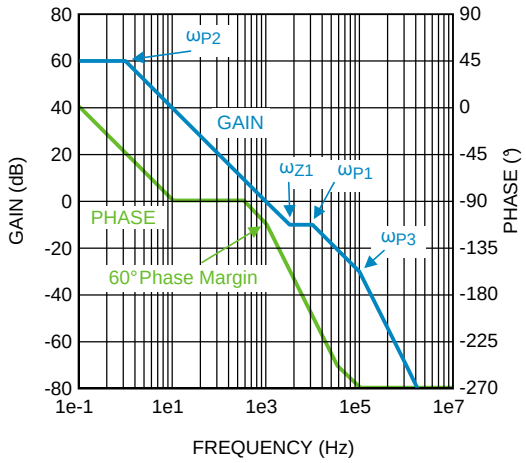


Figure 19. Compensated Loop Gain Frequency Response

8.3.9 Start-Up Regulator

The controller includes a high voltage, low dropout bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor (C_{BYP}) connected to the V_{CC} pin. The recommended bypass capacitance for the V_{CC} regulator is 2.2 µF to 3.3 µF. The output of the V_{CC} regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply is also internally current limited. Figure 20 shows the typical start-up waveforms.

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Feature Description (continued)

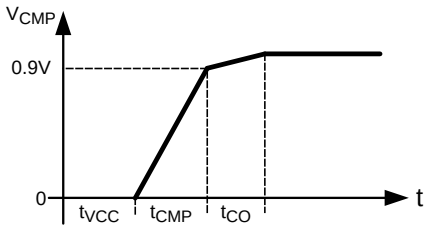


Figure 20. Start-Up Waveforms

First, C_{BYP} is charged to be above V_{CC} UVLO threshold (approximately 4.2 V). The C_{VCC} charging time (t_{VCC}) can be estimated using Equation 19.

$$t_{VCC} = \frac{4.2V}{25\ mA} \times C_{BYP} = 168\Omega \times C_{BYP} \tag{19}$$

C_{CMP} is then charged to 0.9 V over the charging time (t_{CMP}), which can be estimated using Equation 20.

$$t_{CMP} = \frac{0.9V}{25\ \mu A} \times C_{CMP} = 36\ k\Omega \times C_{CMP} \tag{20}$$

Once C_{CMP} = 0.9 V, the part starts switching to charge C_O until the LED current is in regulation. The C_O charging time (t_{CO}) can be roughly estimated using Equation 21.

$$t_{CO} = C_O \times \frac{V_O}{I_{LED}} \tag{21}$$

The system start-up time (t_{SU}) is defined using Equation 22.

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \tag{22}$$

In some configurations, the start-up waveform overshoots the steady state COMP pin voltage. In this case, the LED current and output voltage overshoots also, which can trip the overvoltage or protection, causing a race condition. The easiest way to prevent this is to use a larger compensation capacitor (C_{CMP}), thereby slowing down the control loop.

8.3.10 Overvoltage Lockout (OVLO)

The LM3421 and LM3423 can be configured to detect an output (or input) overvoltage condition through the OVP pin. The pin features a precision 1.24-V threshold with 23 µA (typical) of hysteresis current as shown in Figure 21. When the OVLO threshold is exceeded, the GATE pin is immediately pulled low and a 23-µA current source provides hysteresis to the lower threshold of the OVLO hysteretic band.

If the LEDs are referenced to a potential other than ground (floating), as in the buck-boost and buck configuration, the output voltage (V_O) should be sensed and translated to ground by using a single PNP as shown in Figure 22.

The overvoltage turnoff threshold ($V_{TURN-OFF}$) is defined:

Ground Referenced

$$V_{TURN-OFF} = 1.24V \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}}\right) \tag{23}$$

Floating

$$V_{TURN-OFF} = 1.24V \times \left(\frac{0.5 \times R_{OV1} + R_{OV2}}{R_{OV1}}\right) \tag{24}$$

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Feature Description (continued)

In the ground referenced configuration, the voltage across R_{OV2} is V_O – 1.24 V whereas in the floating configuration it is V_O – 620 mV where 620 mV approximates V_{BE} of the PNP.

The overvoltage hysteresis (V_{HYSO}) is defined using Equation 25.

$$V_{HYSO} = 23\ \mu A \times R_{OV2} \tag{25}$$

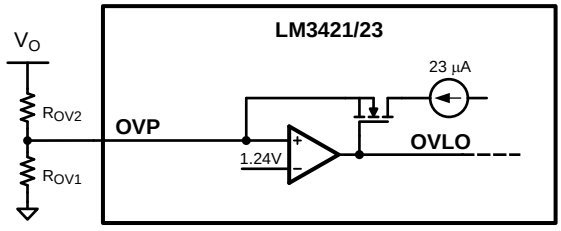


Figure 21. Overvoltage Protection Circuitry

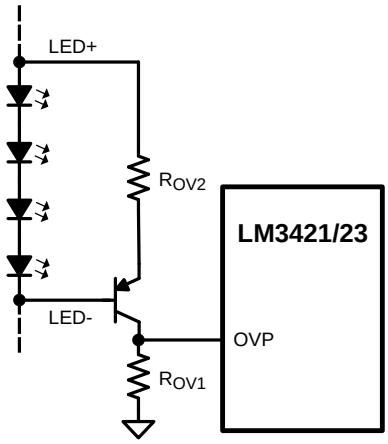


Figure 22. Floating Output OVP Circuitry

The OVLO feature can cause some interesting results if the OVLO trip-point is set too close to V_O. At turnon, the converter has a modest amount of voltage overshoot before the control loop gains control of I_{LED}. If the overshoot exceeds the OVLO threshold, the controller shuts down, opening the dimming MOSFET. This isolates the LED load from the converter and the output capacitance. The voltage then discharges very slowly through the HSP and HSN pins until V_O drops below the lower threshold, where the process repeats. This looks like the LEDs are blinking at around 2 Hz. This mode can be escaped if the input voltage is reduced.

8.3.11 Input Undervoltage Lockout (UVLO)

The nDIM pin is a dual-function input that features an accurate 1.24-V threshold with programmable hysteresis as shown in Figure 23. This pin functions as both the PWM dimming input for the LEDs and as a V_{IN} UVLO. When the pin voltage rises and exceeds the 1.24-V threshold, 23 µA (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.

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Feature Description (continued)

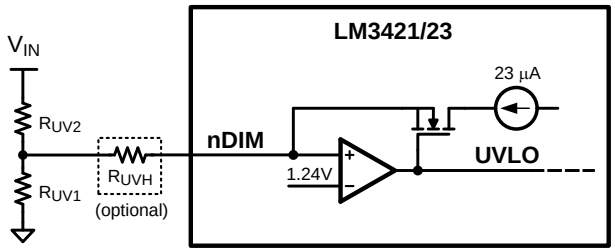


Figure 23. UVLO Circuit

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra series resistor to set the hysteresis. This allows the standard resistor divider to have smaller resistor values minimizing PWM delays due to a pulldown MOSFET at the nDIM pin (see *PWM Dimming* section). In general, at least 3 V of hysteresis is preferable when PWM dimming, if operating near the UVLO threshold.

The turnon threshold ($V_{TURN-ON}$) is defined using Equation 26.

$$V_{TURN\ ON} = 1.24V \times \left(\frac{R_{UV1} + R_{UV2}}{R_{UV1}}\right) \tag{26}$$

The hysteresis (V_{HYS}) is defined as follows:

8.3.11.1 UVLO Only

$$V_{HYS} = 23\,\mu A \times R_{UV2} \tag{27}$$

8.3.11.2 PWM Dimming and UVLO

$$V_{HYS} = 23\,\mu A \times \left(R_{UV2} + \frac{R_{UVH} \times (R_{UV1} + R_{UV2})}{R_{UV1}}\right) \tag{28}$$

When zero current shutdown and UVLO are implemented together, the EN pin can be used to escape UVLO. The nDIM pin pulls up to V_{IN} when EN is pulled low. Therefore, if V_{IN} is within the UVLO hysteretic window when EN is pulled high again, the controller starts-up even though $V_{TURN-ON}$ is not exceeded.

8.3.12 PWM Dimming

The active low nDIM pin can be driven with a PWM signal which controls the main N-channel FET and the dimming FET (dimFET). The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle, (that is, 30% duty cycle equals approximately 30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a V_{IN} UVLO input as described in *Input Undervoltage Lockout (UVLO)* or by tying it directly to V_{CC} or V_{IN}.

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Feature Description (continued)

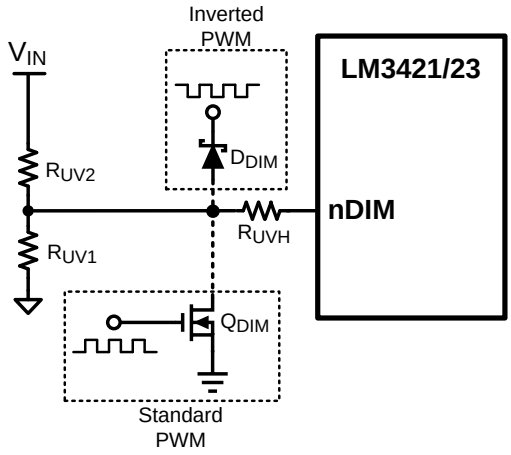


Figure 24. PWM Dimming Circuit

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Figure 24 shows how the PWM signal is applied to nDIM:

1. Connect the dimming MOSFET (Q_{DIM}) with the drain to the nDIM pin and the source to AGND. Apply an external logic-level PWM signal to the gate of Q_{DIM}.
2. Connect the anode of a Schottky diode (D_{DIM}) to the nDIM pin. Apply an inverted external logic-level PWM signal to the cathode of the same diode.

The DDRV pin is a PWM output that follows the nDIM PWM input signal. When the nDIM pin rises, the DDRV pin rises and the PWM latch reset signal is removed allowing the main MOSFET Q1 to turn on at the beginning of the next clock set pulse. In boost and buck-boost topologies, the DDRV pin is used to control a N-channel MOSFET placed in series with the LED load, while it would control a P-channel MOSFET in parallel with the load for a buck topology.

The series dimFET opens the LED load, when nDIM is low, effectively speeding up the rise and fall times of the LED current. Without any dimFET, the rise and fall times are limited by the inductor slew rate and dimming frequencies above 1 kHz are impractical. Using the series dimFET, dimming frequencies up to 30 kHz are achievable. With a parallel dimFET (buck topology), even higher dimming frequencies are achievable.

When using the PWM functionality in a boost regulator, the PWM signal can drive a ground referenced FET. However, with buck-boost and buck topologies, level shifting circuitry is necessary to translate the PWM dim signal to the floating dimFET as shown in Figure 25 and Figure 26. If high side dimming is necessary in a boost regulator using the LM3423, level shifting can be added providing the polarity inverting DPOL pin is pulled low (see *LM3423 Only: DPOL, FLT, TIMR, and LRDY* section) as shown in Figure 27.

When using a series dimFET to PWM dim the LED current, more output capacitance is always better. Typical applications use a minimum of 40 µF for PWM dimming. For most applications, a capacitance of 40 µF provides adequate energy storage at the output when the dimFET turns off and opens the LED load. Then when the dimFET is turned back on, the capacitance helps source current into the load, improving the LED current rise time.

A minimum on-time must be maintained in order for PWM dimming to operate in the linear region of its transfer function. Because the controller is disabled during dimming, the PWM pulse must be long enough such that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and buck-boost regulators, the minimum dimming pulse length in seconds (t_{PULSE}) is:

$$t_{PULSE} = \frac{2 \times I_{LED} \times V_O \times L1}{V_{IN}^2} \quad (29)$$

Even maintaining a dimming pulse greater than t_{PULSE}, preserving linearity at low dimming duty cycles is difficult.

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Feature Description (continued)

The second helpful modification is to remove the C_{FS} capacitor and R_{FS} resistor, eliminating the high-frequency compensation pole. Typically, this does not affect stability, but it speeds up the response of the CSH pin, specifically at the rising edge of the LED current when PWM dimming, thus improving the achievable linearity at low dimming duty cycles.

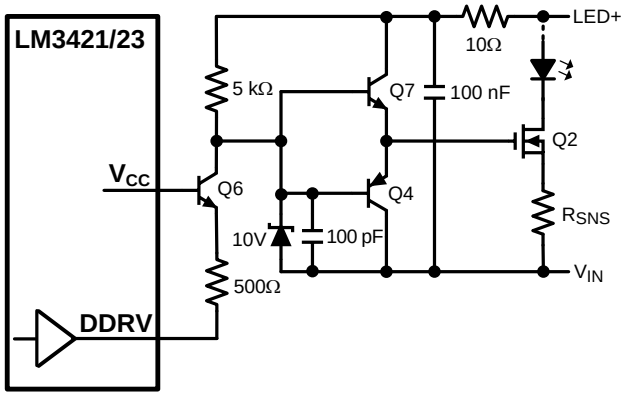


Figure 25. Buck-boost Level-Shifted PWM Circuit

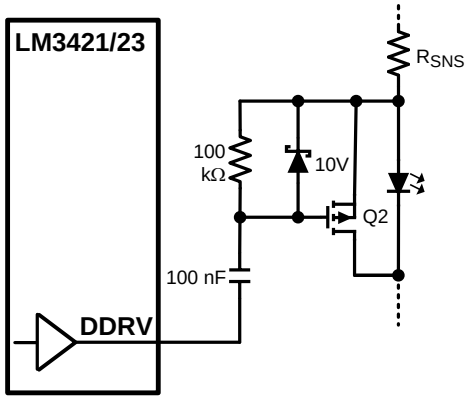


Figure 26. Buck Level-Shifted PWM Circuit

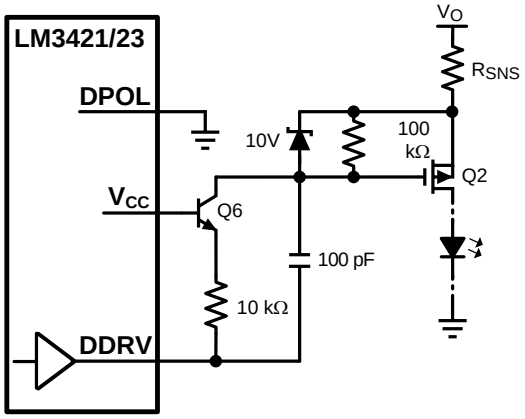


Figure 27. Boost Level-Shifted PWM Circuit

Feature Description (continued)

8.3.13 LM3423 Only: DPOL, FLT, TIMR, and LRDY

The LM3423 has four additional pins: DPOL, FLT, TIMR, and LRDY. The DPOL pin is simply used to invert the DDRV polarity . If DPOL is left open, then it is internally pulled high and the polarity is correct for driving a series N-channel dimFET. If DPOL is pulled low then the polarity is correct for using a series P-channel dimFET in high-side dimming applications. For a parallel P-channel dimFET, as used in the buck topology, leave DPOL open for proper polarity.

The additional TIMR and FLT pins can be used in conjunction with an input disconnect MOSFET switch as shown in Figure 28 to protect the module from various fault conditions.

A fault is detected and an 11.5 µA (typical) current is sourced from the TIMR pin whenever any one of the following conditions exists.

- LED current is above regulation by more than 30%.
- OVLO has engaged.
- Thermal shutdown has engaged.

An external capacitor (C_{TMR}) from TIMR to AGND programs the fault filter time as follows:

$$C_{TMR} = \frac{t_{FLT} \times 11.5\,\mu A}{1.24V} \tag{30}$$

When the voltage on the TIMR pin reaches 1.24 V, the device is latched off and the N-channel MOSFET open-drain FLT pin transitions to a high impedance state. The controller immediatly pulls the TIMR pin to ground (resets) if the fault condition is removed at any point during the filter period. Otherwise, if the timer expires, the fault remains latched until one of these situations occurs:

- The EN pin is pulled low long enough for the V_{CC} pin to drop below 4.1 V (approximately 200 ms) or
- the TIMR pin is pulled to ground or
- a complete power cycle occurs

When using the EN and OVP pins in conjunction with the RPD pulldown pin, a race condition exists when exiting the disabled (EN low) state. When disabled, controller pulls up the OVP pin to the output voltage because the RPD pulldown is disabled, and this appears as if it is a real OVLO condition. The timer pin immediately rises and latches the controller to the fault state. To protect against this behavior, a minimum timer capacitor (C_{TMR} = 220 pF) should be used. If fault latching is not required, short the TMR pin to AGND, which disables the FLT flag function.

The LM3423 also includes an LED Ready (LRDY) flag to notify the system that the LEDs are in proper regulation. The N-channel MOSFET open-drain LRDY pin is pulled low whenever any of the following conditions are met:

1. V_{CC} UVLO has engaged.
2. LED current is below regulation by more than 20%.
3. LED current is above regulation by more than 30%.
4. Overvoltage protection has engaged
5. Thermal shutdown has engaged.
6. A fault has latched the device off.

The LRDY pin is pulled low during start-up of the device and remains low until the LED current is in regulation.

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Feature Description (continued)

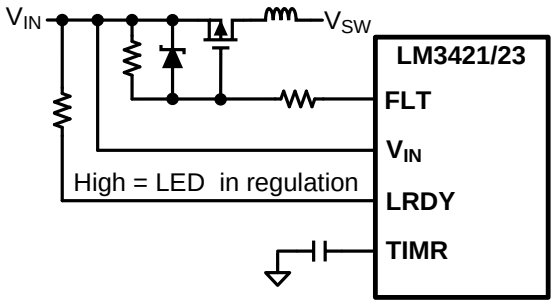


Figure 28. Fault Detection and LED Status Circuit

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Inductor

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transfered to the load in different ways (as an example, buck-boost operation is detailed in the *Current Regulators* section). The size of the inductor, the voltage across it, and the length of the switching subinterval (t_{ON} or t_{OFF}) determines the inductor current ripple ($\Delta i_{L\text{-}PP}$). In the design process, L1 is chosen to provide a desired $\Delta i_{L\text{-}PP}$. For a buck regulator the inductor has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore $\Delta i_{L\text{-}PP}$ is basically equal to the LED ripple current $\Delta i_{LED\text{-}PP}$. However, for boost and buck-boost regulators, there is always an output capacitor which reduces $\Delta i_{LED\text{-}PP}$; therefore, the inductor ripple can be larger than in the buck regulator case where output capacitance is minimal or completely absent.

In general, $\Delta i_{LED\text{-}PP}$ is recommended by manufacturers to be less than 40% of the average LED current (I_{LED}). Therefore, for the buck regulator with no output capacitance, $\Delta i_{L\text{-}PP}$ should also be less than 40% of I_{LED}. For the boost and buck-boost topologies, $\Delta i_{L\text{-}PP}$ can be much higher depending on the output capacitance value. However, $\Delta i_{L\text{-}PP}$ is suggested to be less than 100% of the average inductor current (I_L) to limit the RMS inductor current.

L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current ($I_{L\text{-}RMS}$).

9.1.2 LED Dynamic Resistance

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus R_{SNS}. LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED (V_{LED}) by the forward current (I_{LED}) leads to an incorrect calculation of the dynamic resistance of a single LED (r_{LED}). The result can be 5 to 10 times higher than the true r_{LED} value.

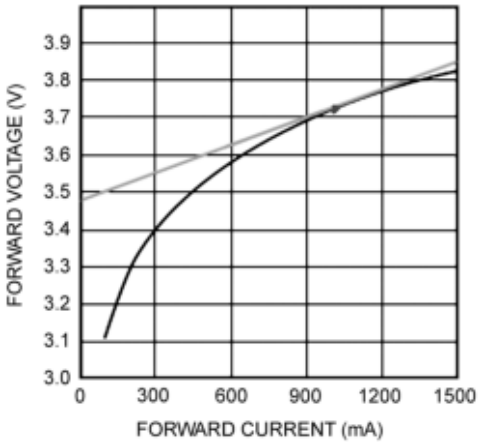


Figure 29. Dynamic Resistance

Obtaining r_{LED} is accomplished by referring to the manufacturer's LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 29. For any application with more than 2 series LEDs, R_{SNS} can be neglected allowing r_D to be approximated as the number of LEDs multiplied by r_{LED}.

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Application Information (continued)

9.1.3 Output Capacitor

For boost and buck-boost regulators, the output capacitor (C_O) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a buck topology simplys reduce the LED current ripple (Δi_{LED-PP}) below the inductor current ripple (Δi_{L-PP}). In all cases, C_O is sized to provide a desired Δi_{LED-PP}. As mentioned in the *Inductor* section, Δi_{LED-PP} is recommended by manufacturers to be less than 40% of the average LED current (I_{LED}).

C_O should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

9.1.4 Input Capacitors

The input capacitance (C_{IN}) provides energy during the discontinuous portions of the switching period. For buck and buck-boost regulators, C_{IN} provides energy during t_{ON} and during t_{OFF}, the input voltage source charges up C_{IN} with the average input current (I_{IN}). For boost regulators, C_{IN} only needs to provide the ripple current due to the direct connection to the inductor. C_{IN} is selected given the maximum input voltage ripple (Δv_{IN-PP}) which can be tolerated. Δv_{IN-PP} is suggested to be less than 10% of the input voltage (V_{IN}).

An input capacitance at least 100% greater than the calculated C_{IN} value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transition of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

For most applications, TI recommends bypassing the V_{IN} pin with an 0.1 µF ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the controller, a 10-Ω series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150-kHz filter to eliminate undesired high-frequency noise.

9.1.5 Main MOSFET / Dimming MOSFET

The controller requires an external N-channel FET (Q1) as the main power MOSFET for the switching regulator. TI recommends Q1 have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. TI recommends the current rating be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the RMS transistor current and the N-channel FET on-resistance (R_{DS-ON}).

When PWM dimming, the controller requires another MOSFET (Q2) placed in series (or parallel for a buck regulator) with the LED load. This MOSFET should have a voltage rating greater than the output voltage (V_O) and a current rating at least 10% higher than the nominal LED current (I_{LED}) . The power rating is simply R_{DS-ON} multiplied by I_{LED}, assuming 100% dimming duty cycle (continuous operation) occurs.

For most applications, choose an N-channel FET that minimizes total gate charge (Q_g) when f_{SW} is high. It that is not possible. minimize the on-resistance $R_{DS(on)}$ to minimize the dominant power losses in the system. Frequently, higher current N-channel FETs in larger packages yield better thermal performance.

9.1.6 Re-Circulating Diode

The controller requires a recirculating diode (D1) to carry the inductor current during the off time (t_{OFF}). The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, TI recommends D1 have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product data sheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.

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Application Information (continued)

9.1.7 Boost Inrush Current

When configured as a boost converter, there is a phantom power path comprised of the inductor, the output diode, and the output capacitor. This path causes two things to happen when power is applied:

1. a very large inrush of current to charge the output capacitor
2. the energy stored in the inductor during this inrush collects in the output capacitor, charging it to a higher potential than the input voltage

Depending on the state of the EN pin, the output capacitor discharges by:

1. EN < 1.3 V: no discharge path (leakage only).
2. EN > 1.3 V, the OVP divider resistor path, if present, and 10 µA into each of the HSP & HSN pins.

In applications using the OVP divider and with EN > 1.3 V, the output capacitor voltage can charge higher than $V_{TURN-OFF}$. In this situation, the FLT pin (LM3423 only) is open and the PWM dimming MOSFET is turned off. This condition (the system appearing disabled) can persist for an undesirably long time. Possible solutions to this condition include:

- Add an inrush diode from V_{IN} to the output as shown in Figure 30.
- Add an NTC thermistor in series with the input to prevent the inrush from overcharging the output capacitor too high.
- Use a current limited source supply.
- Raise the OVP threshold.

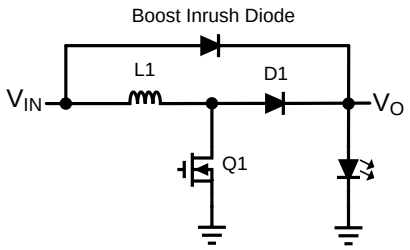


Figure 30. Boost Topology with Inrush Diode

9.1.8 Switching Frequency

An external resistor (R_T) connected between the RCT pin and the switch node (where D1, Q1, and L1 connect), in combination with a capacitor (C_T) between the RCT and AGND pins, sets the off-time (t_{OFF}) as shown in Figure 31. For boost and buck-boost topologies, the V_{IN} proportionality ensures a virtually constant switching frequency (f_{SW}).

For a buck topology, R_T and C_T are also used to set t_{OFF}, however the iinput voltage (V_{IN}) proportionality does not ensure a constant switching frequency. Instead, constant ripple operation can be achieved. Changing the connection of R_T in Figure 31 from V_{SW} to V_{IN} provides a constant ripple over varying V_{IN}. Adding a PNP transistor as shown in Figure 32 provides constant ripple over varying V_O.

The switching frequency is defined:

Buck (Constant Ripple vs. V_{IN})

$$f_{SW} = \frac{25 \times (V_{IN} - V_O)}{R_T \times C_T \times V_{IN}} \quad (31)$$

Buck (Constant Ripple vs. V_O)

$$f_{SW} = \frac{25 \times (V_{IN} \times V_O - V_O^2)}{R_T \times C_T \times V_{IN}^2} \quad (32)$$

Boost and Buck-boost

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Application Information (continued)

$$f_{SW} = \frac{25}{R_T \times C_T} \quad (33)$$

For all topologies, the C_T capacitor is recommended to be 1 nF and should be located very close to the LM34xx-Q1.

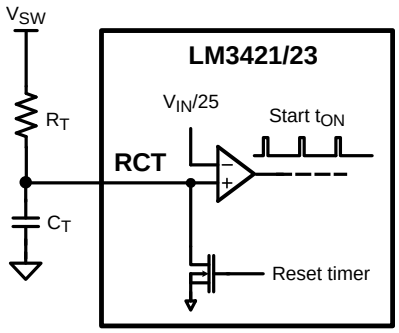


Figure 31. Off-timer Circuitry for Boost and Buck-boost Regulators

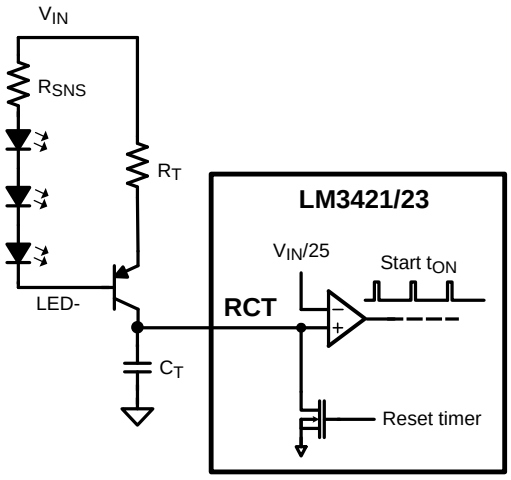


Figure 32. Off-timer Circuitry for Buck Regulators

9.2 Typical Applications

9.2.1 Basic Topology Schematics

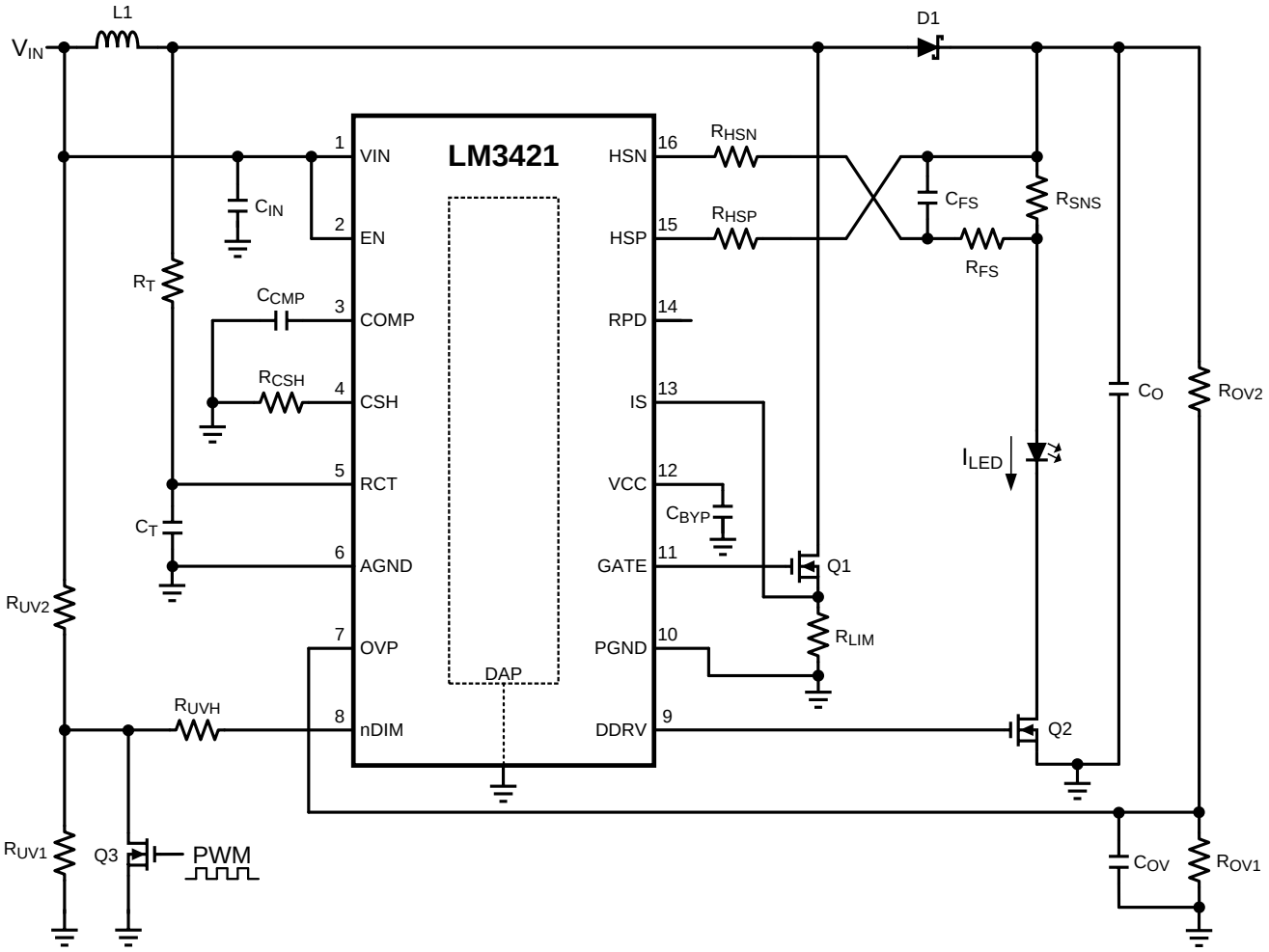


Figure 33. Boost Regulator (V_{IN} < V_O)

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Typical Applications (continued)

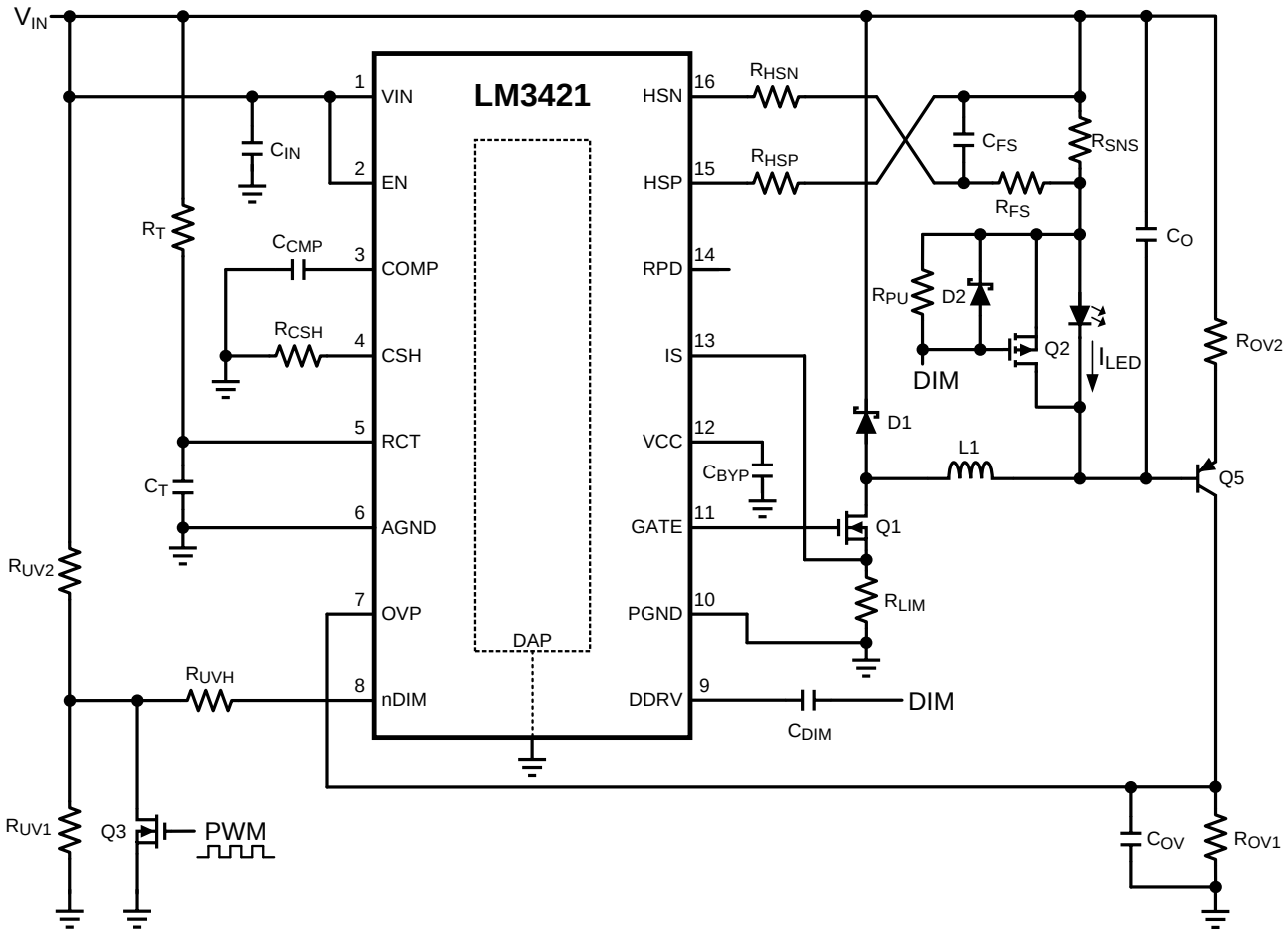


Figure 34. Buck Regulator (V_{IN} > V_O)

Typical Applications (continued)

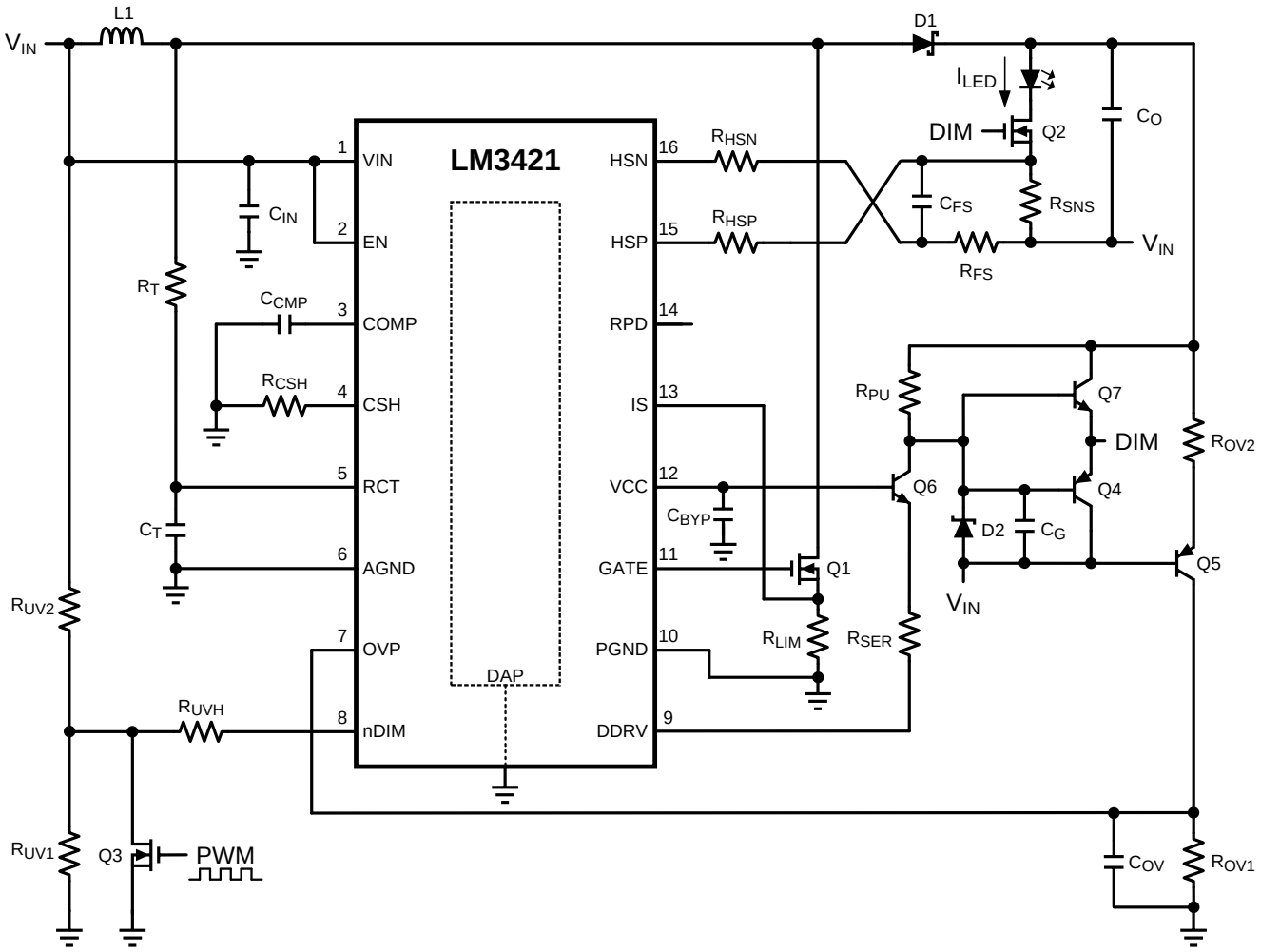


Figure 35. Buck-Boost Regulator

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Typical Applications (continued)

9.2.1.1 Design Requirements

Number of series LEDs: N

Single LED forward voltage: V_{LED}

Single LED dynamic resistance: r_{LED}

Nominal input voltage: V_{IN}

Input voltage range: V_{IN-MAX}, V_{IN-MIN}

Switching frequency: f_{SW}

Current sense voltage: V_{SNS}

Average LED current: I_{LED}

Inductor current ripple: Δi_{L-PP}

LED current ripple: Δi_{LED-PP}

Peak current limit: I_{LIM}

Input voltage ripple: Δv_{IN-PP}

Output OVLO characteristics: $V_{TURN-OFF}$, V_{HYSO}

Input UVLO characteristics: $V_{TURN-ON}$, V_{HYS}

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Operating Point

Given the number of series LEDs (N), the forward voltage (V_{LED}) and dynamic resistance (r_{LED}) for a single LED, solve for the nominal output voltage (V_O) and the nominal LED string dynamic resistance (r_D):

$$V_O = N \times V_{LED} \tag{34}$$

$$r_D = N \times r_{LED} \tag{35}$$

Solve for the ideal nominal duty cycle (D):

Buck:

$$D = \frac{V_O}{V_{IN}} \tag{36}$$

Boost:

$$D = \frac{V_O - V_{IN}}{V_O} \tag{37}$$

Buck-Boost:

$$D = \frac{V_O}{V_O + V_{IN}} \tag{38}$$

Using the same equations, find the minimum duty cycle (D_{MIN}) using maximum input voltage (V_{IN-MAX}) and the maximum duty cycle (D_{MAX}) using the minimum input voltage (V_{IN-MIN}). Also, remember that D' = 1 - D.

9.2.1.2.2 Switching Frequency

Set the switching frequency (f_{SW}) by assuming a C_T value of 1 nF and solving for R_T:

Buck (Constant Ripple vs. V_{IN})

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Typical Applications (continued)

$$R_T = \frac{25 \times \left(V_{IN} - V_O\right)}{f_{SW} \times C_T \times V_{IN}} \quad (39)$$

Buck (Constant Ripple vs. V_O)

$$R_T = \frac{25 \times \left(V_{IN} \times V_O - V_O^2\right)}{f_{SW} \times C_T \times V_{IN}^2} \quad (40)$$

Boost and Buck-Boost

$$R_T = \frac{25}{f_{SW} \times C_T} \quad (41)$$

9.2.1.2.3 Average LED Current

For all topologies, set the average LED current (I_{LED}) knowing the desired current sense voltage (V_{SNS}) and solving for R_{SNS}:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} \quad (42)$$

If the calculated R_{SNS} is too far from a desired standard value, then V_{SNS} requires adjustment to obtain a standard value.

Setup the suggested signal current of 100 µA by assuming R_{CSH} = 12.4 kΩ and solving for R_{HSP}:

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} \quad (43)$$

If the calculated R_{HSP} is too far from a desired standard value, then R_{CSH} can be adjusted to obtain a standard value.

9.2.1.2.4 Inductor Ripple Current

Set the nominal inductor ripple current ($\Delta i_{L\text{-}PP}$) by solving for the appropriate inductor (L1):

Buck

$$L1 = \frac{(V_{IN} - V_O) \times D}{\Delta i_{L-PP} \times f_{SW}} \quad (44)$$

Boost and Buck-Boost

$$L1 = \frac{V_{IN} \times D}{\Delta i_{L-PP} \times f_{SW}} \quad (45)$$

To set the worst case inductor ripple current, use $V_{IN\text{-}MAX}$ and D_{MIN} when solving for L1.

The minimum allowable inductor RMS current rating ($I_{L\text{-}RMS}$) can be calculated as:

Buck

$$I_{L\text{-}RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L\text{-}PP}}{I_{LED}}\right)^2} \quad (46)$$

Boost and Buck-Boost

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L\text{-}PP} \times D'}{I_{LED}}\right)^2} \quad (47)$$

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Typical Applications (continued)

9.2.1.2.5 LED Ripple Current

Set the nominal LED ripple current (Δi_{LED-PP}), by solving for the output capacitance (C_O):

Buck

$$C_O = \frac{\Delta i_{L-PP}}{8 \times f_{SW} \times r_D \times \Delta i_{LED-PP}} \quad (48)$$

Boost and Buck-boost

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED-PP} \times f_{SW}} \quad (49)$$

To set the worst case LED ripple current, use D_{MAX} when solving for C_O. Remember, when PWM dimming, TI recommends using a minimum of 40 µF of output capacitance to improve performance.

The minimum allowable RMS output capacitor current rating (I_{CO-RMS}) can be approximated:

Buck

$$I_{CO-RMS} = \frac{\Delta i_{LED-PP}}{\sqrt{12}} \quad (50)$$

Boost and Buck-boost

$$I_{CO-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (51)$$

9.2.1.2.6 Peak Current Limit

Set the peak current limit (I_{LIM}) by solving for the transistor path sense resistor (R_{LIM}):

$$R_{LIM} = \frac{245\ mV}{I_{LIM}} \quad (52)$$

9.2.1.2.7 Loop Compensation

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

First, the uncompensated loop gain (T_U) of the regulator can be approximated:

Buck

$$T_U = T_{U0} \times \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right)} \quad (53)$$

Boost and Buck-Boost

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \quad (54)$$

Where the pole (ω_{P1}) is approximated:

Buck

$$\omega_{P1} = \frac{1}{r_D \times C_O} \quad (55)$$

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Typical Applications (continued)

Boost

$$\omega_{P1} = \frac{2}{r_D \times C_O} \quad (56)$$

Buck-Boost

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \quad (57)$$

And the RHP zero (ω_{Z1}) is approximated:

Boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{L1} \quad (58)$$

Buck-Boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \quad (59)$$

And the uncompensated DC loop gain (T_{U0}) is approximated:

Buck

$$T_{U0} = \frac{500V \times R_{CSH} \times R_{SNS}}{R_{HSP} \times R_{LIM}} = \frac{620V}{I_{LED} \times R_{LIM}} \quad (60)$$

Boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{2 \times R_{HSP} \times R_{LIM}} = \frac{D' \times 310V}{I_{LED} \times R_{LIM}} \quad (61)$$

Buck-Boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \quad (62)$$

For all topologies, the primary method of compensation is to place a low frequency dominant pole (ω_{P2}), which ensures that there is ample phase margin at the crossover frequency. This is accomplished by placing a capacitor (C_{CMP}) from the COMP pin to AGND, which is calculated according to the lower value of the pole and the RHP zero of the system (shown as a minimizing function):

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} \quad (63)$$

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5 \times 10^6} \quad (64)$$

If analog dimming is used, C_{CMP} should be approximately 4× larger to maintain stability as the LEDs are dimmed to zero.

A high-frequency compensation pole (ω_{P3}) can be used to attenuate switching noise and provide better gain margin. Assuming R_{FS} = 10 Ω, C_{FS} is calculated according to the higher value of the pole and the RHP zero of the system (shown as a maximizing function):

$$\omega_{P3} = \max(\omega_{P1}, \omega_{Z1}) \times 10 \quad (65)$$

$$C_{FS} = \frac{1}{10 \times \omega_{P3}} \quad (66)$$

The total system loop gain (T) can then be written as:

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Typical Applications (continued)

Buck

$$T = T_{U0} \times \frac{1}{\left(1+\frac{s}{\omega_{P1}}\right) \times \left(1+\frac{s}{\omega_{P2}}\right) \times \left(1+\frac{s}{\omega_{P3}}\right)} \quad (67)$$

Boost and Buck-Boost

$$T = T_{U0} \times \frac{\left(1-\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right) \times \left(1+\frac{s}{\omega_{P2}}\right) \times \left(1+\frac{s}{\omega_{P3}}\right)} \quad (68)$$

9.2.1.2.8 Input Capacitance

Set the nominal input voltage ripple (Δv_{IN-PP}) by solving for the required capacitance (C_{IN}):

Buck

$$C_{IN} = \frac{I_{LED} \times (1 - D) \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (69)$$

Boost

$$C_{IN} = \frac{\Delta i_{L-PP}}{8 \times \Delta V_{IN-PP} \times f_{SW}} \quad (70)$$

Buck-Boost

$$C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (71)$$

Use D_{MAX} to set the worst case input voltage ripple, when solving for C_{IN} in a buck-boost regulator and D_{MID} = 0.5 when solving for C_{IN} in a buck regulator.

The minimum allowable RMS input current rating ($I_{CIN-RMS}$) can be approximated:

Buck

$$I_{CIN-RMS} = I_{LED} \times \sqrt{D_{MID} \times (1-D_{MID})} \quad (72)$$

Boost

$$I_{CIN-RMS} = \frac{\Delta i_{L-PP}}{\sqrt{12}} \quad (73)$$

Buck-Boost

$$I_{CIN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (74)$$

9.2.1.2.9 N-channel FET

The N-channel FET voltage rating should be at least 15% higher than the maximum N-channel FET drain-to-source voltage (V_{T-MAX}):

Buck

$$V_{T-MAX} = V_{IN-MAX} \quad (75)$$

Boost

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Typical Applications (continued)

$$V_{T\text{-}MAX} = V_O \quad (76)$$

Buck-Boost

$$V_{T\text{-}MAX} = V_{IN\text{-}MAX} + V_O \quad (77)$$

The current rating should be at least 10% higher than the maximum average N-channel FET current ($I_{T\text{-}MAX}$):

Buck

$$I_{T\text{-}MAX} = D_{MAX} \times I_{LED} \quad (78)$$

Boost and Buck-Boost

$$I_{T\text{-}MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times I_{LED} \quad (79)$$

Approximate the nominal RMS transistor current ($I_{T\text{-}RMS}$) :

Buck

$$I_{T\text{-}RMS} = I_{LED} \times \sqrt{D} \quad (80)$$

9.2.1.2.9.1 Boost and Buck-Boost

$$I_{T\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} \quad (81)$$

Given an N-channel FET with on-resistance ($R_{DS\text{-}ON}$), solve for the nominal power dissipation (P_T):

$$P_T = I_{T\text{-}RMS}^2 \times R_{DSON} \quad (82)$$

9.2.1.2.10 Diode

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage ($V_{RD\text{-}MAX}$):

Buck

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} \quad (83)$$

Boost

$$V_{RD\text{-}MAX} = V_O \quad (84)$$

Buck-Boost

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O \quad (85)$$

The current rating should be at least 10% higher than the maximum average diode current ($I_{D\text{-}MAX}$):

Buck

$$I_{D\text{-}MAX} = (1 - D_{MIN}) \times I_{LED} \quad (86)$$

Boost and Buck-Boost

$$I_{D\text{-}MAX} = I_{LED} \quad (87)$$

Replace D_{MAX} with D in the $I_{D\text{-}MAX}$ equation to solve for the average diode current (I_D). Given a diode with forward voltage (V_{FD}), solve for the nominal power dissipation (P_D):

$$P_D = I_D \times V_{FD} \quad (88)$$

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Typical Applications (continued)

9.2.1.2.11 Output OVLO

For boost and buck-boost regulators, output OVLO is programmed with the turn-off threshold voltage ($V_{TURN-OFF}$) and the desired hysteresis (V_{HYSO}). To set V_{HYSO}, solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{23\,\mu A} \tag{89}$$

To set $V_{TURN-OFF}$, solve for R_{OV1}:

Boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN-OFF} - 1.24V} \tag{90}$$

Buck-Boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN-OFF} - 620\,mV} \tag{91}$$

A small filter capacitor (C_{OVP} = 47 pF) should be added from the OVP pin to ground to reduce coupled switching noise.

9.2.1.2.12 Input UVLO

For all topologies, input UVLO is programmed with the turnon threshold voltage ($V_{TURN-ON}$) and the desired hysteresis (V_{HYS}).

Method 1: If no PWM dimming is required, a two resistor network can be used. To set V_{HYS}, solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{23\,\mu A} \tag{92}$$

To set $V_{TURN-ON}$, solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} \tag{93}$$

Method 2: If PWM dimming is required, a three resistor network is suggested. To set $V_{TURN-ON}$, assume R_{UV2} = 10 kΩ and solve for R_{UV1} as in Method 1. To set V_{HYS}, solve for R_{UVH}:

$$R_{UVH} = \frac{R_{UV1} \times (V_{HYS} - 23\,\mu A \times R_{UV2})}{23\,\mu A \times (R_{UV1} + R_{UV2})} \tag{94}$$

9.2.1.2.13 PWM Dimming Method

PWM dimming can be performed several ways:

Method 1: Connect the dimming MOSFET (Q_3) with the drain to the nDIM pin and the source to AGND. Apply an external PWM signal to the gate of Q_{DIM}. A pulldown resistor may be necessary to properly turn off Q_3.

Method 2: Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

The DDRV pin should be connected to the gate of the dimFET with or without level-shifting circuitry as described in the *PWM Dimming* section. The dimFET should be rated to handle the average LED current and the nominal output voltage.

9.2.1.2.14 Analog Dimming Method

Analog dimming can be performed several ways:

Method 1: Place a potentiometer in series with the R_{CSH} resistor to dim the LED current from the nominal I_{LED} to near zero.

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Typical Applications (continued)

Method 2: Connect a controlled current source as detailed in the *Analog Dimming* section to the CSH pin. Increasing the current sourced into the CSH node decreases the LEDs from the nominal I_{LED} to zero current in the same manner as the thermal foldback circuit.

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Typical Applications (continued)

9.2.2 LM3421 Buck-Boost Application

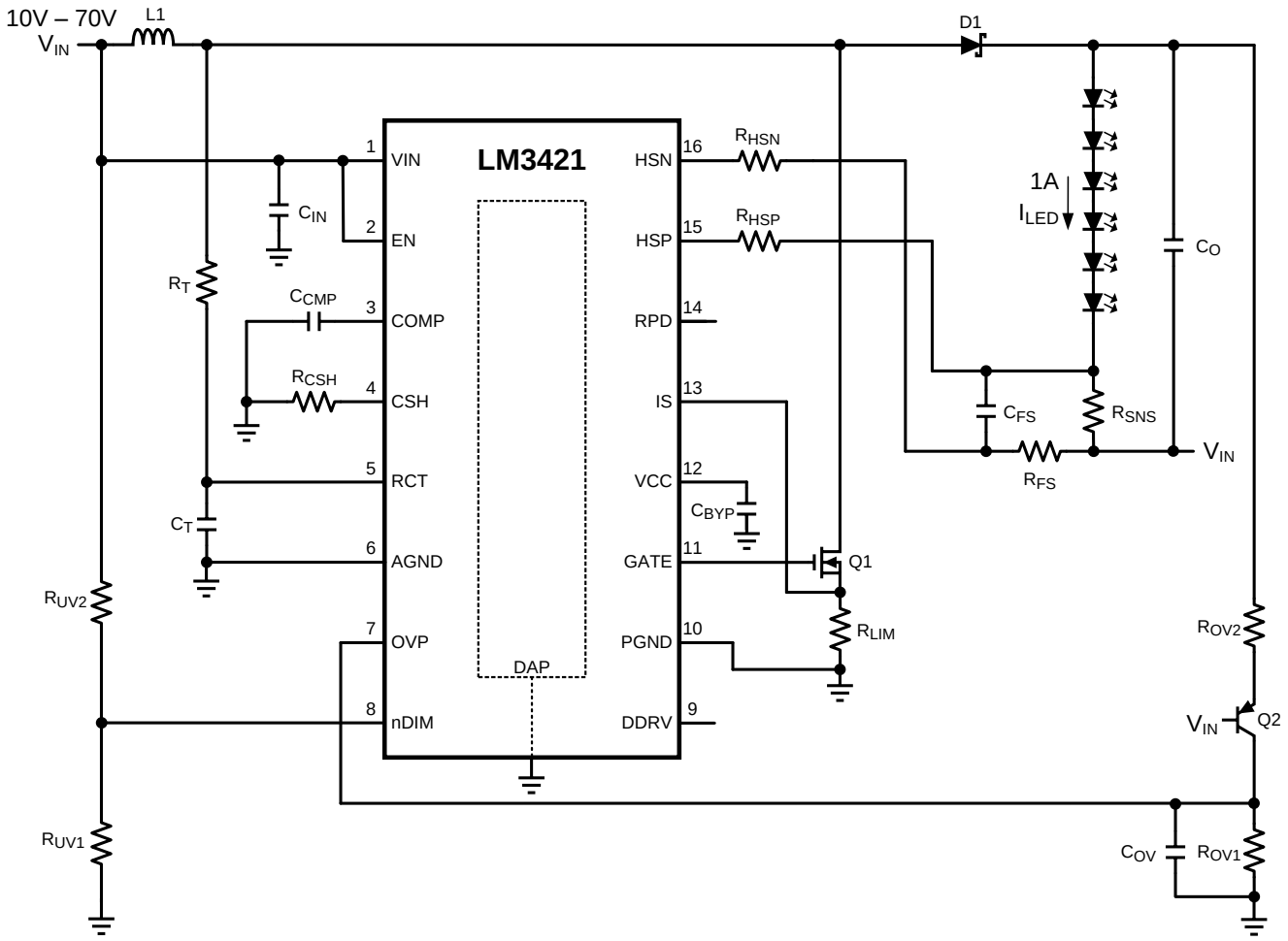


Figure 36. LM3421 Buck-Boost Application

9.2.2.1 Design Requirements

N = 6

V_{LED} = 3.5 V

r_{LED} = 325 mΩ

V_{IN} = 24 V

V_{IN-MIN} = 10 V

V_{IN-MAX} = 70 V

f_{SW} = 500 kHz

V_{SNS} = 100 mV

I_{LED} = 1 A

Δi_{L-PP} = 700 mA

Δi_{LED-PP} = 12 mA

Δv_{IN-PP} = 100 mV

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Typical Applications (continued)

I_{LIM} = 6 A

$V_{TURN\text{-}ON}$ = 10 V

V_{HYS} = 3 V

$V_{TURN\text{-}OFF}$ = 40 V

V_{HYSO} = 10 V

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Operating Point

Solve for V_O and r_D:

$$V_O = N \times V_{LED} = 6 \times 3.5V = 21V \tag{95}$$

$$r_D = N \times r_{LED} = 6 \times 325\ m\Omega = 1.95\Omega \tag{96}$$

Solve for D, D', D_{MAX}, and D_{MIN}:

$$D = \frac{V_O}{V_O + V_{IN}} = \frac{21V}{21V + 24V} = 0.467 \tag{97}$$

$$D' = 1 - D = 1 - 0.467 = 0.533 \tag{98}$$

$$D_{MIN} = \frac{V_O}{V_O + V_{IN\text{-}MAX}} = \frac{21V}{21V + 70V} = 0.231 \tag{99}$$

$$D_{MAX} = \frac{V_O}{V_O + V_{IN\text{-}MIN}} = \frac{21V}{21V + 10V} = 0.677 \tag{100}$$

9.2.2.2.2 Switching Frequency

Assume C_T = 1 nF and solve for R_T:

$$R_T = \frac{25}{f_{SW} \times C_T} = \frac{25}{500\ kHz \times 1\ nF} = 50\ k\Omega \tag{101}$$

The closest standard resistor is 49.9 kΩ; therefore, f_{SW} is:

$$f_{SW} = \frac{25}{R_T \times C_T} = \frac{25}{49.9\ k\Omega \times 1\ nF} = 501\ kHz \tag{102}$$

The chosen component from step 2 is:

C_T = 1 nF

R_T = 49.9 kΩ (103)

9.2.2.2.3 Average LED Current

Solve for R_{SNS}:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} = \frac{100\ mV}{1A} = 0.1\Omega \tag{104}$$

Assume R_{CSH} = 12.4 kΩ and solve for R_{HSP}:

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} = \frac{1A \times 12.4\ k\Omega \times 0.1\Omega}{1.24V} = 1.0\ k\Omega \tag{105}$$

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Typical Applications (continued)

The closest standard resistor for R_{SNS} is actually 0.1 Ω and for R_{HSP} is actually 1 kΩ; therefore, I_{LED} is:

$$I_{LED} = \frac{1.24V \times R_{HSP}}{R_{SNS} \times R_{CSH}} = \frac{1.24V \times 1.0\,k\Omega}{0.1\Omega \times 12.4\,k\Omega} = 1.0A \quad (106)$$

The chosen components from step 3 are:

$$R_{SNS} = 0.1\Omega$$
$$R_{CSH} = 12.4\,k\Omega$$
$$R_{HSP} = R_{HSN} = 1k\Omega \quad (107)$$

9.2.2.2.4 Inductor Ripple Current

Solve for L1:

$$L1 = \frac{V_{IN} \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} = \frac{24V \times 0.467}{700\,mA \times 501\,kHz} = 32\,\mu H \quad (108)$$

The closest standard inductor is 33 µH; therefore, $\Delta i_{L\text{-}PP}$ is:

$$\Delta i_{L\text{-}PP} = \frac{V_{IN} \times D}{L1 \times f_{SW}} = \frac{24V \times 0.467}{33\,\mu H \times 501\,kHz} = 678\,mA \quad (109)$$

Determine minimum allowable RMS current rating:

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta i_{L\text{-}PP} \times D'}{I_{LED}}\right)^2}$$

$$I_{L\text{-}RMS} = \frac{1A}{0.533} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{678\,mA \times 0.533}{1A}\right)^2} = 1.89A \quad (110)$$

The chosen component from step 4 is:

$$\boxed{L1 = 33\,\mu H} \quad (111)$$

9.2.2.2.5 Output Capacitance

Solve for C_O:

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}}$$

$$C_O = \frac{1A \times 0.467}{1.95\Omega \times 12\,mA \times 501\,kHz} = 39.8\,\mu F \quad (112)$$

The closest capacitance totals 40 µF; therefore, $\Delta i_{LED\text{-}PP}$ is:

$$\Delta i_{LED\text{-}PP} = \frac{I_{LED} \times D}{r_D \times C_O \times f_{SW}}$$

$$\Delta i_{LED\text{-}PP} = \frac{1A \times 0.467}{1.95\Omega \times 40\,\mu F \times 501\,kHz} = 12\,mA \quad (113)$$

Determine minimum allowable RMS current rating:

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Typical Applications (continued)

$$I_{CO\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \quad (114)$$

The chosen components from step 5 are:

$$\boxed{C_O = 4 \times 10\ \mu F} \quad (115)$$

9.2.2.2.6 Peak Current Limit

Solve for R_{LIM}:

$$R_{LIM} = \frac{245\ mV}{I_{LIM}} = \frac{245\ mV}{6A} = 0.041\Omega \quad (116)$$

The closest standard resistor is 0.04 Ω; therefore, I_{LIM} is:

$$I_{LIM} = \frac{245\ mV}{R_{LIM}} = \frac{245\ mV}{0.04\Omega} = 6.13A \quad (117)$$

The chosen component from step 6 is:

$$\boxed{R_{LIM} = 0.04\Omega} \quad (118)$$

9.2.2.2.7 Loop Compensation

ω_{P1} is approximated:

$$\omega_{P1} = \frac{1 + D}{r_D \times C_O} = \frac{1.467}{1.95\Omega \times 40\ \mu F} = 19k\frac{rad}{sec} \quad (119)$$

ω_{Z1} is approximated:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} = \frac{1.95\Omega \times 0.533^2}{0.467 \times 33\mu H} = 36k\frac{rad}{sec} \quad (120)$$

T_{U0} is approximated:

$$T_{U0} = \frac{D' \times 620V}{(1 + D) \times I_{LED} \times R_{LIM}} = \frac{0.533 \times 620V}{1.467 \times 1A \times 0.04\Omega} = 5630 \quad (121)$$

To ensure stability, calculate ω_{P2}:

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} = \frac{\omega_{P1}}{5 \times 5630} = \frac{19k\frac{rad}{sec}}{5 \times 5630} = 0.675\frac{rad}{sec} \quad (122)$$

Solve for C_{CMP}:

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5 \times 10^6\Omega} = \frac{1}{0.675\frac{rad}{sec} \times 5 \times 10^6\Omega} = 0.3\ \mu F \quad (123)$$

To attenuate switching noise, calculate ω_{P3}:

$$\omega_{P3} = (\max\ \omega_{P1}, \omega_{Z1}) \times 10 = \omega_{Z1} \times 10$$
$$\omega_{P3} = 36k\frac{rad}{sec} \times 10 = 360k\frac{rad}{sec} \quad (124)$$

Assume R_{FS} = 10 Ω and solve for C_{FS}:

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Typical Applications (continued)

$$C_{FS} = \frac{1}{10\Omega \times \omega_{P3}} = \frac{1}{10\Omega \times 360k\frac{rad}{sec}} = 0.28\,\mu F \tag{125}$$

The chosen components from step 7 are:

$$\boxed{\begin{aligned} C_{CMP} &= 0.33\,\mu F \\ R_{FS} &= 10\Omega \\ C_{FS} &= 0.27\mu F \end{aligned}} \tag{126}$$

9.2.2.2.8 Input Capacitance

Solve for the minimum C_{IN}:

$$C_{IN} = \frac{I_{LED} \times D}{\Delta v_{IN\text{-}PP} \times f_{SW}} = \frac{1A \times 0.467}{100\,mV \times 504\,kHz} = 9.27\,\mu F \tag{127}$$

To minimize power supply interaction a 200% larger capacitance of approximately 20 µF is used, therefore the actual $\Delta v_{IN\text{-}PP}$ is much lower. Because high voltage ceramic capacitor selection is limited, four 4.7-µF X7R capacitors are chosen.

Determine minimum allowable RMS current rating:

$$I_{IN\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \tag{128}$$

The chosen components from step 8 are:

$$\boxed{C_{IN} = 4 \times 4.7\ \mu F} \tag{129}$$

9.2.2.2.9 N-channel FET

Determine minimum Q1 voltage rating and current rating:

$$V_{T\text{-}MAX} = V_{IN\text{-}MAX} + V_O = 70V + 21V = 91V \tag{130}$$

$$I_{T\text{-}MAX} = \frac{0.677}{1 - 0.677} \times 1A = 2.1A \tag{131}$$

A 100-V N-channel FET is chosen with a current rating of 32 A due to the low $R_{DS\text{-}ON}$ = 50 mΩ. Determine $I_{T\text{-}RMS}$ and P_T:

$$I_{T\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} = \frac{1A}{0.533} \times \sqrt{0.467} = 1.28A \tag{132}$$

$$P_T = I_{T\text{-}RMS}^2 \times R_{DSON} = 1.28A^2 \times 50\,m\Omega = 82\,mW \tag{133}$$

The chosen component from step 9 is:

$$\underline{Q1 \rightarrow 32A,\ 100V,\ DPAK} \tag{134}$$

9.2.2.2.10 Diode

Determine minimum D1 voltage rating and current rating:

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Typical Applications (continued)

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O = 70V + 21V = 91V \quad (135)$$

$$I_{D\text{-}MAX} = I_{LED} = 1A \quad (136)$$

A 100-V diode is chosen with a current rating of 12 A and V_{DF} = 600 mV. Determine P_D:

$$P_D = I_D \times V_{FD} = 1A \times 600\,mV = 600\,mW \quad (137)$$

The chosen component from step 10 is:

$$\boxed{D1 \rightarrow 12A,\ 100V,\ DPAK} \quad (138)$$

9.2.2.2.11 Input UVLO

Solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{23\,\mu A} = \frac{3V}{23\,\mu A} = 130\,k\Omega \quad (139)$$

The closest standard resistor is 130 kΩ; therefore, V_{HYS} is:

$$V_{HYS} = R_{UV2} \times 23\,\mu A = 130\,k\Omega \times 23\,\mu A = 2.99V \quad (140)$$

Solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN\text{-}ON} - 1.24V} = \frac{1.24V \times 130\,k\Omega}{10V - 1.24V} = 18.4\,k\Omega \quad (141)$$

The closest standard resistor is 18.2 kΩ, making $V_{TURN\text{-}ON}$:

$$V_{TURN\text{-}ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN\text{-}ON} = \frac{1.24V \times (18.2\,k\Omega + 130\,k\Omega)}{18.2\,k\Omega} = 10.1V \quad (142)$$

The chosen components from step 11 are:

$$\boxed{\begin{aligned} R_{UV1} &= 18.2\,k\Omega \\ R_{UV2} &= 130\,k\Omega \end{aligned}} \quad (143)$$

9.2.2.2.12 Output OVLO

Solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{23\,\mu A} = \frac{10V}{23\,\mu A} = 435\,k\Omega \quad (144)$$

The closest standard resistor is 432 kΩ; therefore, V_{HYSO} is:

$$V_{HYSO} = R_{OV2} \times 23\,\mu A = 432\,k\Omega \times 23\,\mu A = 9.94V \quad (145)$$

Solve for R_{OV1}:

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 0.62V} = \frac{1.24V \times 432\,k\Omega}{40V - 0.62V} = 13.6\,k\Omega \quad (146)$$

The closest standard resistor is 13.7 kΩ, making $V_{TURN\text{-}OFF}$:

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Typical Applications (continued)

$$V_{TURN\text{-}OFF} = \frac{1.24V \times (0.5 \times R_{OV1} + R_{OV2})}{R_{OV1}}$$

$$V_{TURN\text{-}OFF} = \frac{1.24V \times (0.5 \times 13.7\,k\Omega + 432\,k\Omega)}{13.7\,k\Omega} = 39.7V \quad (147)$$

The chosen components from step 12 are:

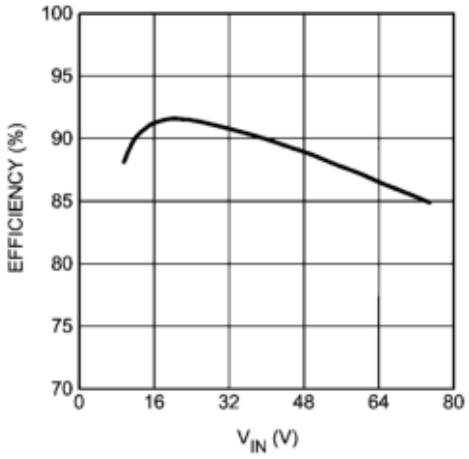
R_{OV1} = 13.7 kΩ
R_{OV2} = 432 kΩ (148)

Table 2. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3421	Buck-boost controller	TI	LM3421MH
1	C_{BYP}	2.2-µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{CMP}	0.33-µF X7R 10% 25V	MURATA	GRM21BR71E334KA01L
1	C_{FS}	0.27-µF X7R 10% 25V	MURATA	GRM21BR71E274KA01L
4	C_{IN}	4.7-µF X7R 10% 100V	TDK	C5750X7R2A475K
4	C_O	10-µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{OV}	47-pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100 V 12 A	VISHAY	12CWQ10FNPBF
1	L1	33 µH 20% 6.3 A	COILCRAFT	MSS1278-333MLB
1	Q1	NMOS 100 V 32 A	FAIRCHILD	FDD3682
1	Q2	PNP 150 V 600 mA	FAIRCHILD	MMBT5401
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10 Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{HSP}, R_{HSN}	1 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04 Ω 1% 1 W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	13.7 kΩ 1%	VISHAY	CRCW080513K7FKEA
1	R_{OV2}	432 kΩ 1%	VISHAY	CRCW0805432KFKEA
1	R_{SNS}	0.1 Ω 1% 1 W	VISHAY	WSL2512R1000FEA
1	R_T	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{UV1}	18.2 kΩ 1%	VISHAY	CRCW080518K2FKEA
1	R_{UV2}	130 kΩ 1%	VISHAY	CRCW0805130KFKEA

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9.2.2.3 Application Curve



V_{OUT} = 21 V

Figure 37. Sample Buck-Boost Efficiency vs Input Voltage.

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9.2.3 LM3421 BOOST Application

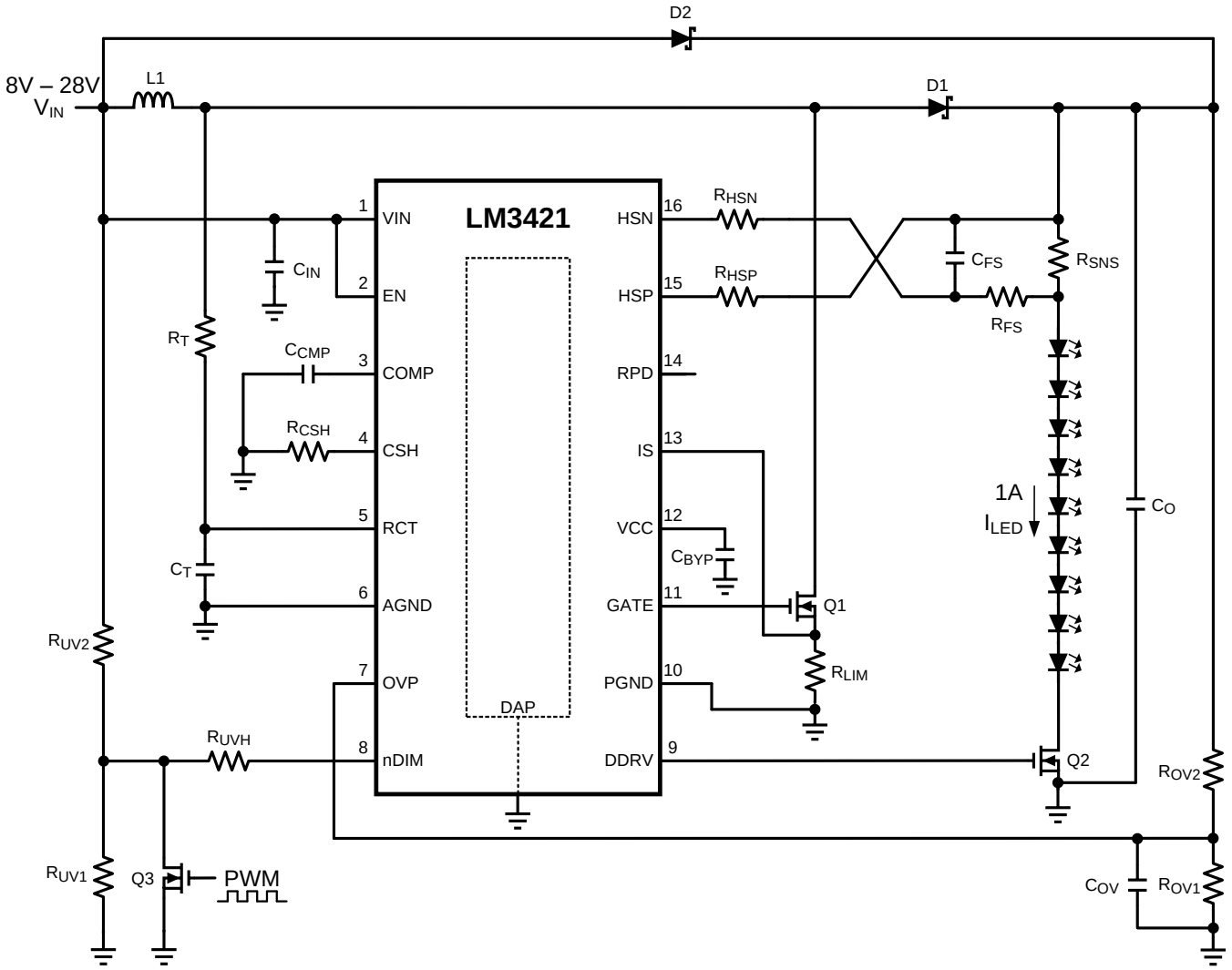


Figure 38. LM3421 BOOST Application

9.2.3.1 Design Requirements

- Input: 8 V to 28 V
- Output: 9 LEDs at 1 A
- PWM Dimming up to 30kHz
- Switching Frequency: 700-kHz

9.2.3.2 Detailed Design Procedure

Table 3. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3421	Boost controller	TI	LM3421MH
1	C_{BYP}	2.2-µF X7R 10% 16 V	MURATA	GRM21BR71C225KA12L
1	C_{CMP}	0.1-µF X7R 10% 25 V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
4	C_{IN}	4.7-µF X7R 10% 100 V	TDK	C5750X7R2A475K
4	C_O	10-µF X7R 10% 50 V	TDK	C4532X7R1H106K
1	C_{OV}	47-pF COG/NPO 5% 50 V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H102JA01D
2	D1, D2	Schottky 60 V 5 A	COMCHIP	CDBC560-G
1	L1	33-µH 20% 6.3 A	COILCRAFT	MSS1278-333MLB
2	Q1, Q2	NMOS 60 V 8 A	VISHAY	SI4436DY
1	Q3	NMOS 60 V 115 mA	ON-SEMI	2N7002ET1G
2	R_{CSH}, R_{OV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0 Ω 1%	VISHAY	CRCW08050000Z0EA
2	R_{HSP}, R_{HSN}	1 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.06 Ω 1% 1 W	VISHAY	WSL2512R0600FEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.1 Ω 1% 1 W	VISHAY	WSL2512R1000FEA
1	R_{UV2}	10 kΩ 1%	VISHAY	CRCW080510K0FKEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{UV1}	1.82 kΩ 1%	VISHAY	CRCW08051K82FKEA
1	R_{UVH}	17.8 kΩ 1%	VISHAY	CRCW080517K8FKEA

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9.2.4 LM3421 Buck-Boost Application

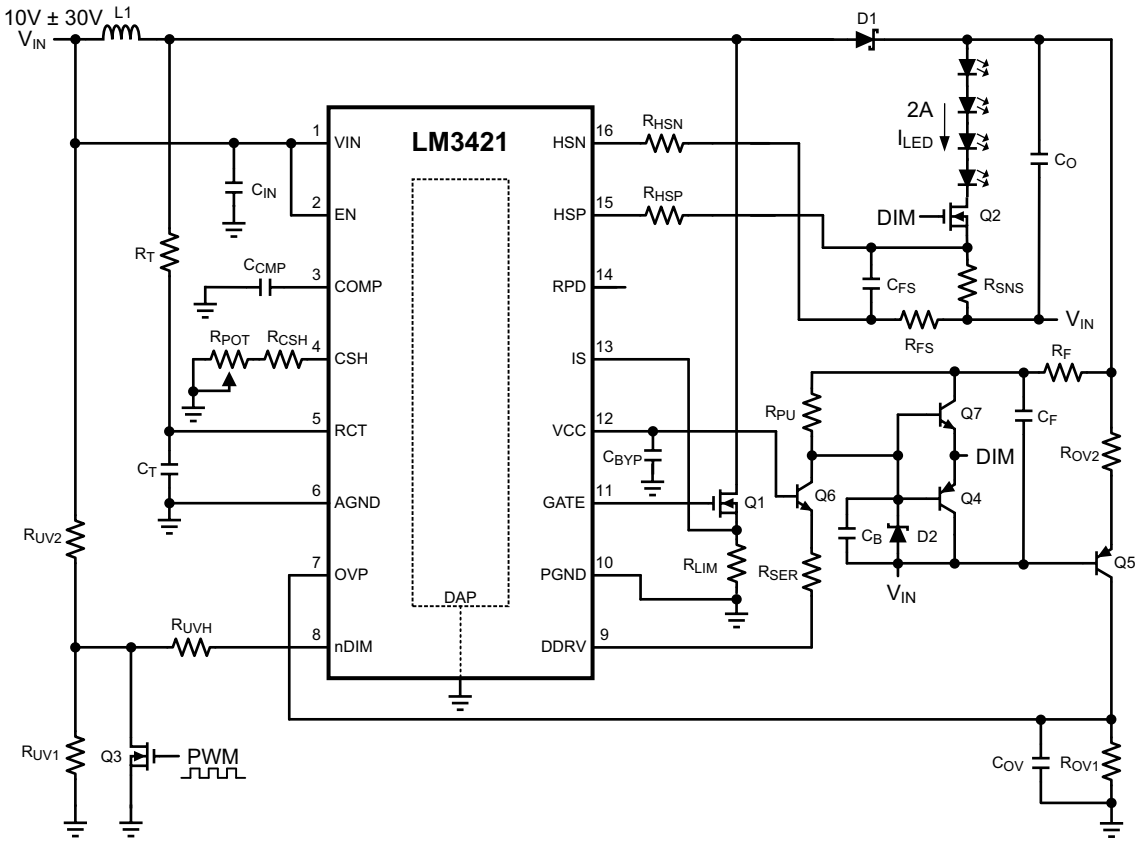


Figure 39. LM3421 Buck-Boost Application

9.2.4.1 Design Requirements

- Input: 10 V to 30 V
- Output: 4 LEDs at 2 A
- PWM Dimming: up to 10 kHz
- Analog Dimming
- Switching Frequency: 600-kHz

9.2.4.2 Detailed Design Procedure

Table 4. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3421	Buck-boost controller	TI	LM3421MH
1	C_B	100-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H101JA01D
1	C_{BYP}	2.2-µF X7R 10% 16 V	MURATA	GRM21BR71C225KA12L
3	C_{CMP}, C_{REF}, C_{SS}	1-µF X7R 10% 25 V	MURATA	GRM21BR71E105KA01L
1	C_F	0.1-µF X7R 10% 25 V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
4	C_{IN}	6.8-µF X7R 10% 50 V	TDK	C5750X7R1H685K
4	C_O	10-µF X7R 10% 50 V	TDK	C4532X7R1H106K
1	C_{OV}	47-pF COG/NPO 5% 50 V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100 V 12 A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10 V 500 mA	ON-SEMI	BZX84C10LT1G
1	L1	22 µH 20% 7.2 A	COILCRAFT	MSS1278-223MLB
2	Q1, Q2	NMOS 60 V 8 A	VISHAY	SI4436DY
1	Q3	NMOS 60 V 260 mA	ON-SEMI	2N7002ET1G
1	Q4	PNP 40 V 200 mA	FAIRCHILD	MMBT5087
1	Q5	PNP 150 V 600 mA	FAIRCHILD	MMBT5401
1	Q6	NPN 300 V 600 mA	FAIRCHILD	MMBTA42
1	Q7	NPN 40 V 200 mA	FAIRCHILD	MMBT6428
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_F	10 Ω 1%	VISHAY	CRCW080510R0FKEA
1	R_{FS}	0 Ω 1%	VISHAY	CRCW08050000Z0EA
1	R_{UV2}	10 kΩ 1%	VISHAY	CRCW080510K0FKEA
2	R_{HSP}, R_{HSN}	1 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04 Ω 1% 1 W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	18.2 kΩ 1%	VISHAY	CRCW080518K2FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{POT}	1-MΩ potentiometer	BOURNS	3352P-1-105
1	R_{PU}	4.99 kΩ 1%	VISHAY	CRCW08054K99FKEA
1	R_{SER}	499 Ω 1%	VISHAY	CRCW0805499RFKEA
1	R_{SNS}	0.05 Ω 1% 1 W	VISHAY	WSL2512R0500FEA
1	R_T	41.2 kΩ 1%	VISHAY	CRCW080541K2FKEA
1	R_{UV1}	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R_{UVH}	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA

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9.2.5 LM3423 Boost Application

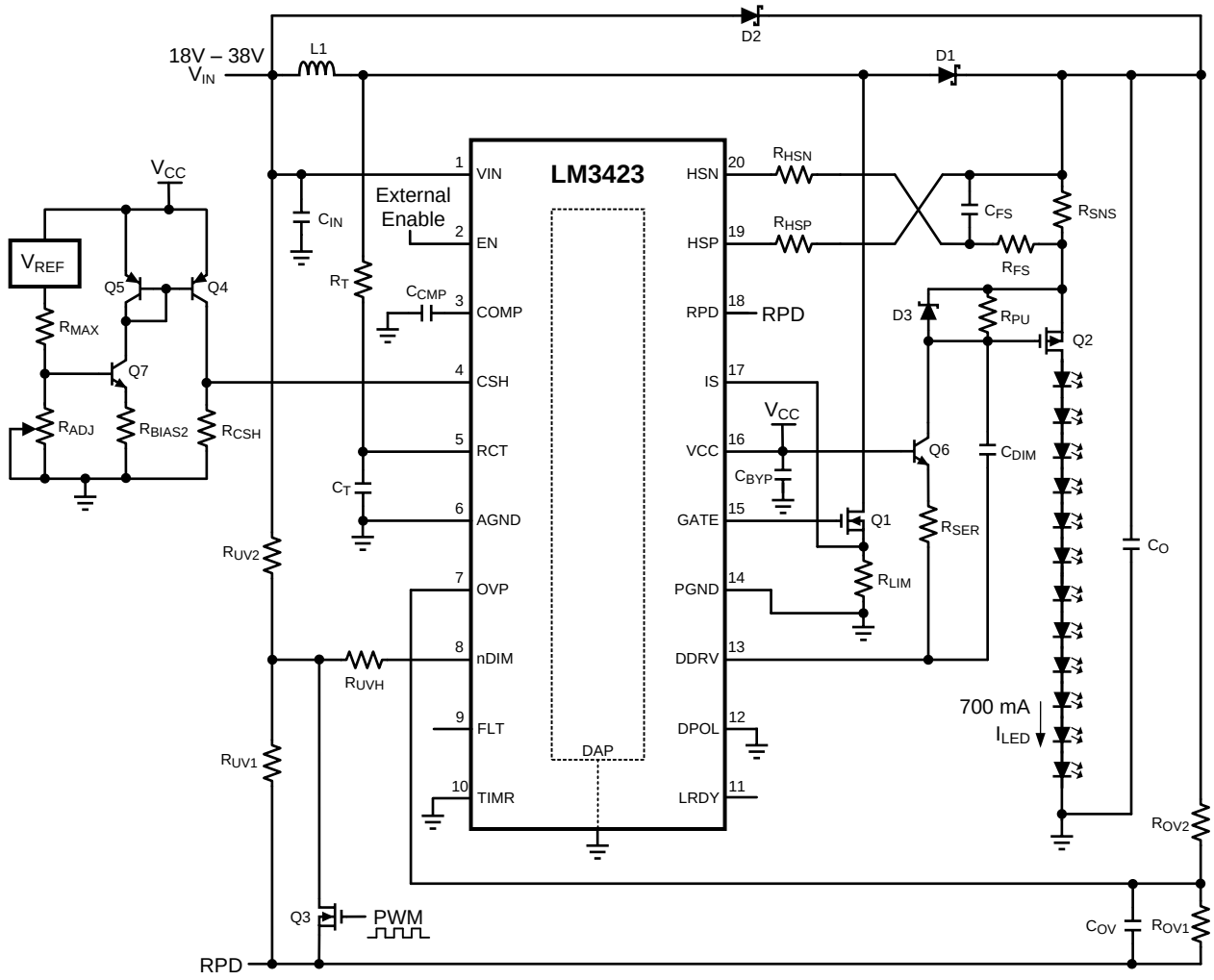


Figure 40. LM3423 Boost Application

9.2.5.1 Design Requirements

- Input: 18 V to 38 V
- Output: 12 LEDs at 700 mA
- High-Side PWM Dimming: up to 30 kHz
- Dimming: Analog
- Zero Current Shutdown
- Switching Frequency: 700-kHz

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9.2.5.2 Detailed Design Procedure

Table 5. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3423	Boost controller	TI	LM3423MH
1	C_{BYP}	2.2-µF X7R 10% 16 V	MURATA	GRM21BR71C225KA12L
1	C_{CMP}	1-µF X7R 10% 25 V	MURATA	GRM21BR71E105KA01L
1	C_{FS}	0.1-µF X7R 10% 25 V	MURATA	GRM21BR71E104KA01L
4	C_{IN}	4.7-µF X7R 10% 100 V	TDK	C5750X7R2A475K
4	C_O	10-µF X7R 10% 50 V	TDK	C4532X7R1H106K
1	C_{OV}	47-pF COG/NPO 5% 50 V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H102JA01D
2	D1, D2	Schottky 60 V 5 A	COMCHIP	CDBC560-G
1	D3	Zener 10 V 500 mA	ON-SEMI	BZX84C10LT1G
1	L1	47 µH 20% 5.3 A	COILCRAFT	MSS1278-473MLB
1	Q1	NMOS 60 V 8 A	VISHAY	SI4436DY
1	Q2	PMOS 70 V 5.7 A	ZETEX	ZXMP7A17K
1	Q3	NMOS 60 V 260 mA	ON-SEMI	2N7002ET1G
1	Q4, Q5 (dual pack)	Dual PNP 40 V 200 mA	FAIRCHILD	FFB3906
1	Q6	NPN 300 V 600 mA	FAIRCHILD	MMBTA42
1	Q7	NPN 40 V 200 mA	FAIRCHILD	MMBT3904
1	R_{ADJ}	100-kΩ potentiometer	BOURNS	3352P-1-104
1	R_{BIAS2}	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA
2	R_{CSH}, R_{OV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10 Ω 1%	VISHAY	CRCW080510R0FKEA
3	R_{HSP}, R_{HSN}, R_{MAX}	1 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.06 Ω 1% 1W	VISHAY	WSL2512R0600FEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{SNS}	0.15 Ω 1% 1W	VISHAY	WSL2512R1500FEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{UV1}	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R_{UV2}	10 kΩ 1%	VISHAY	CRCW080510K0FKEA
1	R_{UVH}	16.9 kΩ 1%	VISHAY	CRCW080516K9FKEA

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9.2.6 LM3421 Buck-Boost Application

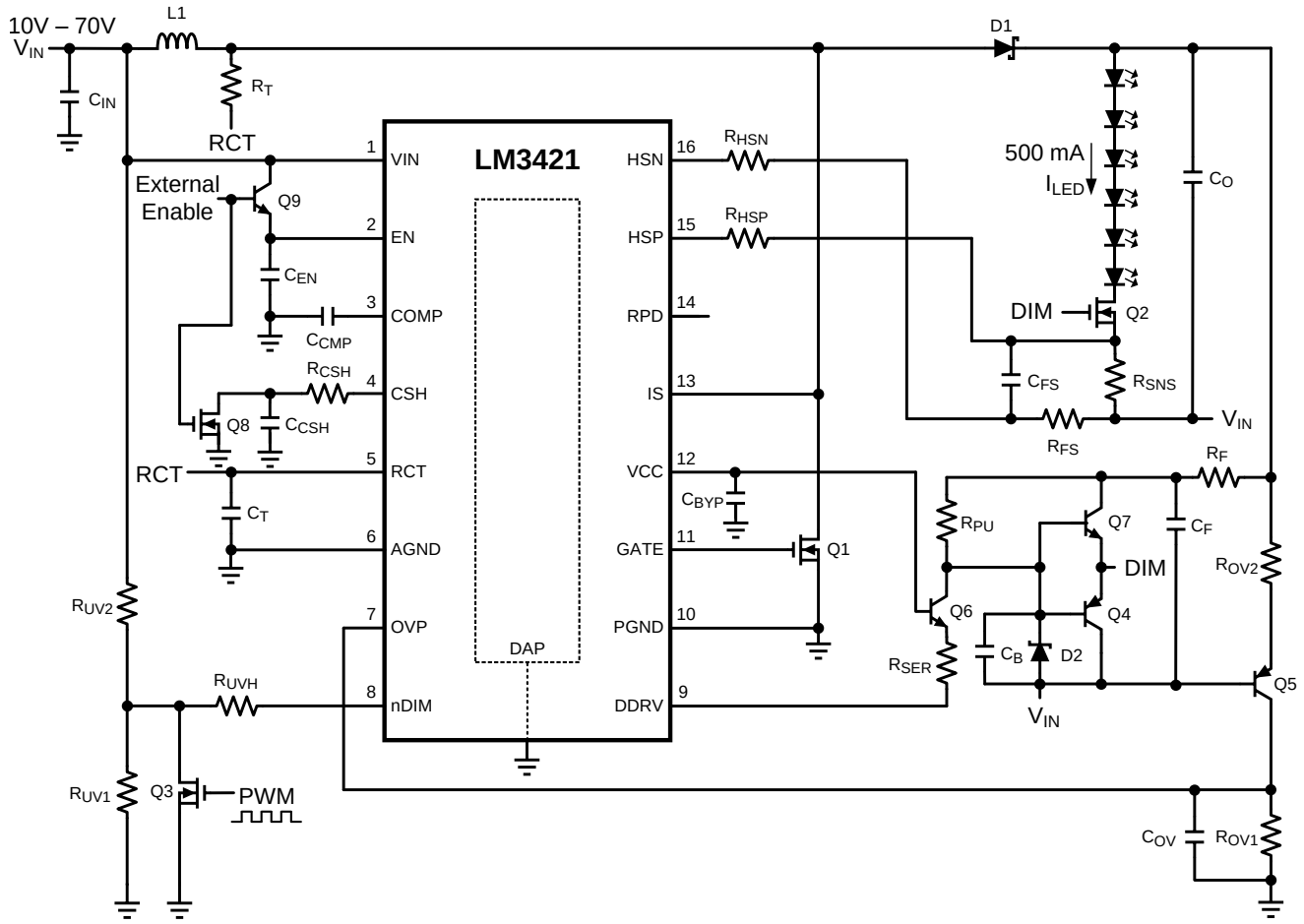


Figure 41. LM3421 Buck-Boost Application

9.2.6.1 Design Requirements

- Input: 10 V to 70 V
- Output: 6 LEDs at 500 mA
- PWM Dimming up to 10 kHz
- Slow Fade Out
- MOSFET R_{DS-ON} Sensing
- 700-kHz Switching Frequency

9.2.6.2 Detailed Design Procedure

Table 6. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3421	Buck-boost controller	TI	LM3421MH
1	C_B	100-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H101JA01D
1	C_{BYP}	2.2-µF X7R 10% 16 V	MURATA	GRM21BR71C225KA12L
1	C_{CMP}	1-µF X7R 10% 25 V	MURATA	GRM21BR71E105KA01L
1	C_F	0.1-µF X7R 10% 25 V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
4	C_{IN}	4.7-µF X7R 10% 100 V	TDK	C5750X7R2A475K
4	C_O	10-µF X7R 10% 50 V	TDK	C4532X7R1H106K
1	C_{OV}	47-pF COG/NPO 5% 50 V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100 V 12 A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10 V 500 mA	ON-SEMI	BZX84C10LT1G
1	L1	68 µH 20% 4.3 A	COILCRAFT	MSS1278-683MLB
2	Q1, Q2	NMOS 100 V 32 A	FAIRCHILD	FDD3682
1	Q3	NMOS 60 V 260 mA	ON-SEMI	2N7002ET1G
2	Q4, Q8	PNP 40 V 200 mA	FAIRCHILD	MMBT5087
1	Q5	PNP 150 V 600 mA	FAIRCHILD	MMBT5401
1	Q6	NPN 300 V 600 mA	FAIRCHILD	MMBTA42
2	Q7, Q9	NPN 40 V 200 mA	FAIRCHILD	MMBT6428
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0 Ω 1%	VISHAY	CRCW08050000Z0EA
1	R_{UV2}	10 kΩ 1%	VISHAY	CRCW080510K0FKEA
2	R_{HSP}, R_{HSN}	1 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{PU}	4.99 kΩ 1%	VISHAY	CRCW08054K99FKEA
1	R_{SER}	499 Ω 1%	VISHAY	CRCW0805499RFKEA
1	R_{SNS}	0.2 Ω 1% 1 W	VISHAY	WSL2512R2000FEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{UV1}	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R_{UVH}	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA

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9.2.7 LM3423 Buck Application

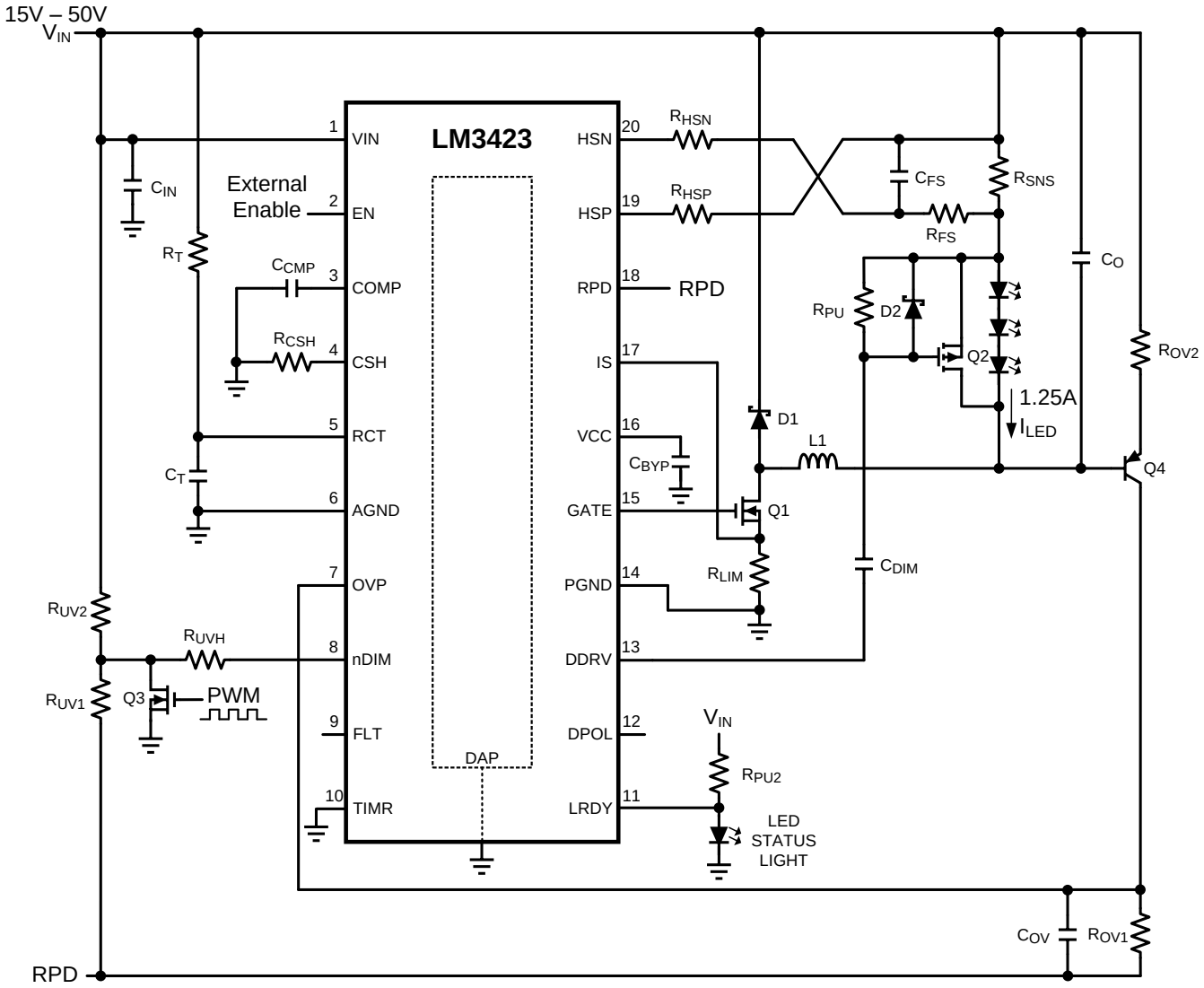


Figure 42. LM3423 Buck Application

9.2.7.1 Design Requirements

- Input: 15 V to 50 V
- Output: 3 LEDs at 1.25 A
- PWM Dimming up to 50 kHz
- LED Status Indicator
- Zero Current Shutdown
- 700-kHz Switching Frequency

9.2.7.2 Detailed Design Procedure

Table 7. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3423	Buck controller	TI	LM3423MH
1	C_{BYP}	2.2-µF X7R 10% 16 V	MURATA	GRM21BR71C225KA12L
2	C_{CMP}, C_{DIM}	0.1 µF X7R 10% 25 V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
4	C_{IN}	4.7-µF X7R 10% 100 V	TDK	C5750X7R2A475K
0	C_O	DNP		
1	C_{OV}	47-pF COG/NPO 5% 50 V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100 V 12 A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10 V 500 mA	ON-SEMI	BZX84C10LT1G
1	L1	22 µH 20% 7.3 A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 60 V 8 A	VISHAY	SI4436DY
1	Q2	PMOS 30 V 6.2 A	VISHAY	SI3483DV
1	Q3	NMOS 60 V 115 mA	ON-SEMI	2N7002ET1G
1	Q4	PNP 150 V 600 mA	FAIRCHILD	MMBT5401
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0 Ω 1%	VISHAY	CRCW08050000OZEA
2	R_{HSP}, R_{HSN}	1 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04 Ω 1% 1 W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	21.5 kΩ 1%	VISHAY	CRCW080521K5FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
3	R_{PU}, R_{PU2}, R_{UV2}	100 kΩ 1%	VISHAY	CRCW0805100KFKEA
1	R_T	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R_{SNS}	0.08 Ω 1% 1 W	VISHAY	WSL2512R0800FEA
1	R_{UV1}	11.5 kΩ 1%	VISHAY	CRCW080511K5FKEA

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9.2.8 LM3423 Buck-Boost Application

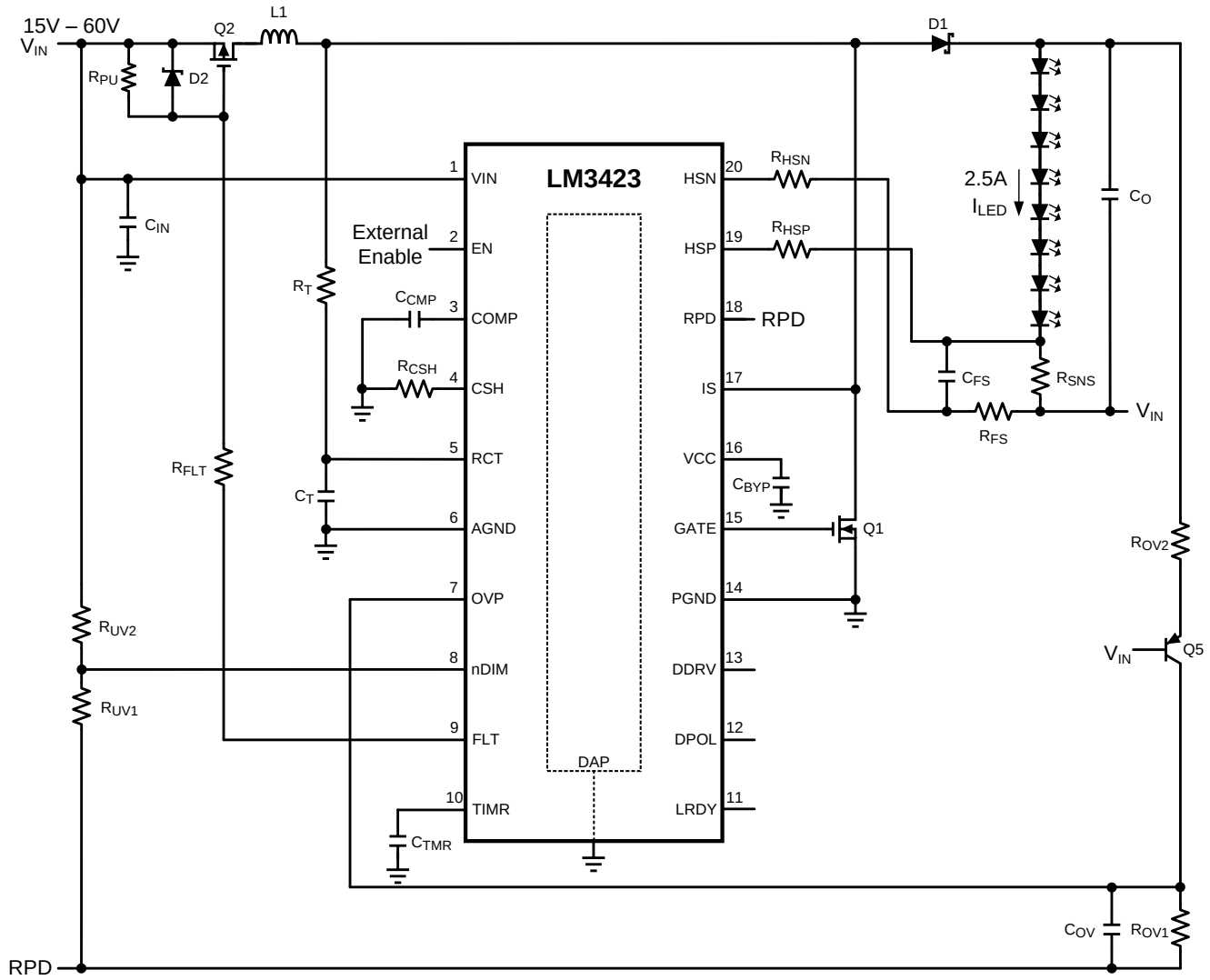


Figure 43. LM3423 Buck-Boost Application

9.2.8.1 Design Requirements

- Input: 15 V to 60 V
- Output: 8 LEDs at 2.5 A
- Fault Input Disconnect
- Zero Current Shutdown
- 500-kHz Switching Frequency

9.2.8.2 Detailed Design Procedure

Table 8. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3423	Buck-boost controller	TI	LM3423MH
1	C_{BYP}	2.2-µF X7R 10% 16 V	MURATA	GRM21BR71C225KA12L
1	C_{CMP}	0.33-µF X7R 10% 25 V	MURATA	GRM21BR71E334KA01L
1	C_{FS}	0.1-µF X7R 10% 25 V	MURATA	GRM21BR71E104KA01L
4	C_{IN}	4.7-µF X7R 10% 100 V	TDK	C5750X7R2A475K
4	C_O	10-µF X7R 10% 50 V	TDK	C4532X7R1H106K
1	C_{OV}	47-pF COG/NPO 5% 50 V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H102JA01D
1	C_{TMR}	220-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H221JA01D
1	D1	Schottky 100 V 12 A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10 V 500 mA	ON-SEMI	BZX84C10LT1G
1	L1	22 µH 20% 7.2 A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 100 V 32 A	FAIRCHILD	FDD3682
1	Q2	PMOS 70 V 5.7 A	ZETEX	ZXMP7A17K
1	Q5	PNP 150 V 600 mA	FAIRCHILD	MMBT5401
2	R_{CSH}, R_{OV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10 Ω 1%	VISHAY	CRCW080510R0FKEA
2	R_{FLT}, R_{PU2}	100 kΩ 1%	VISHAY	CRCW0805100KFKEA
2	R_{HSP}, R_{HSN}	1 kΩ 1%	VISHAY	CRCW08051K00FKEA
2	R_{LIM}, R_{SNS}	0.04 Ω 1% 1 W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_T	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{UV1}	13.7 kΩ 1%	VISHAY	CRCW080513K7FKEA
1	R_{UV2}	150 kΩ 1%	VISHAY	CRCW0805150KFKEA

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9.2.9 LM3421 SEPIC Application

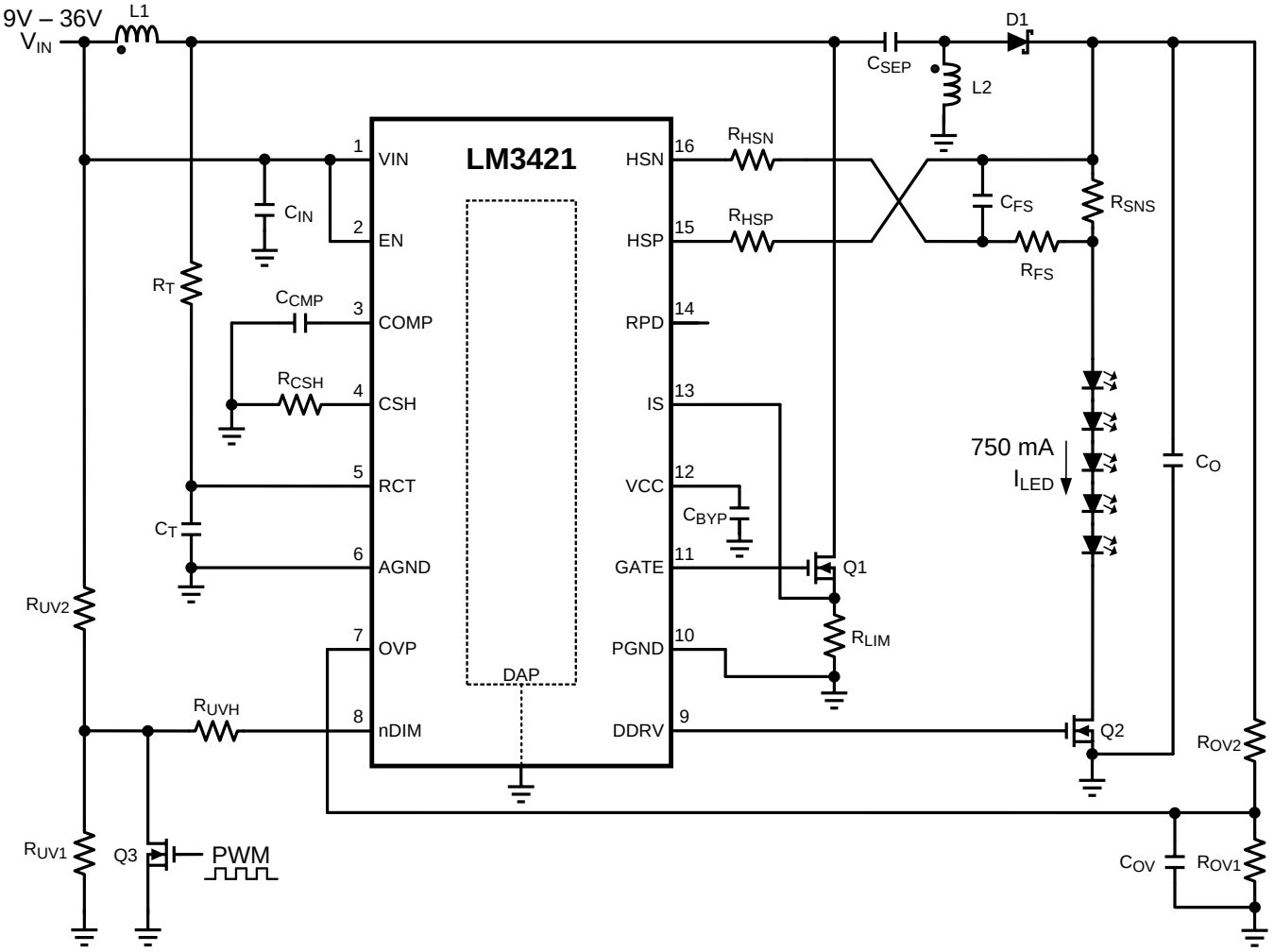


Figure 44. LM3421 SEPIC Application

9.2.9.1 Design Procedure

- Input: 9 V to 36 V
- Output: 5 LEDs at 750 mA
- PWM Dimming up to 30 kHz
- 500-kHz Switching Frequency

9.2.9.2 Detailed Design Procedure

Table 9. Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3421	SEPIC controller	TI	LM3421MH
1	C_{BYP}	2.2-µF X7R 10% 16 V	MURATA	GRM21BR71C225KA12L
1	C_{CMP}	0.47-µF X7R 10% 25 V	MURATA	GRM21BR71E474KA01L
0	C_{FS}	DNP		
4	C_{IN}	4.7-µF X7R 10% 100 V	TDK	C5750X7R2A475K
4	C_O	10-µF X7R 10% 50 V	TDK	C4532X7R1H106K
1	C_{SEP}	1-µF X7R 10% 100 V	TDK	C4532X7R2A105K
1	C_{OV}	47-pF COG/NPO 5% 50 V	AVX	08055A470JAT2A
1	C_T	1000-pF COG/NPO 5% 50 V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 60 V 5 A	COMCHIP	CDBC560-G
2	L1, L2	68 µH 20% 4.3 A	COILCRAFT	DO3340P-683
2	Q1, Q2	NMOS 60 V 8 A	VISHAY	SI4436DY
1	Q3	NMOS 60 V 115 mA	ON-SEMI	2N7002ET1G
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0 Ω 1%	VISHAY	CRCW08050000OZEA
2	R_{HSP}, R_{HSN}	750 Ω 1%	VISHAY	CRCW0805750RFKEA
1	R_{LIM}	0.04 Ω 1% 1 W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
2	R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{SNS}	0.1 Ω 1% 1 W	VISHAY	WSL2512R1000FEA
1	R_T	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{UV1}	1.62 kΩ 1%	VISHAY	CRCW08051K62FKEA
1	R_{UV2}	10 kΩ 1%	VISHAY	CRCW080510K0FKEA
1	R_{UVH}	16.9 kΩ 1%	VISHAY	CRCW080516K9FKEA

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10 Power Supply Recommendations

10.1 General Recommendations

The device is designed to operate from an input voltage supply range from 4.5 V to 75 V. This input supply should be well regulated. If the input supply is located more than a few inches from the EVM or PCB, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10.2 Input Supply Current Limit

It is important to set the output current limit of your input supply to an appropriate value to avoid delays in your converter analysis and optimization. If not set high enough, current limit can be tripped during start-up or when your converter output power is increased, causing a foldback or shutdown condition. It is a common oversight when powering up a converter for the first time.

11 Layout

11.1 Layout Guidelines

- The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines allows maximum noise rejection and minimal generation of EMI within the circuit.
- Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM34xx-Q1 buck regulator contains the input capacitor (C_{IN}), the recirculating diode (D1), the N-channel MOSFET (Q1), and the sense resistor (R_{LIM}). In the LM34xx-Q1 boost regulator, the discontinuous current flows through the output capacitor (C_O), D1, Q1, and R_{LIM}. In the buck-boost regulator, both loops are discontinuous and should be carefully layed out. These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.
- The RT, COMP, CSH, IS, HSP and HSN pins are all high-impedance inputs which couple external noise easily; therefore, the loops containing these nodes should be minimized whenever possible.
- In some applications the LED or LED array can be far away (several inches or more) from the controller or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

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11.2 Layout Example

Note critical paths and component placement:

Minimize power loop containing discontinuous currents

Minimize signal current loops (components close to IC)

- Ground plane under IC for signal routing helps minimize noise coupling

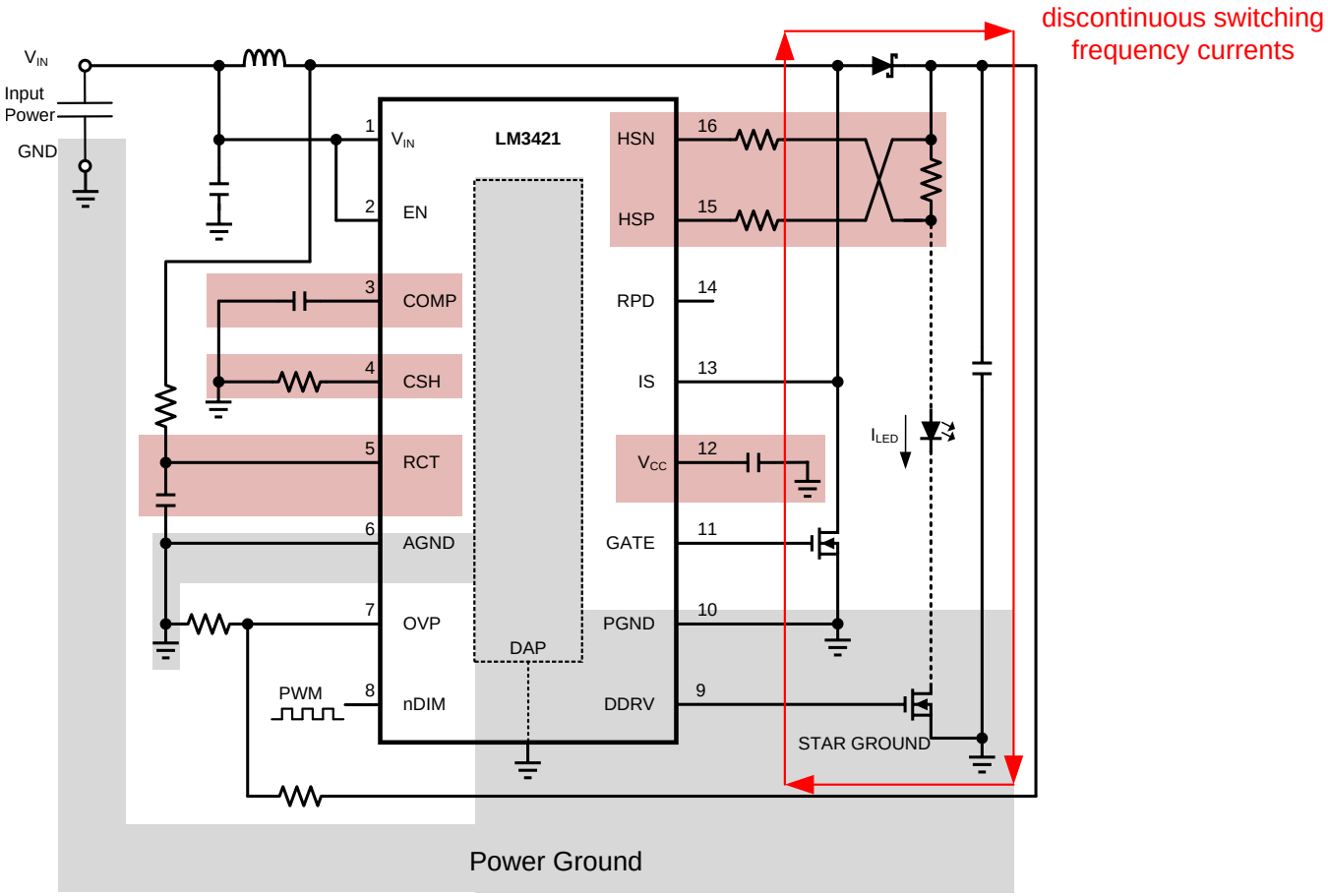


Figure 45. LM3421 Boost Layout Guideline

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM3421	Click here	Click here	Click here	Click here	Click here
LM3421-Q1	Click here	Click here	Click here	Click here	Click here
LM3423	Click here	Click here	Click here	Click here	Click here
LM3423-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3421MH/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH
LM3421MH/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH
LM3421MH/NOPB.B	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH
LM3421MHX/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH
LM3421MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH
LM3421MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH
LM3423MH/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH
LM3423MH/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH
LM3423MH/NOPB.B	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH
LM3423MHX/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH
LM3423MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH
LM3423MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM3421, LM3423 :

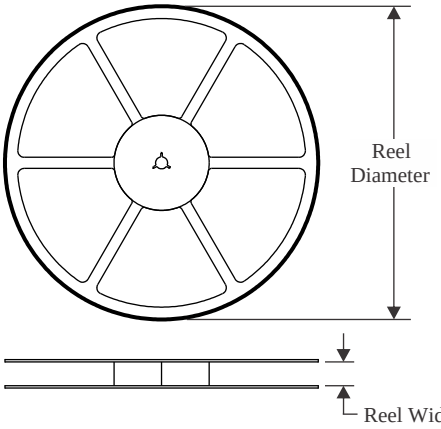
- Automotive : LM3421-Q1, LM3423-Q1

NOTE: Qualified Version Definitions:

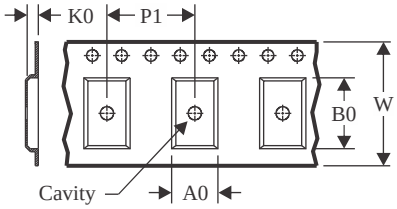
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

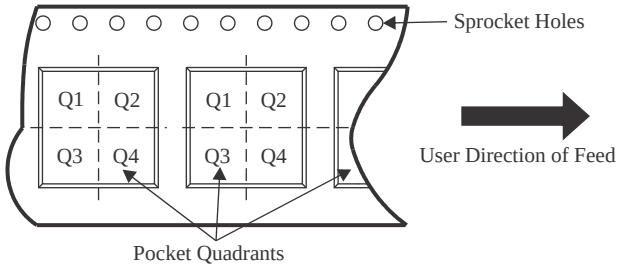


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

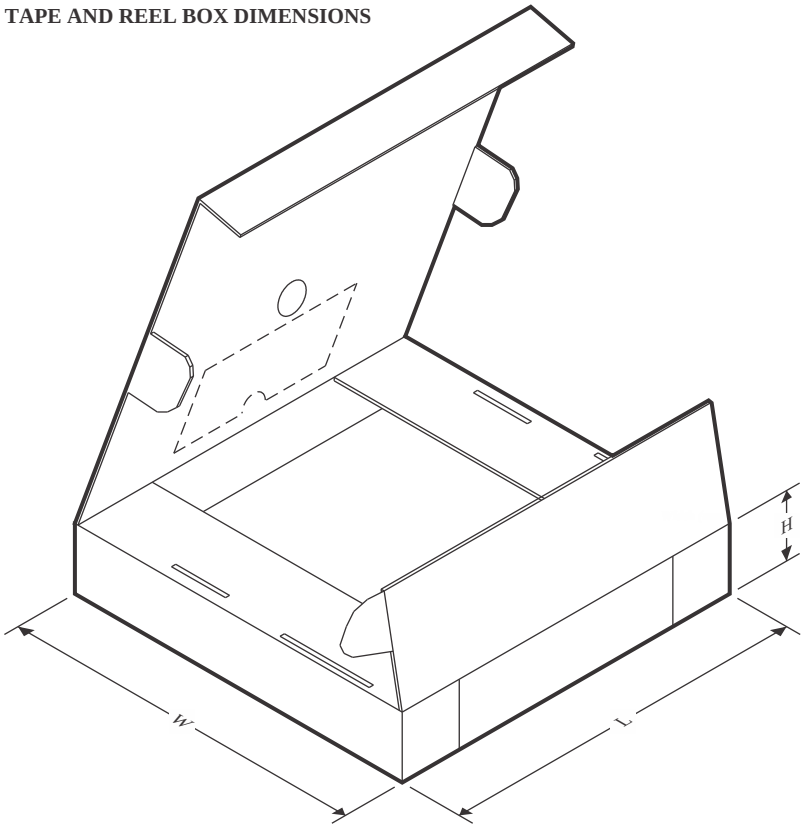
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3421MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM3423MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

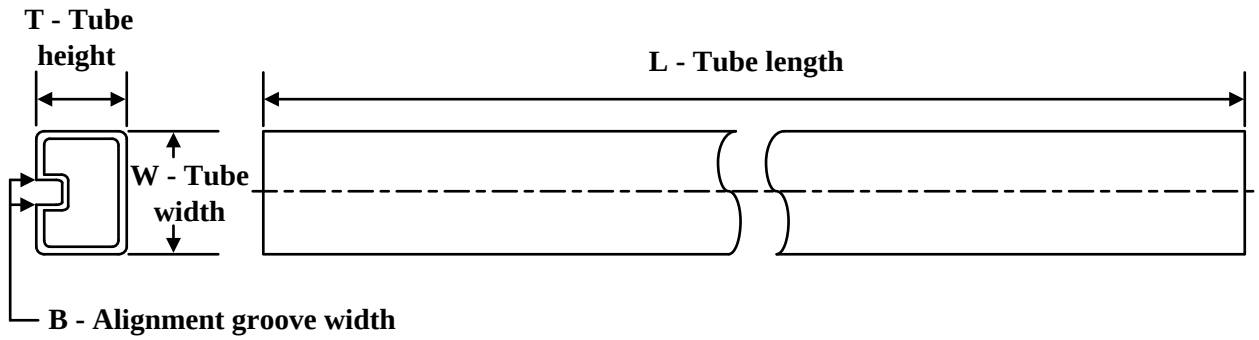
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

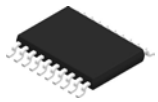
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3421MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM3423MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3421MH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM3421MH/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM3421MH/NOPB.B	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM3423MH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM3423MH/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM3423MH/NOPB.B	PWP	HTSSOP	20	73	495	8	2514.6	4.06

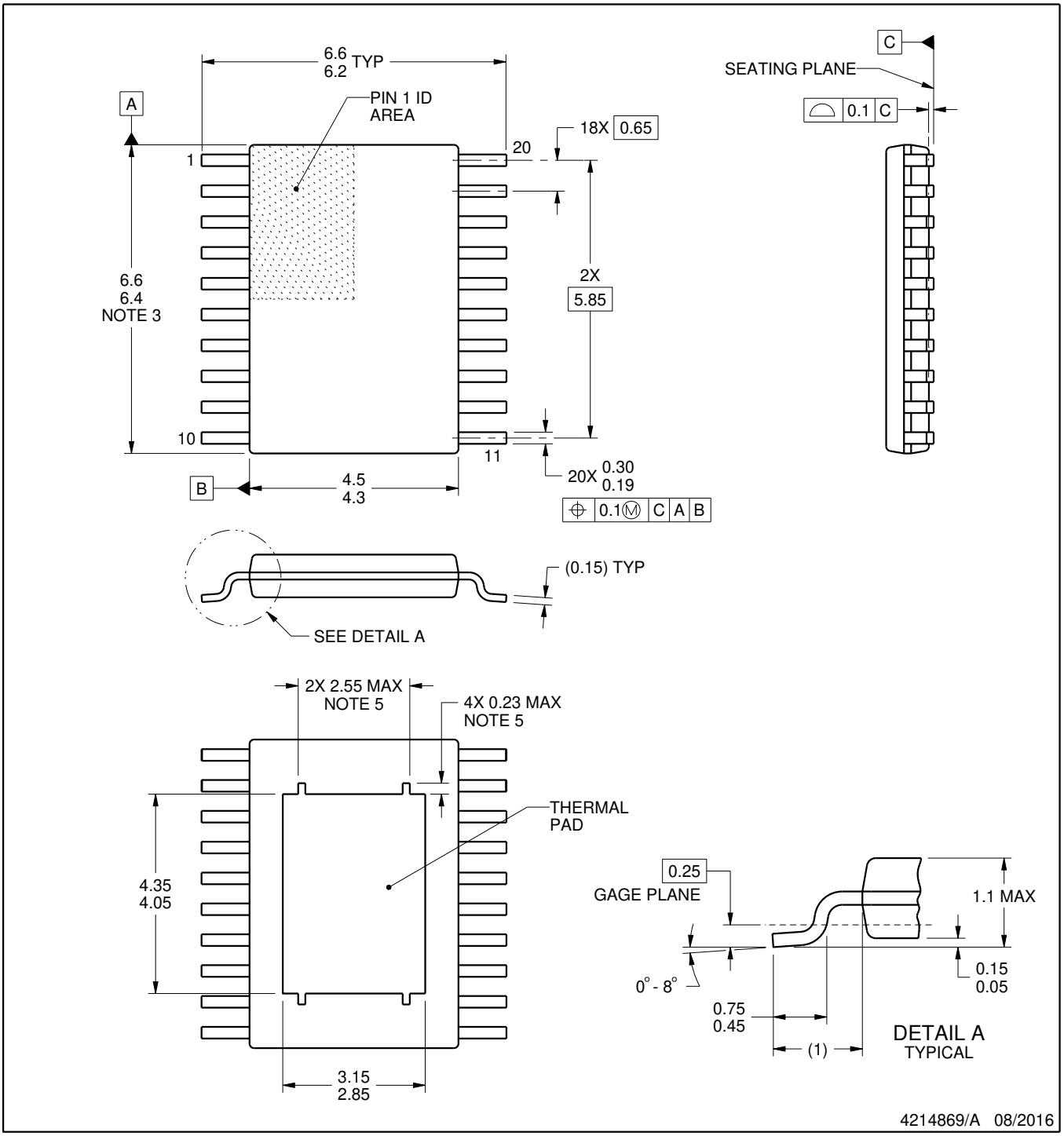


PACKAGE OUTLINE

PWP0020A

PowerPAD™ TSSOP - 1.1 mm max height

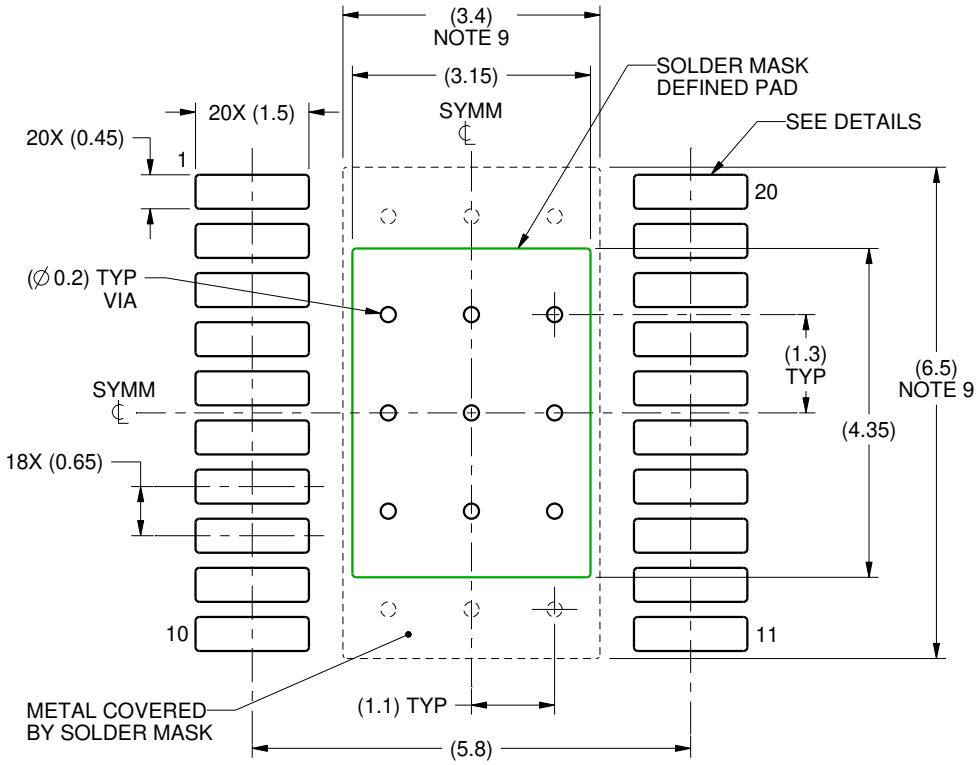
PLASTIC SMALL OUTLINE



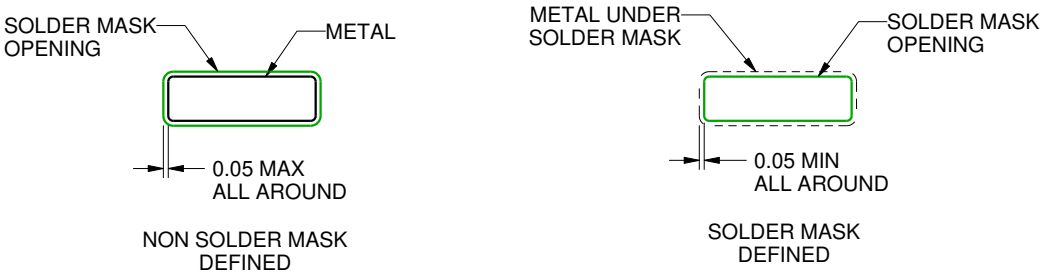
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

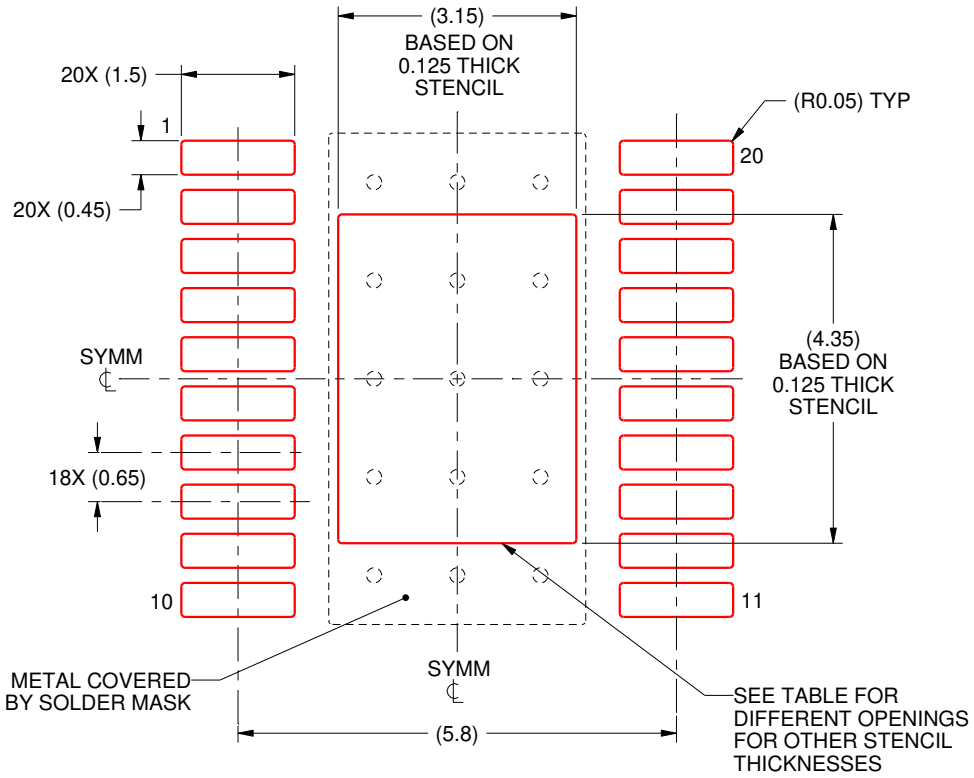


SOLDER MASK DETAILS
PADS 1-20

4214869/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.52 X 4.86
0.125	3.15 X 4.35 (SHOWN)
0.15	2.88 X 3.97
0.175	2.66 X 3.68

4214869/A 08/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

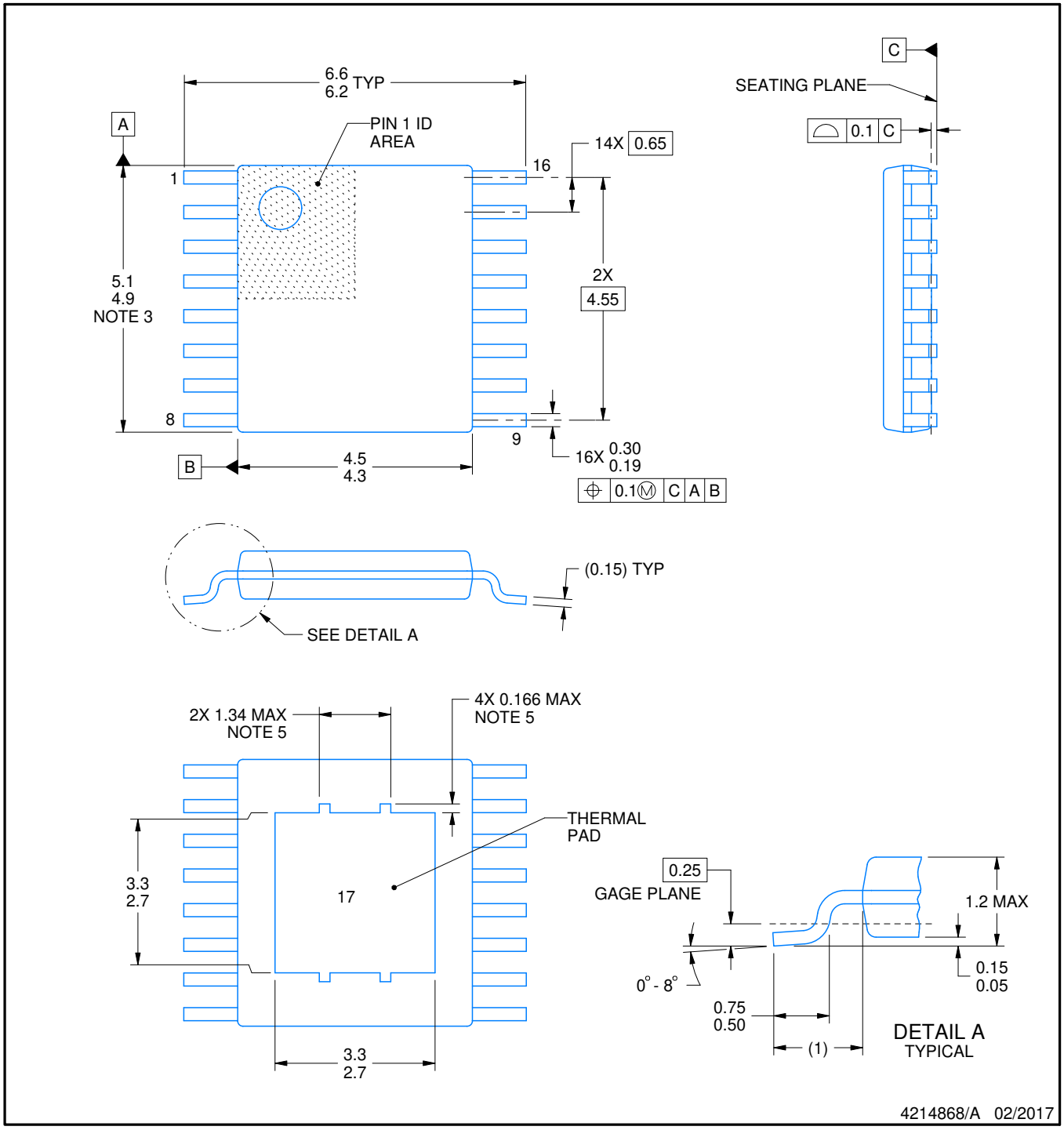


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

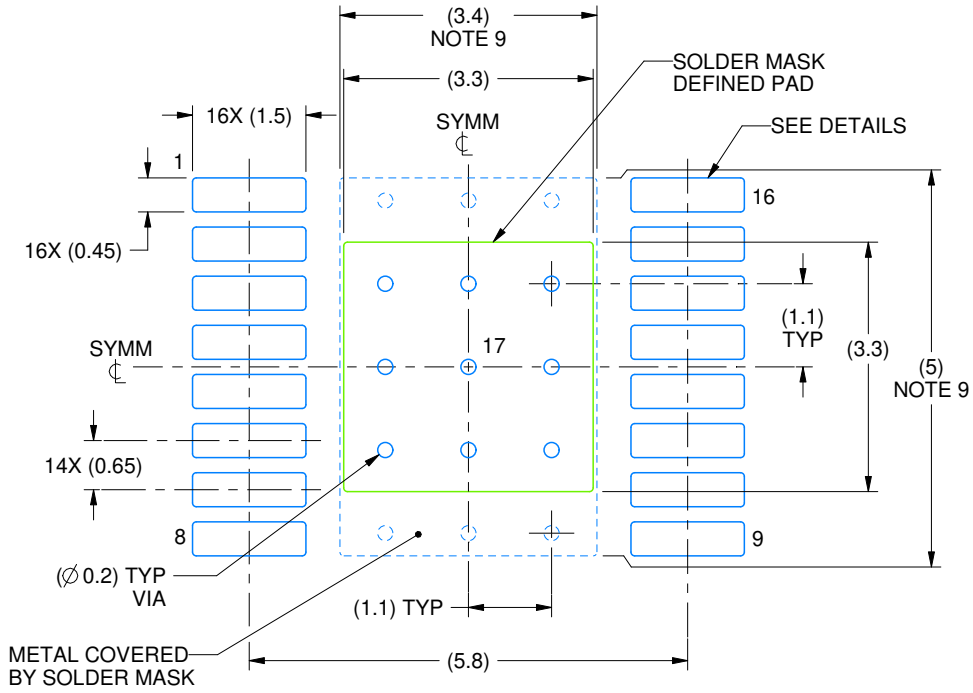
PLASTIC SMALL OUTLINE



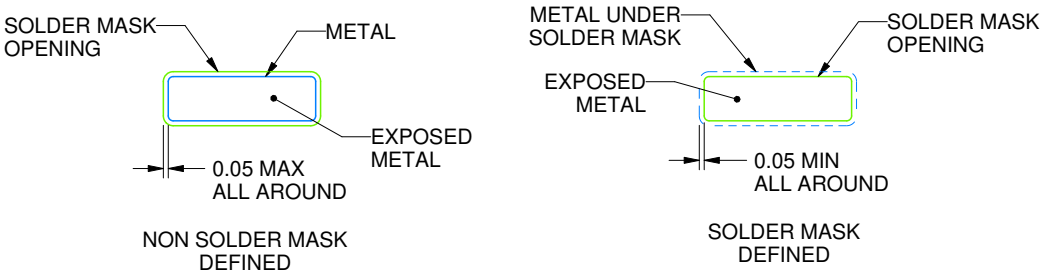
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

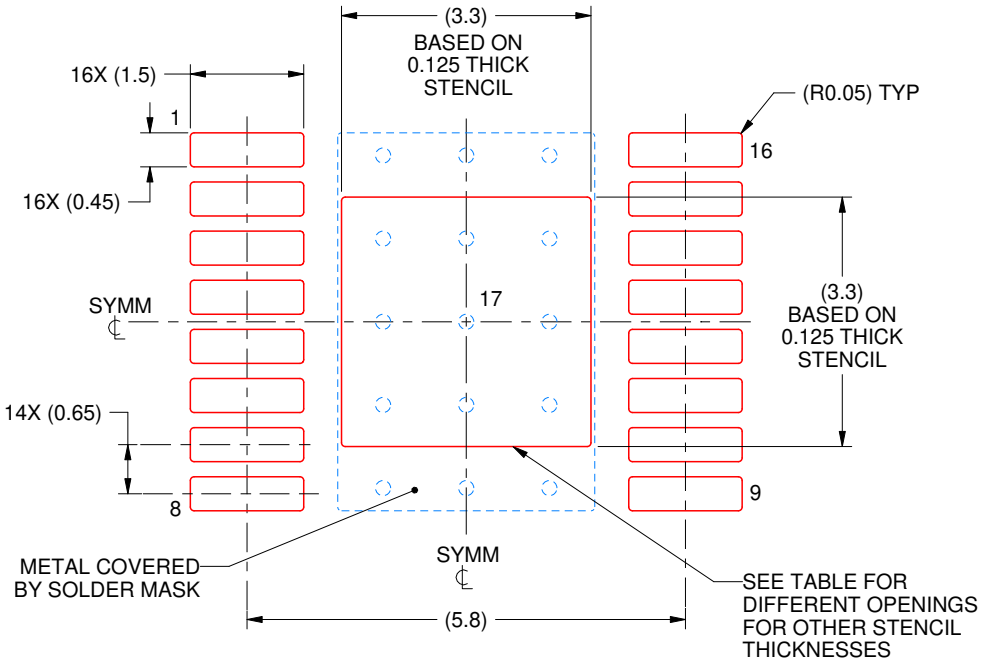


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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