LM5045 Full-Bridge PWM Controller With Integrated MOSFET Drivers

1 Features

- Highest Integration Controller for Small Form Factor, High-Density Power Converters
- High-Voltage Start-Up Regulator
- Intelligent Sync Rectifier Start-Up Allows Linear Turnon Into Prebiased Loads
- Synchronous Rectifiers Disabled in UVLO mode and Hiccup Mode
- Two Independent, Programmable Synchronous Rectifier Dead-Time Adjustments
- Four High-Current 2A Bridge Gate Drivers
- Wide-Bandwidth Optocoupler Interface
- Configurable for Either Current Mode or Voltage Mode Control
- Dual-Mode Overcurrent Protection
- Resistor Programmed 2MHz Oscillator
- Programmable Line UVLO and OVP

2 Applications

- E-Bike
- Military: Radar and Electronic Warfare
- Power: Telecom DC-DC Module: Analog
- Private Branch Exchange (PBX)
- Solar Power Inverters
- Vector Signal Generators
- Microwave Ovens
- Point-to-Point Microwave Backhaul
- Power: Telecom/Server AC/DC Supply: Dual Controller: Analog
- Solar Micro-Inverters
- TETRA Base Stations
- Washing Machine: Low-End

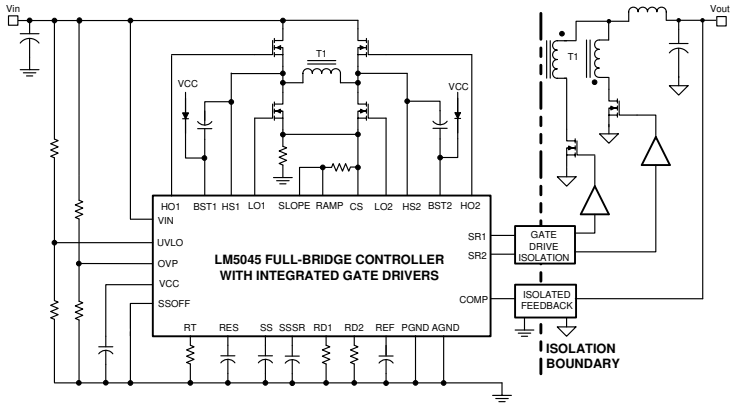
3 Description

The LM5045 PWM controller contains all of the features necessary to implement full-bridge topology power converters using either current mode or voltage mode control. This device is intended to operate on the primary side of an isolated DC-DC converter with input voltage up to 100V. This highly integrated controller-driver provides dual 2A high-side and low-side gate drivers for the four external bridge MOSFETs plus control signals for the secondary-side synchronous rectifier MOSFETs. External resistors program the leading and trailing edge dead-time between the main and synchronous rectifier control signals. Intelligent start-up of the synchronous rectifiers allows monotonic turnon of the power converter even with prebias load conditions. Additional features include cycle-by-cycle current limiting, hiccup mode restart, programmable soft-start, synchronous rectifier soft-start, and a 2MHz capable oscillator with synchronization capability and thermal shutdown.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
LM5045	HTSSOP (28)	9.70mm × 4.40mm
	WQFN (28)	5.00mm × 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Full-Bridge Power Converter

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

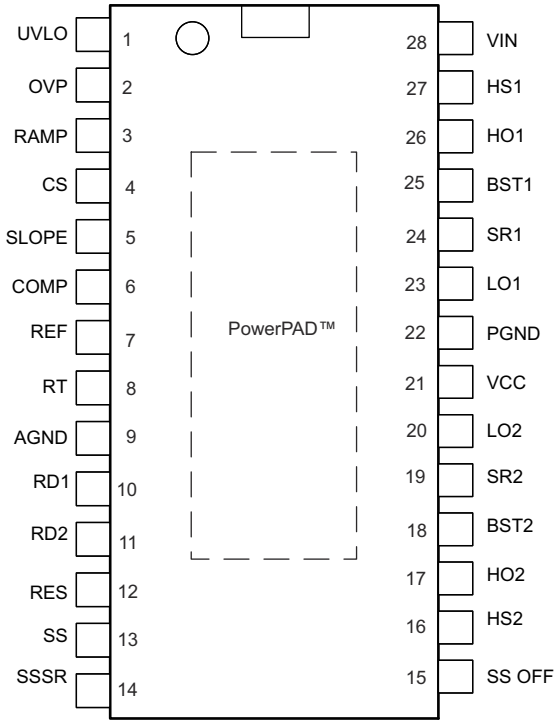

Figure 4-1. PWP Package 28-Pin HTSSOP With PowerPAD™ Top View

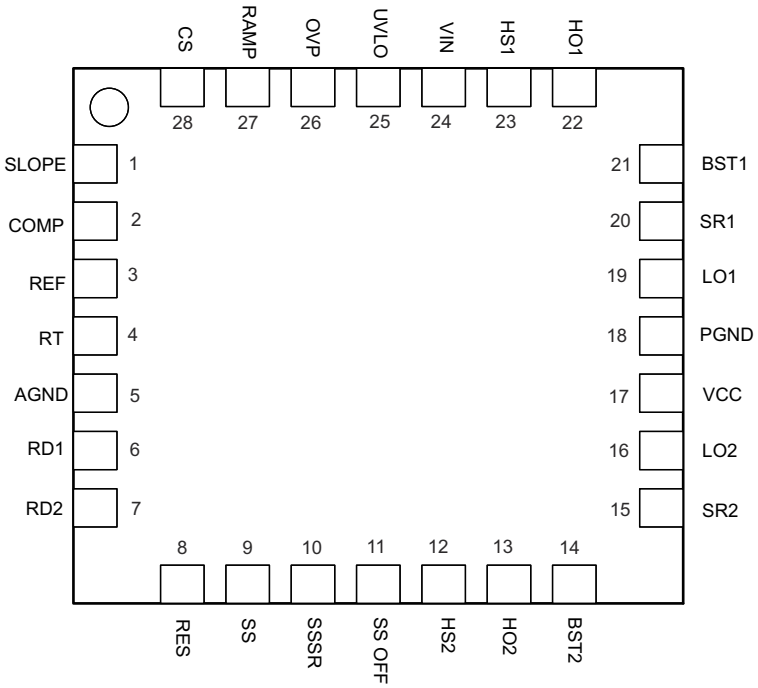

Figure 4-2. RSG Package 28-Pin WQFN, 5 mm × 5 mm Top View

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION	APPLICATION INFORMATION
NAME	HTSSOP	WQFN			
AGND	9	5	O	Analog Ground	Connect directly to the Power Ground.
BST1	25	21	I	Gate Drive Bootstrap	Bootstrap capacitors connected between BST1, 2 and SW1, 2 provide bias supply for the high side HO1, 2 gate drivers. External diodes are required between VCC and BST1, 2 to charge the bootstrap capacitors when SW1, 2 are low.
BST2	18	14			
COMP	6	2	I	Input to the Pulse Width Modulator	An external opto-coupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is at maximum with zero input current, while 1 mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the AC voltage across the opto-coupler.
CS	4	28	I	Current Sense Input	If CS exceeds 750 mV the PWM output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 40 nS after either output switches high to blank leading edge transients.
HO1	26	22	O	High Side Output Driver	High side PWM outputs capable of driving the upper MOSFET of the bridge with 1.5-A peak source and 2-A peak sink current.
HO2	17	13			
HS1	27	23	I	Switch Node	Common connection of the high side FET source, low side FET drain and transformer primary winding.
HS2	16	12			
LO1	23	19	O	Low Side Output Driver	Alternating output of the PWM gate driver. Capable of 1.5-A peak source and 2-A peak sink current.
LO2	20	16			
OVP/OTP	2	26	I	Overvoltage Protection	An external voltage divider from the input power supply sets the shutdown level during an over-voltage condition. Alternatively, an external NTC thermistor voltage divider can be used to set the shutdown temperature. The threshold is 1.25 V. Hysteresis is set by an internal current that sources 20 µA of current into the external resistor divider.
PGND	22	18	O	Power Ground	Connect directly to Analog Ground
RAMP	3	27	I	Input to PWM Comparator	Modulation ramp for the PWM comparator. This ramp can be a signal representative of the primary current (current mode) or proportional to the input voltage (feed-forward voltage mode). This pin is reset to GND at the end of every cycle.
RD1	10	6	I	Synchronous Rectifier Leading Edge Delay	The resistance connected between RD1 and AGND sets the delay from the falling edge of SR1 or SR2 and the rising edge of HO2/LO1 or HO1/LO2, respectively.
RD2	11	7	I	Synchronous Rectifier Trailing Edge Delay	The resistance connected between RD2 and AGND sets the delay from the falling edge of HO1/LO2 or HO2/LO1 and the rising edge of SR2 or SR1, respectively.
REF	7	3	O	Output of a 5V reference	Maximum output current is 15 mA. Locally decouple with a 0.1-µF capacitor.
RES	12	8	I	Restart Timer	Whenever the CS pin exceeds the 750-mV cycle-cycle current limit threshold, 30-µA current is sourced into the RES capacitor for the remainder of the PWM cycle. If the RES capacitor voltage reaches 1.0 V, the SS capacitor is discharged to disable the HO1, HO2, LO1, LO2 and SR1, SR2 outputs. The SS pin is held low until the voltage on the RES capacitor has been ramped between 2-V and 4-V eight times by 10-µA charge and 5-µA discharge currents. After the delay sequence, the SS capacitor is released to initiate a normal start-up sequence.
RT/SYNC	8	4	O	Oscillator Frequency Control and Frequency Synchronization	The resistance connected between RT and AGND sets the oscillator frequency. Synchronization is achieved by AC coupling a pulse to the RT/SYNC pin that raises the voltage at least 1.5 V above the 2-V nominal bias level.

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Table 4-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION	APPLICATION INFORMATION
NAME	HTSSOP	WQFN			
SLOPE	5	1	O	Slope Compensation Current	A ramping current source from 0 to 100 µA is provided for slope compensation in current mode control. This pin can be connected through an appropriate resistor to the CS pin to provide slope compensation. If slope compensation is not required, SLOPE must be tied to ground.
SR1	24	20	O	Synchronous Rectifier Driver	Control output for synchronous rectifier gate. Capable of peak sourcing 100 mA and sinking 400 mA.
SR2	19	15	O	Synchronous Rectifier Driver	Control output for synchronous rectifier gate. Capable of peak sourcing 100 mA and sinking 400 mA.
SS	13	9	I	Soft-Start Input	An internal 20-µA current source charges the SS pin during start-up. The input to the PWM comparator gradually rises as the SS capacitor charges to steadily increase the PWM duty cycle. Pulling the SS pin to a voltage below 20 0mV stops PWM pulses at HO1, 2 and LO1, 2 and turns off the synchronous rectifier FETs to a low state.
SSOFF	15	11	I	Soft-Stop Disable	When SS OFF pin is connected to the AGND, the LM5045 soft-stops in the event of a VIN UVLO and Hiccup mode current limit condition. If the SSOFF pin is connected to REF pin, the controller hard-stops on any fault condition. Refer to Table 6-1 for more details.
SSSR	14	10	I	Secondary Side Soft-Start	An external capacitor and an internal 20-µA current source set the soft-start ramp for the synchronous rectifiers. The SSSR capacitor charge-up is enabled after the first output pulse and SS > 2 V and Icomp < 800 µA
UVLO	1	25	I	Line Undervoltage Lockout	An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4-V threshold the VCC and REF regulators are enabled. At the 1.25-V threshold, the SS pin is released and the controller enters the active mode. Hysteresis is set by an internal current sink that pulls 20 µA from the external resistor divider.
VCC	21	17	I	Output of Start-Up Regulator	The output voltage of the start-up regulator is initially regulated to 9.5 V. Once the secondary side soft-start (SSSR pin) reaches 1 V, the VCC output is reduced to 7.7 V. If an auxiliary winding raises the voltage on this pin above the regulation set-point, the internal start-up regulator will shutdown, thus reducing the IC power dissipation.
VIN	28	24	I	Input Power Source	Input to the Start-up Regulator. Operating input range is 14 V to 100 V. For power sources outside of this range, the LM5045 can be biased directly at VCC by an external regulator.

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5 Specifications

5.1 Absolute Maximum Ratings

	MIN[1]	MAX	UNIT
VIN to GND	–0.3	105	V
HS to GND[2]	–5	105	V
BST1/BST2 to GND	–0.3	116	V
BST1/BST2 to HS1/HS2	–0.3	16	V
HO1/HO2 to HS1/HS2[3]	–0.3	BST1/BST2 + 0.3	V
LO1/LO2/SR1/SR2[3]	–0.3	V_{CC} + 0.3	V
V_{CC} to GND	–0.3	16	V
REF,SSOFF,RT,OVP,UVLO to GND	–0.3	7	V
RAMP	–0.3	7	V
COMP		–0.3	V
COMP Input Current		10	mA
All other inputs to GND[3]	–0.3	REF + 0.3	V
Junction Temperature		150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Section 5.5*.
(2) The negative HS voltage must never be more negative than VCC–16 V. For example, if VCC = 12 V, the negative transients at HS must not exceed –4 V.
(3) These pins are output pins and as such should not be connected to an external voltage source. The voltage range listed is the limits the internal circuitry is designed to reliably tolerate in the application circuit.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN Voltage	14		100	V
External Voltage Applied to VCC	10		14	V
Junction Temperature	–40		125	°C
SLOPE	–0.3		2	V

5.4 Thermal Information

THERMAL METRIC[1]		LM5045		UNIT
		PWP	RSG	
		28 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4	4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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5.5 Electrical Characteristics

Limits in standard typeface are for T_J = 25°C only; MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, RT = 25 kΩ, RD1 = RD2 = 20 kΩ. No load on HO1, HO2, LO1, LO2, SR1, SR2, COMP = 0 V, UVLO = 2.5 V, OVP = 0 V, SSOFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
START-UP REGULATOR (V_{CC} PIN)						
V_{CC1}	V_{CC} voltage	I_{CC}= 10 mA (SSSR < 1 V)	9.3	9.6	9.9	V
V_{CC2}	V_{CC} voltage	I_{CC}= 10 mA (SSSR > 1 V)	7.5	7.8	8.1	V
$I_{CC(Lim)}$	V_{CC} current limit	V_{CC}= 6 V	60	80		mA
$I_{CC(ext)}$	V_{CC} supply current	Supply current into VCC from an externally applied source. V_{CC} = 10 V		4.6		mA
	V_{CC} load regulation	I_{CC} from 0 to 50 mA		35		mV
$V_{CC(UV)}$	V_{CC} undervoltage threshold	Positive going VCC	V_{CC1}–0.2	V_{CC1}–0.1		V
		Negative going VCC	5.9	6.3	6.7	V
I_{IN}	V_{IN} operating current			4		mA
	V_{IN} shutdown current	V_{IN} = 20 V, V_{UVLO} = 0 V		300	520	µA
		V_{IN} = 100 V, V_{UVLO} = 0 V		350	550	µA
	V_{IN} start-up regulator leakage	V_{CC}=10 V		160		µA
VOLTAGE REFERENCE REGULATOR (REF PIN)						
V_{REF}	REF voltage	I_{REF} = 0 mA	4.85	5	5.15	V
	REF voltage regulation	I_{REF} = 0 to 10 mA		25	50	mV
$I_{REF(Lim)}$	REF current limit	V_{REF} = 4.5 V	15	20		mA
V_{REFUV}	V_{REF} undervoltage threshold	Positive going V_{REF}	4.3	4.5	4.7	V
	Hysteresis			0.25		V
UNDERVOLTAGE LOCK OUT AND SHUTDOWN (UVLO PIN)						
V_{UVLO}	Under-voltage threshold		1.18	1.25	1.32	V
I_{UVLO}	Hysteresis current	UVLO pin sinking current when V_{UVLO} < 1.25 V	16	20	24	µA
	Undervoltage standby enable threshold	UVLO voltage rising	0.32	0.4	0.48	V
	Hysteresis			0.05		V
V_{OVP}	OVP shutdown threshold	OVP rising	1.18	1.25	1.32	V
	OVP hysteresis current	OVP sources current when OVP > 1.25 V	16	20	24	µA
SOFT-START (SS PIN)						
I_{SS}	SS charge current	V_{SS} = 0 V	16	20	24	µA
	SS threshold for SSSR charge current enable	I_{COMP} < 800 µA	1.93	2	2.2	V
	SS output low voltage	Sinking 100 µA		40		mV
	SS threshold to disable switching			200		mV
I_{SSSR}	SSSR charge current	V_{SS} > 2 V, I_{COMP} < 800 µA	16	20	24	µA
$I_{SSSR-DIS1}$	SSSR discharge current 1	V_{UVLO} < 1.25 V	54	65	75	µA
$I_{SSSR-DIS2}$	SSSR discharge current 2	V_{RES} > 1 V	109	125	147	µA
	SSSR output low voltage	Sinking 100 µA		50		mV
	SSSR threshold to enable SR1/SR2			1.2		V
CURRENT SENSE INPUT (CS PIN)						
V_{CS}	Current limit threshold		0.71	0.75	0.785	V

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5.5 Electrical Characteristics (continued)

Limits in standard typeface are for T_J = 25°C only; MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, RT = 25 kΩ, RD1 = RD2 = 20 kΩ. No load on HO1, HO2, LO1, LO2, SR1, SR2, COMP = 0 V, UVLO = 2.5 V, OVP = 0 V, SSOFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CS delay to output			65		ns
	CS leading edge blanking			50		ns
R_{CS}	CS sink impedance (clocked)	Internal FET sink impedance		18	45	Ω
SOFT-STOP DISABLE (SS OFF PIN)						
$V_{IH(min)}$	SSOFF Input-threshold			2.8		V
	SSOFF pulldown resistance			200		kΩ
CURRENT LIMIT RESTART (RES Pin)						
R_{RES}	RES pulldown resistance	Termination of hiccup timer		37		Ω
V_{RES}	RES hiccup threshold			1		V
	RES upper counter threshold			4		V
	RES lower counter threshold			2		V
$I_{RES-SRC1}$	Charge current source 1	V_{RES} < 1 V, V_{CS}> 750 mV		30		µA
$I_{RES-SRC2}$	Charge current source 2	1 V < V_{RES} < 4 V		10		µA
$I_{RES-DIS2}$	Discharge current source 1	V_{CS} < 750 mV		5		µA
$I_{RES-DIS2}$	Discharge current source 2	2 V < V_{RES} < 4 V		5		µA
	Ratio of time in hiccup mode to time in current limit	V_{RES} > 1 V, Hiccup counter		147		
VOLTAGE FEED-FORWARD (RAMP PIN)						
	RAMP sink impedance (Clocked)			5.5	20	Ω
OSCILLATOR (RT PIN)						
F_{SW1}	Frequency (LO1, half oscillator frequency)	R_T = 25 kΩ	185	200	215	kHz
F_{SW2}	Frequency (LO1, half oscillator frequency)	R_T = 10 kΩ	420	480	540	kHz
	DC level			2		V
	RT sync threshold		2.8	3	3.3	V

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5.5 Electrical Characteristics (continued)

Limits in standard typeface are for T_J = 25°C only; MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, RT = 25 kΩ, RD1 = RD2 = 20 kΩ. No load on HO1, HO2, LO1, LO2, SR1, SR2, COMP = 0 V, UVLO = 2.5 V, OVP = 0 V, SSOFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONOUS RECTIFIER TIMING CONTROL (RD1 and RD2 PINS)						
T1	SR trailing edge delay SR turnoff to HO&LO both on	R_{D1} = 20 kΩ	45	65	90	ns
		R_{D1} = 100 kΩ	232	300	388	ns
T2	SR leading edge HO or LO turnoff to SR turnon	R_{D2} = 20 kΩ	43	65	90	ns
		R_{D2} = 100 kΩ	227	300	384	ns
COMP PIN						
V_{PWM-OS}	COMP current to RAMP offset	V_{RAMP} = 0 V	680	800	940	µA
V_{SS-OS}	SS to RAMP offset	V_{RAMP} = 0 V	0.78	1.0	1.22	V
	COMP current to RAMP gain	$\Delta RAMP/\Delta I_{COMP}$		2400		Ω
	SS to RAMP gain	ΔSS/ΔRAMP		0.5		
	COMP current for SSSR charge current enable	V_{SS} > 2 V	690	800	915	µA
	COMP to output delay			120		ns
	Minimum duty cycle	I_{COMP} = 1 mA			0%	
SLOPE COMPENSATION (SLOPE PIN)						
I_{SLOPE}	Slope compensation current ramp	Peak of RAMP current		100		µA
BOOST (BST PIN)						
$V_{Bst\ uv}$	BST under-voltage threshold	$V_{BST} – V_{HS}$ rising	3.8	4.7	5.6	V
	Hysteresis			0.5		V
HO1, HO2, LO1, LO2 GATE DRIVERS						
V_{OL}	Low-state output voltage	$I_{HO/LO}$ = 100 mA		0.16	0.32	V
V_{OH}	High-state output voltage	$I_{HO/LO}$ = 100 mA $V_{OHL} = V_{CC} – V_{LO}$ $V_{OHH} = V_{BST} – V_{HO}$		0.27	0.495	V
	Rise Time	C-load = 1000 pF		16		ns
	Fall Time	C-load = 1000 pF		11		ns
I_{OHL}	Peak Source Current	$V_{HO/LO}$ = 0 V		1.5		A
I_{OLL}	Peak Sink Current	$V_{HO/LO} = V_{CC}$		2		A
SR1, SR2 GATE DRIVERS						
V_{OL}	Low-state output voltage	$I_{SR1/SR2}$ = 10 mA		0.05	0.1	V
V_{OH}	High-state output voltage	$I_{SR1/SR2}$ = 10 mA, $V_{OH} = V_{REF} – V_{SR}$		0.17	0.28	V
	Rise Time	C-load = 1000 pF		60		ns
	Fall Time	C-load = 1000 pF		20		ns
I_{OHL}	Peak Source Current	V_{SR} = 0 V		0.1		A
I_{OLL}	Peak Sink Current	$V_{SR} = V_{REF}$		0.4		A
THERMAL SHUTDOWN						
TSD	Thermal Shutdown Temp			160		°C
	Thermal Shutdown Hysteresis			25		°C

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5.6 Typical Characteristics

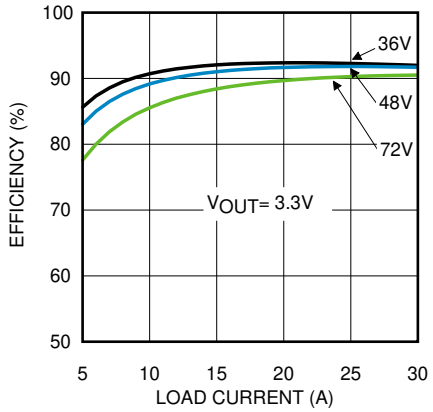

Figure 5-1. Application Board Efficiency

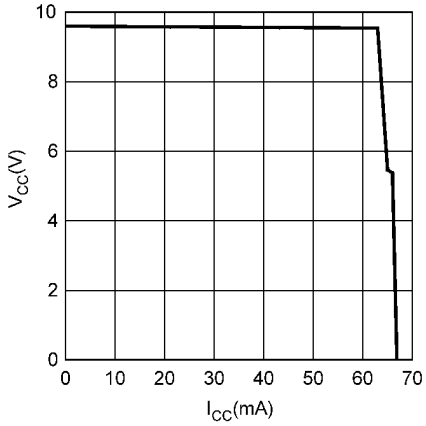

Figure 5-2. V_{CC} vs I_{CC}

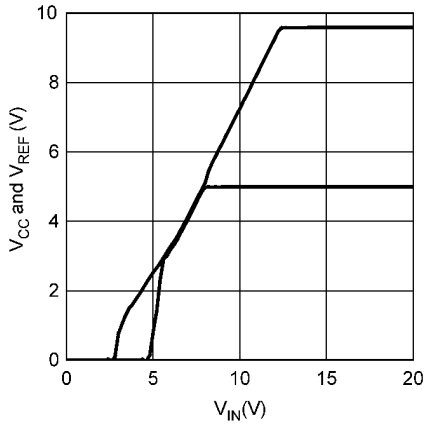

Figure 5-3. V_{CC} and V_{REF} vs V_{IN}

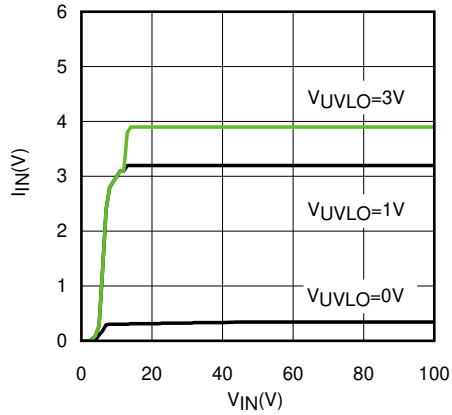

Figure 5-4. I_{IN} vs V_{IN}

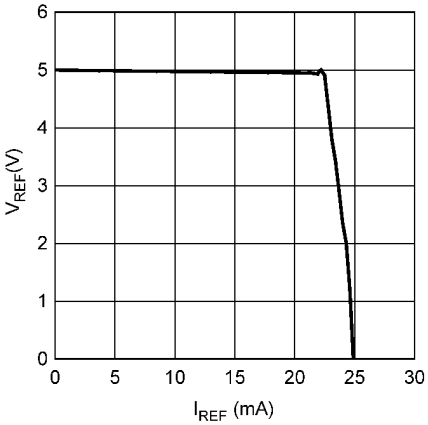

Figure 5-5. V_{REF} vs I_{REF}

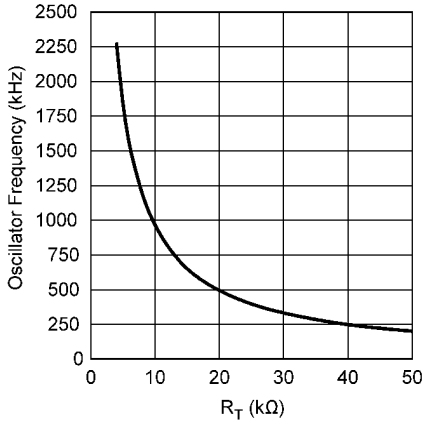

Figure 5-6. Oscillator Frequency vs R_T

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5.6 Typical Characteristics (continued)

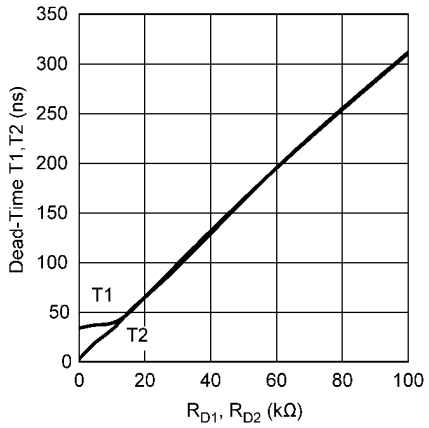

Figure 5-7. Dead-Time T1, T2 vs R_{D1}, R_{D2}

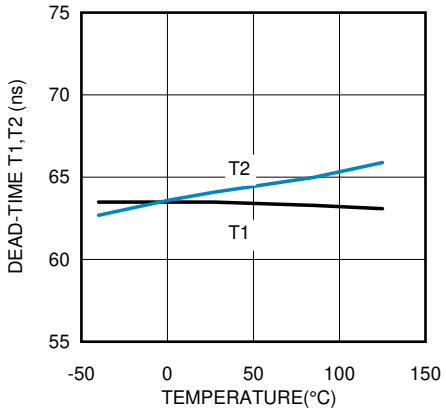

Figure 5-8. Dead-Time T1, T2 vs. Temperature

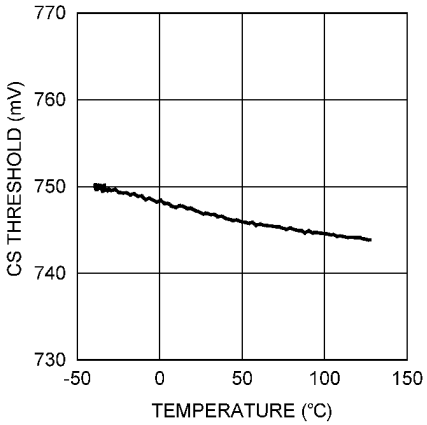

Figure 5-9. CS Threshold vs Temperature

6 Detailed Description

6.1 Overview

The LM5045 PWM controller contains all of the features necessary to implement a full-bridge topology power converter using either current mode or voltage mode control. This device is intended to operate on the primary side of an isolated DC-DC converter with input voltage up to 100 V. This highly integrated controller-driver provides dual 2-A high-side and low-side gate drivers for the four external bridge MOSFETs plus control signals for secondary side synchronous rectifiers. External resistors program the leading and trailing edge dead-time between the main and synchronous rectifier control signals. Intelligent start-up of synchronous rectifier allows turnon of the power converter into the prebias loads. Cycle-by-cycle current limit protects the power components from load transients while hiccup mode protection limits average power dissipation during extended overload conditions. Additional features include programmable soft-start, soft-start of the synchronous rectifiers, and a 2-MHz capable oscillator with synchronization capability and thermal shutdown.

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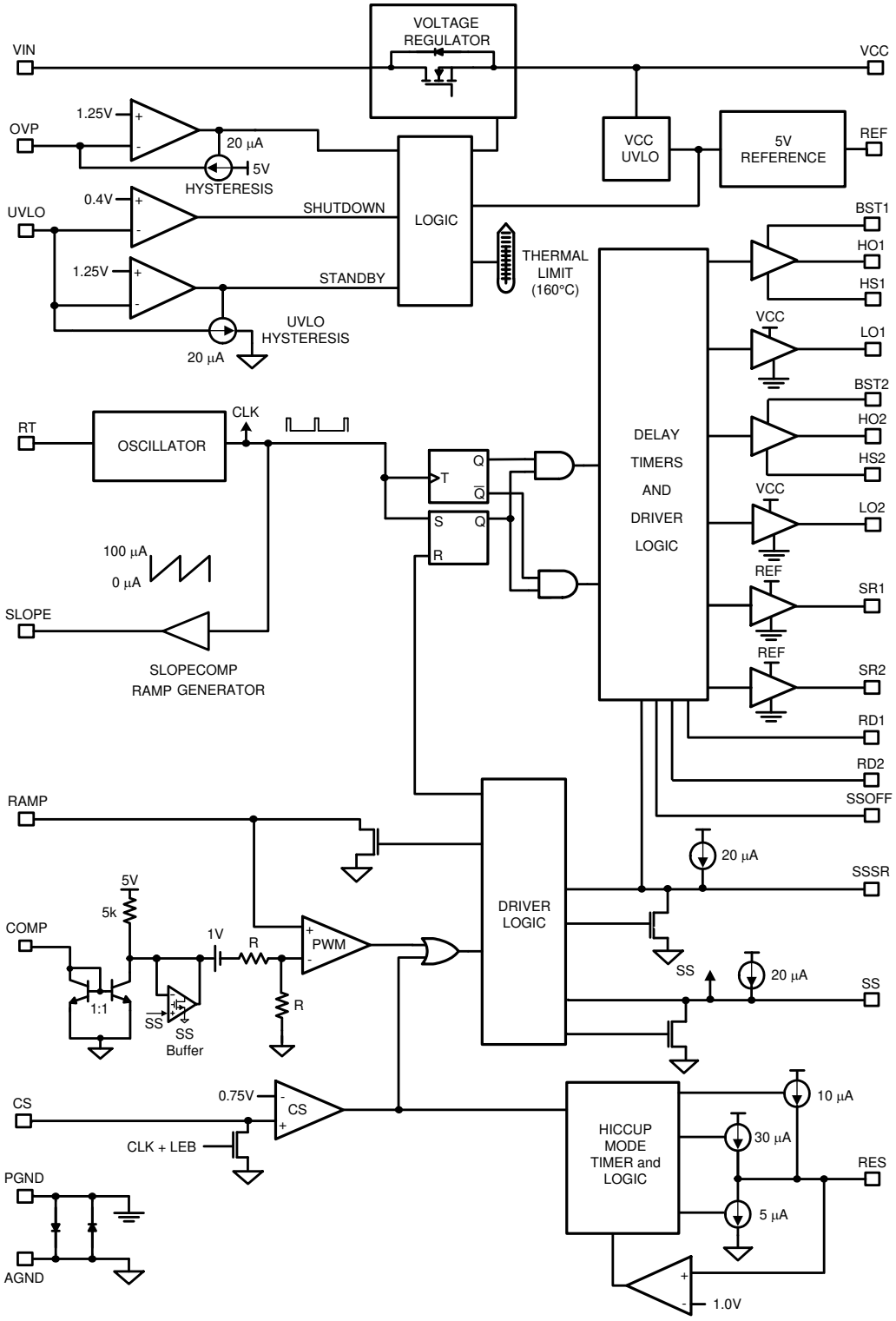
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 High-Voltage Start-Up Regulator

The LM5045 contains an internal high-voltage start-up regulator that allows the input pin (VIN) to be connected directly to the supply voltage over a wide range from 14 V to 100 V. The input can withstand transients up to 105 V. When the UVLO pin potential is greater than 0.4 V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the gate drivers (HO1/HO2 and LO1/LO2). When the voltage on the VCC pin exceeds its undervoltage (UV) threshold, the internal voltage reference (REF) reaches its regulation set point of 5 V and the UVLO voltage is greater than 1.25 V, the soft-start capacitor is released and normal operation begins. The regulator output at VCC is internally current limited. The value of the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.47 µF to 10 µF.

The internal power dissipation of the LM5045 can be reduced by powering VCC from an external supply. The output voltage of the VCC regulator is initially regulated to 9.5 V. After the synchronous rectifiers are engaged (which is approximately when the output voltage in within regulation), the VCC voltage is reduced to 7.7 V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the power dissipation of the controller. The VCC UV circuit will still function in this mode, requiring that VCC never falls below its UV threshold during the start-up sequence. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. Therefore, the auxiliary VCC voltage should never exceed the VIN voltage.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. This implementation is shown in the *Section 7* section. The external bias must be greater than 10 V and less than the VCC maximum voltage rating of 14 V.

6.3.2 Line Undervoltage Detector

The LM5045 contains a dual level undervoltage lockout (UVLO) circuit. When the UVLO pin voltage is below 0.4 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4 V but less than 1.25 V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed their respective under-voltage thresholds and the UVLO pin voltage is greater than 1.25 V, the soft-start capacitor is released and the normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25 V when VIN enters the desired operating range. UVLO hysteresis is accomplished with an internal 20 µA current sink that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current sink is deactivated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25 V threshold, the current sink is enabled causing the voltage at the UVLO pin to quickly fall. The hysteresis of the 0.4 V shutdown comparator is internally fixed at 50 mV.

The UVLO pin can also be used to implement various remote enable / disable functions. Turning off the converter by forcing the UVLO pin to standby condition (0.4 V < UVLO < 1.25 V) provides a controlled soft-stop. Refer to the *Section 6.3.16* section for more details.

6.3.3 Overvoltage Protection

An external voltage divider can be used to set either an overvoltage or an overtemperature protection. During an OVP condition, the SS and SSSR capacitors are discharged and all the outputs are disabled. The divider must be designed such that the voltage at the OVP pin is greater than 1.25 V when overvoltage/temperature condition exists. Hysteresis is accomplished with an internal 20 µA current source. When the OVP pin voltage exceeds 1.25 V, the 20 µA current source is activated to quickly raise the voltage at the OVP pin. When the OVP pin voltage falls below the 1.25 V threshold, the current source is deactivated causing the voltage at the OVP to quickly fall. Refer to the *Section 7* section for more details.

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6.3.4 Reference

The REF pin is the output of a 5-V linear regulator that can be used to bias an optocoupler transistor and external housekeeping circuits. The regulator output is internally current limited to 15 mA. The REF pin must be locally decoupled with a ceramic capacitor, the recommended range of values are from 0.1 µF to 10 µF

6.3.5 Oscillator, Sync Input

The LM5045 oscillator frequency is set by a resistor connected between the RT pin and AGND. The RT resistor should be located very close to the device. To set a desired oscillator frequency (F_{OSC}), the necessary value of RT resistor can be calculated from the following equation:

$$R_T = \frac{1}{F_{OSC} \times 1 \times 10^{-10}} \tag{1}$$

For example, if the desired oscillator frequency is 400 kHz, that is, each phase (LO1 or LO2) at 200 kHz, the value of R_T will be 25 kΩ. If the LM5045 is to be synchronized to an external clock, that signal must be coupled into the RT pin through a 100 pF capacitor. The RT pin voltage is nominally regulated at 2.0 V and the external pulse amplitude should lift the pin to between 3.5 V and 5.0 V on the low-to-high transition. The synchronization pulse width should be between 15 and 200 ns. The RT resistor is always required, whether the oscillator is free running or externally synchronized and the SYNC frequency must be equal to, or greater than the frequency set by the RT resistor. When syncing to an external clock, it is recommended to add slope compensation by connecting an appropriate resistor from the VCC pin to the CS pin. Also disable the SLOPE pin by grounding it.

6.3.6 Cycle-by-Cycle Current Limit

The CS pin is to be driven by a signal representative of the primary current of the transformer. If the voltage on the CS pin exceeds 0.75 V, the current sense comparator immediately terminates the PWM cycle. A small RC filter connected to the CS pin and located near the controller is recommended to suppress noise. An internal 18-Ω MOSFET discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 40 ns after the start of a new PWM cycle to blank leading edge spikes. The current sense comparator is very fast and may respond to short duration noise pulses. Layout is critical for the current sense filter and the sense resistor. The capacitor associated with CS filter must be placed very close to the device and connected directly to the CS and AGND pins. If a current sense transformer is used, both the leads of the transformer secondary should be routed to the filter network, which should be located close to the IC. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together near the AGND pin, and a single connection should be made to the power ground (sense resistor ground point).

6.3.7 Hiccup Mode

The LM5045 provides a current limit restart timer to disable the controller outputs and force a delayed restart (such as Hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmed by the external capacitor at the RES pin. During each PWM cycle, the LM5045 either sources or sinks current from the RES capacitor. If current limit is detected, the 5 µA current sink is disabled and a 30µA current source is enabled. If the RES voltage reaches the 1.0 V threshold, the following restart sequence occurs, as shown in Figure 6-1:

- The SS and SSSR capacitors are fully discharged
- The 30 µA current source is turned-off and the 10 µA current source is turned-on.
- Once the voltage at the RES pin reaches 4.0 V the 10 µA current source is turned-off and a 5µA current sink is turned-on, ramping the voltage on the RES capacitor down to 2.0 V.
- Once RES capacitor reaches 2.0 V, threshold, the 10 µA current source is turned-on again. The RES capacitor voltage is ramped between 4.0 V and 2.0 V eight times.
- When the counter reaches eight, the RES pin voltage is pulled low and the soft-start capacitor is released to begin a soft-start sequence. The SS capacitor voltage slowly increases. When the SS voltage reaches 1.0 V, the PWM comparator will produce the first narrow pulse.

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- If the overload condition persists after restart, cycle-by-cycle current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence.
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 5 µA current sink and the normal operation resumes.

The hiccup mode function can be completely disabled by connecting the RES pin to the AGND pin. In this configuration the cycle-by-cycle protection will limit the maximum output current indefinitely, no hiccup restart sequences will occur.

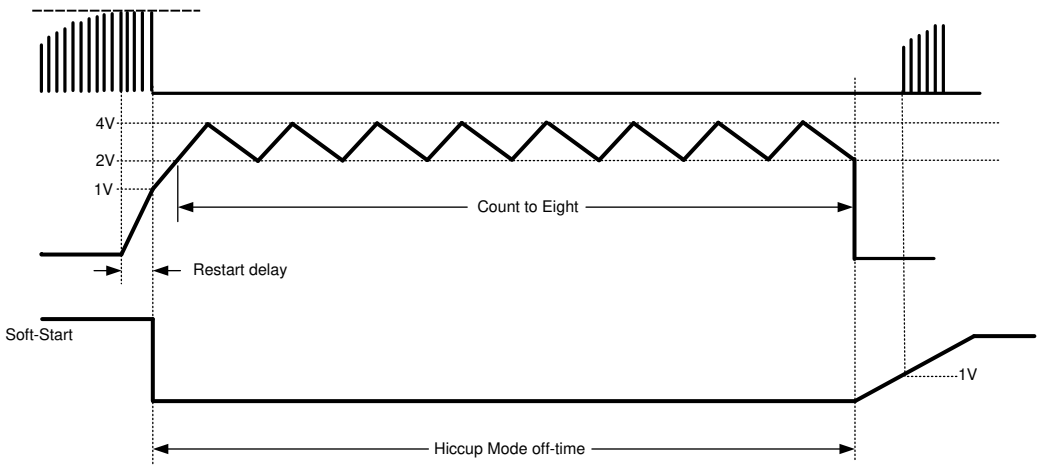

Figure 6-1. Hiccup Mode Delay and Soft-Start Timing Diagram

6.3.8 PWM Comparator

The LM5045 pulse width modulator (PWM) comparator is a three input device, it compares the signal at the RAMP pin to the loop error signal or the soft-start, whichever is lower, to control the duty cycle. This comparator is optimized for speed to achieve minimum controllable duty cycles. The loop error signal is received from the external feedback and isolation circuit in the form of a control current into the COMP pin. The COMP pin current is internally mirrored by a matching pair of NPN transistors which sink current through a 5-kΩ resistor connected to the 5-V reference. The resulting control voltage passes through a 1-V offset, followed by a 2:1 resistor divider before being applied to the PWM comparator.

An optocoupler detector can be connected between the REF pin and the COMP pin. Because the COMP pin is controlled by a current input, the potential difference across the optocoupler detector is nearly constant. The bandwidth limiting phase delay which is normally introduced by the significant capacitance of the optocoupler is thereby greatly reduced. Higher loop bandwidths can be realized because the bandwidth limiting pole associated with the optocoupler is now at a much higher frequency. The PWM comparator polarity is configured such that with no current flowing into the COMP pin, the controller produces maximum duty cycle.

6.3.9 Ramp Pin

The voltage at the RAMP pin provides the modulation ramp for the PWM comparator. The PWM comparator compares the modulation ramp signal at the RAMP pin to the loop error signal to control the duty cycle. The modulation ramp signal can be implemented either as a ramp proportional to the input voltage, known as feed-forward voltage mode control, or as a ramp proportional to the primary current, known as current mode control. The RAMP pin is reset by an internal MOSFET with an $R_{DS(ON)}$ of 5.5 Ω at the conclusion of each PWM cycle. The ability to configure the RAMP pin for either voltage mode or current mode allows the controller to be implemented for the optimum control method depending upon the design constraints. Refer to the *Section 7* section for more details on configuring the RAMP pin for feed-forward voltage mode control and peak current mode control.

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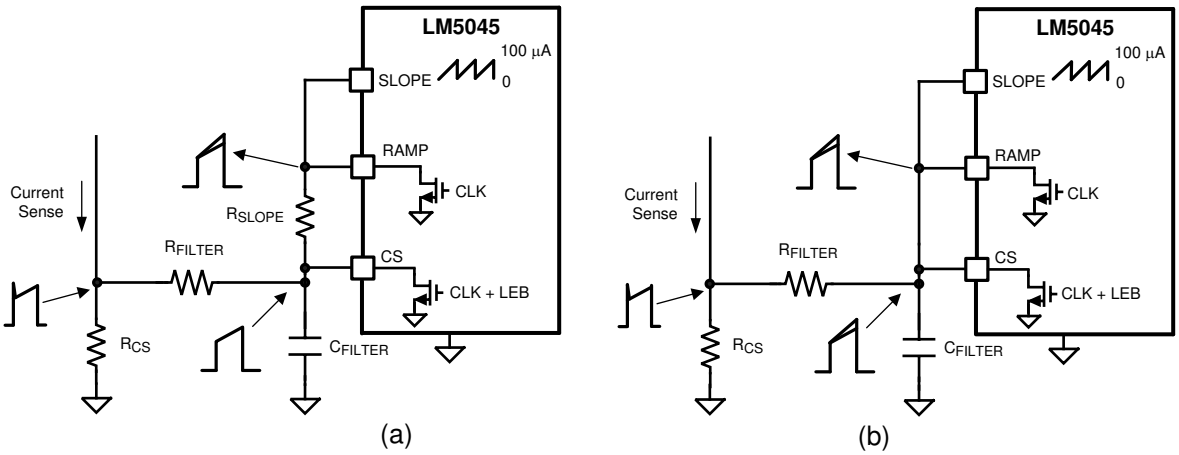
6.3.10 Slope Pin

For duty cycles greater than 50% (25% for each phase), peak current mode control is subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles. This can be eliminated by adding an artificial ramp, known as slope compensation, to the modulating signal at the RAMP pin. The SLOPE pin provides a current source ramping from 0 to 100µA, at the frequency set by the RT resistor, for slope compensation. The ramping current source at the SLOPE pin can be used in several different ways to add slope compensation to the RAMP signal:

- As shown in Figure 6-2(a), the SLOPE and RAMP pins can be connected together through an appropriate resistor to the CS pin. This configuration will inject current sense signal plus slope compensation to the RAMP pin but CS pin will not see any slope compensation. Therefore, in this scheme slope compensation will not affect the current limit.
- In a second configuration, as shown in Figure 6-2(b), the SLOPE, RAMP and CS pins can be tied together. In this configuration the ramping current source from the SLOPE pin will flow through the filter resistor and filter capacitor, therefore both the CS pin and the RAMP pin will see the current sense signal plus the slope compensation ramp. In this scheme, the current limit is compensated by the slope compensation and the current limit onset point will vary.

If the slope compensation is not required for example, in feed-forward voltage mode control, the SLOPE pin must be connected to the AGND pin. When the RT pin is synched to an external clock, it is recommended to disable the SLOPE pin and add slope compensation externally by connecting an appropriate resistor from the VCC pin to the CS pin. Refer to the *Section 7* section for more details.



A. Slope Compensation Configured for PWM Only (No Current Limit Slope)
B. Slope Compensation Configured for PWM and Current Limit

Figure 6-2. Slope Compensation Configuration

6.3.11 Soft-Start

The soft-start circuit allows the power converter to gradually reach a steady state operating point, thereby reducing the start-up stresses and current surges. When bias is supplied to the LM5045, the SS capacitor is discharged by an internal MOSFET. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and is charged with a 20-µA current source. Once the SS pin voltage crosses the 1-V offset, SS controls the duty cycle. The PWM comparator is a three input device; it compares the RAMP signal against the lower of the signals between the soft-start and the loop error signal. In a typical isolated application, as the secondary bias is established, the error amplifier on the secondary side soft-starts and establishes closed-loop control, steering the control away from the SS pin.

One method to shutdown the regulator is to ground the SS pin. This forces the internal PWM control signal to ground, reducing the output duty cycle quickly to zero. Releasing the SS pin begins a soft-start cycle and normal operation resumes. A second shutdown method is presented in the *Section 7.2.2.3* section.

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6.3.12 Gate Driver Outputs

The LM5045 provides four gate drivers: two floating high-side gate drivers HO1 and HO2 and two ground referenced low-side gate drivers LO1 and LO2. Each internal driver is capable of source 1.5-A peak and sinking 2-A peak. Initially, the diagonal HO1 and LO2 are turned-on together, followed by an off-time when all the four gate driver outputs are off. In the subsequent phase the diagonal HO2 and LO1 are turned on together followed by an off-time. The low-side gate drivers are powered directly by the VCC regulator. The HO1 and HO2 gate drivers are powered from a bootstrap capacitor connected between BST1/BST2 and HS1/HS2, respectively. An external diode connected between VCC (anode pin) and BST (cathode pin) provides the high-side gate driver power by charging the bootstrap capacitor from VCC when the corresponding switch node (HS1/HS2 pin) is low. When the high side MOSFET is turned on, BST1 rises to a peak voltage equal to VCC + V_{HS1} where V_{HS1} is the switch node voltage.

The BST and VCC capacitors should be placed close to the pins of the LM5045 to minimize voltage transients due to parasitic inductances because the peak current sourced to the MOSFET gates can exceed 1.5 A. The recommended value of the BST capacitor is 0.1 µF or greater. A low ESR / ESL capacitor, such as a surface mount ceramic, should be used to prevent voltage droop during the HO transitions.

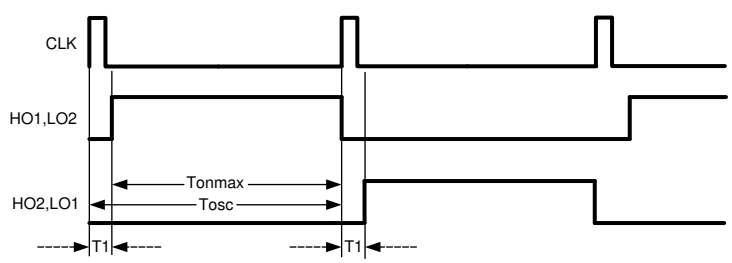
If the COMP pin is open circuit, the outputs will operate at maximum duty cycle. The maximum duty cycle for each phase is limited by the dead-time set by the RD1 resistor. If the RD1 resistor is set to zero then the maximum duty cycle is slightly less than 50% due to the internally fixed dead-time. The internally fixed dead-time is 30ns which does not vary with the operating frequency. The maximum duty cycle for each output can be calculated from the following equation:

$$D_{MAX} = \frac{\left(\frac{1}{F_{OSC}}\right) - (T1)}{\left(\frac{2}{F_{OSC}}\right)} \tag{2}$$

where

- T1 is the time set by the RD1 resistor
- F_{OSC} is the frequency of the oscillator

For example, if the oscillator frequency is set at 400 kHz and the T1 time set by the RD1 resistor is 60 ns, the resulting D_{MAX} will be equal to 0.488.



$$T_{OSC} = \frac{1}{F_{OSC}}$$

$$T1 \ \alpha \ RD1$$

Figure 6-3. Timing Diagram Illustrating the Maximum Duty Cycle and Dead-Time Set by RD1

6.3.13 Synchronous Rectifier Control Outputs (SR1 and SR2)

Synchronous rectification (SR) of the transformer secondary provides higher efficiency, especially for low output voltage converters, compared to the diode rectification. The reduction of rectifier forward voltage drop (0.5 V to 1.5 V) to 10 mV to 200 mV VDS voltage for a MOSFET significantly reduces rectification losses. In a typical

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application, the transformer secondary winding is center tapped, with the output power inductor in series with the center tap. The SR MOSFETs provide the ground path for the energized secondary winding and the inductor current. From Figure 6-4 it can be seen that when the HO1/LO2 diagonal is turned ON, power transfer is enabled from the primary. During this period, the SR1 MOSFET is enabled and the SR2 MOSFET is turned-off. The secondary winding connected to the SR2 MOSFET drain is twice the voltage of the center tap at this time. At the conclusion of the HO1/LO2 pulse, the inductor current continues to flow through the SR2 MOSFET body diode. Because the body diode causes more loss than the SR MOSFET, efficiency can be improved by minimizing the T2 period while maintaining sufficient timing margin over all conditions (component tolerances, etc.) to prevent the shoot-through current. When HO2/LO1 enables power transfer from the primary, the SR2 MOSFET is enabled and the SR1 MOSFET is off.

During the freewheeling period, the inductor current is almost equally shared between both the SR1 and SR2 MOSFETs which effectively shorts the transformer secondary. The SR2 MOSFET is disabled before HO1/LO2 is turned-on. The SR2 MOSFET body diode continues to carry about the half inductor current until the primary power raises the SR2 MOSFET drain voltage and reverse biases the body diode. Ideally, dead-time T1 would be set to the minimum time that allows the SR MOSFET to turn off before the SR MOSFET body diode starts conducting.

The SR drivers are powered by the REF regulator and each SR output is capable of sourcing 0.1 A and sinking 0.4-A peak. The amplitude of the SR drivers is limited to 5 V. The 5-V SR signals enable the LM5045 to transfer SR control across the isolation barrier either through a solid-state isolator or a pulse transformer. The actual gate sourcing and sinking currents for the synchronous MOSFETs are provided by the secondary-side bias and gate drivers.

T1 and T2 can be programmed by connecting a resistor between RD1 and RD2 pins and AGND. It should be noted that while RD1 effects the maximum duty cycle, RD2 does not. The RD1 and RD2 resistors should be located very close to the device. The formula for RD1 and RD2 resistors are given below:

$$RD(1,2) = \frac{T(1,2)}{3\ pF};\ \text{For } 20k < (1,2) < 100k \tag{3}$$

If the desired dead-time for T1 is 60ns, then the RD1 will be 20 kΩ.

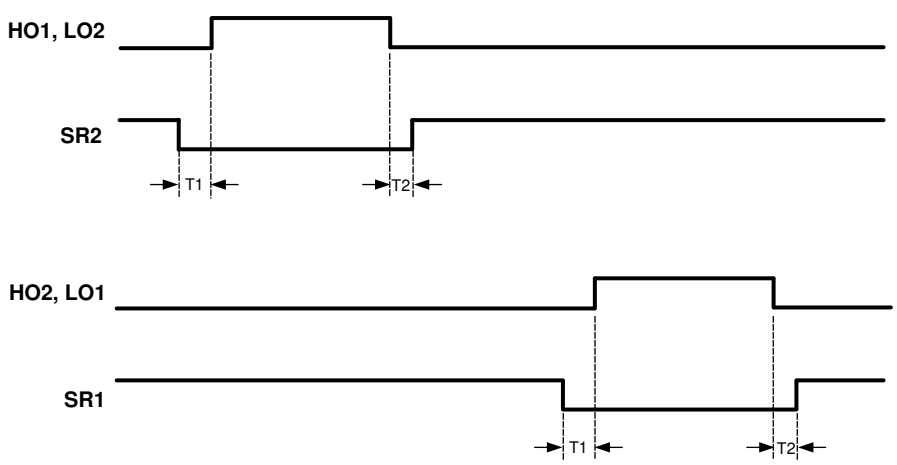
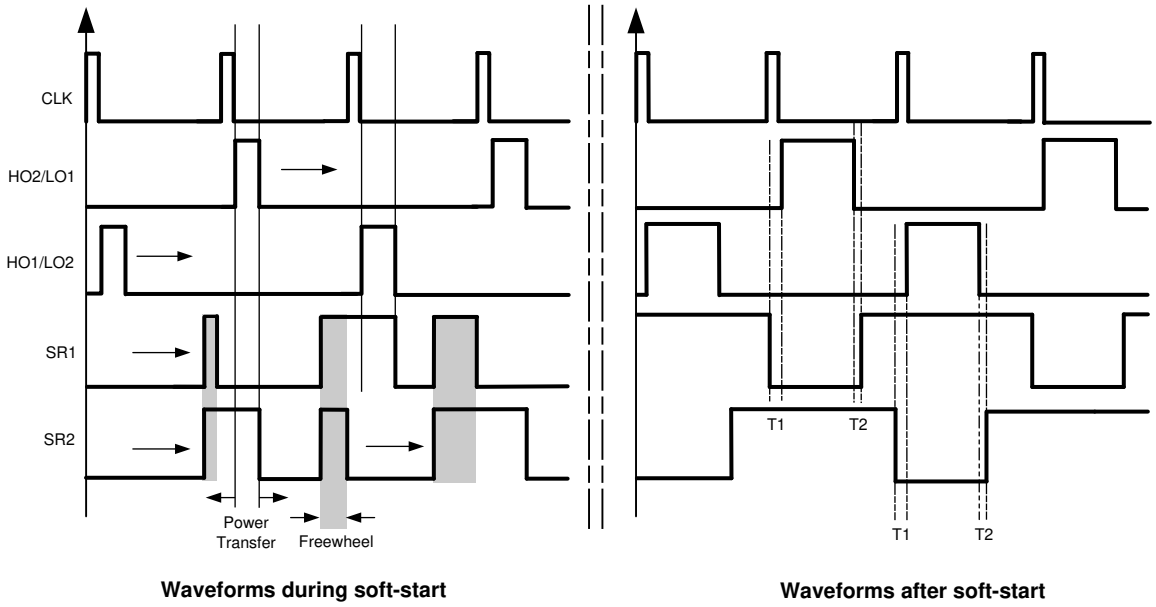


Figure 6-4. Synchronous Rectifier Timing Diagram

6.3.14 Soft-Start of the Synchronous Rectifiers

In addition to the basic soft-start already described, the LM5045 contains a second soft-start function that gradually turns on the synchronous rectifiers to their steady-state duty cycle. This function keeps the synchronous rectifiers off during the basic soft-start allowing a linear start-up of the output voltage even into pre-biased loads. Then the SR output duty cycle is gradually increased to prevent output voltage disturbances due to the difference in the voltage drop between the body diode and the channel resistance of the synchronous

MOSFETs. Initially, when bias is supplied to the LM5045, the SSSR capacitor is discharged by an internal MOSFET. When the SS capacitor reaches a 2-V threshold and once it is established that COMP is in control of the duty cycle such as I_{COMP} < 800 µA, the SSSR discharge is released and SSSR capacitor begins charging with a 20-µA current source. Once the SSSR cap crosses the internal 1-V threshold, the LM5045 begins the soft-start of the synchronous FETs. The SR soft-start follows a leading edge modulation technique such as the leading edge of the SR pulse is soft-started as opposed trailing edge modulation of the primary FETs. As shown in the Figure 6-5(a), SR1 and SR2 are turned-on simultaneously with a narrow pulse-width during the freewheeling cycle. At the end of the freewheel cycle, that is, at the rising edge of the internal CLK, the SR FET in-phase with the next power transfer cycle is kept on while the SR FET out of phase with it is turned-off. The in-phase SR FET is kept on throughout the power transfer cycle and at the end of it, both the primary FETs and the in-phase SR FETs are turned-off together. The synchronous rectifier outputs can be disabled by grounding the SSSR pin.



A. Waveforms during Soft-Start
B. Waveforms after Soft-Start

Figure 6-5. Waveforms

6.3.15 Prebias Startup

A common requirement for power converters is to have a monotonic output voltage start-up into a prebiased load such as a precharged output capacitor. In a prebiased load condition, if the synchronous rectifiers are engaged prematurely they will sink current from the precharged output capacitors resulting in an undesired output voltage dip. This condition is undesirable and could potentially damage the power converter. The LM5045 uses unique control circuitry to ensure intelligent turnon of the synchronous rectifiers such that the output has a monotonic start-up. Initially, the SSSR capacitor is held at ground to disable the synchronous MOSFETs allowing the body diode to conduct. The synchronous rectifier soft-start is initiated once it is established the duty cycle is controlled by the COMP instead of the soft-start capacitor, that is, I_{COMP} < 800 µA and the voltage at the SS pin > 2 V. The SSSR capacitor is then released and is charged by a 20-µA current source. Further, as shown in Figure 6-6, a 1-V offset on the SSSR pin is used to provide additional delay. This delay ensures the output voltage is in regulation avoiding any reverse current when the synchronous MOSFETs are engaged.

6.3.16 Soft-Stop

As shown in Figure 6-7, if the UVLO pin voltage falls below the 1.25-V standby threshold, but above the 0.4-V shutdown threshold, the SSSR capacitor is soft-stopped with a 60-µA current source (3 times the charging

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current). Once the SSSR pin reaches the 1.0-V threshold, both the SS and SSSR pins are immediately discharged to GND. Soft-stopping the power converter gradually winds down the energy in the output capacitors and results in a monotonic decay of the output voltage. During the hiccup mode, the same sequence is executed except that the SSSR is discharged with a 120-µA current source (6 times the charging current). In case of an OVP, VCC UV, thermal limit or a VREF UV condition, the power converter hard-stops, whereby all of the control outputs are driven to a low state immediately.

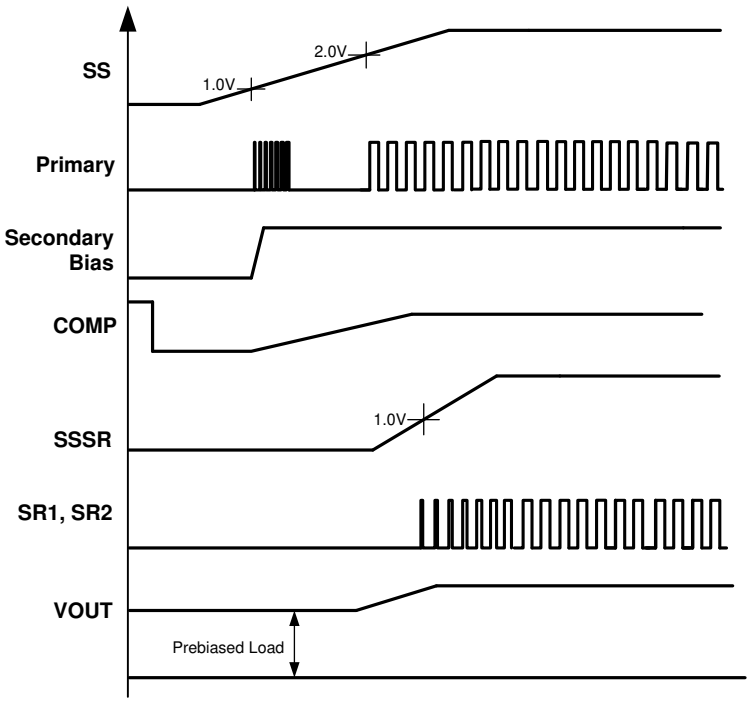

Figure 6-6. Prebias Voltage Start-up Waveforms

6.3.17 Soft-Stop Off

The Soft-Start Off (SSOFF) pin gives additional flexibility by allowing the power converter to be configured for hard-stop during line UVLO and hiccup mode condition. If the SS OFF pin is pulled up to the 5-V REF pin, the power converter hard-stops in any fault condition. Hard-stop drives each control output to a low state immediately. Refer to Table 6-1 for more details.

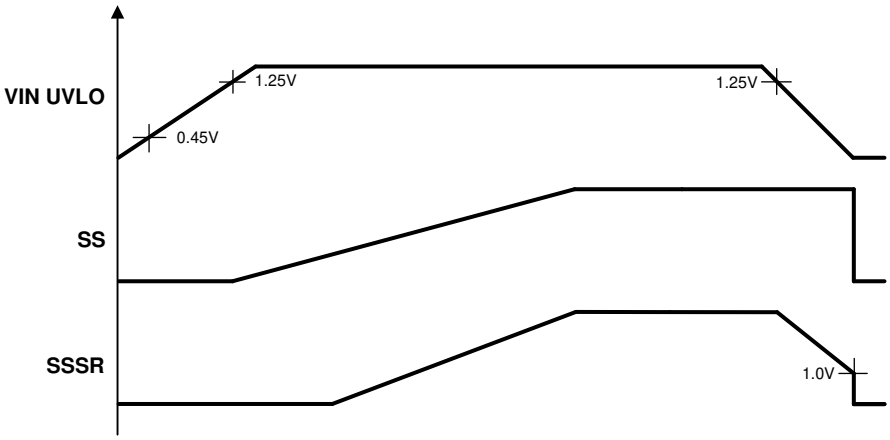

Figure 6-7. Stop-Stop Waveforms During a UVLO Event

Table 6-1. Soft-Stop in Fault Conditions

FAULT CONDITION (1)	SSSR
UVLO (UVLO<1.25V)	Soft-Stop 3x the charging rate
OVP (OVP>1.25V)	Hard-Stop
Hiccup (CS>0.75 and RES>1V)	Soft-Stop 6x the charging rate
VCC/VREF UV	Hard-Stop
Internal Thermal Limit	Hard-Stop

(1) Note: All the above conditions are valid with SSOFF pin tied to GND. If SSOFF=5V, the LM5045 hard-stops in all the conditions. The SS pin remains high in all the conditions until the SSSR pin reaches 1V.

6.3.18 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 160°C, the controller is forced into a shutdown state with the output drivers, the bias regulators (VCC and REF) disabled. This helps to prevent catastrophic failures from accidental device overheating. During thermal shutdown, the SS and SSSR capacitors are fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (140°C).

6.4 Device Functional Modes

6.4.1 Control Method Selection

The LM5045 is a versatile PWM control IC that can be configured for either current mode control or voltage mode control. The choice of the control method usually depends upon the designer preference. The following must be taken into consideration while selecting the control method. Current mode control can inherently balance flux in both phases of the full-bridge topology. The full-bridge topology, like other double ended topologies, is susceptible to the transformer core saturation. Any asymmetry in the volt-second product applied between the two alternating phases results in flux imbalance that causes a dc buildup in the transformer. This continual dc buildup may eventually push the transformer into saturation. The volt-second asymmetry can be corrected by employing current mode control. In current mode control, a signal representative of the primary current is compared against an error signal to control the duty cycle. In steady-state, this results in each phase being terminated at the same peak current by adjusting the pulse-width and thus applying equal volt-seconds to both the phases.

Current mode control can be susceptible to noise and sub-harmonic oscillation, while voltage mode control employs a larger ramp for PWM and is usually less susceptible. Voltage-mode control with input line feed-forward also has excellent line transient response. When configuring for voltage mode control, a dc blocking capacitor can be placed in series with the primary winding of the power transformer to avoid any flux imbalance that may cause transformer core saturation.

6.4.2 Voltage Mode Control Using the LM5045

To configure the LM5045 for voltage mode control, an external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create a saw-tooth modulation ramp signal shown in Figure 6-8. The slope of the signal at RAMP will vary in proportion to the input line voltage. The varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. With a constant error signal, the on-time (T_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt- Second product of the transformer primary. Using a line feed-forward ramp for PWM control requires very little change in the voltage regulation loop to compensate for changes in input voltage, as compared to a fixed slope oscillator ramp. Furthermore, voltage mode control is less susceptible to noise and does not require leading edge filtering. Therefore, it is a good choice for wide input range power converters. Voltage mode control requires a Type-III compensation network, due to the complex-conjugate poles of the L-C output filter.

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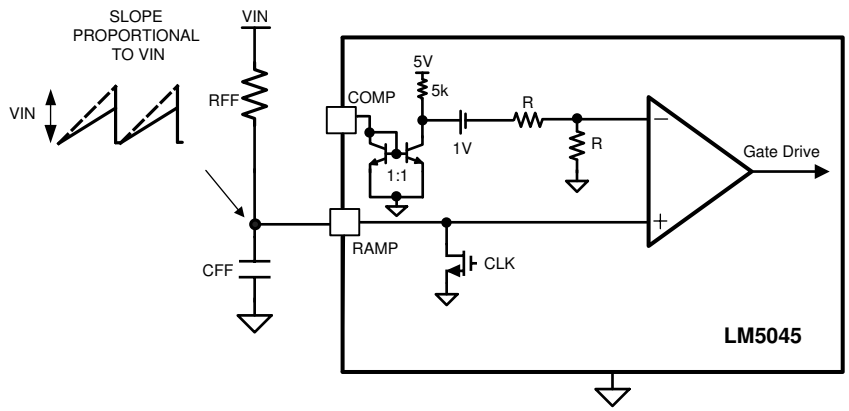

Figure 6-8. Feed-Forward Voltage Mode Configuration

The recommended capacitor value range for C_{FF} is from 100 pF to 1800 pF. Referring to Figure 6-8, it can be seen that C_{FF} value must be small enough to be discharged with in the clock pulse-width which is typically within 50ns. The $R_{DS(ON)}$ of the internal discharge FET is 5.5 Ω.

The value of R_{FF} required can be calculated from

$$R_{FF} = \frac{-1}{F_{OSC} \times C_{FF} \times \ln\left(1 - \frac{V_{RAMP}}{VIN_{MIN}}\right)} \tag{4}$$

For example, assuming a V_{RAMP} of 1.5 V (a good compromise of signal range and noise immunity), at VIN_{MIN} of 36 V (oscillator frequency of 400 kHz and C_{FF} = 470 pF results in a value for R_{FF} of 125 kΩ.

6.4.3 Current Mode Control Using the LM5045

The LM5045 can be configured for current mode control by applying a signal proportional to the primary current to the RAMP pin. One way to achieve this is shown in Figure 6-9. The primary current can be sensed using a current transformer or sense resistor, the resulting signal is filtered and applied to the RAMP pin through a resistor used for slope compensation. It can be seen that the signal applied to the RAMP pin consists of the primary current information from the CS pin plus an additional ramp for slope compensation, added by the resistor R_{SLOPE}.

The current sense resistor is selected such that during over current condition, the voltage across the current sense resistor is above the minimum CS threshold of 728 mV.

In general, the amount of slope compensation required to avoid sub-harmonic oscillation is equal to at least one-half the down-slope of the output inductor current, transformed to the primary. To mitigate sub-harmonic oscillation after one switching period, the slope compensation must be equal to one times the down slope of the filter inductor current transposed to primary. This is known as deadbeat control. The slope compensation resistor required to implement dead-beat control can be calculated as follows:

$$R_{SLOPE} = \frac{V_{OUT} \times R_{CS}}{L_{FILTER} \times F_{OSC} \times I_{SLOPE} \times N_{TR}} \tag{5}$$

where

- N_{TR} is the turns-ratio with respect to the secondary

For example, for a 3.3 V output converter with a turns-ratio between primary and secondary of 9:1, an output filter inductance (L_{FILTER}) of 800 nH and a current sense resistor (R_{SENSE}) of 150 mΩ, R_{SLOPE} of 1.67 kΩ will suffice.

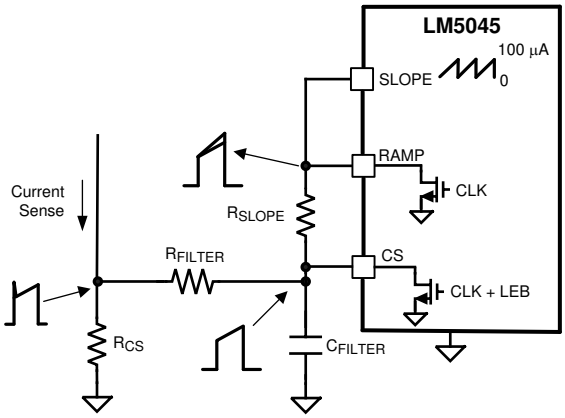

Figure 6-9. Current Mode Configuration

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LM5045 is a highly integrated PWM controller that contains all of the features necessary for implementing full-bridge topology power converters using either current mode or voltage mode control. The device targets DC-DC converter applications with input voltages of up to 100 Vdc and output power in the range 100 W to 1 kW.

7.2 Typical Application

The following schematic shows an example of a 100W full-bridge converter controlled by LM5045. The operating input voltage range is 36 V to 75 V, and the output voltage is 3.3 V. The output current capability is 30 A. The converter is configured for current mode control with external slope compensation. An auxiliary winding is used to raise the VCC voltage to reduce the controller power dissipation.

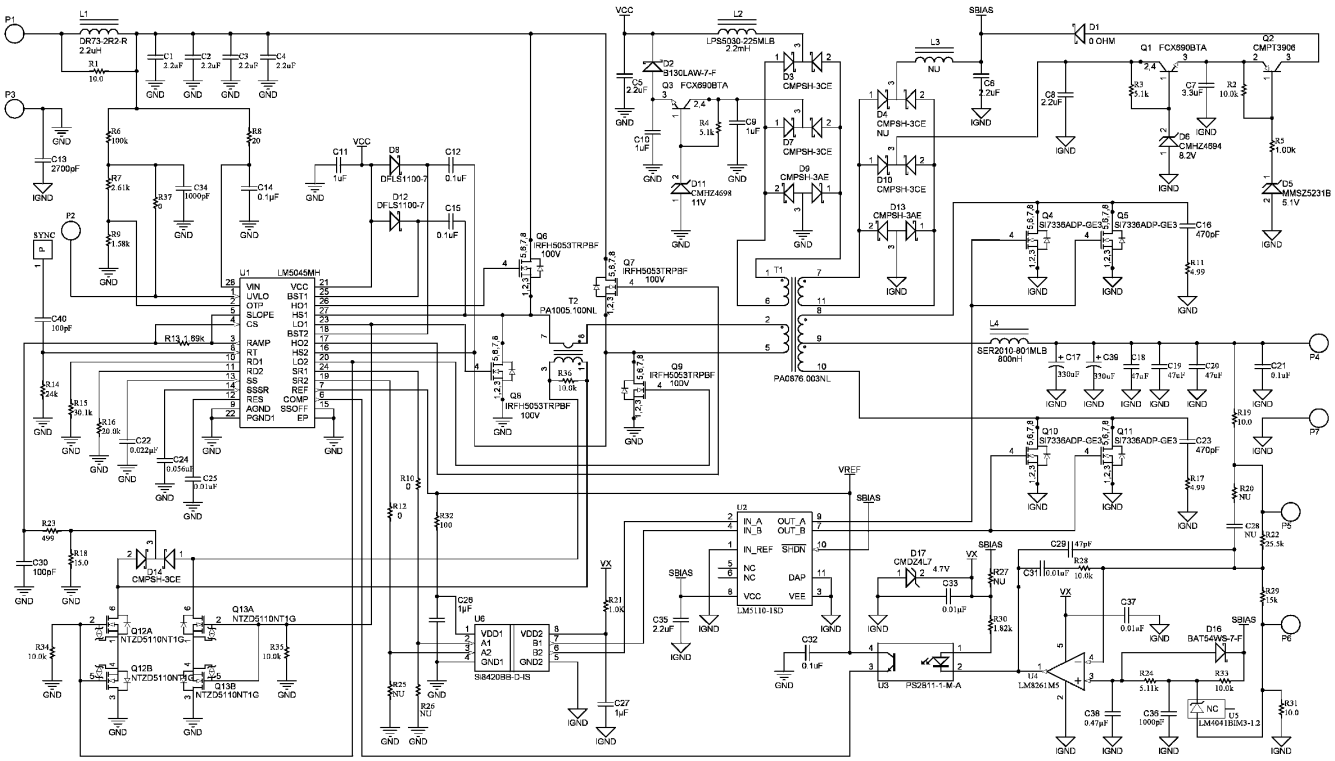

Figure 7-1. Evaluation Board Schematic

7.2.1 Design Requirements

PARAMETERS	VALUE
Input operating range	36 V to 75 V
Output voltage	3.3 V
Measured efficiency at 48 V	92% at 30A
Frequency of operation	420 kHz

PARAMETERS	VALUE
Board size	2.28 x 1.45 x 0.5 inches
Load Regulation	0.2%
Line Regulation	0.1%
Line UVLO	34V/32V on/off
Hiccup Mode	Current Limit

7.2.2 Detailed Design Procedure

7.2.2.1 VIN and V_{CC}

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary in the range of the 14 to 100 V. It is recommended that the filter shown in Figure 7-2 be used to suppress the transients that may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5045. The current into VIN depends primarily on the operating current of the LM5045, the switching frequency, and any external loads on the VCC pin, that typically include the gate capacitances of the power MOSFETs. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This pin must raise VCC voltage above 8 V to shut off the internal start-up regulator.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the IC, the current into the VIN pin drops below 1mA. VIN should remain at a voltage equal to or above the VCC voltage to avoid reverse current through the internal body diode of the internal VCC regulator.

7.2.2.2 For Applications With > 100 VIN

For applications where the system input voltage exceeds 100 V, VIN can be powered from an external start-up regulator as shown in Figure 7-3. In this configuration, the VIN and VCC pins should be connected together. The voltage at the VCC and VIN pins must be greater than 10 V (> Max VCC reference voltage) yet not exceed 16 V. To enable operation the VCC voltage must be raised above 10 V. The voltage at the VCC pin must not exceed 16 V. The voltage source at the right side of Figure 7-3 is typically derived from the power stage, and becomes active once the LM5045's outputs are active.

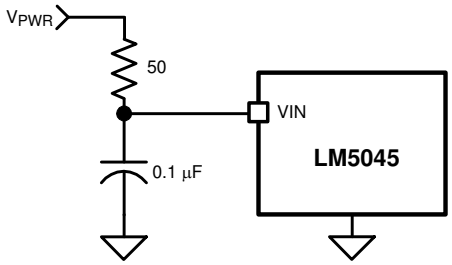

Figure 7-2. Input Transient Protection

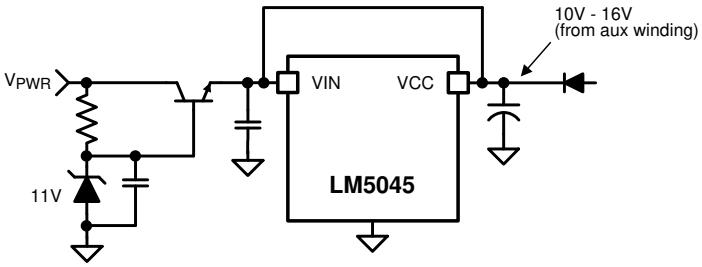

Figure 7-3. Start-Up Regulator For V_{PWR} > 100 V

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7.2.2.3 UVLO and OVP Voltage Divider Selection

Two dedicated comparators connected to the UVLO and OVP pins are used to detect undervoltage and overvoltage conditions. The threshold values of both these comparators are set at 1.25 V. The two functions can be programmed independently with two separate voltage dividers from VIN to AGND as shown in Figure 7-4 and Figure 7-4, or with a three-resistor divider as shown in Figure 7-4. Independent UVLO and OVP pins provide greater flexibility for the user to select the operational voltage range of the system. When the UVLO pin voltage is below 0.4 V, the controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.4 V but less than 1.25 V the controller is in standby mode. Once the UVLO pin voltage is greater than 1.25 V, the controller is fully enabled. Two external resistors can be used to program the minimum operational voltage for the power converter as shown in Figure 7-4. When the UVLO pin voltage falls below the 1.25 V threshold, an internal 20 µA current sink is enabled to lower the voltage at the UVLO pin, thus providing threshold hysteresis. Resistance values for R_1 and R_2 can be determined from the following equations:

$$R_1 = \frac{V_{HYS}}{20\ \mu A}$$

$$R_2 = \frac{1.25V \times R_1}{V_{PWR\text{-}OFF} - 1.25V - (20\ \mu A \times R1)} \tag{6}$$

where

- V_{PWR} is the desired turnon voltage
- V_{HYS} is the desired UVLO hysteresis at V_{PWR}

For example, if the LM5045 is to be enabled when V_{PWR} reaches 33 V, and disabled when V_{PWR} is decreased to 31 V, R_1 should be 100 kΩ, and R_2 should be 4.2 kΩ. The voltage at the UVLO pin should not exceed 7 V at any time.

Two external resistors can be used to program the maximum operational voltage for the power converter as shown in Figure 7-4. When the OVP pin voltage rises above the 1.25 V threshold, an internal 20-µA current source is enabled to raise the voltage at the OVP pin, thus providing threshold hysteresis. Resistance values for R_1 and R_2 can be determined from the following equations:

$$R_1 = \frac{V_{HYS}}{20\ \mu A}$$

$$R_2 = \frac{1.25V \times R_1}{V_{PWR} - 1.25V + (20\ \mu A \times R1)} \tag{7}$$

If the LM5045 is to be disabled when $V_{PWR\text{-}OFF}$ reaches 80 V and enabled when it is decreased to 78 V. R_1 should be 100 kΩ, and R_2 should be 1.5 kΩ. The voltage at the OVP pin should not exceed 7 V at any time.

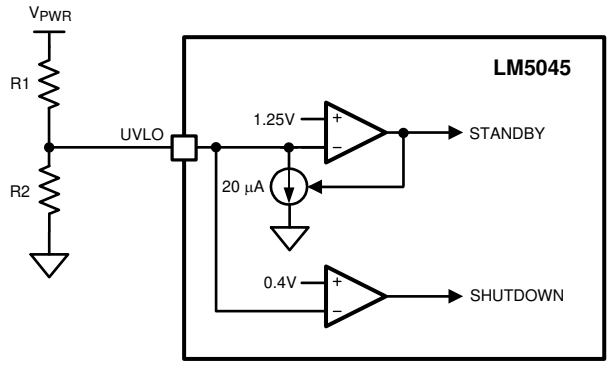

Figure 7-4. Basic UVLO Configuration

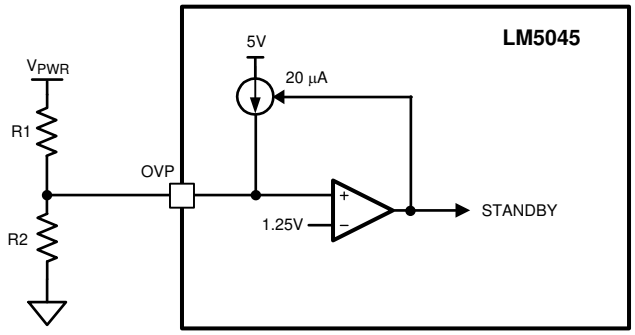

Figure 7-5. Basic OVP Configuration

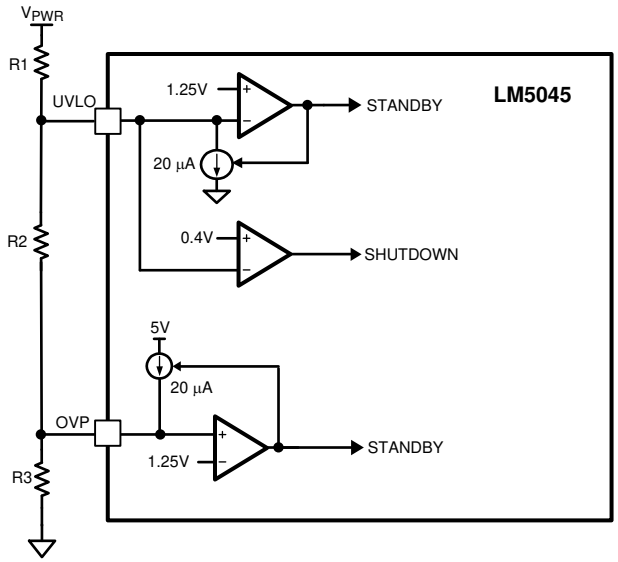

Figure 7-6. UVLO/OVP Divider

The UVLO and OVP can also be set together using a 3 resistor divider ladder as shown in Figure 7-6. R_1 is calculated as explained in the basic UVLO divider selection. Using the same values, as in the above two examples, for the UVLO and OVP set points, R_1 and R_3 remain the same at 100 kΩ and 1.5 kΩ. The R_2 is 2.7 kΩ obtained by subtracting R_3 from 4.2 kΩ.

Remote configuration of the controller's operational modes can be accomplished with open drain device(s) connected to the UVLO pin as shown in Figure 7-7.

Figure 7-8 shows an application of the OVP comparator for Remote Thermal Protection using a thermistor (or multiple thermistors) which may be located near the main heat sources of the power converter. The negative temperature coefficient (NTC) thermistor is nearly logarithmic, and in this example a 100 kΩ thermistor with the β material constant of 4500 Kelvin changes to approximately 2 kΩ at 130°C. Setting R_1 to one-third of this resistance (665 Ω) establishes 130°C as the desired trip point (for VREF = 5 V). In a temperature band from 20°C below to 20°C above the OVP threshold, the voltage divider is nearly linear with 25mV per °C sensitivity.

R_2 provides temperature hysteresis by raising the OVP comparator input by R_2 x 20µA. For example, if a 22kΩ resistor is selected for R_2, then the OVP pin voltage will increase by 22 kΩ x 20 µA = 506 mV. The NTC temperature must therefore fall by 506 mV / 25 mV per °C = 20°C before the LM5045 switches from standby mode to the normal mode.

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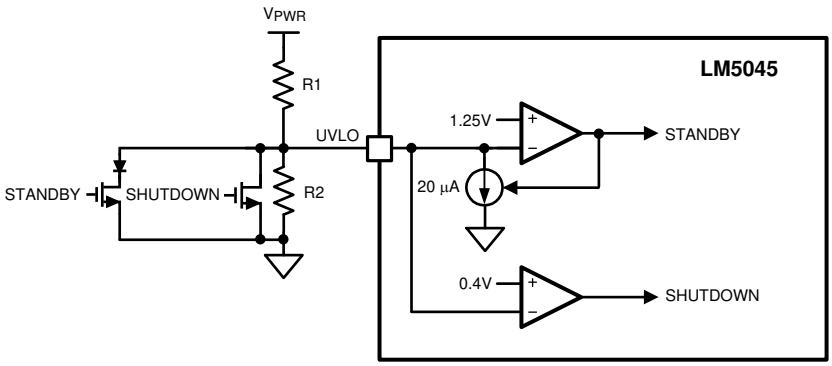

Figure 7-7. Remote Standby and Disable Control

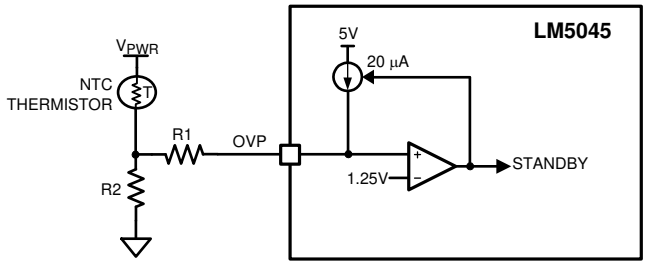

Figure 7-8. Remote Thermal Protection

7.2.2.4 Current Sense

The CS pin receives an input signal representative of its transformer's primary current, either from a current sense transformer or from a resistor located at the junction of source pin of the primary switches, as shown in Figure 7-9 and Figure 7-10, respectively. In both the cases, the filter components R_F and C_F should be located as close to the IC as possible, and the ground connection from the current sense transformer, or R_{SENSE} should be a dedicated trace to the appropriate GND pin. Please refer to the *Section 9* section for more layout tips.

The current sense components must provide a signal > 710 mV at the CS pin during an over-load event. Once the voltage on the CS pin crosses the current limit threshold, the current sense comparator terminates the PWM pulse and starts to charge the RES pin. Depending on the configuration of the RES pin, the LM5045 will eventually initiate a hiccup mode restart or be in continuous current limit.

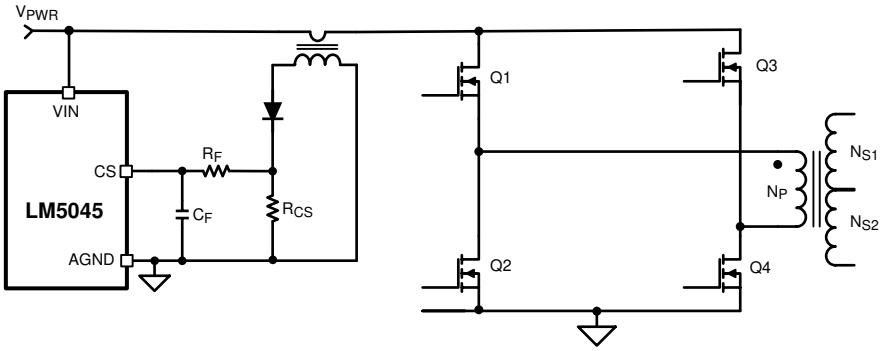

Figure 7-9. Transformer Current Sense

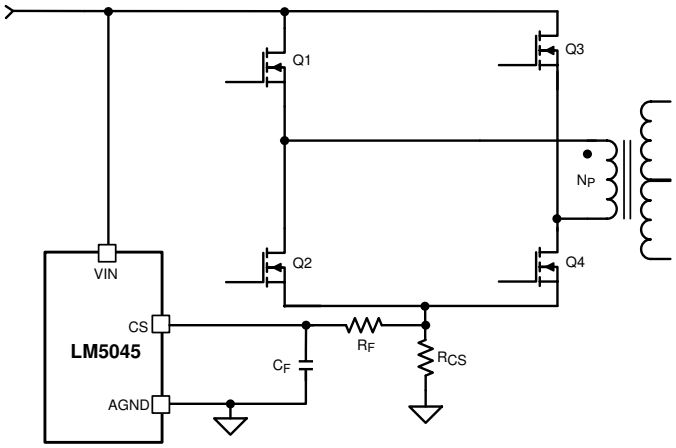

Figure 7-10. Resistor Current Sense

7.2.2.5 Hiccup Mode Current Limit Restart

The operation of the hiccup mode restart circuit is explained in the section. During a continuous current limit condition, the RES pin is charged with 30 µA current source. The restart delay time required to reach the 1.0 V threshold is given by:

$$T_{CS} = \frac{C_{RES} \times 1.0V}{30\ \mu A} \tag{8}$$

This establishes the time allowed before the IC initiates a hiccup restart sequence. For example, if the C_{RES} = 0.01 µF, the time TCS as noted in Figure 7-11 below is 334 µs. Once the RES pin reaches 1.0 V, the 30 µA current source is turned-off and a 10 µA current source is turned-on during the ramp up to 4 V and a 5 µA is turned on during the ramp down to 2 V. The hiccup mode off-time is given by:

$$T_{HICCUP} = \frac{C_{RES} \times (2.0V \times 8)}{5\ \mu A} + \frac{C_{RES} \times ((2.0V \times 8) + 1.0V)}{10\ \mu A} \tag{9}$$

With a C_{RES} = 0.01 µF, the hiccup time is 49 ms. Once the hiccup time is finished, the RES pin is pulled low and the SS pin is released allowing a soft-start sequence to commence. Once the SS pin reaches 1 V, the PWM pulses will commence. The hiccup mode provides a cool-down period for the power converter in the event of a sustained overload condition thereby lowering the average input current and temperature of the power components during such an event.

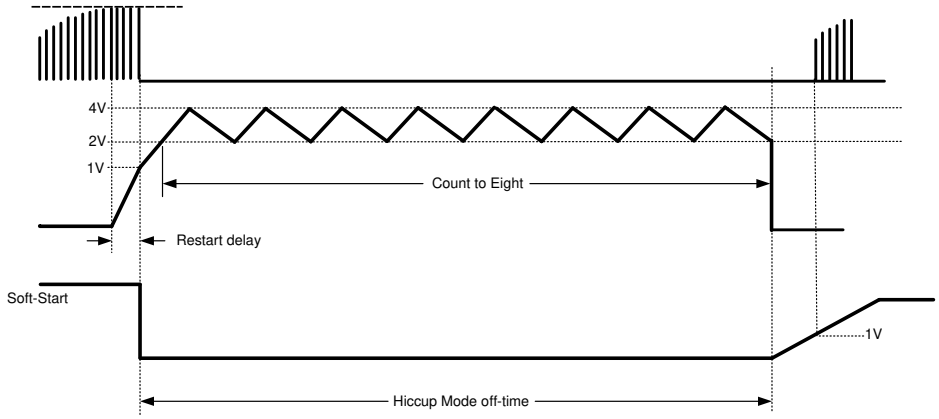

Figure 7-11. Hiccup Mode Delay and Soft-Start Timing Diagram

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7.2.2.6 Augmenting the Gate Drive Strength

The LM5045 includes powerful 2-A integrated gate drivers. However, in certain high-power applications (> 500 W), it might be necessary to augment the strength of the internal gate driver to achieve higher efficiency and better thermal performance. In high power applications, typically, the I^2xR loss in the primary MOSFETs is significantly higher than the switching loss. To minimize the I^2xR loss, either the primary MOSFETs are paralleled or MOSFETs with low $R_{DS\ (on)}$ are employed. Both these scenarios increase the total gate charge to be driven by the controller IC. An increase in the gate charge increases the FET transition time and hence increases the switching losses. Therefore, to keep the total losses within a manageable limit the transition time must be reduced.

Generally, during the Miller capacitance charge/discharge the total available driver current is lower during the turnoff process than during the turnon process and often it is enough to speed-up the turnoff time to achieve the efficiency and thermal goals. This can be achieved simply by employing a PNP device, as shown in Figure 7-12, from gate to source of the power FET. During the turnon process, when the LO1 goes high, the current is sourced through the diode D1 and the BJT Q1 provides the path for the turnoff current. Q1 should be located as close to the power FET as possible so that the turnoff current has the shortest possible path to the ground and does not have to pass through the controller.

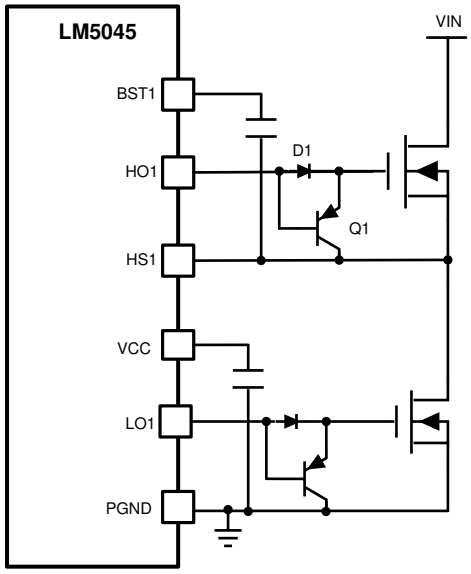

Figure 7-12. Circuit to Speed-Up the Turnoff Process

Depending on the gate charge characteristics of the primary FET, if it is required to speed up both the turnon and the turnoff time, a bipolar totem pole structure as shown in Figure 7-13 can be used. When LO1 goes high, the gate to source current is sourced through the NPN transistor Q1 and similar to the circuit shown in Figure 7-12 when LO1 goes low, the PNP transistor Q2 expedites the turnoff process.

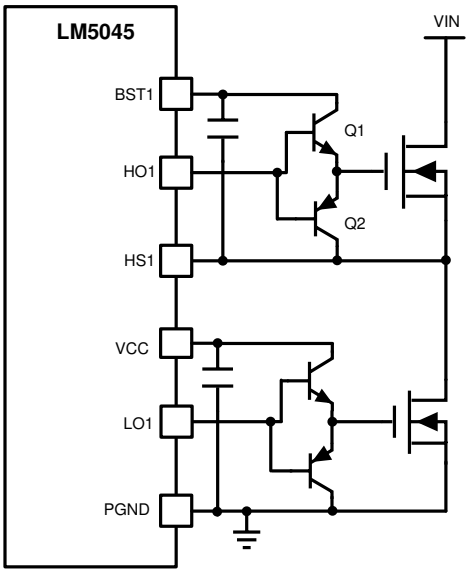

Figure 7-13. Bipolar Totem Pole Arrangement

Alternatively, a low-side gate driver such as LM5112 can be used instead of the discrete totem pole. The LM5112 comes in a small package with a 3A source and a 7A sink capability. While driving the high-side FET, the HS1 acts as a local ground and the boot capacitor between the BST and HS pins acts as VCC.

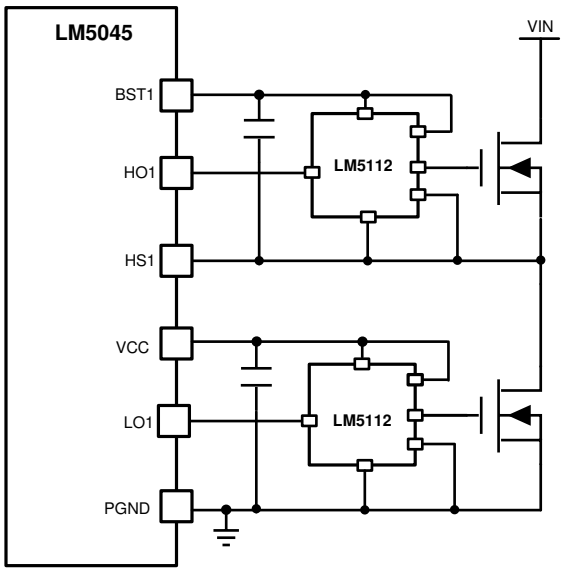

Figure 7-14. Using a Low-Side Gate Driver to Augment Gate Drive Strength

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7.2.3 Application Curve

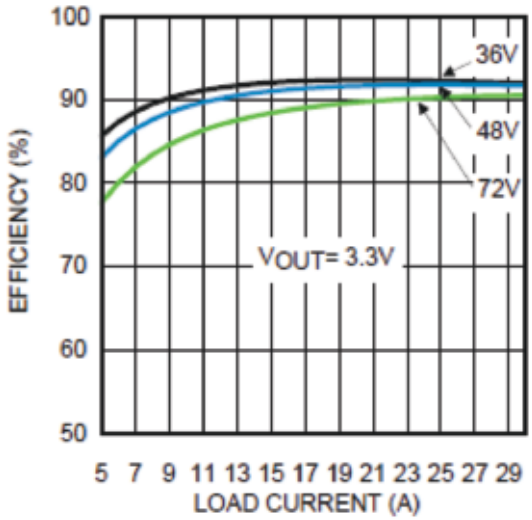

Figure 7-15. Application Board Efficiency

8 Power Supply Recommendations

The LM5045 can be used to control power levels up to 1 kW. Therefore the current levels can be considerable. Care should be taken that components with the correct current rating are chosen. This would include magnetic components, power MOSFETS and diodes, connectors and wire sizes. Input and output capacitors should have the correct ripple current rating. The use of a multilayer PCB is recommended with a copper area chosen to ensure the LM5045 is operating below its maximum junction temperature.

Full power loading should never be attempted with providing with providing adequate cooling.

9 Layout

9.1 Layout Guidelines

The LM5045 current sense and PWM comparators are very fast and respond to short duration noise pulses. The components at the CS, COMP, SLOPE, RAMP, SS, SSSR, RES, UVLO, OVP, RD1, RD2, and RT pins should be physically close as possible to the IC, thereby minimizing noise pickup on the PC board trace inductance. Eliminating or minimizing via's in these critical connections are essential. Layout consideration is critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of the transformer should be connected via a dedicated PC board trace to the AGND pin, rather than through the ground plane. If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground trace should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

The gate drive outputs of the LM5045 should have short, direct paths to the power MOSFETs to minimize inductance in the PC board. The boot-strap capacitors required for the high side gate drivers should be located very close to the IC and connected directly to the BST and HS pins. The VCC and REF capacitors should also be placed close to their respective pins with short trace inductance. Low ESR and ESL ceramic capacitors are recommended for the boot-strap, VCC and the REF capacitors. The two ground pins (AGND, PGND) must be connected together directly underneath the IC with a short, direct connection, to avoid jitter due to relative ground bounce.

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9.2 Layout Example

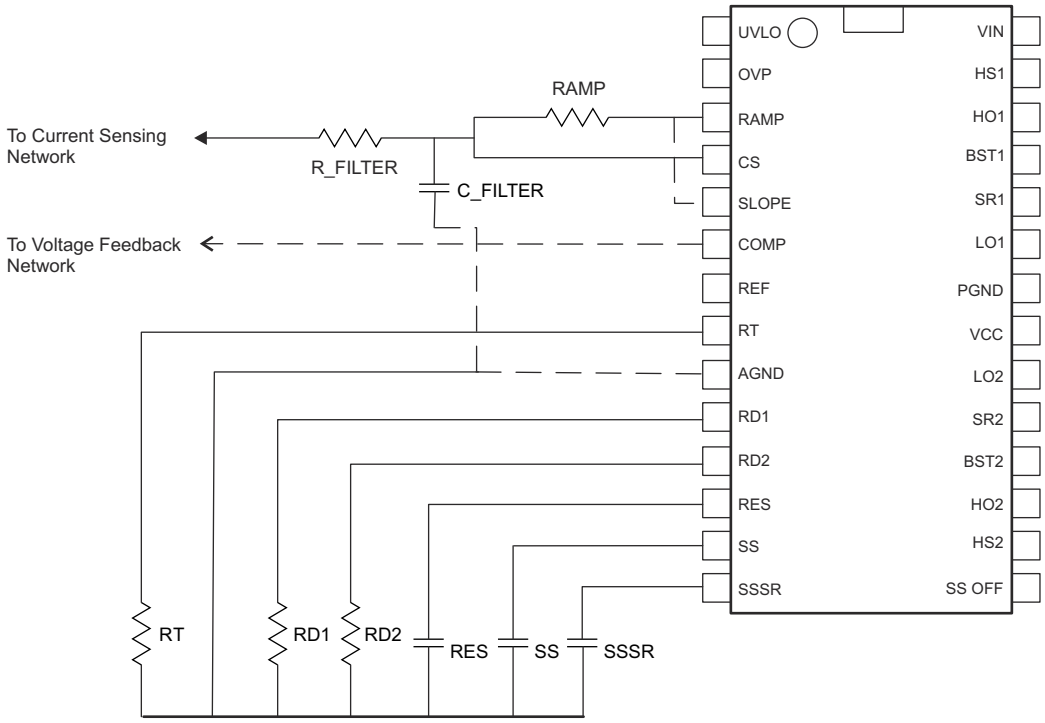

Figure 9-1. Layout of Components Around RAMP, CS, SLOPE, COMP, RT, RD1, RD2, RES, SS, and SSR

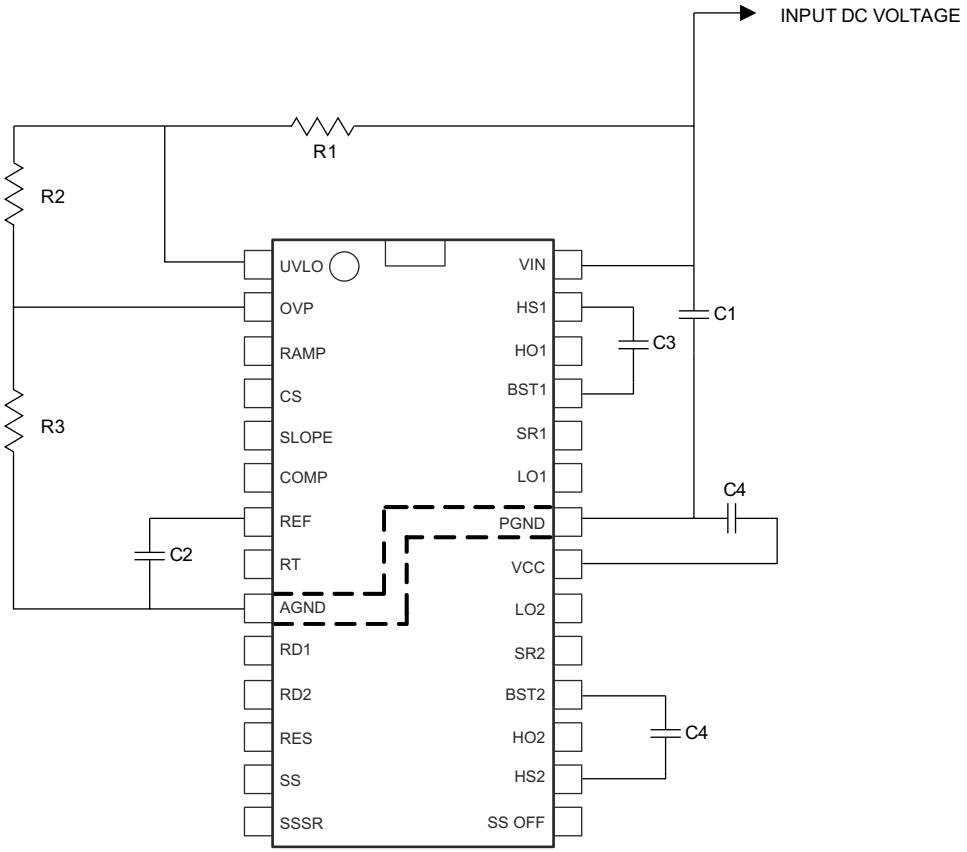

Figure 9-2. Layout of Components Around VIN, VCC, AGND, PGND UVLO, OVP, REF, BST1, BST2, HS1, and HS2

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10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2015) to Revision I (May 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision G (March 2013) to Revision H (January 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision F (March 2013) to Revision G (March 2013)	Page
• Changed layout of National Data Sheet to TI format	25

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5045MH/NOPB	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5045 MH
LM5045MH/NOPB.A	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5045 MH
LM5045MHX/NOPB	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5045 MH
LM5045MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5045 MH
LM5045SQ/NOPB	Active	Production	WQFN (RSG) | 28	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5045
LM5045SQ/NOPB.A	Active	Production	WQFN (RSG) | 28	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5045
LM5045SQX/NOPB	Active	Production	WQFN (RSG) | 28	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5045
LM5045SQX/NOPB.A	Active	Production	WQFN (RSG) | 28	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5045

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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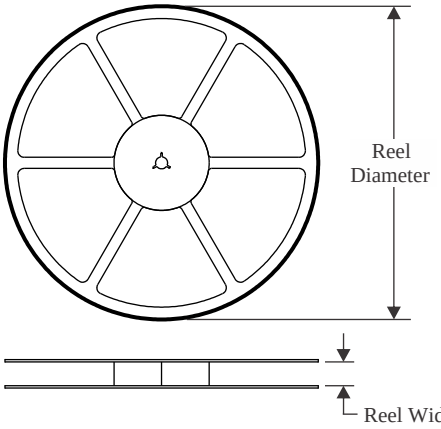
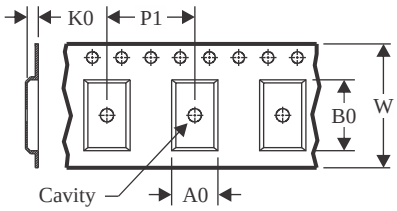
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

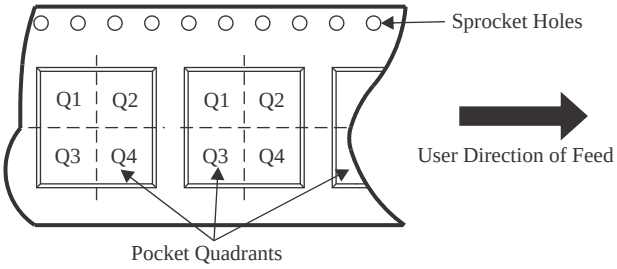


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

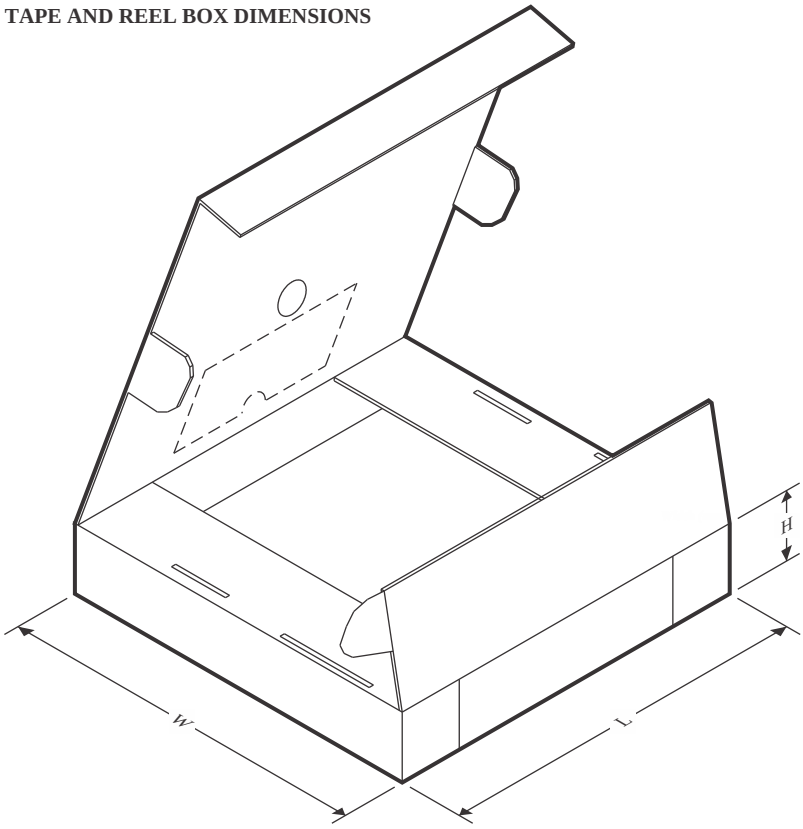
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5045MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1
LM5045SQ/NOPB	WQFN	RSG	28	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM5045SQX/NOPB	WQFN	RSG	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

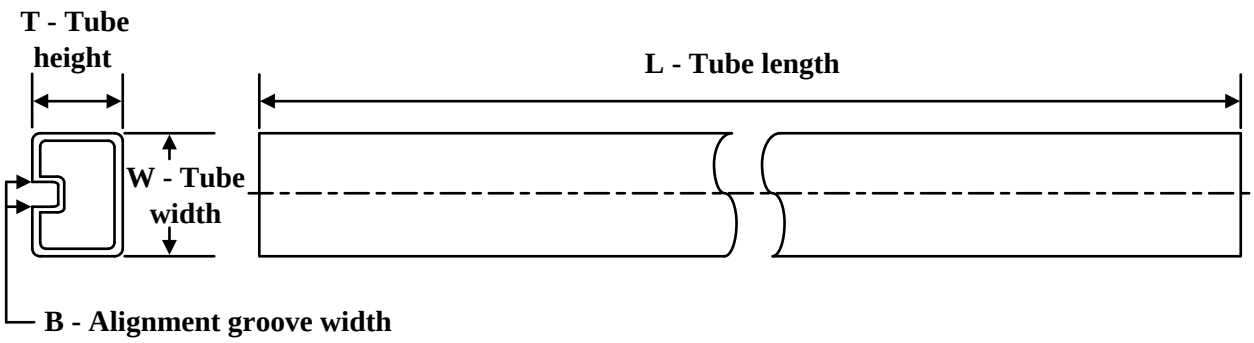
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5045MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0
LM5045SQ/NOPB	WQFN	RSG	28	1000	208.0	191.0	35.0
LM5045SQX/NOPB	WQFN	RSG	28	4500	367.0	367.0	35.0

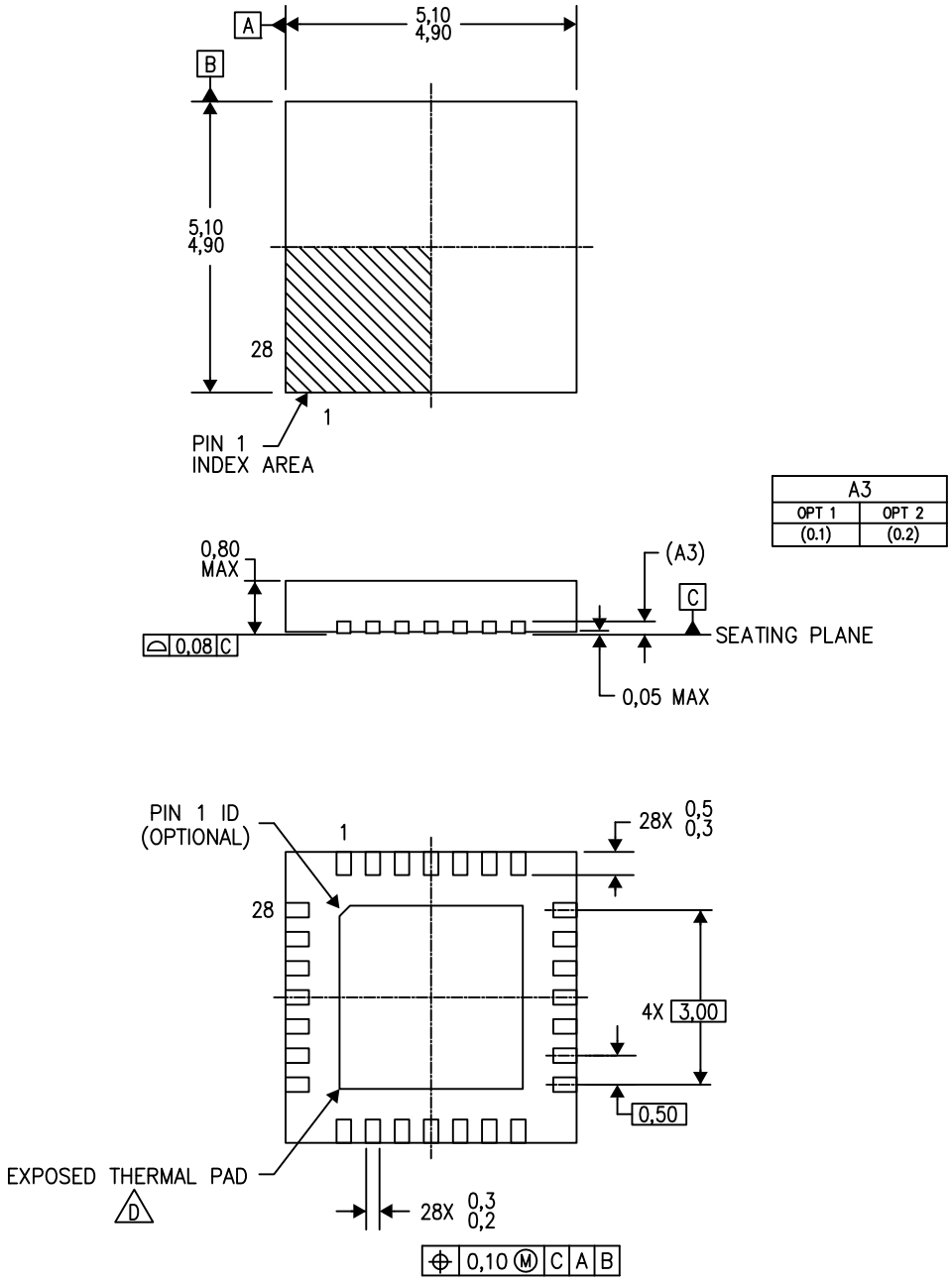
TUBE



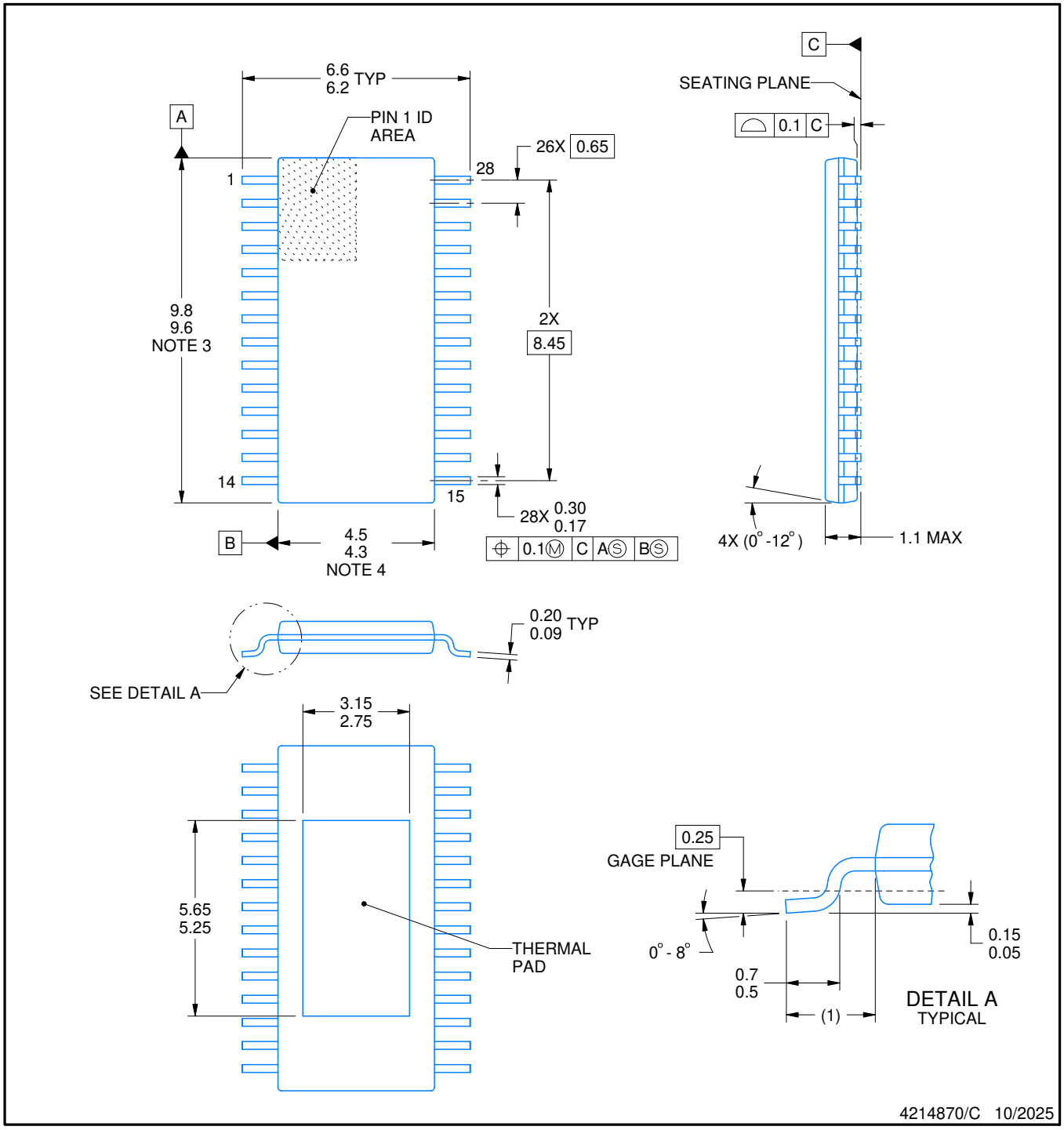
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5045MH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM5045MH/NOPB.A	PWP	HTSSOP	28	48	495	8	2514.6	4.06

RSG (S-PWQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD



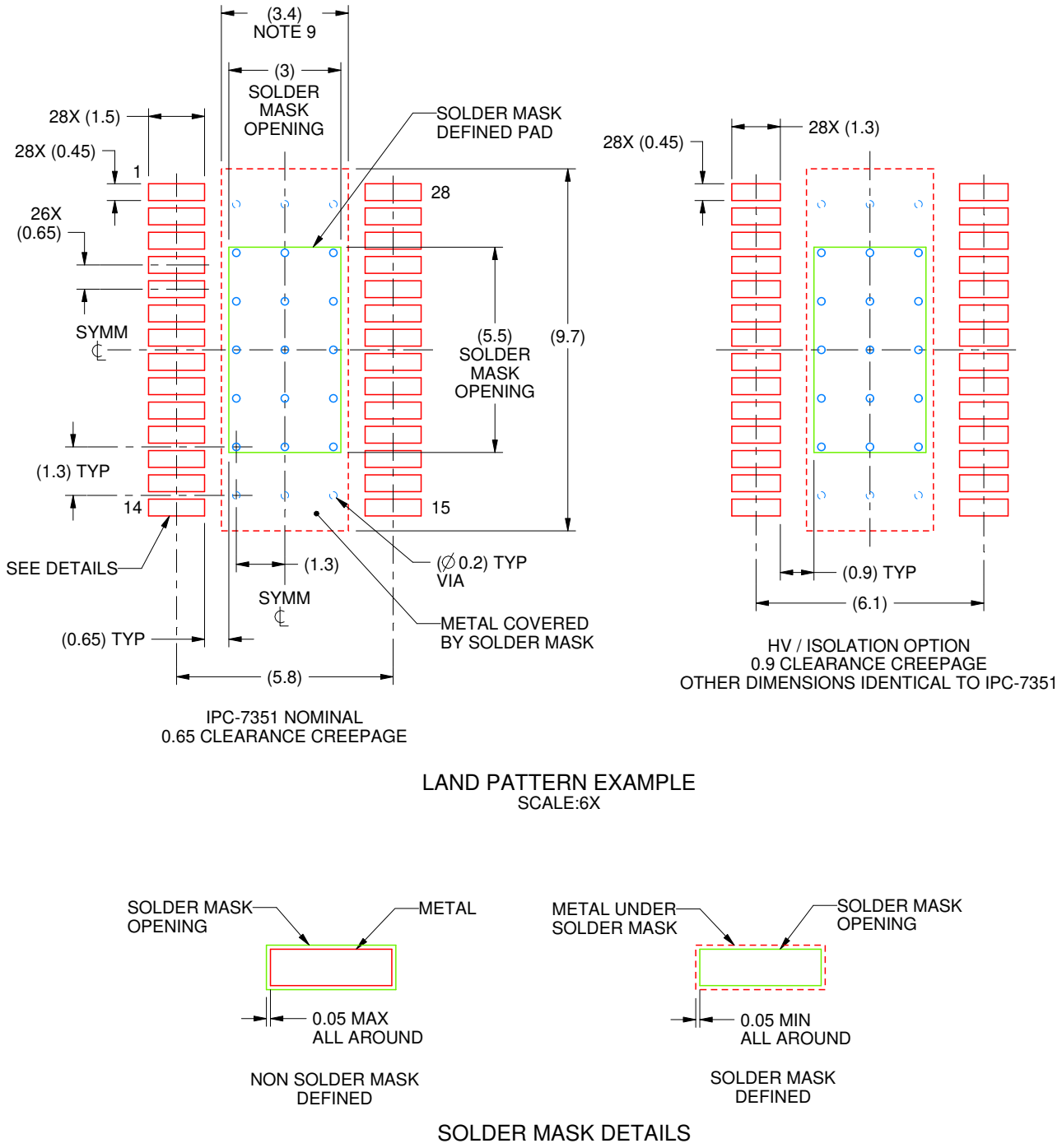
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.



PowerPAD is a trademark of Texas Instruments.

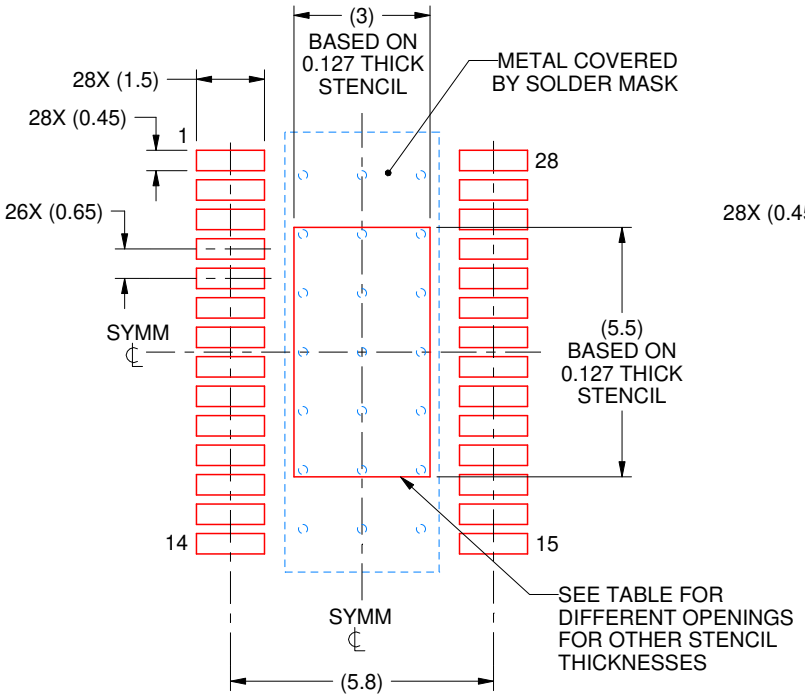
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

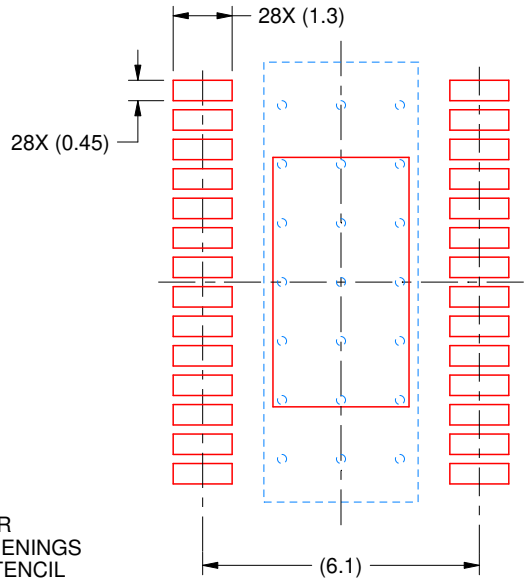


NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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