# LM6588 TFT-LCD Quad, 16V RRIO High Output Current Operational Amplifier

**Check for Samples: LM6588**

## FEATURES

- **($V_S$ = 5V, $T_A$ = 25°C Typical Values Unless Specified)**
- **Input Common Mode Voltage 0.5V Beyond Rails**
- **Output Voltage Swing ($R_L$ = 2kΩ) 50mV from Rails**
- **Output Short Circuit Current ±200mA**
- **Continuous Output Current 75mA**
- **Supply Current (Per Amp, No Load) 750µA**
- **Supply Voltage Range 5V to 16V**
- **Unity Gain Stable**
- **−3dB Bandwidth ($A_V$ = +1) 24MHz**
- **Slew Rate 11V/µSec**
- **Settling Time 270ns**
- **SOIC-14 and TSSOP-14 Package**
- **Manufactured in TI's State-of-the-art Bonded Wafer, Trench Isolated Complementary Bipolar VIP10™ Technology for High Performance at Low Power Levels**

## APPLICATIONS

- **LCD Panel $V_{COM}$ Driver**
- **LCD Panel Gamma Buffer**
- **LCD Panel Repair Amp**

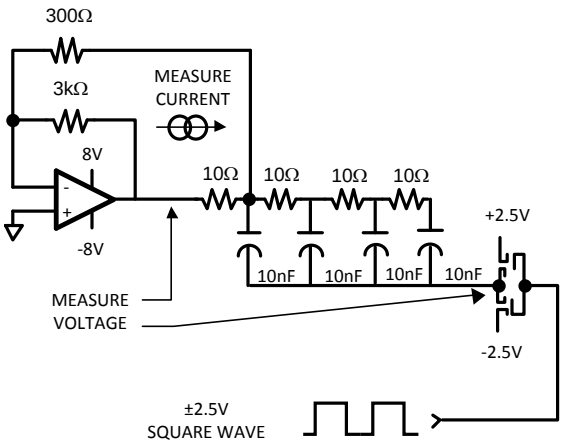
## DESCRIPTION

The LM6588 is a low power, high voltage, rail-to-rail input-output amplifier ideally suited for LCD panel $V_{COM}$ driver and gamma buffer applications. The LM6588 contains four unity gain stable amplifiers in one package. It provides a common mode input ability of 0.5V beyond the supply rails, as well as an output voltage range that extends to within 50mV of either supply rail. With these capabilities, the LM6588 provides maximum dynamic range at any supply voltage. Operating on supplies ranging from 5V to 16V, while consuming only 750µA per amplifier, the LM6588 has a bandwidth of 24MHz (−3dB).

The LM6588 also features fast slewing and settling times, along with a high continuous output capability of 75mA. This output stage is capable of delivering approximately 200mA peak currents in order to charge or discharge capacitive loads. These features are ideal for use in TFT-LCDs.

The LM6588 is available in the industry standard 14-pin SOIC package and in the space-saving 14-pin TSSOP package. The amplifiers are specified for operation over the full −40°C to +85°C temperature range.

### Test Circuit Diagram

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2]

| | | |
|---|---|---|
| ESD Tolerance[3] | Human Body Model | 2.5KV |
| | Machine Model | 250V |
| Supply Voltage ($V^+$ - $V^-$) | | 18V |
| Differential Input Voltage | | ±5.5V |
| Output Short Circuit to Ground[4] | | Continuous |
| Storage Temperature Range | | −65°C to 150°C |
| Input Common Mode Voltage | | $V^-$ to $V^+$ |
| Junction Temperature[5] | | 150°C |

(1) Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For testing purposes, ESD was applied using human body model, 1.5kΩ in series with 100pF.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC board.

## Operating Ratings[1]

| | | |
|---|---|---|
| Supply Voltage | | $4V \le V_S \le 16V$ |
| Temperature Range | | −40°C to +85°C |
| Thermal Resistance ($\theta_{JA}$) | SOIC-14 | 145°C/W |
| | TSSOP-14 | 155°C/W |

(1) Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.


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## 16V DC Electrical Characteristics[1]

Unless otherwise specified, all limits ensured for at $T_J$ = 25°C, $V_{CM}$ = ½$V_S$ and $R_L$ = 2kΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | 0.7 | 4<br>**6** | mV |
| TC $V_{OS}$ | Input Offset Voltage Average Drift | | | 5 | | μV/°C |
| $I_B$ | Input Bias Current | | | −0.3/+0.3 | ±1<br>**±7** | μA |
| $I_{OS}$ | Input Offset Current | | | 16 | 150<br>**300** | nA |
| $R_{IN}$ | Input Resistance | Common Mode | | 20 | | MΩ |
| | | Differential Mode | | 0.5 | | |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = 0 to +16V | 75<br>**70** | 103 | | dB |
| | | $V_{CM}$ = 0 to 14.5V | 78<br>**72** | 103 | | |
| PSRR | Power Supply Rejection Ratio | $V_{CM}$ = ±1V | 80<br>**75** | 103 | | dB |
| CMVR | Input Common-Mode Voltage Range | CMRR > 50dB | 16.2 | 0<br>16 | −0.2 | V |
| $A_V$ | Large Signal Voltage Gain[4] | $R_L$ = 2kΩ, $V_O$ = 0.5 to +15.5V | 80<br>**75** | 108 | | dB |
| $V_O$ | Output Swing High | $R_L$ = 2kΩ | 15.8<br>**15.6** | 15.9 | | V |
| | Output Swing Low | $R_L$ = 2kΩ | | 0.100 | 0.200 | |
| $I_{SC}$ | Output Short Circuit Current[5] | Sourcing | 170 | 230 | | mA |
| | | Sinking | 170 | 230 | | |
| $I_{CONT}$ | Continuous Output Current[6] | Sourcing | | 40 | | mA |
| | | Sinking | | 40 | | |
| $I_S$ | Supply Current (per Amp) | | | 800 | 1200<br>**1500** | μA |

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See applications section for information on temperature de-rating of this device.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing.
(5) Continuous operation at these output currents will exceed the power dissipation ability of the device
(6) Power dissipation limits may be exceeded if all four amplifiers source or sink 40mA. Voltage across the output transistors and their output currents must be taken into account to determine the power dissipation of the device

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## 16V AC Electrical Characteristics[1]

Unless otherwise specified, all limits ensured for at $T_J$ = 25°C, $V_{CM}$ = ½$V_S$ and $R_L$ = 2kΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate[4] | $A_V$ = +1, $V_{IN}$ = 10$V_{PP}$ | 8 | 15 | | V/µs |
| | Unity Gain Bandwidth Product | | | 15.4 | | MHz |
| | −3dB Frequency | $A_V$ = +1 | 10 | 24 | | MHz |
| $\Phi_m$ | Phase Margin | | | 61 | | deg |
| $t_s$ | Settling Time (0.1%) | $A_V$ = −1, $A_O$ = ±5V, $R_L$ = 500Ω | | 780 | | ns |
| $t_p$ | Propagation Delay | $A_V$ = −2, $V_{IN}$ = ±5V, $R_L$ = 500Ω | | 20 | | ns |
| HD2 | 2nd Harmonic Distortion $F_{IN}$ = 1MHz[5] | $V_{OUT}$ = 2$V_{PP}$ | | −53 | | dBc |
| HD3 | 3rd Harmonic Distortion $F_{IN}$ = 1MHz[5] | $V_{OUT}$ = 2$V_{PP}$ | | −40 | | dBc |
| $e_n$ | Input-Referred Voltage Noise | f = 10kHz | | 23 | | nV/√Hz |

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$ > $T_A$. See applications section for information on temperature de-rating of this device.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Slew rate is the average of the raising and falling slew rates.
(5) Harmonics are measured with $A_V$ = +2 and $R_L$ = 100Ω and $V_{IN}$ = 1$V_{PP}$ to give $V_{OUT}$ = 2$V_{PP}$.


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## 5V DC Electrical Characteristics[1]

Unless otherwise specified, all limits ensured for at $T_J$ = 25°C, $V_{CM}$ = ½$V_S$ and $R_L$ = 2kΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | 0.7 | 4<br>**6** | mV |
| TC $V_{OS}$ | Input Offset Voltage Average Drift | | | 10 | | μV/°C |
| $I_B$ | Input Bias Current | | | −0.3/+0.3 | ±1<br>**±7** | μA |
| $I_{OS}$ | Input Offset Current | | | 20 | 150<br>**300** | nA |
| $R_{IN}$ | Input Resistance | Common Mode | | 20 | | MΩ |
| | | Differential Mode | | 0.5 | | |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ Stepped from 0 to 5V | 70<br>**66** | 105 | | dB |
| | | $V_{CM}$ Stepped from 0 to 3.5V | 75<br>**70** | 105 | | |
| PSRR | Power Supply Rejection Ratio | $V_S$ = $V_{CC}$ = 3.5V to 5.5V | 80<br>**75** | 92 | | dB |
| CMVR | Input Common-Mode Voltage Range | CMRR > 50dB | <br>5.2 | 0.0<br>5.0 | −0.2 | V |
| $A_V$ | Large Signal Voltage Gain[4] | $R_L$ = 2kΩ, $V_O$ = 0 to 5V | 80<br>**75** | 106 | | dB |
| $V_O$ | Output Swing High[5] | $R_L$ = 2kΩ | 4.85<br>**4.7** | 4.95 | | V |
| | Output Swing Low[5] | $R_L$ = 2kΩ | | 0.05 | 0.15 | |
| $I_{SC}$ | Output Short Circuit Current[6] | Sourcing | 160 | 200 | | mA |
| | | Sinking | 160 | 200 | | |
| $I_{CONT}$ | Continuous Output Current[7] | Sourcing | | 75 | | mA |
| | | Sinking | | 75 | | |
| $I_S$ | Supply Current (per Amp) | | | 750 | 1000<br>**1250** | μA |

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$ > $T_A$. See applications section for information on temperature de-rating of this device.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing.
(5) The open loop output current is specified, by the measurement of the open loop output voltage swing.
(6) Continuous operation at these output currents will exceed the power dissipation ability of the device
(7) Power dissipation limits may be exceeded if all four amplifiers source or sink 40mA. Voltage across the output transistors and their output currents must be taken into account to determine the power dissipation of the device

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## 5V AC Electrical Characteristics[1]

Unless otherwise specified, all limits ensured for at $T_J$ = 25°C, $V_{CM}$ = ½$V_S$ and $R_L$ = 2kΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate[4] | $A_V$ = +1, $V_{IN}$ = 3.5$V_{PP}$ | | 11 | | V/µs |
| | Unity Gain Bandwidth Product | | | 15.3 | | MHz |
| | −3dB Frequency | $A_V$ = +1 | 10 | 24 | | MHz |
| $\Phi_m$ | Phase Margin | | | 56 | | deg |
| $t_s$ | Settling Time (0.1%) | $A_V$ = −1, $V_O$ = ±1V, $R_L$ = 500Ω | | 270 | | ns |
| $t_p$ | Propagation Delay | $A_V$ = −2, $V_{IN}$ = ±1V, $R_L$ = 500Ω | | 21 | | ns |
| HD2 | 2nd Harmonic Distortion $F_{IN}$ = 1MHz[5] | $V_{OUT}$ = 2$V_{PP}$ | | −53 | | dBc |
| HD3 | 3rd Harmonic Distortion $F_{IN}$ = 1MHz[5] | $V_{OUT}$ = 2$V_{PP}$ | | −40 | | dBc |
| $e_n$ | Input-Referred Voltage Noise | f = 10kHz | | 23 | | nV/√Hz |

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See applications section for information on temperature de-rating of this device.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Slew rate is the average of the raising and falling slew rates.
(5) Harmonics are measured with $A_V$ = +2 and $R_L$ = 100Ω and $V_{IN}$ = 1$V_{PP}$ to give $V_{OUT}$ = 2$V_{PP}$.

## Connection Diagram

**14-Pin SOIC/TSSOP**

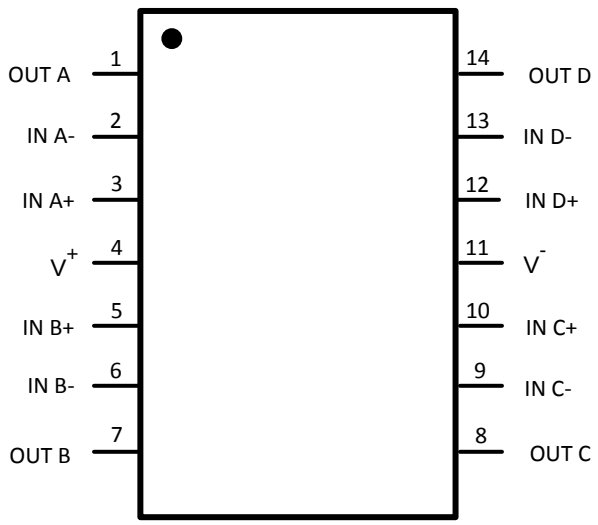


**Figure 1. Top View**


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## Typical Performance Characteristics

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V_{CM}$ = 1/2$V_S$ and $R_L$ = 2kΩ.

**Gain Phase vs. Temperature ($V_S$ = 5V)**

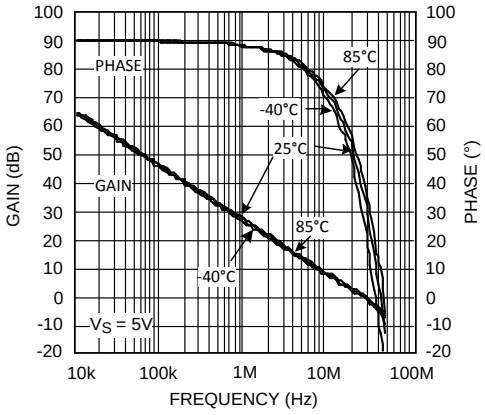


**Figure 2.**

**Gain Phase vs. Temperature ($V_S$ = 16V)**

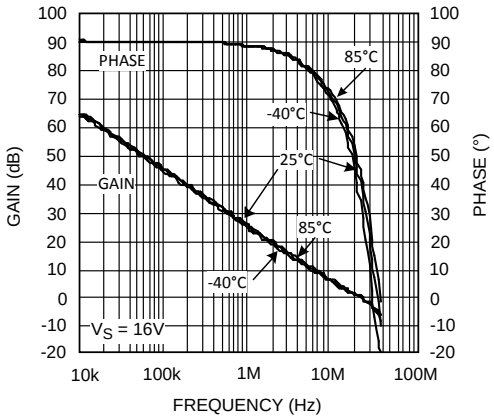


**Figure 3.**

**Gain Phase vs. Capacitive Loading ($V_S$ = 5V)**

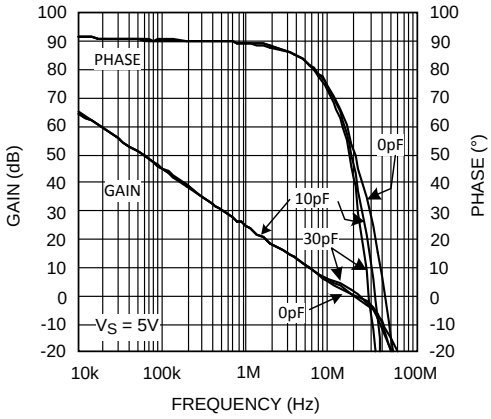


**Figure 4.**

**Gain Phase vs. Capacitive Loading ($V_S$ = 16V)**

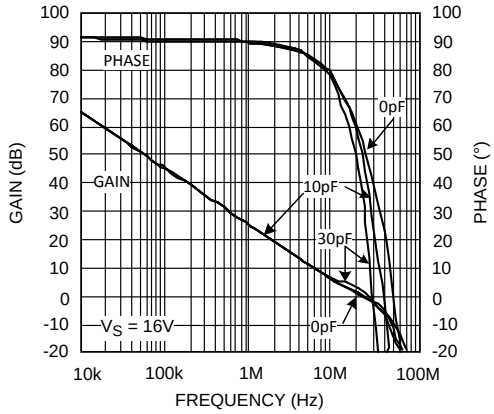


**Figure 5.**

**PSRR ($V_S$ = 5V)**

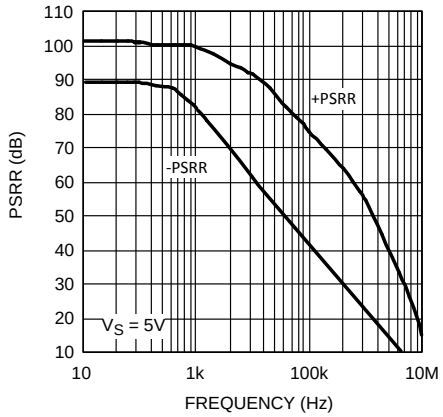


**Figure 6.**

**PSRR ($V_S$ = 16V)**

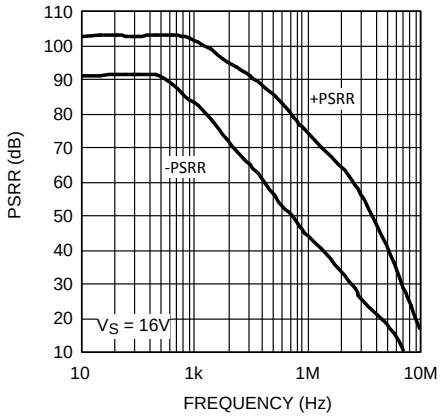


**Figure 7.**

## Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V_{CM}$ = 1/2$V_S$ and $R_L$ = 2kΩ.

**CMRR ($V_S$ = 5V)**

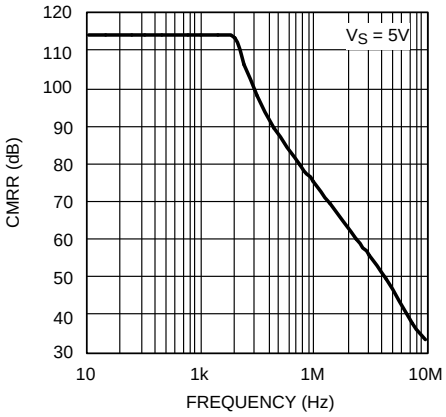


**Figure 8.**

**CMRR ($V_S$ = 16V)**

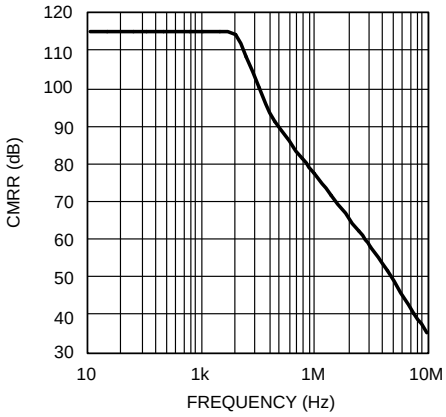


**Figure 9.**

**Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)**

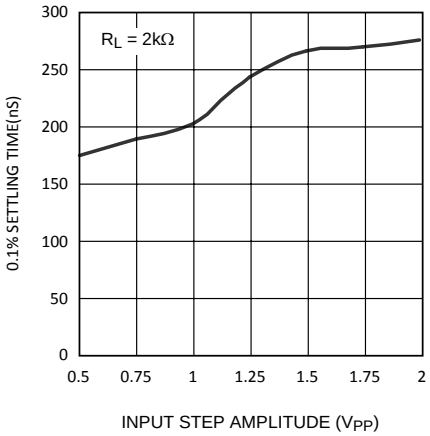


**Figure 10.**

**Settling Time vs. Capacitive Loading (Output Slew and Settle Time)**

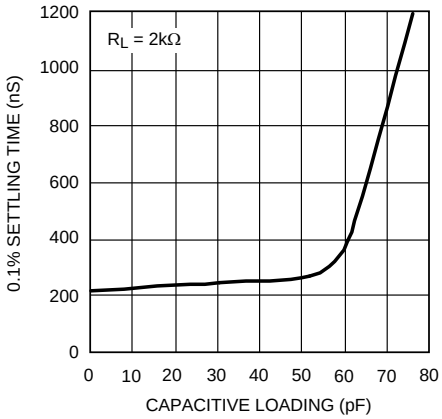


**Figure 11.**

**Crosstalk Rejection vs. Frequency (Output to Output)**

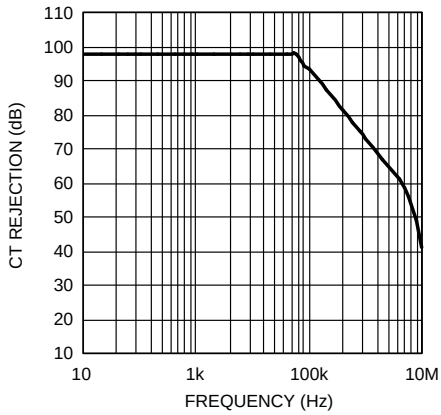


**Figure 12.**

**Input Voltage Noise vs. Frequency**

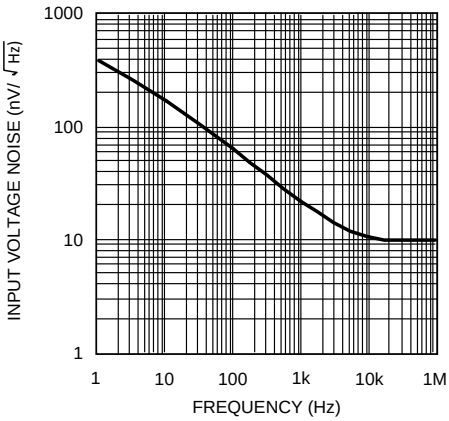


**Figure 13.**


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## Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V_{CM}$ = 1/2$V_S$ and $R_L$ = 2kΩ.

**Stability vs. Capacitive Load Unity Gain ($V_S$ = 16V)**

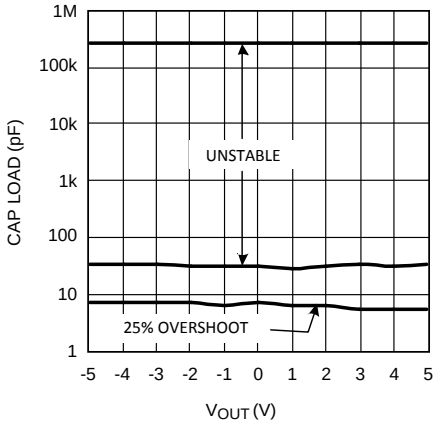


**Figure 14.**

**Large Signal Step Response**

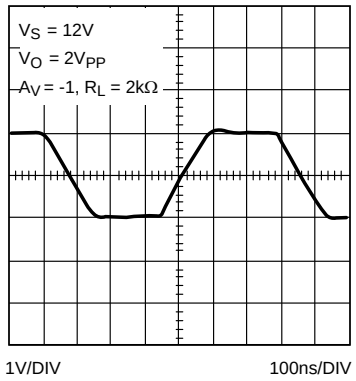


**Figure 15.**

**Small Signal Step Response**

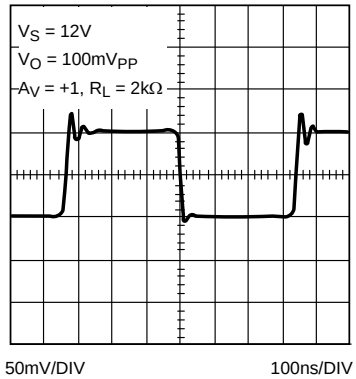


**Figure 16.**

**Small Signal Step Response**

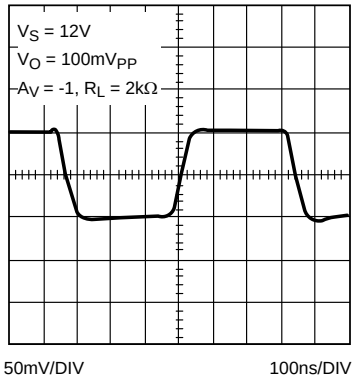


**Figure 17.**

**Closed Loop Output Impedance vs. Frequency ($A_V$ = +1)**

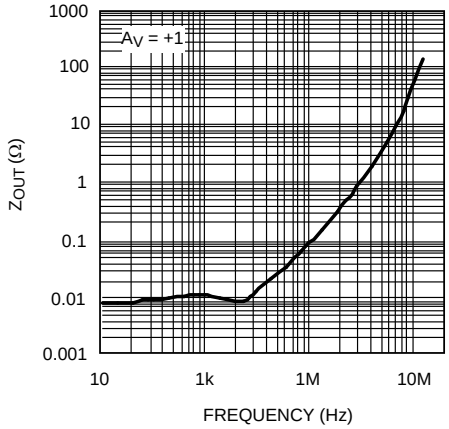


**Figure 18.**

**$I_{SUPPLY}$ vs. Common Mode Voltage ($V_S$ = ±5V)**

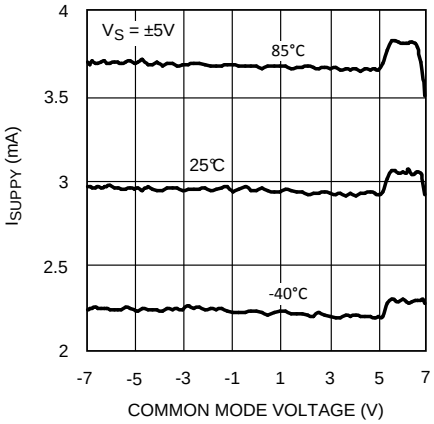


**Figure 19.**

## Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V_{CM}$ = 1/2$V_S$ and $R_L$ = 2kΩ.

**$V_{OS}$ vs. Common Mode Voltage ($V_S$ = 16V)**

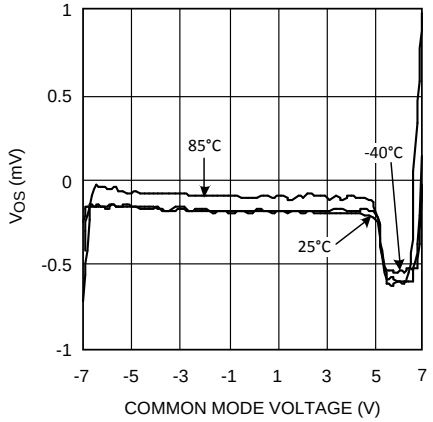


**Figure 20.**

**$V_{OS}$ vs. $V_{OUT}$ (Typical Unit), ($V_S$ = 10V)**

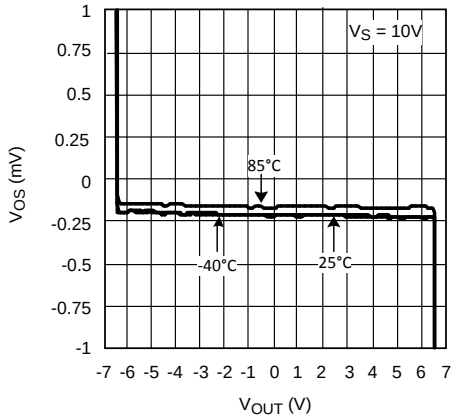


**Figure 21.**

**$V_{OUT}$ from $V^+$ vs. $I_{SOURCE}$**

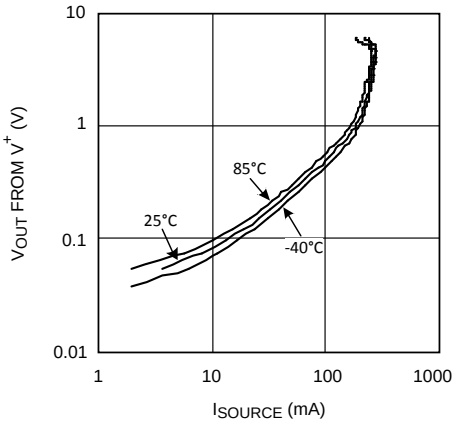


**Figure 22.**

**$V_{OUT}$ from $V^-$ vs. $I_{SINK}$**

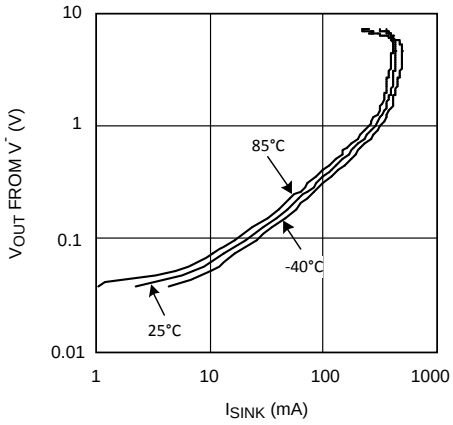


**Figure 23.**

**$I_{SUPPLY}$ vs. Supply Voltage**

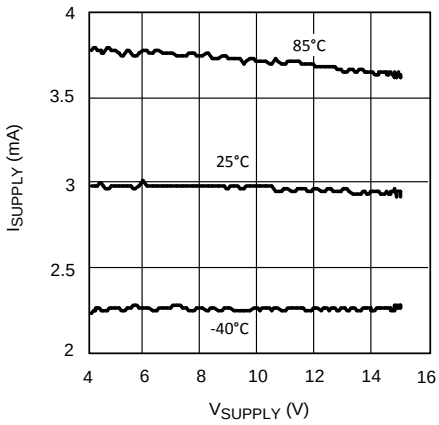


**Figure 24.**


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## Application Notes

### CIRCUIT DESCRIPTION
### GENERAL & SPEC

The LM6588 is a bipolar process operational amplifier. It has an exceptional output current capability of 200mA. The part has both rail to rail inputs and outputs. It has a −3dB bandwidth of 24MHz. The part has input voltage noise of 23nV/$\sqrt{Hz}$, and 2$^{nd}$ and 3$^{rd}$ harmonic distortion of −53dB and −40dB respectively.

### INPUT SECTION

The LM6588 has rail to rail inputs and thus has an input range over which the device may be biased of $V^-$ minus 0.5V, and $V^+$ plus 0.5V. The ultimate limit on input voltage excursion is the ESD protection diodes on the input pins. The most important consideration in Rail-to-Rail input op amps is to understand the input structure. Most Rail-to-Rail input amps use two differential input pairs to achieve this function. This is how the LM6588 works. A conventional PNP differential transistor pair provides the input gain from 0.5V below the negative rail to about one volt below the positive rail. At this point internal circuitry activates a differential NPN transistor pair that allows the part to function from 1 volt below the positive rail to 0.5V above the positive rail. The effect on the inputs pins is as if there were two different op amps connected to the inputs. This has several unique implications.

- The input offset voltage will change, sometimes from positive to negative as the inputs transition between the two stages at about a volt below the positive rail. this effect is seen in the $V_{OS}$ vs. $V_{CM}$ chart in the Typical Performance Characteristics section of this datasheet.
- The input bias currents can be either positive or negative. Do not expect a consistent flow in or out of the pins.
- The part will have different specifications depending on whether the NPN or PNP stage is operating.
- There is a little more input capacitance then a single stage input although the ESD diodes often swamp out the added base capacitance.
- Since the input offset voltages can change from positive to negative the output may not be monotonic when the inputs are transitioning between the two stages and the part is in a high gain configuration.

It should be remembered that swinging the inputs across the input stage transition may cause output distortion and accuracy anomalies. It is also worth noting that anytime any amps inputs are swung near the rails THD and other specs are sure to suffer.

### OUTPUT SECTION

#### *Current Rating*

The LM6588 has an output current rating, sinking or sourcing, of 200mA. The LM6588 is ideally suited to loads that require a high value of peak current but only a reduced value of average current. This condition is typical of driving the gate of a MOSFET. While the output drive rating is 200mA peak, and the output structure supports rail-to-rail operation, the attainable output current is reduced when the gain and drive conditions are such that the output voltage approaches either rail.

#### *Output Power*

Because of the increased output drive capability, internal heat dissipation must be held to a level that does not increase the junction temperature above its maximum rated value of 150° C.

#### *Power Requirements*

The LM6588 operates from a voltage supply, of $V^+$ and ground, or from a $V^-$ and $V^+$ split supply. Single-ended voltage range is +5V to +16V and split supply range is ±2.5V to ±8.0V.

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## APPLICATION HINTS
## POWER SUPPLIES

### *Sequencing*

Best practice design technique for operational amplifiers includes careful attention to power sequencing. Although the LM6588 is a bipolar op amp, recommended op amp turn on power sequencing of ground (or $V^-$), followed by $V^+$, followed by input signal should be observed. Turn off power sequence should be the reverse of the turn-on sequence. Depending on how the amp is biased the outputs may swing to the rails on power-on or power-off. Due to the high output currents and rail to rail output stage in the LM6588 the output may oscillate very slightly if the power is slowly raised between 2V and 4V The part is unconditionally stable at 5V. Quick turn-off and turn-on times will eliminate oscillation problems.

### *PSRR and Noise*

Care should be taken to minimize the noise in the power supply rails. The figure of merit for an op amp's ability to keep power supply noise out of the signal is called Power Supply Rejection Ratio (PSRR). Observe from the PSRR charts in the Typical Performance Characteristics section that the PSRR falls of dramatically as the frequency of the noise on the power supply line goes up. This is one of the reasons switching power supplies can cause problems. It should also be noticed from the charts that the negative supply pin is far more susceptible to power noise. The design engineer should determine the switching frequencies and ripple voltages of the power supplies in the system. If required, a series resistor or in the case of a high current op amp like the LM6588, a series inductor can be used to filter out the noise.

### *Transients*

In addition to the ripple and noise on the power supplies there are also transient voltage changes. This can be caused by another device on the same power supply suddenly drawing current or suddenly stopping a current draw. The design engineer should insure that there are no damaging transients induced on the power supply lines when the op amp suddenly changes current delivery.

## LAYOUT

### *Ground Planes*

Do not assume the ground (or more properly, the common or return) of the power supply is an ocean of zero impedance. The thinner the trace, the higher the resistance. Thin traces cause tiny inductances in the power lines. These can react against the large currents the LM6588 is capable of delivering to cause oscillations, instability, overshoot and distortion. A ground plane is the most effective way of insuring the ground is a uniform low impedance. If a four layer board cannot be used, consider pouring a plane on one side of a two layer board. If this cannot be done be sure to use as wide a trace as practicable and use extra decoupling capacitors to minimize the AC variations on the ground rail.

### *Decoupling*

A high-speed, high-current amp like the LM6588 must have generous decoupling capacitors. They should be as close to the power pins as possible. Putting them on the back side opposite the power pins may give the tightest layout. If ground and power planes are available, the placement of the decoupling caps are not as critical.

### *Breadboards*

The high currents and high frequencies the LM6588 operates at, as well as thermal considerations, require that prototyping of the design be done on a circuit board as opposed to a "Proto-Board" style breadboard.

## STABILITY

### *General:*

High speed parts with large output current capability require special care to insure lack of oscillations. Keep the "+" pin isolated from the output to insure stability. As noted above care should be take to insure the large output currents do not appear in the ground or ground plane and then get coupled into the "+" pin. As always, good tight layout is essential as is adequate use of decoupling capacitors on the power supplies.


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### *Unity Gain*

The unity gain or voltage-follower configuration is the most subject to oscillation. If a part is stable at unity gain it is almost certain to work in other configurations. In certain applications where the part is setting a reference voltage or is being used as a buffer greater stability can be achieved by configuring the part as a gain of −1 or −2 or +2.

### *Phase Margin*

The phase margin of an op amps gain-phase plot is an indication of the stability of the amp. It is desirable to have at least 45°C of phase margin to insure stability in all cases. The LM6588 has 60°C of phase margin even with it's large output currents and Rail-to-Rail output stage, which are generally more prone to stability issues.

### *Capacitive Load*

The LM6588 can withstand 30pF of capacitive load in a unity gain configuration before stability issues arise. At very large capacitances, the load capacitor will attenuate the gain like any other heavy load and the part becomes stable again. The LM6588 will be stable at 330nF and higher load capacitance. Refer to the chart in the Typical Performance Characteristics section.

### OUTPUT

### *Swing vs. Current*

The LM6588 will get to about 25mV or 30mV of either rail when there is no load. The LM6588 can sink or source hundreds of milliamperes while remaining less then 0.5V away from the rail. It should be noted that if the outputs are driven to the rail and the part can no longer maintain the feedback loop, the internal circuitry will deliver large base currents into the huge output transistors, trying to get the outputs to get past the saturation voltage. The base currents will approach 16 milliamperes and this will appear as an increase in power supply current. Operating at this power dissipation level for extended periods will damage the part, especially in the higher thermal resistance TSSOP package. Because of this phenomenon, unused parts should not have the inputs strapped to either rail, but should have the inputs biased at the midpoint or at least a diode drop (0.6V) within the rails.

### *Self Heating*

As discussed above the LM6588 is capable of significant power by virtue of its 200mA current handling capability. A TSSOP package cannot sustain these power levels for more then a brief period.

## TFT Display Application

### INTRODUCTION

In today's high-resolution TFT displays, op amps are used for the following three functions:

1. $V_{COM}$ Driver
2. Gamma Buffer
3. Panel Repair Buffer

All of these functions utilize op amps as non-inverting, unity-gain buffers. The $V_{COM}$ Driver and Gamma Buffer are buffers that supply a well regulated DC voltage. A Panel Repair Buffer, on the other hand, provides a high frequency signal that contains part of the display's visual image.

In an effort to reduce production costs, display manufacturers use a minimum variety of different parts in their TFT displays. As a result, the same type of op amp will be used for the $V_{COM}$ Driver, Gamma Buffer, and Panel Repair Buffer. To perform all these functions, such an op amp must have the following characteristics:

1. Large output current drive
2. Rail to rail input common mode range
3. Rail to rail output swing
4. Medium speed gain bandwidth and slew rate

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The LM6588 meets these requirements. It has a rail-to-rail input and output, typical gain bandwidth and slew rate of 15MHz and 15V/µs, and it can supply up to 200mA of output current. The following sections will describe the operation of $V_{COM}$ Drivers, Gamma Buffers, and Panel Repair Buffers, showing how the LM6588 is well suited for each of these functions.

## BRIEF OVERVIEW OF TFT DISPLAY

To better understand these op amp applications, let's first review a few basic concepts of how a TFT display operates. Figure 25 is a simplified illustration of an LCD pixel. The top and bottom plates of each pixel consist of Indium-Tin oxide (ITO), which is a transparent, electrically conductive material. ITO lies on the inner surfaces of two glass substrates that are the front and back glass panels of a TFT display. Sandwiched between the two ITO plates is an insulating material (liquid crystal) that alters the polarization of light to a lesser a greater amount, depending on how much voltage ($V_{PIXEL}$) is applied across the two plates. Polarizers are placed on the outer surfaces of the two glass substrates, which in combination with the liquid crystal create a variable light filter that modulates light transmitted from the back to the front of a display. A pixel's bottom plate lies on the backside of a display where a light source is applied, and the top plate lies on the front, facing the viewer. On a Twisted Neumatic (TN) display, which is typical of most TFT displays, a pixel transmits the greatest amount of light when $V_{PIXEL}$ is less ±0.5V, and it becomes less transparent as this voltage increases with either a positive or negative polarity. In short, an LCD pixel can be thought of as a capacitor, through which, a controlled amount of light is transmitted by varying $V_{PIXEL}$.

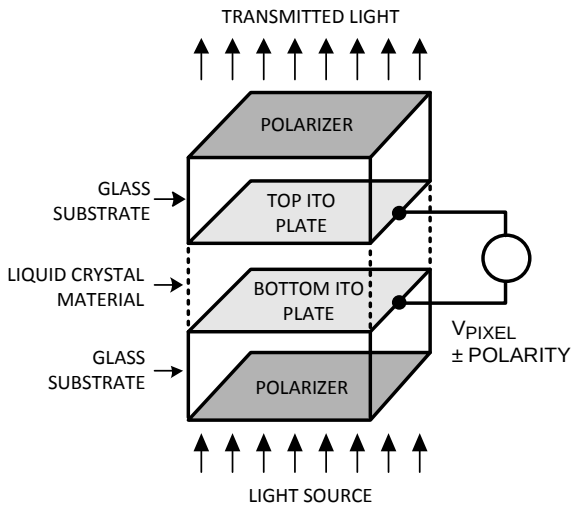


**Figure 25. Individual LCD Pixel**


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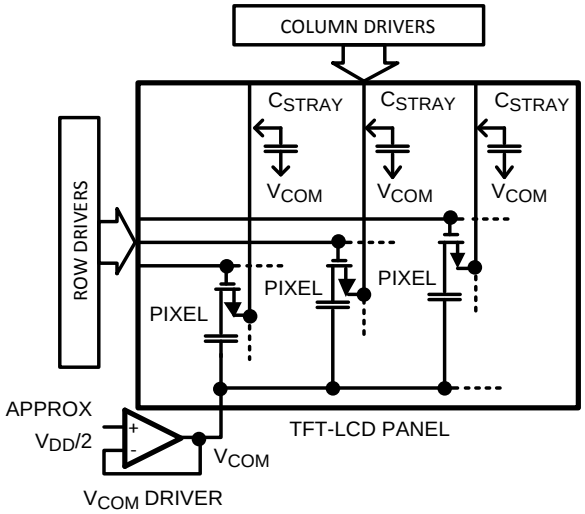


**Figure 26. TFT Display**

Figure 26 is a simplified block diagram of a TFT display, showing how individual pixels are connected to the row, column, and $V_{COM}$ lines. Each pixel is represented by capacitor with an NMOS transistor connected to its top plate. Pixels in a TFT panel are arranged in rows and columns. Row lines are connected to the NMOS gates, and column lines to the NMOS sources. The back plate of every pixel is connected to a common voltage called $V_{COM}$. Pixel brightness is controlled by voltage applied to the top plates, and the Column Drivers supply this voltage via the column lines. Column Drivers 'write' this voltage to the pixels one row at a time, and this is accomplished by having the Row Drivers select an individual row of pixels when their voltage levels are transmitted by the Column Drivers. The Row Drivers sequentially apply a large positive pulse (typically 25V to 35V) to each row line. This turns-on NMOS transistors connected to an individual row, allowing voltages from the column lines to be transmitted to the pixels.

### $V_{COM}$ DRIVER

The $V_{COM}$ driver supplies a common voltage ($V_{COM}$) to all the pixels in a TFT panel. $V_{COM}$ is a constant DC voltage that lies in the middle of the column drivers' output voltage range. As a result, when the column drivers write to a row of pixels, they apply voltages that are either positive or negative with respect to $V_{COM}$. In fact, the polarity of a pixel is reversed each time its row is selected. This allows the column drivers to apply an alternating voltage to the pixels rather than a DC signal, which can 'burn' a pattern into an LCD display.

When column drivers write to the pixels, current pulses are injected onto the $V_{COM}$ line. These pulses result from charging stray capacitance between $V_{COM}$ and the column lines (see Figure 26), which ranges typically from 16pF to 33pF per column. Pixel capacitance contributes very little to these pulses because only one pixel at a time is connected to a column, and the capacitance of a single pixel is on the order of only 0.5pF. Each column line has a significant amount of series resistance (typically 2kΩ to 40kΩ), so the stray capacitance is distributed along the entire length of a column. This can be modeled by the multi-segment RC network shown in Figure 27. The total capacitance between $V_{COM}$ and the column lines can range from 25nF to 100nF, and charging this capacitance can result in positive or negative current pulses of 100mA, or more. In addition, a similar distributed capacitance of approximately the same value exists between $V_{COM}$ and the row lines. Therefore, the $V_{COM}$ driver's load is the sum of these distributed RC networks with a total capacitance of 50nF to 200nF, and this load can modeled like the circuit in Figure 27.

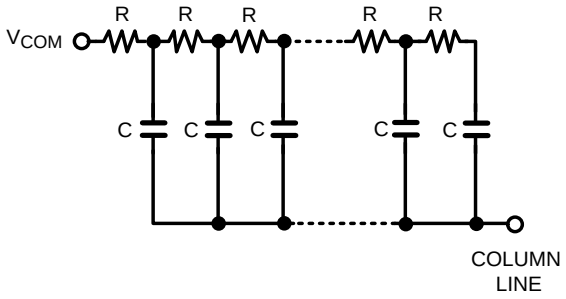


**Figure 27. Model of Impedance between $V_{COM}$ and Column Lines**

A $V_{COM}$ driver is essentially a voltage regulator that can source and sink current into a large capacitive load. To simplify the analysis of this driver, the distributed RC network of Figure 27 has been reduced to a single RC load in Figure 28. This load places a large capacitance on the $V_{COM}$ driver output, resulting in an additional pole in the op amp's feedback loop. However, the op amp remains stable because $C_{LOAD}$ and $R_{ESR}$ create a zero that cancels the effect of this pole. The range of $C_{LOAD}$ is 50nF to 200nF and $R_{ESR}$ is 20Ω to 100Ω, so this zero will have a frequency in the range of 8KHz to 160KHz, which is much lower than the gain bandwidth of most op amps. As a result, the $V_{COM}$ load adds very little phase lag when op amp loop gain is unity, and this allows the $V_{COM}$ Driver to remain stable. This was verified by measuring the small-signal bandwidth of the LM6588 with the RC load of Figure 28. When driving an RC load of 50nF and 20Ω, the LM6588 has a unity gain frequency of 6.12MHz with 41.5°C of phase margin. If the load capacitor is increased to 200nF and the resistance remains 20Ω, the unity gain frequency is virtually unchanged: 6.05MHz with 42.9°C of phase margin.

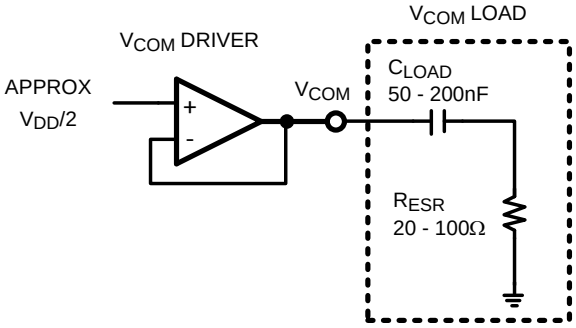


**Figure 28. $V_{COM}$ Driver with Simplified Load**

A $V_{COM}$ Driver's large-signal response time is determined by the op amp's maximum output current, not by its slew rate. This is easily shown by calculating how much output current is required to slew a 50nF load capacitance at the LM6588 slew rate of 14V/µs:

$$I_{OUT} = 14V/\mu s \times 50nF = 700mA \quad (1)$$

700mA exceeds the maximum current specification for the LM6588 and almost all other op amps, confirming that a $V_{COM}$ driver's speed is limited by its peak output current. In order to minimize $V_{COM}$ transients, the op amp used as a $V_{COM}$ Driver must supply large values of output current.


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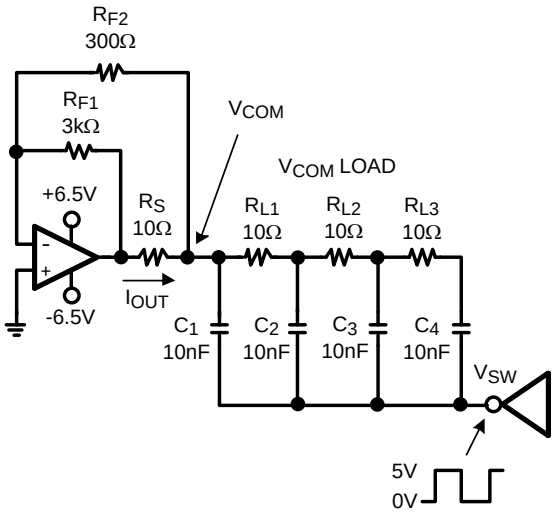


**Figure 29. $V_{COM}$ Driver Test Circuit**

Figure 29 is a common test circuit used for measuring $V_{COM}$ driver response time. The RC network of $R_{L1}$ to $R_{L3}$ and $C_1$ to $C_4$ models the distributed RC load of a $V_{COM}$ line. This RC network is a gross simplification of what the actual impedance is on a TFT panel. However, it does provide a useful test for measuring the op amp's transient response when driving a large capacitive load. A low impedance MOSFET driver applies a 5V square wave to $V_{SW}$, generating large current pulses in the RC network. Scope photos from this circuit are shown in Figure 30 and Figure 31. Figure 30 shows the test circuit generates positive and negative voltage spikes with an amplitude of ±3.2V at the $V_{COM}$ node, and both transients settle-out in approximately 2µs. As mentioned before, the speed at which these transients settle-out is a function of the op amp's peak output current. The $I_{OUT}$ trace in Figure 31 shows that the LM6588 can sink and source peak currents of −200mA and 200mA. This ability to supply large values of output current makes the LM6588 extremely well suited for $V_{COM}$ Driver applications.

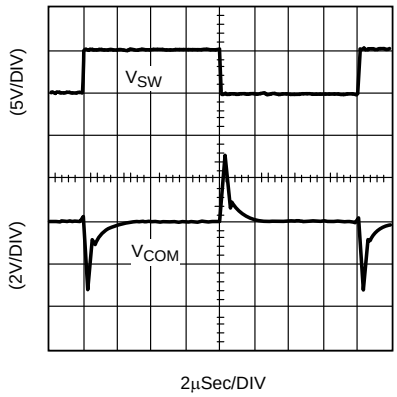


**Figure 30. $V_{SW}$ and $V_{COM}$ Waveforms from $V_{COM}$**

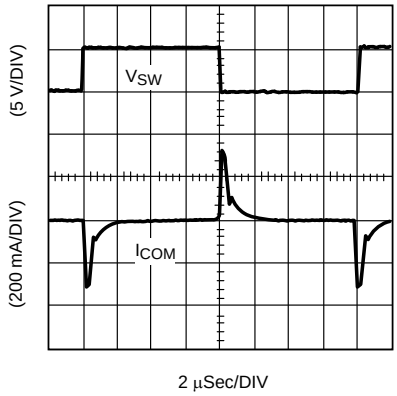


**Figure 31. $V_{SW}$ and $I_{OUT}$ Waveforms from $V_{COM}$ Test Circuit**

## GAMMA BUFFER

Illumination in a TFT display, also referred to as grayscale, is set by a series of discrete voltage levels that are applied to each LCD pixel. These voltage levels are generated by resistive DAC networks that reside inside each of the column driver ICs. For example, a column driver with 64 Grayscale levels has a two 6 bit resistive DACs. Typically, the two DACs will have their 64 resistors grouped into four segments, as shown in Figure 32. Each of these segments is connected to external voltage lines, VGMA1 to VGMA10, which are the Gamma Levels. VGMA1 to VGMA5 set grayscale voltage levels that are positive with respect to $V_{COM}$ (high polarity gamma levels). VGMA6 to VGMA10 set grayscale voltages negative with respect to $V_{COM}$ (low polarity gamma levels).

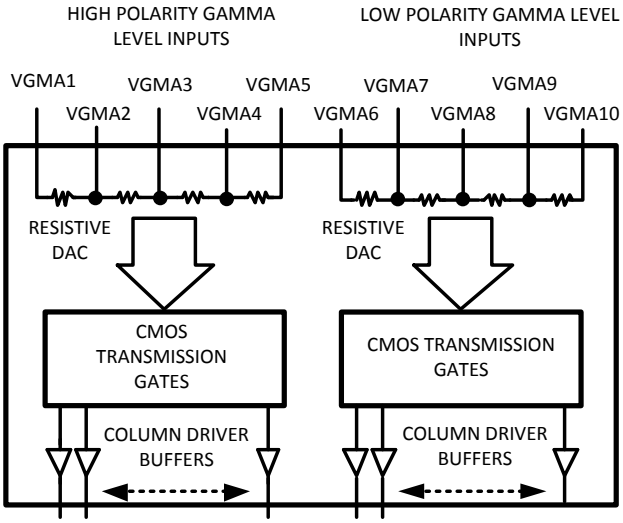


**Figure 32. Simplified Schematic of Column Driver IC**


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Figure 33 shows how column drivers in a TFT display are connected to the gamma levels. VGMA1, VGMA5, VGMA6, and VGMA10 are driven by the Gamma Buffers. These buffers serve as low impedance voltage sources that generate the display's gamma levels. The Gamma Buffers' outputs are set by a simple resistive ladder, as shown in Figure 33. Note that VGMA2 to VGMA4 and VGMA7 to VGMA9 are usually connected to the column drivers even though they are not driven by external buffers. Doing so, forces the gamma levels in all the column drivers to be identical, minimizing grayscale mismatch between column drivers. Referring again to Figure 33, the resistive load of a column driver DAC (i.e. resistance between GMA1 to GMA5) is typically 10kΩ to 15kΩ. On a typical display such as XGA, there can be up to 10 column drivers, so the total resistive load on a Gamma Buffer output can be as low as 1kΩ. The voltage between VGMA1 and VGMA5 can range from 3V to 6V, depending on the type of TFT panel. Therefore, maximum load current supplied by a Gamma Buffer is approximately 6V/1kΩ = 6mA, which is a relatively light load for most op amps. In many displays, VGMA1 can be less than 500mV below $V_{DD}$, and VGMA10 can be less than 500mV above ground. Under these conditions, an op amp used for the Gamma Buffer must have rail-to-rail inputs and outputs, like the LM6588.

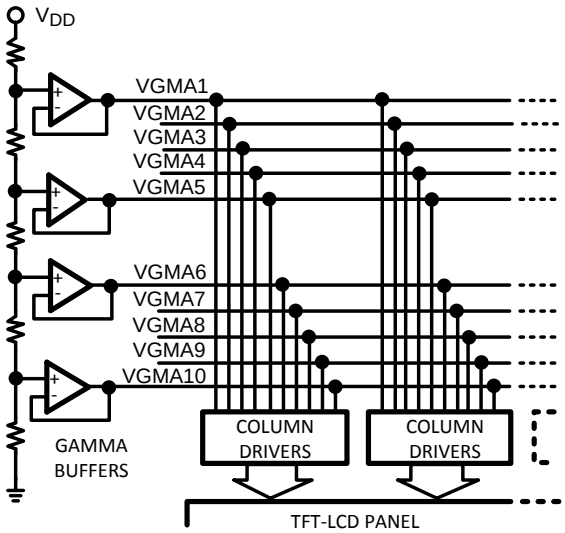


**Figure 33. Basic Gamma Buffer Configuration**

Another important specification for Gamma Buffers is small signal bandwidth and slew rate. When column drivers select which voltage levels are written to a row of pixels, their internal DACs inject current spikes into the Gamma Lines. This generates voltage transients at the Gamma Buffer outputs, and they should settle-out in less than 1µs to insure a steady output voltage from the column drivers. Typically, these transients have a maximum amplitude of 2V, so a gamma buffer must have sufficient bandwidth and slew rate to recover from a 2V transient in 1µs or less.

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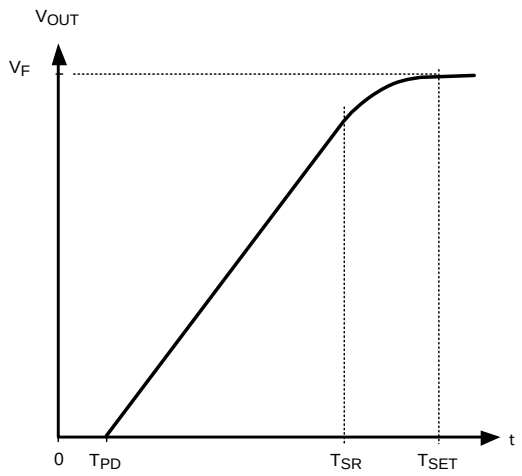


**Figure 34. Large Signal Transient Response of an Operational Amplifier**

Figure 34 illustrates how an op amp responds to a large-signal transient. When such a transient occurs at t = 0, the output does not start changing until $T_{PD}$, which is the op amp's propagation delay time (typically 20ns for the LM6588). The output then changes at the op amp's slew rate from t = $T_{PD}$ to $T_{SR}$. From t = $T_{SR}$ to $T_{SE}$T, the output settles to its final value ($V_F$) at a speed determined by the op amp's small-signal frequency response. Although propagation delay and slew limited response time (t = 0 to $T_{SR}$) can be calculated from data sheet specifications, the small signal settling time ($T_{SR}$ to $T_{SET}$) cannot. This is because an op amp's gain vs. frequency has multiple poles, and as a result, small-signal settling time can not be calculated as a simple function of the op amp's gain bandwidth. Therefore, the only accurate method for determining op amp settling time is to measure it directly.

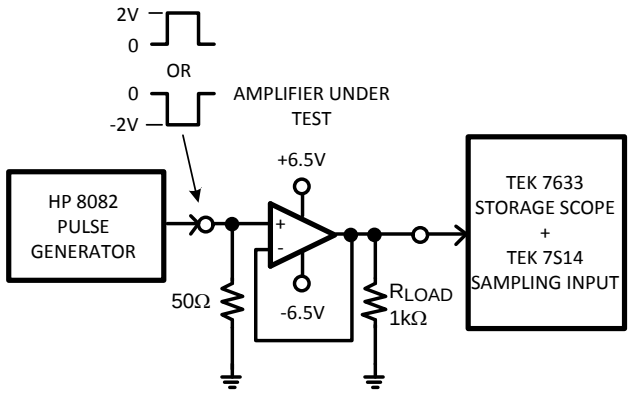


**Figure 35. Gamma Buffer Settling Time Test Circuit**

The test circuit in Figure 35 was used to measure LM6588 settling time for a 2V pulse and 1kΩ load, which represents the maximum transient amplitude and output load for a gamma buffer. With this test system, the LM6588 settled to within ±30mV of 2V pulse in approximately 170ns. Settling time for a 0 to –2V pulse was slightly less, 150ns. These values are much smaller than the desired response time of 1µs, so the LM6588 has sufficient bandwidth and slew rate for regulating gamma line transients.

## PANEL REPAIR BUFFER

It is not uncommon for a TFT panel to be manufactured with an open in one or two of its column or row lines. In order to repair these opens, TFT panels have uncommitted repair lines that run along their periphery. When an open line is identified during a panel's final assembly, a repair line re-routes its signal past the open. Figure 36 illustrates how a column is repaired. The column driver's output is sent to the other end of an open column via a repair line, and the repair line is driven by a panel repair buffer. When a column or row line is repaired, the

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capacitance on that line increases substantially. For instance, a column typically has 50pF to 100pF of line capacitance, but a repaired column can have up to 200pF. Column drivers are not designed to drive this extra capacitance, so a panel repair buffer provides additional output current to the repaired column line. Note that there is typically a 20Ω to 100Ω resistor in series with the buffer output. This resistor isolates the output from the 200pF of capacitance on a repaired column line, ensuring that the buffer remains stable. A pole is created by this resistor and capacitance, but its frequency will be in the range of 8MHz to 40MHz, so it will have only a minor effect on the buffer's transient response time. Panel repair buffers transmit a column driver signal, and as mentioned in the gamma buffer section, this signal is set by the gamma levels. It was also mentioned that many displays have upper and lower gamma levels that are within 500mV of the supply rails. Therefore, op amps used as panel repair buffers should have rail-to-rail input and stages. Otherwise, they may clip the column driver signal.

The signal from a panel repair buffer is stored by a pixel when the pixel's row is selected. In high-resolution displays, each row is selected for as little as 11µs. To insure that a pixel has adequate time to settle-out during this brief period, a panel repair buffer should settle to within 1% of its final value approximately 1µs after a row is selected. This is hardest to achieve when transmitting a column line's maximum voltage swing, which is the difference between the upper and lower gamma levels (i.e. voltage between VGMA1 and VGMA10). For a LM6588, the most demanding application occurs in displays that operate from a 16V supply. In these displays, voltage difference between the top and bottom gamma levels can be as large as 15V, so the LM6588 needs to transmit a ±15V pulse and settle to within 60mV of its final value in approximately 1µs (60mV is approximately 1% of the dynamic range of the high or low polarity gamma levels). LM6588 settling times for 15V and –15V pulses were measured in a test circuit similar to the one in Figure 35. $V^+$ and $V^-$ were set to 15.5V and –0.5V, respectively, when measuring settling time for a 0V to 15V pulse. Likewise, $V^+$ and $V^-$ were set to 0.5V and –15.5V when measuring settling time for a 0V to –15V pulse. In both cases, the LM6588 output was connected to a series RC load of 51Ω and 200pF. When tested this way, the LM6588 settled to within 60mV of 15V or –15V in approximately 1.1µs. These observed values are very close to the desired 1µs specification, demonstrating that the LM6588 has the bandwidth and slew rate required for repair buffers in high-resolution TFT displays.

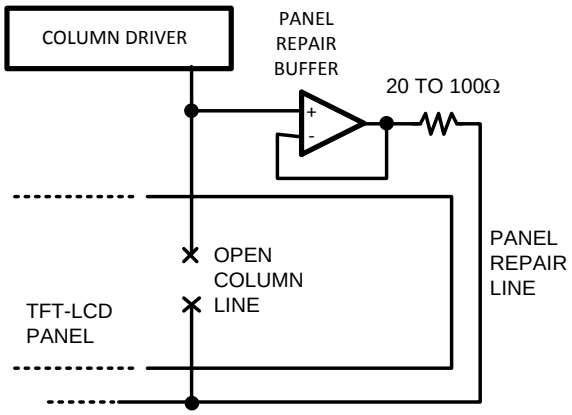


**Figure 36. Panel Repair Buffer**

## SUMMARY

This application note provided a basic explanation of how op amps are used in TFT displays, and it also presented the specifications required for these op amps. There are three major op amp applications in a display: $V_{COM}$ Driver, Gamma Buffer, and Panel Repair Buffer, and the LM6588 can be used for all of them. As a $V_{COM}$ Driver, the LM6588 can supply large values of output current to regulate $V_{COM}$ load transients. It has rail-to-rail input common-mode range and output swing required for gamma buffers and panel repair buffers. It also has the necessary gain bandwidth and slew-rate for regulating gamma levels and driving column repair lines. All these features make the LM6588 very well suited for use in TFT displays.

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## REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 21 |


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM6588MA/NOPB | NRND | Production | SOIC (D) \| 14 | 55 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6588MA |
| LM6588MA/NOPB.A | NRND | Production | SOIC (D) \| 14 | 55 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6588MA |
| LM6588MAX/NOPB | NRND | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6588MA |
| LM6588MAX/NOPB.A | NRND | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6588MA |
| LM6588MT/NOPB | NRND | Production | TSSOP (PW) \| 14 | 94 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM658 8MT |
| LM6588MT/NOPB.A | NRND | Production | TSSOP (PW) \| 14 | 94 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM658 8MT |
| LM6588MTX/NOPB | NRND | Production | TSSOP (PW) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM658 8MT |
| LM6588MTX/NOPB.A | NRND | Production | TSSOP (PW) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM658 8MT |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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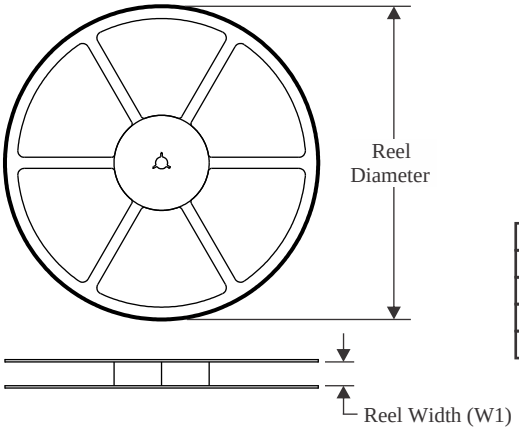
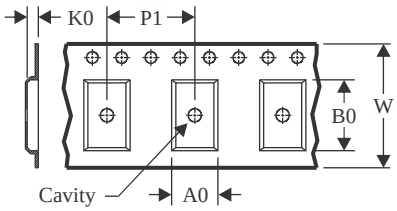
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

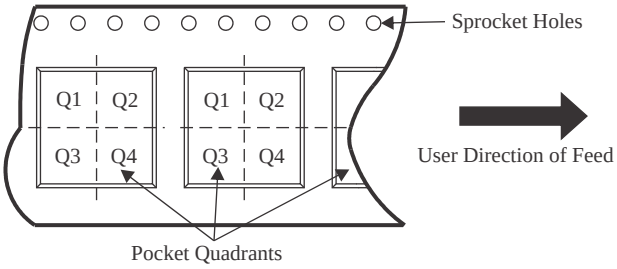



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

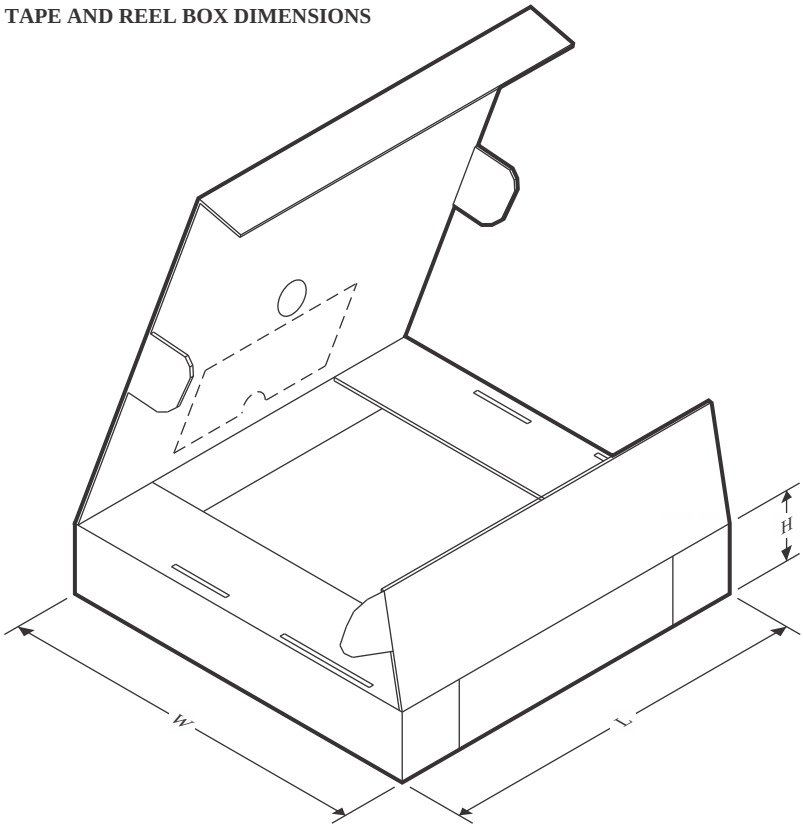
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM6588MAX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LM6588MTX/NOPB | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

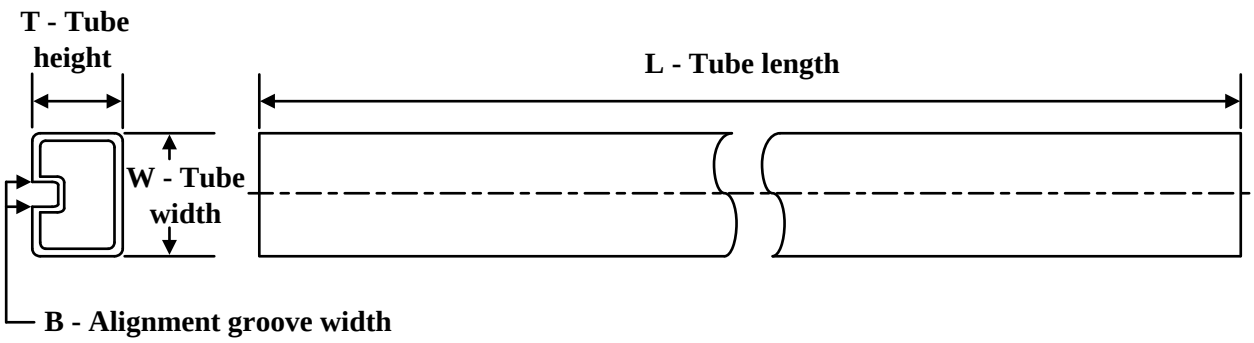
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

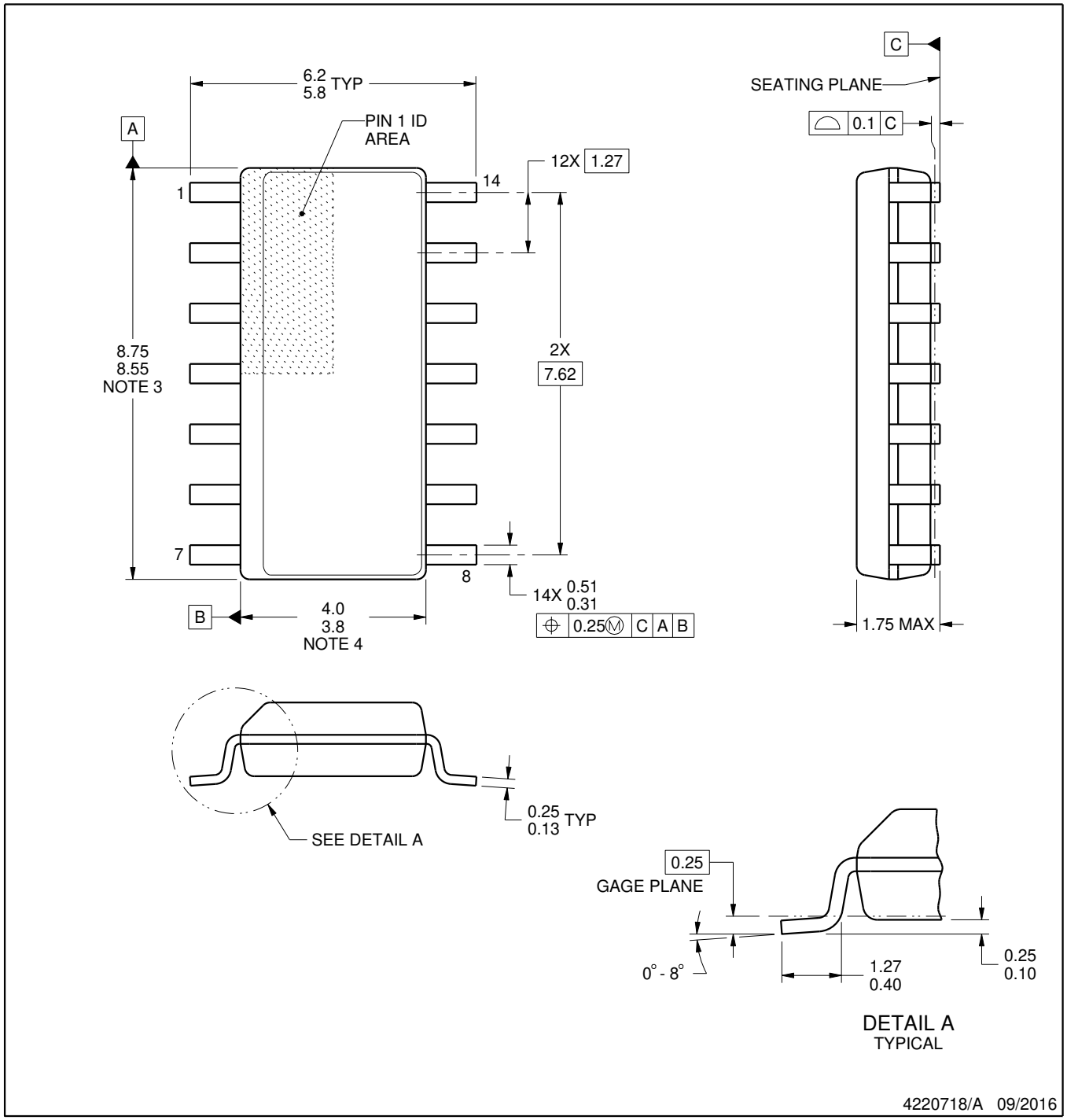
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM6588MAX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6588MTX/NOPB | TSSOP | PW | 14 | 2500 | 367.0 | 367.0 | 35.0 |

## TUBE



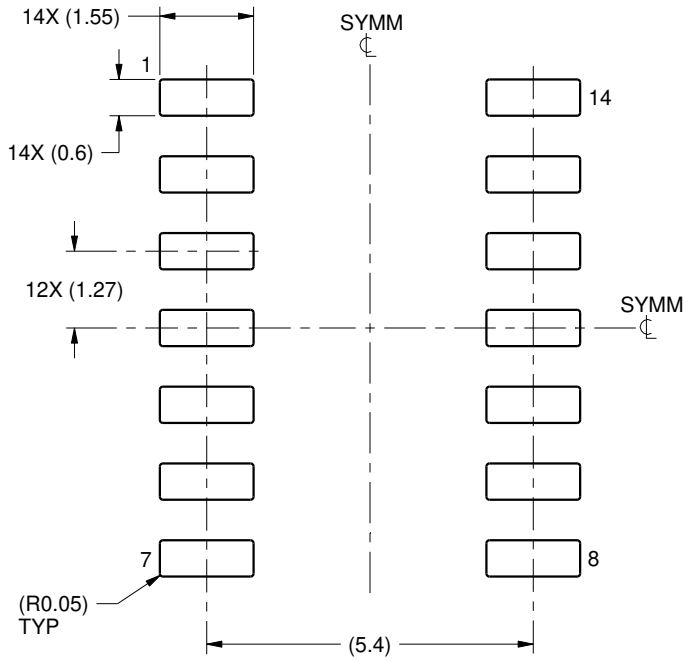

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM6588MA/NOPB | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LM6588MA/NOPB.A | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LM6588MT/NOPB | PW | TSSOP | 14 | 94 | 495 | 8 | 2514.6 | 4.06 |
| LM6588MT/NOPB.A | PW | TSSOP | 14 | 94 | 495 | 8 | 2514.6 | 4.06 |

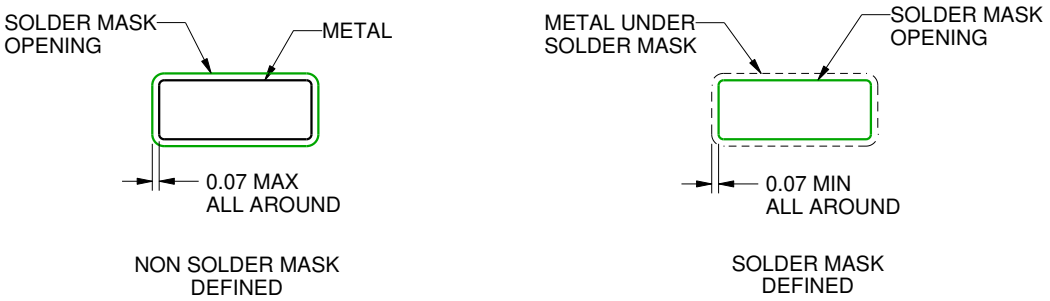



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X

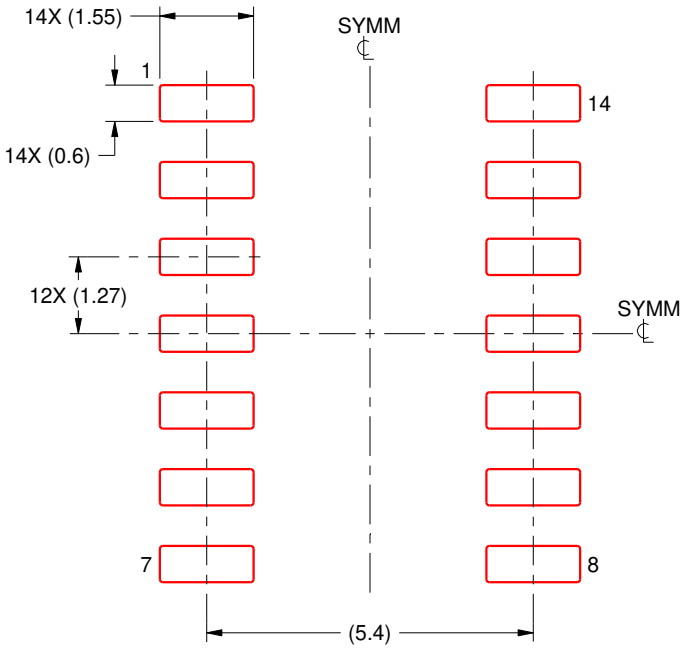



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

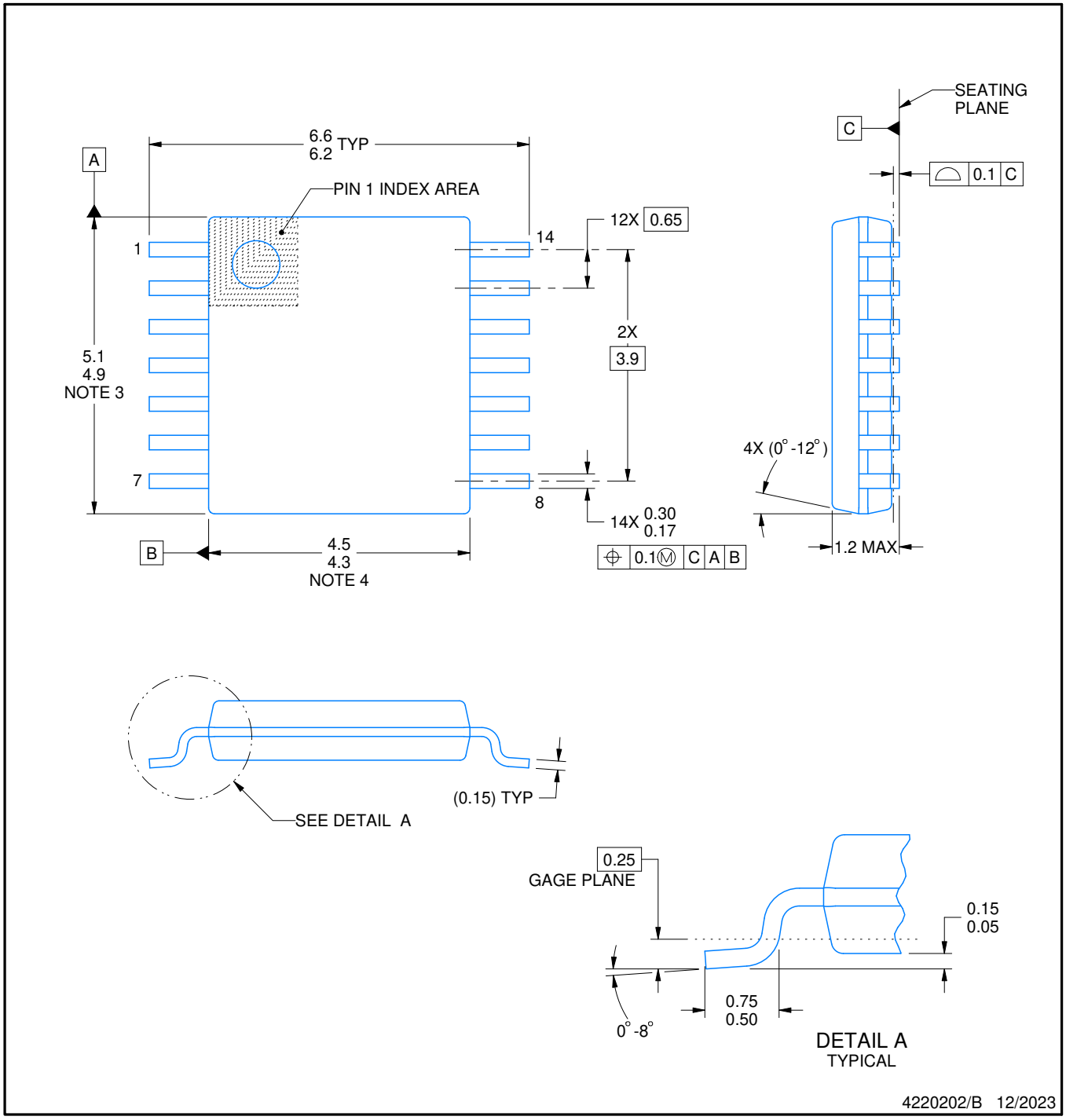



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

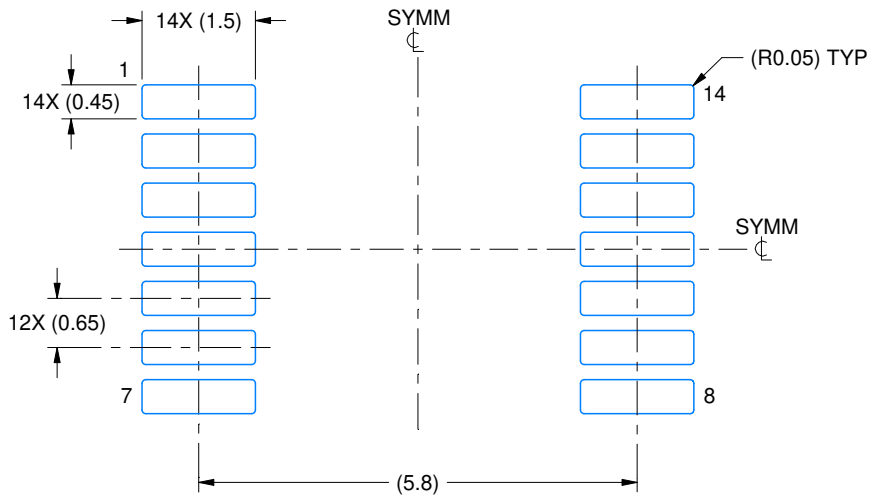
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

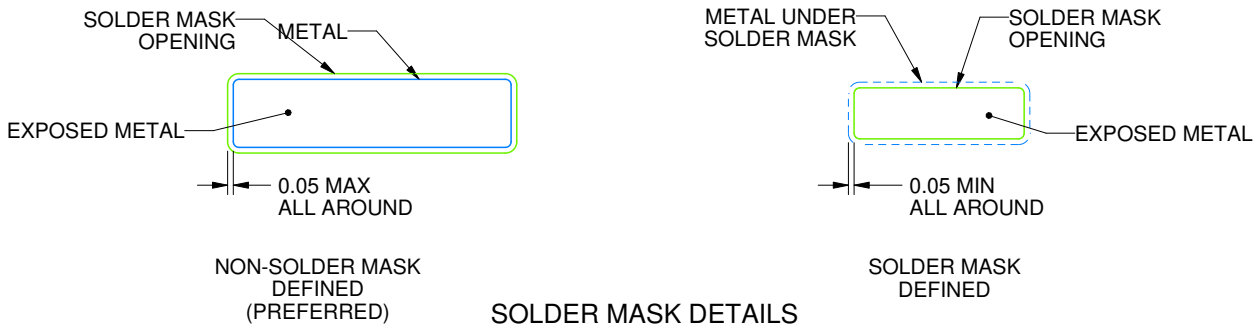



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

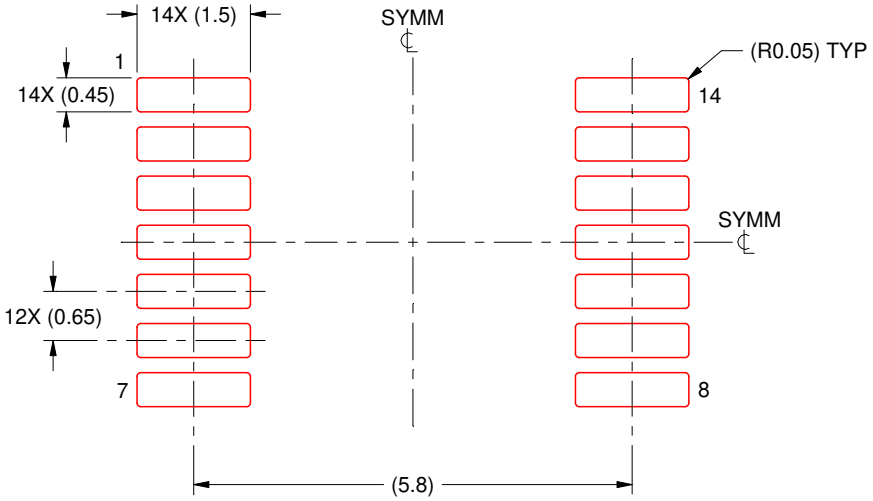



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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