LM96000 Hardware Monitor with Integrated Fan Control

Check for Samples: LM96000

FEATURES

- **2-wire, SMBus 2.0 Compliant, Serial Digital Interface**
- **8-bit ΣΔ ADC**
- **Monitors VCCP, 2.5V, 3.3 VSBY, 5.0V, and 12V Motherboard/processor Supplies**
- **Monitors 2 Remote Thermal Diodes**
- **Programmable Autonomous Fan Control Based on Temperature Readings**
- **Noise Filtering of Temperature Reading for Fan Control**
- **1.0°C Digital Temperature Sensor Resolution**
- **3 PWM Fan Speed Control Outputs**
- **Provides High and Low PWM Frequency Ranges**
- **4 Fan Tachometer Inputs**
- **Monitors 5 VID Control Lines**
- **24-pin TSSOP Package**
- **XOR-tree Test Mode**

APPLICATIONS

- **Desktop PC**
- **Microprocessor based equipment**
  - **(e.g. Base-stations, Routers, ATMs, Point of Sales)**

KEY SPECIFICATIONS

- **Voltage Measurement Accuracy ±2% FS (max)**
- **Resolution 8-bits, 1°C**
- **Temperature Sensor Accuracy ±3°C (max)**
- **Temperature Range**
  - **LM96000 Operational 0°C to +85°C**
  - **Remote Temp Accuracy 0°C to +125°C**
- **Power Supply Voltage +3.0V to +3.6V**
- **Power Supply Current 0.53 mA**

DESCRIPTION

The LM96000, hardware monitor, has a two wire digital interface compatible with SMBus 2.0. Using an 8-bit ΣΔ ADC, the LM96000 measures:

- the temperature of two remote diode connected transistors as well as its own die
- the VCCP, 2.5V, 3.3VSBY, 5.0V, and 12V supplies (internal scaling resistors).

To set fan speed, the LM96000 has three PWM outputs that are each controlled by one of three temperature zones. High and low PWM frequency ranges are supported. The LM96000 includes a digital filter that can be invoked to smooth temperature readings for better control of fan speed. The LM96000 has four tachometer inputs to measure fan speed. Limit and status registers for all measured values are included.

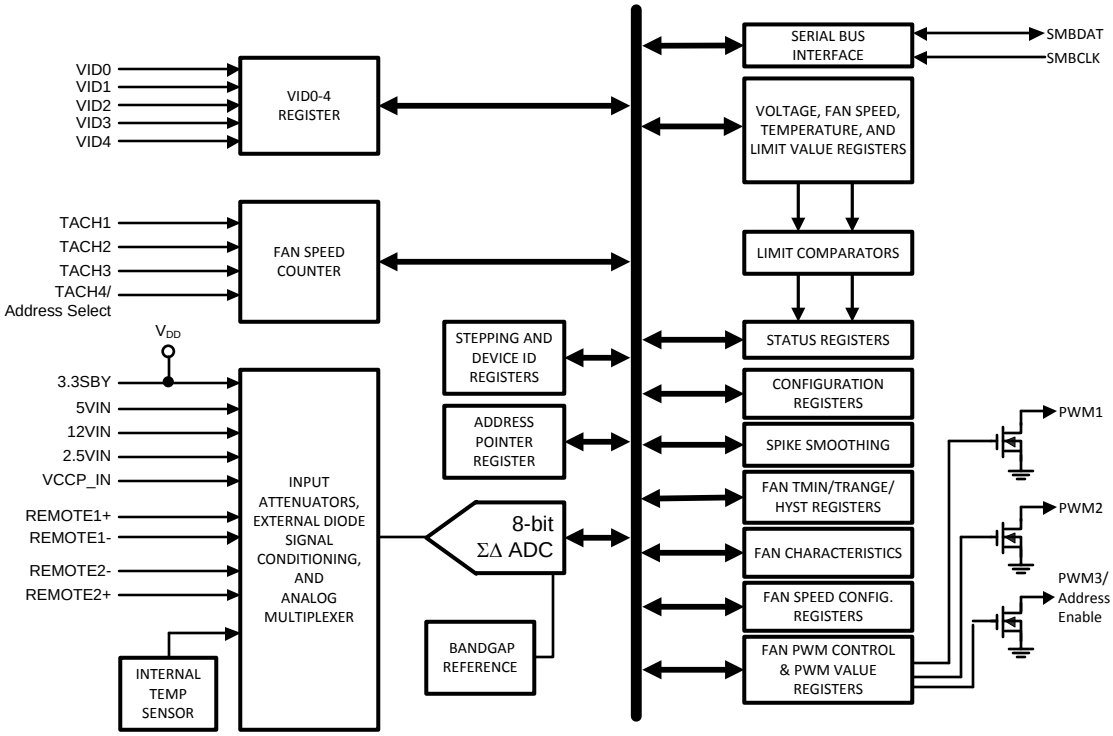
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Block Diagram



Connection Diagram

Top View

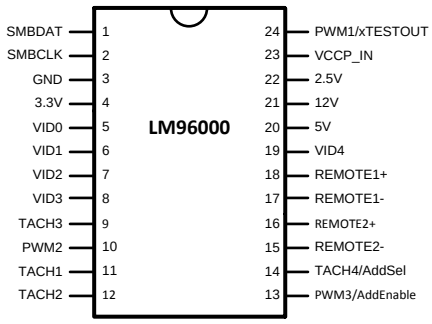


Figure 1. 24-Pin TSSOP Package

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Pin Descriptions

	Name	Pin No.	Type	Name and Function/Connection
SMBus	SMBDAT	1	Digital I/O (Open-Drain)	System Management Bus Data. Open-drain output. 5V tolerant, SMBus 2.0 compliant.
	SMBCLK	2	Digital Input	System Management Bus Clock. Tied to Open-drain output. 5V tolerant, SMBus 2.0 compliant.
Processor VID Lines	VID0	5	Digital Input	Voltage identification signal from the processor. This value is read in the VID0–VID4 Status Register.
	VID1	6	Digital Input	Voltage identification signal from the processor. This value is read in the VID0–VID4 Status Register.
	VID2	7	Digital Input	Voltage identification signal from the processor. This value is read in the VID0–VID4 Status Register.
	VID3	8	Digital Input	Voltage identification signal from the processor. This value is read in the VID0–VID4 Status Register.
	VID4	19	Digital Input	Voltage identification signal from the processor. This value is read in the VID0–VID4 Status Register.
Power	3.3V	4	POWER	+3.3V pin. Can be powered by +3.3V Standby power if monitoring in low power states is required. This pin also serves as the analog input to monitor the 3.3V supply. This pin should be bypassed with a 0.1µf capacitor in parallel with 100pf. A bulk capacitance of approximately 10µf needs to be in the near vicinity of the LM96000.
	GND	3	GROUND	Ground for all analog and digital circuitry.
Voltage Inputs	5V	20	Analog Input	Analog input for +5V monitoring.
	12V	21	Analog Input	Analog input for +12V monitoring.
	2.5V	22	Analog Input	Analog input for +2.5V monitoring.
	VCCP_IN	23	Analog Input	Analog input for VCCP (processor voltage) monitoring.
Remote Diodes	Remote1+	18	Remote Thermal Diode Positive Input	Positive input (current source) from the first remote thermal diode. Serves as the positive input into the A/D. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor.
	Remote1−	17	Remote Thermal Diode Negative Input	Negative input (current sink) from the first remote thermal diode. Serves as the negative input into the A/D. Connected to THERMDC pin of Pentium processor or the emmiter of a diode connected MMBT3904 NPN transistor.
	Remote2+	16	Remote Thermal Diode Positive Output	Positive input (current source) from the first remote thermal diode. Serves as the positive input into the A/D. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor.
	Remote2−	15	Remote Thermal Diode Negative Input	Negative input (current sink) from the first remote thermal diode. Serves as the negative input into the A/D. Connected to THERMDC pin of Pentium processor or the emmiter of a diode connected MMBT3904 NPN transistor.
Fan Tachometer Inputs	TACH1	11	Digital Input	Input for monitoring tachometer output of fan 1.
	TACH2	12	Digital Input	Input for monitoring tachometer output of fan 2.
	TACH3	9	Digital Input	Input for monitoring tachometer output of fan 3.
	TACH4/Address Select	14	Digital Input	Input for monitoring tachometer output of fan 4. If in Address Select Mode, determines the SMBus address of the LM96000.
Fan Control	PWM1/xTest Out	24	Digital Open-Drain Output	Fan speed control 1. When in XOR tree test mode, functions as XOR Tree output.
	PWM2	10	Digital Open-Drain Output	Fan speed control 2.
	PWM3/$\overline{\text{Address Enable}}$	13	Digital Open-Drain Output	Fan speed control 3. Pull to ground at power on to enable Address Select Mode (Address Select pin controls SMBus address of the device).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1) (2) (3)

Supply Voltage, V+		−0.5V to 6.0V
Voltage on Any Digital Input or Output Pin		−0.5V to 6.0V
Voltage on 12V Analog Input		−0.5V to 16V
Voltage on 5V Analog Input		−0.5V to 6.66V
Voltage on Remote1+, Remote2+,		−0.5V to (V+ + 0.05V)
Current on Remote1−, Remote2−		±1 mA
Voltage on Other Analog Inputs		−0.5V to 6.0V
Input Current on Any Pin (4)		±5 mA
Package Input Current (4)		±20 mA
Package Dissipation at T_A = 25°C		See (5)
ESD Susceptibility (6)	Human Body Model	2500V
	Machine Model	250V
Storage Temperature		−65°C to +150°C
Soldering process must comply with reflow temperature profile specifications. See www.ti.com/packaging (7)		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise noted.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} >V+), the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to four. Parasitic components and/or ESD protection circuitry are shown below for the LM96000's pins. The nominal breakdown voltage the zener is 6.5V. Care should be taken not to forward bias the parasitic diode D1 present on pins D+ and D−. Doing so by more that 50 mV may corrupt temperature measurements. SNP stands for snap-back device.
(5) Thermal resistance junction-to-ambient when attached to a double-sided printed circuit board with 1 oz. foil is 113 °C/W.
(6) Human body model, 100pF discharged through a 1.5kΩ resistor. Machine model, 200pF discharged directly into each pin.
(7) Reflow temperature profiles are different for packages containing lead (Pb) than for those that do not.

Operating Ratings (1) (2)

LM96000 Operating Temperature Range	0°C ≤ T_A ≤ +85°C
Remote Diode Temperature Range	0°C ≤ T_D ≤ +125°C
Supply Voltage (3.3V nominal)	+3.0V to +3.6V
V_{IN} Voltage Range	
+12V V_{IN}	−0.05V to 16V
+5V V_{IN}	−0.05V to 6.66V
+3.3V V_{IN}	3.0V to 4.4V
VCCP_IN and All Other Inputs	−0.05V to (V+ + 0.05V)
VID0–VID4	−0.05V to 5.5V
Typical Supply Current	0.53 mA

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise noted.

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DC Electrical Characteristics

The following specifications apply for V+ = 3.0V to 3.6V, and all analog input source impedance R_S = 50Ω unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} =0°C to T_{MAX}=85°C;** all other limits $T_A = T_J$= 25°C. T_A is the ambient temperature of the LM96000; T_J is the junction temperature of the LM96000; T_D is the thermal diode junction temperature.

Parameter		Test Conditions	Typical (1)	Limits (2)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
	Supply Current (3)	Converting, Interface and Fans Inactive, Peak Current	1.8	**3.5**	mA (max)
		Converting, Interface and Fans Inactive, Average Current	0.53		mA
	Power-On Reset Threshold Voltage			**1.6**	V (min)
				2.8	V (max)
TEMPERATURE TO DIGITAL CONVERTER CHARACTERISTICS					
	Resolution		1 8		°C Bits
	Temperature Accuracy (See (4) for Thermal Diode Processor Type)	T_D=25°C		±2.5	°C (max)
		T_D=0°C to 100°C	±1	**±3**	°C (max)
		T_D=100°C to 125°C		**±4**	°C (max)
	Temperature Accuracy using Internal Diode. (5) See (6) for the thermal resistance to be used in the self-heating calculation.		±1	**±3**	°C (max)
I_{DS}	External Diode Current Source	High Level	188	280	µA (max)
		Low Level	11.75		µA
	External Diode Current Ratio		16		
ANALOG TO DIGITAL CONVERTER CHARACTERISTICS					
TUE	Total Unadjusted Error (7)			**±2**	%FS (max)
DNL	Differential Non-linearity		1		LSB
	Power Supply Sensitivity		±1		%/V
	Total Monitoring Cycle Time (8)	All Voltage and Temperature readings	182	**200**	ms (max)
	Input Resistance, all analog inputs		210	**140**	kΩ (min)
				400	kΩ (max)
DIGITAL OUTPUT: PWM1, PWM2, PWM3, XTESTOUT					
I_{OL}	Logic Low Sink Current	V_{OL}=0.4V		**8**	mA (min)
V_{OL}	Logic Low Level	I_{OUT} = +8 mA		**0.4**	V (max)

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(3) The average current can be calculated from the peak current using the following equation:Quiescent current will not increase substantially with an SMBus transaction.
(4) The accuracy of the LM96000CIMT is ensured when using the thermal diode of Intel Pentium 4 90nm processors or any thermal diode with a non-ideality of 1.011 and series resistance of 3.33Ω. When using a 2N3904 type transistor as a thermal diode the error band will be typically shifted by -?°C.
(5) Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM96000 and the thermal resistance.
(6) Thermal resistance junction-to-ambient when attached to a double-sided printed circuit board with 1 oz. foil is 113 °C/W.
(7) TUE , total unadjusted error, includes ADC gain, offset, linearity and reference errors. TUE is defined as the "actual Vin" to achieve a given code transition minus the "theoretical Vin" for the same code. Therefore, a positive error indicates that the input voltage is greater than the theoretical input voltage for a given code. If the theoretical input voltage was applied to an LM96000 that has positive error, the LM96000's reading would be less than the theoretical.
(8) This specification is provided only to indicate how often temperature and voltage data is updated. The LM96000 can be read at any time without regard to conversion state (and will yield last conversion result).

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DC Electrical Characteristics (continued)

The following specifications apply for V+ = 3.0V to 3.6V, and all analog input source impedance R_S = 50Ω unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} =0°C to T_{MAX}=85°C;** all other limits $T_A = T_J$= 25°C. T_A is the ambient temperature of the LM96000; T_J is the junction temperature of the LM96000; T_D is the thermal diode junction temperature.

Parameter		Test Conditions	Typical (1)	Limits (2)	Units (Limits)
SMBUS OPEN-DRAIN OUTPUT: SMBDAT					
V_{OL}	Logic Low Output Voltage	I_{OUT} = +4 mA		**0.4V**	V (max)
I_{OH}	High Level Output Current	V_{OUT} = V+	0.1	**10**	µA (max)
SMBUS INPUTS: SMBCLK. SMBDAT					
V_{IH}	Logic Input High Voltage			**2.1**	V (min)
V_{IL}	Logic Input Low Voltage			**0.8**	V (max)
V_{HYST}	Logic Input Hysteresis Voltage		300		mV
DIGITAL INPUTS: ALL					
V_{IH}	Logic Input High Voltage			**2.1**	V (min)
V_{IL}	Logic Input Low Voltage			**0.8**	V (max)
V_{TH}	Logic Input Threshold Voltage		1.5		V
I_{IH}	Logic High Input Current	V_{IN} = V+	0.005	**10**	µA (max)
I_{IL}	Logic Low Input Current	V_{IN} = GND	−0.005	**−10**	µA (max)
C_{IN}	Digital Input Capacitance		20		pF

AC Electrical Characteristics

The following specifications apply for V+ = 3.0V to 3.6V unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} =0°C to T_{MAX}=85°C;** all other limits $T_A = T_J$= 25°C.

Parameter		Test Conditions	Typical (1)	Limits (2)	Units (Limits)
TACHOMETER ACCURACY					
	Fan Count Accuracy			**±10**	% (max)
	Fan Full-Scale Count			**65536**	(max)
	Fan Counter Clock Frequency		90		kHz
	Fan Count Conversion Time		0.7	**1.4**	sec (max)
FAN PWM OUTPUT					
	Frequency Setting Accuracy			**±10**	% (max)
	Frequency Range		10 30		Hz kHz
	Duty-Cycle Range	Low frequency range		**0 to 100**	% (max)
	Duty-Cycle Resolution (8-bits)		0.390625		%
	Spin-Up Time Interval Range		100 4000		ms ms
	Spin-Up Time Interval Accuracy			**±10**	% (max)
SPIKE SMOOTHING FILTER					
	Time Interval Deviation			**±10**	% (max)
	Time Interval Range		35 0.8		sec sec

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Limits are specified to TI's AOQL (Average Outgoing Quality Level).

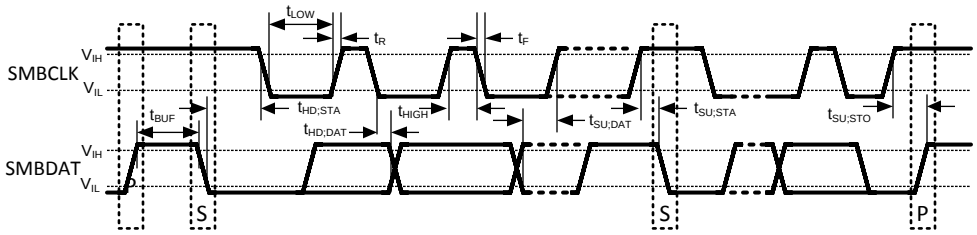
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AC Electrical Characteristics (continued)

The following specifications apply for V+ = 3.0V to 3.6V unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} =0°C to T_{MAX}=85°C;** all other limits $T_A = T_J$= 25°C.

Parameter		Test Conditions	Typical (1)	Limits (2)	Units (Limits)
SMBUS TIMING CHARACTERISTICS					
f_{SMB}	SMBus Operating Frequency			**10** **100**	kHz (min) kHz (max)
f_{BUF}	SMBus Free Time Between Stop And Start Condition			**4.7**	µs (min)
t_{HD_STA}	Hold Time After (Repeated) Start Condition (after this period, the first clock is generated)			**4.0**	µs (min)
$t_{SU:STA}$	Repeated Start Condition Setup Time			**4.7**	µs (min)
$t_{SU:STO}$	Stop Condition Setup Time			**4.0**	µs (min)
$t_{HD:DAT}$	Data Output Hold Time			**300**	ns (min)
				930	ns (max)
$t_{SU:DAT}$	Data Input Setup Time			**250**	ns (min)
$t_{TIMEOUT}$	Data And Clock Low Time To Reset Of SMBus Interface Logic(3)			**25** **35**	ms (min) ms (max)
t_{LOW}	Clock Low Period			**4.7**	µs (min)
t_{HIGH}	Clock High Period			**4.0** **50**	µs (min) µs (max)
t_F	Clock/Data Fall Time			**300**	ns (max)
t_R	Clock/Data Rise Time			**1000**	ns (max)
t_{POR}	Time from Power-On-Reset to LM96000 Reset and Operational	V+ > 2.8V		**500**	ms (max)

(3) Holding the SMBDAT and/or SMBCLK lines Low for a time interval greater than $t_{TIMEOUT}$ will reset the LM96000's SMBus state machine, therefore setting the SMBDAT pin to a high impedance state.



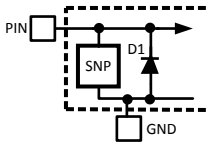
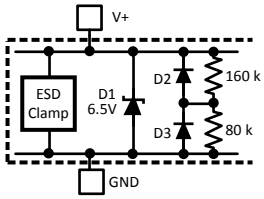
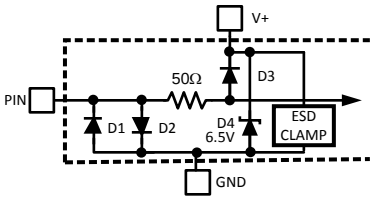
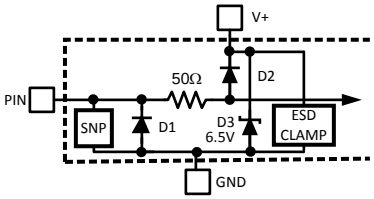
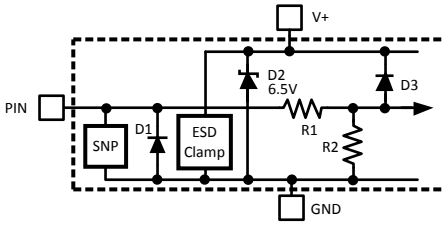
Pin No.	Pin Name	Circuit	All Input Circuits
1	SMBDAT	A	
2	SMBCLK		
3	GND	B	
4	3.3V		

Figure 2. Circuit A

Pin No.	Pin Name	Circuit	All Input Circuits
5	VID0	A	 Figure 3. Circuit B
6	VID1		
7	VID2		
8	VID3		
9	TACH3		
10	PWM2		 Figure 4. Circuit C
11	TACH1		
12	TACH2		
13	PWM3/AddEnable		
14	TACH4/AddSel		
15	REMOTE2−	C	 Figure 5. Circuit D
16	REMOTE2+	D	
17	REMOTE1−	C	
18	REMOTE1+	D	
19	VID4	A	
20	5V	E	 Figure 6. Circuit E
21	12V		
22	2.5V		
23	VCCP_IN		
24	PWM1/xTEXTOUT	A	

FUNCTIONAL DESCRIPTION

1.0 SMBUS

The LM96000 is compatible with devices that are compliant to the SMBus 2.0 specification. More information on this bus can be found at: http://www.smbus.org/. Compatibility of SMBus2.0 to other buses is discussed in the SMBus 2.0 specification.

1.1 Addressing

LM96000 is designed to be used primarily in desktop systems that require only one monitoring device.

If only one LM96000 is used on the motherboard, the designer should be sure that the PWM3/Address Enable pin is High during the first SMBus communication addressing the LM96000. PWM3/Address Enable is an open drain I/O pin that at power-on defaults to the input state of Address Enable. A maximum of 10k pull-up resistance on PWM3/Address Enable is required to assure that the SMBus address of the device will be locked at 010 1110b, which is the default address of the LM96000.

During the first SMBus communication TACH4 and PWM3 can be used to change the SMBus address of the LM96000 to 0101101b or 0101100b. LM96000 address selection procedure:

- A 10 kΩ pull-down resistor to ground on the PWM3/Address Enable pin is required. Upon power up, the LM96000 will be placed into Address Enable mode and assign itself an SMBus address according to the state of the Address Select input. The LM96000 will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the LM96000 address, 0 1011b. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection. When the

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PWM3/$\overline{\text{Address Enable}}$ pin is not used to change the SMBus address of the LM96000, it will remain in a high state until the first communication with the LM96000. After the first SMBus transaction is completed PWM3 and TACH4 will return to normal operation.

$\overline{\text{Address Enable}}$	Address Select	Board Implementation	SMBus Address
0	0	Pulled to ground through a 10 kΩ resistor	010 1100b, 2Ch
0	1	Pulled to 3.3V or to GND through a 10 kΩ resistor	010 1101b, 2Dh
1	X	Pulled to 3.3V through a 10 kΩ resistor	010 1110b, 2Eh

In this way, up to three LM96000 devices can exists on an SMBus at any time. Multiple LM96000 devices can be used to monitor additional processors and temperature zones. When using the non-default addresses the TACH4 and PWM3 will not function. As shown in the timing diagram the Address Enable pin must remain low in order for the latched address to remain in effect. If the address enable pin is pulled high after the first SMBus communication, then the LM96000 SMBus address will revert to the default value (2Eh) after the first five clocks of next SMBus communication.

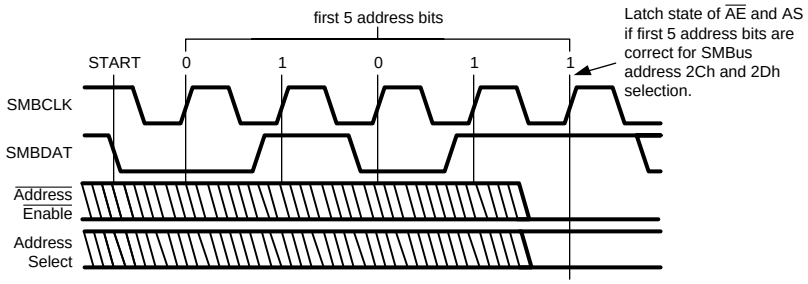


Figure 7. Address Latch Enable low during and after first communication

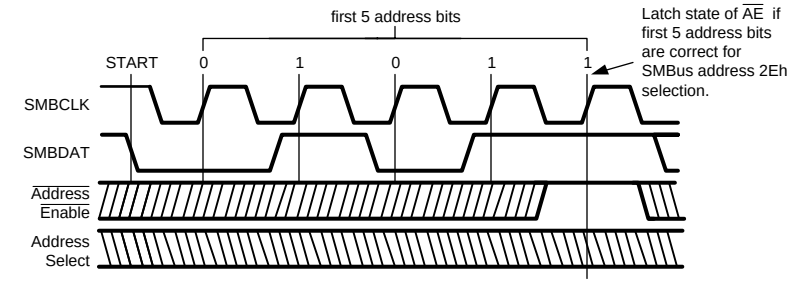


Figure 8. Address Latch Enable high during first communication

2.0 FAN REGISTER DEVICE SET-UP

The BIOS will follow the following steps to configure the fan registers on the LM96000. The registers corresponding to each function are listed. All steps may not be necessary if default values are acceptable. Regardless of all changes made by the BIOS to the fan limit and parameter registers during configuration, the LM96000 will continue to operate based on default values until the START bit (bit 0), in the Ready/Lock/Start/Override register (address 40h), is set. Once the fan mode is updated, by setting the START bit to 1, the LM96000 will operate using the values that were set by the BIOS in the fan control limit and parameter registers (adress 5Ch through 6Eh).

1. Set limits and parameters (not necessarily in this order):
   - – [5F-61h] Set PWM frequencies and auto fan control range.
   - – [62-63h] Set spike smoothing and min/off.
   - – [5C-5Eh] Set the fan spin-up delays.
   - – [5C-5Eh] Match each fan with a corresponding thermal zone.

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– – [67-69h] Set the fan temperature limits.
– – [6A-6Ch] Set the temperature absolute limits.
– – [64-66h] Set the PWM minimum duty cycle.
– – [6D-6Eh] Set the temperature Hysteresis values.

2. [40h] Set bit 0 (START) to update fan control and limit register values and start fan control based on these new values.
3. [40h] Set bit 1 (LOCK) to lock the fan limit and parameter registers (optional).

3.0 AUTO FAN CONTROL OPERATING MODE

The LM96000 includes the circuitry for automatic fan control. In Auto Fan Mode, the LM96000 will automatically adjust the PWM duty cycle of the PWM outputs. PWM outputs are assigned to a thermal zone based on the fan configuration registers. It is possible to have more than one PWM output assigned to a thermal zone. For example, PWM outputs 2 and 3, connected to two chassis fans, may both be controlled by thermal zone 2. At any time, the temperature of a zone exceeds its absolute limit, all PWM outputs will go to 100% duty cycle to provide maximum cooling to the system.

4.0 REGISTER SET

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
20h	R	2.5V	7	6	5	4	3	2	1	0	N/A	
21h	R	VCCP_IN	7	6	5	4	3	2	1	0	N/A	
22h	R	3.3V	7	6	5	4	3	2	1	0	N/A	
23h	R	5V	7	6	5	4	3	2	1	0	N/A	
24h	R	12V	7	6	5	4	3	2	1	0	N/A	
25h	R	Processor (Zone1) Temp	7	6	5	4	3	2	1	0	N/A	
26h	R	Internal (Zone2) Temp	7	6	5	4	3	2	1	0	N/A	
27h	R	Remote (Zone3) Temp	7	6	5	4	3	2	1	0	N/A	
28h	R	Tach1 LSB	7	6	5	4	3	2	LEVEL1	LEVEL0	N/A	
29h	R	Tach1 MSB	15	14	13	12	11	10	9	8	N/A	
2Ah	R	Tach2 LSB	7	6	5	4	3	2	LEVEL1	LEVEL0	N/A	
2Bh	R	Tach2 MSB	15	14	13	12	11	10	9	8	N/A	
2Ch	R	Tach3 LSB	7	6	5	4	3	2	LEVEL1	LEVEL0	N/A	
2Dh	R	Tach3 MSB	15	14	13	12	11	10	9	8	N/A	
2Eh	R	Tach4 LSB	7	6	5	4	3	2	LEVEL1	LEVEL0	N/A	
2Fh	R	Tach4 MSB	15	14	13	12	11	10	9	8	N/A	
30h	R/W	Fan1 Current PWM Duty	7	6	5	4	3	2	1	0	N/A	

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Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
31h	R/W	Fan2 Current PWM Duty	7	6	5	4	3	2	1	0	N/A	
32h	R/W	Fan3 Current PWM Duty	7	6	5	4	3	2	1	0	N/A	
3Eh	R	Company ID	7	6	5	4	3	2	1	0	01h	
3Fh	R	Version/ Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	68h	
40h	R/W	Ready/Lock/Start/Override	RES	RES	RES	RES	OVRID	READY	LOCK	START	00h	
41h	R	Interrupt Status Register 1	ERR	ZN3	ZN2	ZN1	5V	3.3V	VCCP	2.5V	00h	
42h	R	Interrupt Status Register 2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	RES	12V	00h	
43h	R	VID0–4	RES	RES	RES	VID4	VID3	VID2	VID1	VID0	N/A	
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00h	
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FFh	
46h	R/W	VCCP Low Limit	7	6	5	4	3	2	1	0	00h	
47h	R/W	VCCP High Limit	7	6	5	4	3	2	1	0	FFh	
48h	R/W	3.3V Low Limit	7	6	5	4	3	2	1	0	00h	
49h	R/W	3.3V High Limit	7	6	5	4	3	2	1	0	FFh	
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h	
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh	
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h	
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh	
4Eh	R/W	Processor (Zone1) Low Temp	7	6	5	4	3	2	1	0	81h	

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Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
4Fh	R/W	Processor (Zone1) High Temp	7	6	5	4	3	2	1	0	7Fh	
50h	R/W	Internal (Zone2) Low Temp	7	6	5	4	3	2	1	0	81h	
51h	R/W	Internal (Zone2) High Temp	7	6	5	4	3	2	1	0	7Fh	
52h	R/W	Remote (Zone3) Low Temp	7	6	5	4	3	2	1	0	81h	
53h	R/W	Remote (Zone3) High Temp	7	6	5	4	3	2	1	0	7Fh	
54h	R/W	Tach1 Minimum LSB	7	6	5	4	3	2	1	0	FFh	
55h	R/W	Tach1 Minimum MSB	15	14	13	12	11	10	9	8	FFh	
56h	R/W	Tach2 Minimum LSB	7	6	5	4	3	2	1	0	FFh	
57h	R/W	Tach2 Minimum MSB	15	14	13	12	11	10	9	8	FFh	
58h	R/W	Tach3 Minimum LSB	7	6	5	4	3	2	1	0	FFh	
59h	R/W	Tach3 Minimum MSB	15	14	13	12	11	10	9	8	FFh	
5Ah	R/W	Tach4 Minimum LSB	7	6	5	4	3	2	1	0	FFh	
5Bh	R/W	Tach4 Minimum MSB	15	14	13	12	11	10	9	8	FFh	
5Ch	R/W	Fan1 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	✓
5Dh	R/W	Fan2 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	✓
5Eh	R/W	Fan3 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	✓
5Fh	R/W	Fan1 Range/Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C4h	✓
60h	R/W	Fan2 Range/Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C4h	✓

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Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
61h	R/W	Fan3 Range/Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C4h	✓
62h	R/W	Min/Off, Zone1 Spike Smoothing	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00H	✓
63h	R/W	Zone2, Zone3 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00h	✓
64h	R/W	Fan1 PWM Minimum	7	6	5	4	3	2	1	0	80h	✓
65h	R/W	Fan2 PWM Minimum	7	6	5	4	3	2	1	0	80h	✓
66h	R/W	Fan3 PWM Minimum	7	6	5	4	3	2	1	0	80h	✓
67h	R/W	Zone1 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah	✓
68h	R/W	Zone2 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah	✓
69h	R/W	Zone3 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah	✓
6Ah	R/W	Zone1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h	✓
6Bh	R/W	Zone2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h	✓
6Ch	R/W	Zone3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h	✓
6Dh	R/W	Zone1, Zone2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44h	✓
6Eh	R/W	Zone3 Hysteresis	H3-3	H3-2	H3-1	H3-0	RES	RES	RES	RES	40h	✓
6Fh	R/W	XOR Test Tree Enable	RES	RES	RES	RES	RES	RES	RES	XEN	00h	✓
74h	R/W	Tach Monitor Mode	RES	RES	T3/4-1	T3/4-0	T2-1	T2-0	T1-1	T1-0	00h	

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Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
75h	R/W	Fan Spin-up Mode	RES	RES	RES	RES	RES	PWM3 SU	PWM2 SU	PWM1 SU	7h	✓

4.1 Register 20-24h: Voltage Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
20h	R	2.5V	7	6	5	4	3	2	1	0	N/A
21h	R	VCCP	7	6	5	4	3	2	1	0	N/A
22h	R	3.3V	7	6	5	4	3	2	1	0	N/A
23h	R	5V	7	6	5	4	3	2	1	0	N/A
24h	R	12V	7	6	5	4	3	2	1	0	N/A

The Register Names difine the typical input voltage at which the reading is ¾ full scale or C0h.

The Voltage Reading registers are updated automatically by the LM96000 at a minimum frequency of 4 Hz. These registers are read only — a write to these registers has no effect.

4.2 Register 25-27h: Temperature Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
25h	R	Processor (Zone1) Temp	7	6	5	4	3	2	1	0	N/A
26h	R	Internal (Zone2) Temp	7	6	5	4	3	2	1	0	N/A
27h	R	Remote (Zone3) Temp	7	6	5	4	3	2	1	0	N/A

The Temperature Reading registers reflect the current temperatures of the internal and remote diodes. Processor (Zone1) Temp register reports the temperature measured by the thermal diode connected to the Remote1− and Remote1+ pins, Remote (Zone3) Temp register reports the temperature measured by the thermal diode connected to the the Remote2− and Remote2+ pins, and the Internal (Zone2) Temp register reports the temperature measured by the internal (junction) temperature sensor. Temperatures are represented as 8 bit, 2's complement, signed numbers, in Celsius, as shown below in Table 1. The Temperature Reading register will return a value of 80h if the remote diode pins are not used by the board designer or are not functioning properly. This reading will cause the zone limit bit(s) (bits 6 and 4) in the Interrupt Status Register (41h) and the remote diode fault status bit(s) (bit 6 or 7) in the Interrupt Status Register 2 (42h) to be set. The Temperature Reading registers are updated automatically by the LM96000 at a minimum frequency of 4 Hz. These registers are read only — a write to these registers has no effect.

Table 1. Temperature vs Register Reading

Temperature	Reading (Dec)	Reading (Hex)
−127°C	−127	81h
. . .	. . .	. . .
−50°C	−50	CEh
. . .	. . .	. . .
0°C	0	00h

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Table 1. Temperature vs Register Reading (continued)

Temperature	Reading (Dec)	Reading (Hex)
. . .	. . .	. . .
127°C	127	7Fh
(SENSOR ERROR)		80h

4.3 Register 28-2Fh: Fan Tachometer Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
28h 29h	R R	Tach1 LSB Tach1 MSB	7 15	6 14	5 13	4 12	3 11	2 10	LEVEL1 9	LEVEL0 8	N/A N/A
2Ah 2Bh	R R	Tach2 LSB Tach2 MSB	7 15	6 14	5 13	4 12	3 11	2 10	LEVEL1 9	LEVEL0 8	N/A N/A
2Ch 2Dh	R R	Tach3 LSB Tach3 MSB	7 15	6 14	5 13	4 12	3 11	2 10	LEVEL1 9	LEVEL0 8	N/A N/A
2Eh 2Fh	R R	Tach4 LSB Tach4 MSB	7 15	6 14	5 13	4 12	3 11	2 10	LEVEL1 9	LEVEL0 8	N/A N/A

The Fan Tachometer Reading registers contain the number of 11.111 µs periods (90 kHz) between full fan revolutions. The results are based on the time interval of two tachometer pulses, since most fans produce two tachometer pulses per full revolution. These registers will be updated at least once every second.

The value, for each fan, is represented by a 16-bit unsigned number.

The Fan Tachometer Reading registers will always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional.

The least two significant bits (LEVEL1 and LEVEL2) of the least significant byte are used to indicate the accuracy level of the tachometer reading. The accuracy ranges from most to least accurate. [LEVEL1:LEVEL2]=11indicates a most accurate value, [LEVEL1:LEVEL2]=01 indicates the least accurate value and [LEVEL1:LEVEL2]=00 is reserved for future use.

FF FFh indicates that the fan is not spinning, or that the tachometer input is not connected to a valid signal. These registers are read only — a write to these registers has no effect.

When the LSByte of the LM96000 16-bit register is read, the other byte (MSByte) is latched at the current value until it is read. At the end of the MSByte read the Fan Tachometer Reading registers are updated.

During spin-up, the PWM duty cycle reported is 0%.

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4.4 Register 30-32h: Current PWM Duty

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
30h	R/W	Fan1 Current PWM Duty	7	6	5	4	3	2	1	0	N/A
31h	R/W	Fan2 Current PWM Duty	7	6	5	4	3	2	1	0	N/A
32h	R/W	Fan3 Current PWM Duty	7	6	5	4	3	2	1	0	N/A

The Current PWM Duty registers store the current duty cycle at each PWM output. At initial power-on, the PWM duty cycle is 100% and thus, when read, this register will return FFh. After the Ready/Lock/Start/Override register Start bit is set, this register and the PWM signals will be updated based on the algorithm described in the Auto Fan Control Operating Mode section.

When read, the Current PWM Duty registers return the current PWM duty cycle. These registers are read only unless the fan is in manual (test) mode, in which case a write to these registers will directly control the PWM duty cycle for each fan. The PWM duty cycle is represented as shown in the following table.

Current Duty	Value (Decimal)	Value (Hex)
0%	0	00h
0.3922%	1	01h
. . .	. . .	. . .
25.098%	64	40h
. . .	. . .	. . .
50.196%	128	80h
. . .	. . .	. . .
100%	255	FFh

4.5 Register 3Eh: Company ID

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	01h

The company ID register contains the company identification number. For Texas Instruments this is 01h. This number is assigned by Intel and is a method for uniquely identifying the part manufacturer. This register is read only — a write to this register has no effect.

4.6 Register 3Fh: Version/Stepping

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Fh	R	Version/Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	68h

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The four least significant bits of the Version/Stepping register [3.0] contain the current stepping of the LM96000 silicon. The four most significant bits [7.4] reflect the LM96000 base device number when set to a value of 0110b. For the LM96000, this register will read 01101000b (68h). Bit 3 of the stepping field is set to indicate that the LM96000 is a super-set of the LM85 family of products.

The register is used by application software to identify which device in the hardware monitor family of ASICs has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-arounds for bugs found in a specific silicon stepping.

This register is read only — a write to this register has no effect.

4.7 Register 40h: Ready/Lock/Start/Override

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
40h	R/W	Ready/Lock/Start/Override	RES	RES	RES	RES	OVRID	READY	LOCK	START	00h

Bit	Name	R/W	Default	Description
0	START	R/W	0	When software writes a 1 to this bit, the LM96000 fan monitoring and PWM output control functions will use the values set in the fan control limit and parameter registers (address 5Ch through 6Eh). Before this bit is set, the LM96000 will not update the used register values, the default values will remain in effect. Whenever this bit is set to 0, the LM96000 fan monitoring and PWM output control functions use the default fan limits and parameters, regardless of the current values in the limit and parameter registers (5C through 6Eh). The LM96000 will preserve the values currently stored in the limit and parameter registers when this bit is set or cleared. This bit is not effected by the state of the Lock bit. It is expected that all limit and parameter registers will be set by BIOS or application software prior to setting this bit.
1	LOCK	R/W	0	Setting this bit to 1 locks specified limit and parameter registers. Once this bit is set, limit and parameter registers become read only and will remain locked until the device is powered off. This register bit becomes read only once it is set.
2	READY	R	0	The LM96000 sets this bit automatically after the part is fully powered up, has completed the power-up-reset process, and after all A/D converters are properly functioning.
3	OVRID	R/W		If this bit is set to 1, all PWM outputs will go to 100% duty cycle regardless of whether or not the lock bit is set. The OVRID bit has precedence over the disabled mode. Therefore, when OVRID is set the PWM will go to 100% even if the PWM is in the disabled mode.
4–7	Reserved	R	0	Reserved

4.8 Register 41h: Interrupt Status Register 1

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
41h	R	Interrupt Status 1	ERR	ZN3	ZN2	ZN1	5V	3.3V	VCCP	2.5V	00h

The Interrupt Status Register 1 bits will be automatically set, by the LM96000, whenever a fault condition is detected. A fault condition is detected whenever a measured value is outside the window set by its limit registers. ZN3 and ZN1 bits will be set when a diode fault condition, such as a disconect or short, is detected. More than one fault may be indicated in the interrupt register when read. This register will hold a set bit(s) until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the LM96000 after it is read by software, if the fault condition is no longer exists. Once set, the Interrupt Status Register 1 bits will remain set until a read event occurs, even if the fault condition no longer exists

This register is read only — a write to this register has no effect.

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Bit	Name	R/W	Default	Description
0	2.5V_Error	R	0	The LM96000 automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	VCCP_Error	R	0	The LM96000 automatically sets this bit to 1 when the VCCP input voltage is less than or equal to the limit set in the VCCP Low Limit register or greater than the limit set in the VCCP High Limit register.
2	3.3V_Error	R	0	The LM96000 automatically sets this bit to 1 when the 3.3V input voltage is less than or equal to the limit set in the 3.3V Low Limit register or greater than the limit set in the 3.3V High Limit register.
3	5V_Error	R	0	The LM96000 automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Zone 1 Limit Exceeded	R	0	The LM96000 automatically sets this bit to 1 when the temperature input measured by the Remote1− and Remote1+ inputs is less than or equal to the limit set in the Processor (Zone1) Low Temp register or more than the limit set in the Processor (Zone1) High Temp register. This bit will be set when a diode fault is detected.
5	Zone 2 Limit Exceeded	R	0	The LM96000 automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the Internal (Zone2) Low Temp register or greater than the limit set in the Internal (Zone2) High Temp register.
6	Zone 3 Limit Exceeded	R	0	The LM96000 automatically sets this bit to 1 when the temperature input measured by the Remote2− and Remote2+ inputs is less than or equal to the limit set in the Internal (Zone2) Low Temp register or greater than the limit set in the Remote (Zone3) High Temp register. This bit will be set when a diode fault is detected.
7	Error in Status Register 2	R	0	If there is a set bit in Status Register 2, this bit will be set to 1.

4.9 Register 42h: Interrupt Status Register 2

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
42h	R	Interrupt Status Register 2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	RES	12V	00h

The Interrupt Status Register 2 bits will be automatically set, by the LM96000, whenever a fault condition is detected. Interrupt Status Register 2 identifies faults caused by temperature sensor error, fan speed droping below minimum set by the tachometer minimum register, the 12V input voltage going outside the window set by its limit registers. Interrupt Status Register 2 will hold a set bit until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the LM96000 after it is ready by software, if fault condition no longer exists. Once set, the Interrupt Status Register 2 bits will remain set until a read event occurs, even if the fault no longer exists

This register is read only — a write to this register has no effect.

Bit	Name	R/W	Default	Description
0	+12V_Error	R	0	The LM96000 automatically sets this bit to 1 when the 12V input voltage either falls below the limit set in the 12V Low Limit register or exceeds the limit set in the 12V High Limit register.
1	Reserved	R	0	Reserved
2	Fan1 Stalled	R	0	The LM96000 automatically sets this bit to 1 when the TACH1 input reading is above the value set in the Tach1 Minimum MSB and LSB registers.
3	Fan2 Stalled	R	0	The LM96000 automatically sets this bit to 1 when the TACH2 input reading is above the value set in the Tach2 Minimum MSB and LSB registers.
4	Fan3 Stalled	R	0	The LM96000 automatically sets this bit to 1 when the TACH3 input reading is above the value set in the Tach3 Minimum MSB and LSB registers.
5	Fan4 Stalled	R	0	The LM96000 automatically sets this bit to 1 when the TACH4 input reading is above the value set in the Tach4 Minimum MSB and LSB registers.

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Bit	Name	R/W	Default	Description
6	Remote Diode 1 Fault	R	0	The LM96000 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote1+ or Remote1− thermal diode input pins. A diode fault will also set bit 4, Diode 1 Zone Limit bit, of Interrupt Status Register 1.
7	Remote Diode 2 Fault	R	0	The LM96000 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote2+ or Remote2− thermal diode input pins. A diode fault will also set bit 6, Diode 2 Zone Limit bit, of Interrupt Status Register 1.

4.10 Register 43h: VID

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
43h	R	VID0–4	RES	RES	RES	VID4	VID3	VID2	VID1	VID0	

The VID register contains the values of LM96000 VID0–VID4 input pins. This register indicates the status of the VID lines that interconnect the processor to the Voltage Regulator Module (VRM). Software uses the information in this register to determine the voltage that the processor is designed to operate at. With this information, software can then dynamically determine the correct values to place in the VCCP Low Limit and VCCP High Limit registers.

This register is read only — a write to this register has no effect.

4.11 Registers 44-4Dh: Voltage Limit Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00h
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FFh
46h	R/W	VCCP Low Limit	7	6	5	4	3	2	1	0	00h
47h	R/W	VCCP High Limit	7	6	5	4	3	2	1	0	FFh
48h	R/W	3.3V Low Limit	7	6	5	4	3	2	1	0	00h
49h	R/W	3.3V High Limit	7	6	5	4	3	2	1	0	FFh
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh

If a voltage input either exceeds the value set in the voltage high limit register or falls below the value set in the voltage low limit register, the corresponding bit will be set automatically by the LM96000 in the interrupt status registers (41-42h). Voltages are presented in the registers at ¾ full scale for the nominal voltage, meaning that at nominal voltage, each input will be C0h, as shown in Table 2.

Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

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Table 2. Voltage Limits vs Register Setting

Input	Nominal Voltage	Register Setting at Nominal Voltage	Maximum Voltage	Register Reading at Maximum Voltage	Minimum Voltage	Register Reading at Minimum Voltage
2.5V	2.5V	C0h	3.32V	FFh	0V	00h
VCCP	2.25V	C0h	3.00V	FFh	0V	00h
3.3V	3.3V	C0h	4.38V	FFh	3.0V	AFh
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

4.12 Registers 4E-53h: Temperature Limit Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
4Eh	R/W	Processor (Zone1) Low Temp	7	6	5	4	3	2	1	0	81h
4Fh	R/W	Processor (Zone1) High Temp	7	6	5	4	3	2	1	0	7Fh
50h	R/W	Processor (Zone2) Low Temp	7	6	5	4	3	2	1	0	81h
51h	R/W	Processor (Zone2) High Temp	7	6	5	4	3	2	1	0	7Fh
52h	R/W	Processor (Zone3) Low Temp	7	6	5	4	3	2	1	0	81h
53h	R/W	Processor (Zone3) High Temp	7	6	5	4	3	2	1	0	7Fh

If an external temperature input or the internal temperature sensor either exceeds the value set in the corresponding high limit register or falls below the value set in the corresponding low limit register, the corresponding bit will be set automatically by the LM96000 in the Interrupt Status Register 1 (41h). For example, if the temperature read from the Remote1− and Remote1+ inputs exceeds the Processor (Zone1) High Temp register limit setting, Interrupt Status Register 1 ZN1 bit will be set. The temperature limits in these registers are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in Table 3.

Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Table 3. Temperature Limits vs Register Settings

Temperature	Reading (Decimal)	Reading (Hex)
−127°C	−127	81h
. . .	. . .	. . .
−50°C	−50	CEh
. . .	. . .	. . .
0°C	0	00h

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Table 3. Temperature Limits vs Register Settings (continued)

Temperature	Reading (Decimal)	Reading (Hex)
. . .	. . .	. . .
50°C	50	32h
. . .	. . .	. . .
127°C	127	7Fh

4.13 Registers 54-5Bh: Fan Tachometer Low Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
54h 55h	R/W R/W	Tach1 Minimum LSB Tach1 Minimum MSB	7 15	6 14	5 13	4 12	3 11	2 10	1 9	0 8	FFh FFh
56h 57h	R/W R/W	Tach2 Minimum LSB Tach2 Minimum MSB	7 15	6 14	5 13	4 12	3 11	2 10	1 9	0 8	FFh FFh
58h 59h	R/W R/W	Tach3 Minimum LSB Tach3 Minimum MSB	7 15	6 14	5 13	4 12	3 11	2 10	1 9	0 8	FFh FFh
5Ah 5Bh	R/W R/W	Tach4 Minimum LSB Tach4 Minimum MSB	7 15	6 14	5 13	4 12	3 11	2 10	1 9	0 8	FFh FFh

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at low speeds, so care should be taken in software to ensure that the limit is high enough not to cause sporadic alerts. The fan tachometer will not cause a bit to be set in Interrupt Status Register 2 if the current value in Current PWM Duty registers is 00h or if the fan 1 disabled via the Fan Configuration Register. Interrupts will never be generated for a fan if its minimum is set to FF FFh.

Given the insignificance of Bit 0 and Bit 1, these bits could be programmed to remember which fan is which, as follows.

Fan	Bit 1	Bit 0
CPU	0	0
Memory	0	1
Chassis Front	1	0
Chassis Rear	1	1

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Setting the Ready/Lock/Start/Override register Lock bit has no effect these registers.

4.14 Registers 5C-5Eh: Fan Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
5Ch	R/W	Fan1 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	✓
5Dh	R/W	Fan2 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	✓
5Eh	R/W	Fan3 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	✓

This register becomes Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Bits [7:5] Zone/Mode

Bits [7:5] of the Fan Configuration registers associate each fan with a temperature sensor. When in Auto Fan Mode the fan will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If 'Hottest' option is selected (101 or 110), the fan will be controlled by the hottest of zones 2 and 3, or of zones 1, 2, and 3. To determine the 'Hottest' zone the PWM level for each zone is calculated then the the highest PWM value is selected. When in manual control mode, the Current PWM duty registers (30h-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. When the fan is disabled (100) the corresponding PWM output should be driven low (or high, if inverted).

Zone 1: External Diode 1 (processor)
Zone 2: Internal Sensor
Zone 3: External Diode 2

Table 4. Fan Zone Setting

ZON[2:0]	Fan Configuration
000	Fan on zone 1 auto
001	Fan on zone 2 auto
010	Fan on zone 3 auto
011	Fan always on full
100	Fan disabled
101	Fan controlled by hottest of zones 2, 3
110	Fan controlled by hottest of zones 1, 2, 3
111	Fan manually controlled (Test Mode)

Bit [4] PWM Invert

Bit [4] inverts the PWM output. If set to 0, 100% duty cycle will yield an output that is always high. If set to 1, 100% duty cycle will yield an output that is always low.

Bit [3] Reserved

Bits [2:0] Spin Up

Bits [2:0] specify the 'spin up' time for the fan. When a fan is being started from a stationary state, the PWM output is held at 100% duty cycle for the time specified in the Table 5 below before scaling to a lower speed.

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Table 5. Fan Spin-Up Register

SPIN[2:0]	Spin Up Time
000	0 sec
001	100 ms
010	250 ms
011	400 ms
100	700 ms
101	1000 ms
110	2000 ms
111	4000 ms

4.15 Registers 5F-61h: Auto Fan Speed Range, PWM Frequency

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
5Fh	R/W	Zone1 Range/Fan1 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C4h	✓
60h	R/W	Zone2 Range/Fan2 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C4h	✓
61h	R/W	Zone3 Range/Fan3 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C4h	✓

In Auto Fan Mode, when the temperature for a zone is above the Temperature Limit (Registers 67-69h) and below its Absolute Temperature Limit (Registers 6A-6Ch), the speed of a fan assigned to that zone is determined as follows.

When the temperature reaches the Fan Temp Limit for a zone, the PWM output assigned to that zone will be Fan PWM Minimum. Between Fan Temp Limit and (Fan Temp Limit + Range), the PWM duty cycle will increase linearly according to the temperature as shown in Figure 9 below. The PWM duty cycle will be 100% at (Fan Temp Limit + Range).

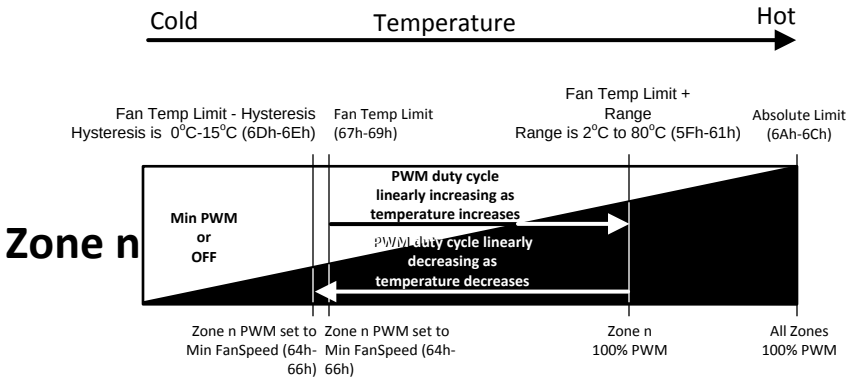


Figure 9. Fan Activity above Fan Temp Limit

Example for PWM1 assigned to Zone 1:

- – Zone 1 Fan Temp Limit (Register 67h) is set to 50°C (32h).
- – Range (Register 5Fh) is set to 8°C (6xh).
- – Fan 1 PWM Minimum (Register 64h) is set to 50% (32h).

In this case, the PWM1 duty cycle will be 50% at 50°C.

Since (Zone 1 Fan Temp Limit) + (Zone 1 Range) = 50°C + 8°C = 58°C, the fan will run at 100% duty cycle when the temperature of the Zone 1 sensor reaches 58°C.

Since the midpoint of the fan control range is 54°C, and the median duty cycle is 75% (Halfway between the PWM Minimum and 100%), PWM1 duty cycle would be 75% at 54°C.

Above (Zone 1 Fan Temp Limit) + (Zone 1 Range), the duty cycle will be 100%.

PWM frequency bits [3:0]

The PWM frequency bits [3:0] determine the PWM frequency for the fan.The LM96000 has high and low frequency ranges for the PWM outputs, that are controlled by the HLFRQ bit.

PWM Frequency Selection (Default = 0011 = 30.04 Hz).

Table 6. Register Setting vs PWM Frequency

HLFRQ	Freq [2:0]	PWM Frequency
0	000	10.01 Hz
0	001	15.02 Hz
0	010	23.14 Hz
0	011	30.04 Hz
0	100	38.16 Hz
0	101	47.06 Hz
0	110	61.38 Hz
0	111	94.12 Hz
1	000	22.5 kHz
1	001	24 kHz
1	010	25.7 kHz
1	011	25.7 kHz
1	100	27.7 kHz
1	101	27.7 kHz
1	110	30 kHz
1	111	30 kHz

Range Selection RAN [3:0]

RAN [3:0]	Range (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67

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RAN [3:0]	Range (°C)
1100	32
1101	40
1110	53.33
1111	80

This register becomes Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

4.16 Registers 62, 63h: Min/Off, Spike Smoothing

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
62h	R/W	Min/Off, Zone1 Spike Smoothing	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00h	✓
63h	R/W	Zone2, Zone3 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00h	✓

The Off/Min Bits [7:5] specify whether the duty cycle will be 0% or Minimum Fan Duty when the measured temperature falls below the Temperature LIMIT register setting (see table below). OFF1 applies to fan 1, OFF2 applies to fan 2, and OFF3 applies to fan 3.

If the Remote1 or Remote2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the LM96000. If these spikes are not ignored, the CPU fan (if connected to LM96000) may turn on prematurely and produce unpleasant noise. For this reason, any zone that is connected to a chipset or processor should have spike smoothing enabled.

When spike smoothing is enabled, the temperature reading registers will still reflect the current value of the temperature — not the 'smoothed out' value.

ZN1E, ZN2E, and ZN3E enable temperature smoothing for zones 1, 2, and 3 respectively.
ZN1-2, ZN1-1, and ZN1-0 control smoothing time for Zone 1.
ZN2-2, ZN2-1, and ZN2-0 control smoothing time for Zone 2.
ZN3-2, ZN3-1, and ZN3-0 control smoothing time for Zone 3.

These registers become ready only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.

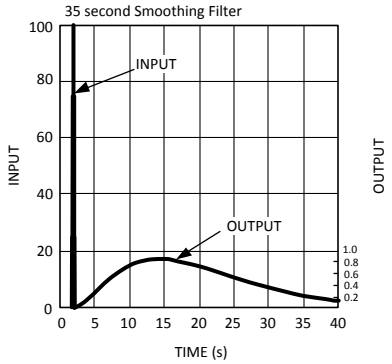


Figure 10. What LM96000 Auto Fan Control Sees With and Without Spike Smoothing

Table 7. Spike Smoothing

ZN-X[2:0]	Spike Smoothed Over
000	35 seconds
001	17.6 seconds
010	11.8 seconds
011	7.0 seconds
100	4.4 seconds
101	3.0 seconds
110	1.6 seconds
111	.8 seconds

Table 8. PWM Output Below Limit Depending on Value of Off/Min

Off/Min	PWM Action
0	At 0% duty below LIMIT
1	At Min PWM Duty below LIMIT

4.17 Registers 64-66h: Minimum PWM Duty Cycle

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
64h	R/W	Fan1 PWM Minimum	7	6	5	4	3	2	1	0	80h	✓
65h	R/W	Fan2 PWM Minimum	7	6	5	4	3	2	1	0	80h	✓
66h	R/W	Fan3 PWM Minimum	7	6	5	4	3	2	1	0	80h	✓

These registers specify the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting.

This register becomes Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Table 9. PWM Duty vs Register Setting for PWM Low Frequency Range

Current Duty	Value (Decimal)	Value (Hex)
0%	0	00h
0.3922%	1	01h
. . .	. . .	. . .
25.098%	64	40h
. . .	. . .	. . .
50.196%	128	80h
. . .	. . .	. . .
100%	255	FF

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PWM Duty Cycle vs Register Setting for PWM High Frequency Range

22.5KHz PWM Frequency						
PWM Duty Cycle Level (%)	**Value in Decimal**			**Value in Hex**		
0.00	0			0		
6.25	1	-	15	01	-	0F
12.50	16	-	31	10	-	1F
18.75	32	-	47	20	-	2F
25.00	48	-	63	30	-	3F
31.25	64	-	79	40	-	4F
37.50	80	-	95	50	-	5F
43.75	96	-	111	60	-	6F
50.00	112	-	127	70	-	7F
56.25	128	-	143	80	-	8F
62.50	144	-	159	90	-	9F
68.75	160	-	175	A0	-	AF
75.00	176	-	191	B0	-	BF
81.25	192	-	207	C0	-	CF
87.50	208	-	223	D0	-	DF
93.75	224	-	239	E0	-	EF
100.00	240	-	255	F0	-	FF

24KHz PWM Frequency						
PWM Duty Cycle Level (%)	**Value in Decimal**			**Value in Hex**		
0	0			0		
6.67	1	-	16	01	-	10
13.33	17	-	33	11	-	21
20.00	34	-	50	22	-	32
26.67	51	-	67	33	-	43
33.33	68	-	84	44	-	54
40.00	85	-	101	55	-	65
46.67	102	-	118	66	-	76
53.33	119	-	136	77	-	88
60.00	137	-	153	89	-	99
66.67	154	-	170	9A	-	AA
73.33	171	-	187	AB	-	BB
80.00	188	-	204	BC	-	CC
86.67	205	-	221	CD	-	DD
93.33	222	-	238	DE	-	EE
100.00	239	-	255	EF	-	FF

25.7KHz PWM Frequency						
PWM Duty Cycle Level (%)	**Value in Decimal**			**Value in Hex**		
0	0			0		
7.14	1	-	17	01	-	11
14.29	18	-	36	12	-	24
21.43	37	-	54	25	-	36
28.57	55	-	72	37	-	48
35.71	73	-	90	49	-	5A
42.86	91	-	109	5B	-	6D

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25.7KHz PWM Frequency						
PWM Duty Cycle Level (%)	**Value in Decimal**			**Value in Hex**		
50.00	110	-	127	6E	-	7F
57.14	128	-	145	80	-	91
64.29	146	-	164	92	-	A4
71.43	165	-	182	A5	-	B6
78.57	183	-	200	B7	-	C8
85.71	201	-	218	C9	-	DA
92.86	219	-	237	DB	-	ED
100.00	238	-	255	EE	-	FF

27.7KHz PWM Frequency						
PWM Duty Cycle Level (%)	**Value in Decimal**			**Value in Hex**		
0	0			0		
7.69	1	-	19	01	-	13
15.38	20	-	38	14	-	26
23.08	39	-	58	27	-	3A
30.77	59	-	78	3B	-	4E
38.46	79	-	97	4F	-	61
46.15	98	-	117	62	-	75
53.85	118	-	137	76	-	89
61.54	138	-	157	8A	-	9D
69.23	158	-	176	9E	-	B0
76.92	177	-	196	B1	-	C4
84.62	197	-	216	C5	-	D8
92.31	217	-	235	D9	-	EB
100.00	236	-	255	EC	-	FF

30KHz PWM Frequency						
PWM Duty Cycle Level (%)	**Value in Decimal**			**Value in Hex**		
0	0			0		
8.33	1	-	20	01	-	14
16.67	21	-	42	15	-	2A
25.00	43	-	63	2B	-	3F
33.33	64	-	84	40	-	54
41.67	85	-	106	55	-	6A
50.00	107	-	127	6B	-	7F
58.33	128	-	148	80	-	94
66.67	149	-	170	95	-	AA
75.00	171	-	191	AB	-	BF
83.33	192	-	212	C0	-	D4
91.67	213	-	234	D5	-	EA
100.00	235	-	255	EB	-	FF

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4.18 Registers 67-69h: Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
67h	R/W	Zone1 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah	✓
68h	R/W	Zone2 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah	✓
69h	R/W	Zone3 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah	✓

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the algorithm set forth in the Auto Fan Range, PWM Frequency register description.

Default = 90°C = 5Ah (1)

This register becomes Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Table 10. Temperature Limit vs Register Setting

Temperature	Reading (Decimal)	Reading (Hex)
−127°C	−127	81h
. . .	. . .	. . .
−50°C	−50	CEh
. . .	. . .	. . .
0°C	0	00h
. . .	. . .	. . .
50°C	50	32h
. . .	. . .	. . .
127°C	127	7Fh

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4.19 Registers 6A-6Ch: Absolute Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
6Ah	R/W	Zone1 Absolute Temp Limit	7	6	5	4	3	2	1	0	64h	✓
6Bh	R/W	Zone2 Absolute Temp Limit	7	6	5	4	3	2	1	0	64h	✓
6Ch	R/W	Zone3 Absolute Temp Limit	7	6	5	4	3	2	1	0	64h	✓

In the Auto Fan mode, if a zone exceeds the temperature set in the Absolute Temperature Limit register, all of the PWM outputs will increase its duty cycle to 100%. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event. If set to 80h (-128°C), the feature is disabled. Default=100°C=64h

These registers become Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect. After power up the default values are used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to these registers are possible.

Table 11. Absolute Limit vs Register Setting

Temperature	Reading (Decimal)	Reading (Hex)
−127°C	−127	81h
. . .	. . .	. . .
−50°C	−50	CEh
. . .	. . .	. . .
0°C	0	00h
. . .	. . .	. . .
50°C	50	32h
. . .	. . .	. . .
127°C	127	7Fh

4.20 Registers 6D-6Eh: Zone Hysteresis Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
6Dh	R/W	Zone1 and Zone2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44h	✓
6Eh	R/W	Zone3 Hysteresis	H3-3	H3-2	H3-1	H3-0	RES	RES	RES	RES	40h	✓

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If the temperature is above Fan Temp Limit, then drops below Fan Temp Limit, the following will occur:

- – The fan will remain on, at Fan PWM Minimum, until the temperature goes a certain amount below Fan Temp Limit.
- – The Hysteresis registers control this amount. See below table for details.

These registers become Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to thses registers shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Table 12. Hysteresis Settings

Setting	HYSTERESIS
0h	0°C
. . .	. . .
5h	5°C
. . .	. . .
Fh	15°C

4.21 Register 6Fh: Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
6Fh	R/W	Test Register	RES	RES	RES	RES	RES	RES	RES	XEN	00h

If the XEN bit is set high, the part will be placed into XOR tree test mode. Clearing the bit (writing a 0 to the XEN bit) brings the part out of XOR tree test mode.

This register becomes Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this registers shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

4.22 Registers 70-7Fh: Vendor Specific Registers

These registers are for vendor specific features, including test registers. They will not default to a specific value on power up.

4.22.1 Register 74h: Tachometer Monitor Mode

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value	Lock?
74h	R/W	Tach Monitor Mode	RES	RES	T3/4-1	T3/4-0	T2-1	T2-0	T1-1	T1-0	00h	

Each fan TACH input has 4 possible modes of operation when using the low frequency range for the PWM outputs. Mode 0 is the only mode that is available when using the high frequecy range for the PWM outputs. The modes for TACH3 and TACH4 share control bits T3/4-[1:0]; TACH2 is controlled by T2-[1:0]; TACH1 is controlled by T1-[1:0]. The result reported in all modes is based on 2 pulses per revolution. In order for modes 2 and 3 to function properly it is required that the:

- PWM1 output must control the fan that has it's tachometer output connected to the TACH1 LM96000 input.
- PWM2 output must control the fan that has it's tachometer output connected to the TACH2 LM96000 input.
- PWM3 output must control the fans that have their tachometer outputs connected to the TACH3 or TACH4 LM96000 inputs.

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Setting (Tn[1:0])	Mode	Function
00	0	Traditional tach input monitor, false readings when under minimum detctable RPM
01	1	Traditional tach input monitor, FFFFh reading when under minimum detectable RPM
10	2	Most accurate readings, FFFFh reading when under minimum detectable RPM
11	3	Least effect on programmed PWM of Fan, FFFFh reading when under minimum detectable RPM

• **Mode 0:**	This mode uses the conventional method for fan tachometer pulse detection and does not include any circuitry to compensate for PWM Fan drive. This mode should be used when PWM drive is not used to power the fan. This mode may report a false RPM reading when under minimum detectable RPM as shown in the following table.
• **Mode 1:**	This mode uses the conventional method for fan tach detection. The reading will be FFFFh if it is below minimum detectable RPM.
• **Mode 2:**	This mode is optimized for accurate RPM readings and activates circuitry that extends the lower side of the RPM reading as shown in the following table.
• **Mode 3:**	This mode minimizes the effect on the RPM setting and activates circuitry that extends the lower side of the RPM reading as shown in the following table.

PWM Frequency	Mode 0 and 1 Minimum RPM	Mode 2 and 3 Minimum RPM
10.01	841	210
15.02	1262	315
23.14	1944	420
30.04	2523	420
38.16	3205	420
47.06	3953	420
61.38	5156	420
94.12	7906	420

This register is not effected when the Ready/Lock/Start/Override register Lock bit is set. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

4.22.2 Register 75h: Fan Spin-up Mode

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock?
75h	R/W	Fan Spin-up Mode	RES	RES	RES	RES	RES	PWM3 SU	PWM2 SU	PWM1 SU	7h	✓

The PWM SU bit configures the PWM spin-up mode. If PWM SU is cleared the spin-up time will terminate after time programmed by the Fan Configuration register has elapsed. When set to a 1, the spin-up time will terminate early if the TACH reading exceeds the Tach Minimum value or after the time programmed by the Fan Configuration register has elapsed, whichever occurs first.

This register becomes Read Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

4.23 Undefined Registers

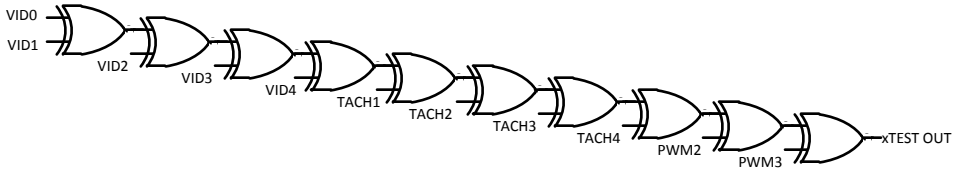
Any reads to undefined registers will always return 00h. Writes to undefined registers will have no effect and will not return an error.

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5.0 XOR TEST MODE

The LM96000 incorporates a XOR tree test mode. When the test mode is enabled by setting the “XEN” bit high in the Test Register at address 6Fh via the SMBus, the part will enter XOR test mode.

Since the test mode an XOR tree, the order of the signals in the tree is not important. SMBDAT and SMBCLK are not to be included in the test tree.



APPLICATIONS INFORMATION

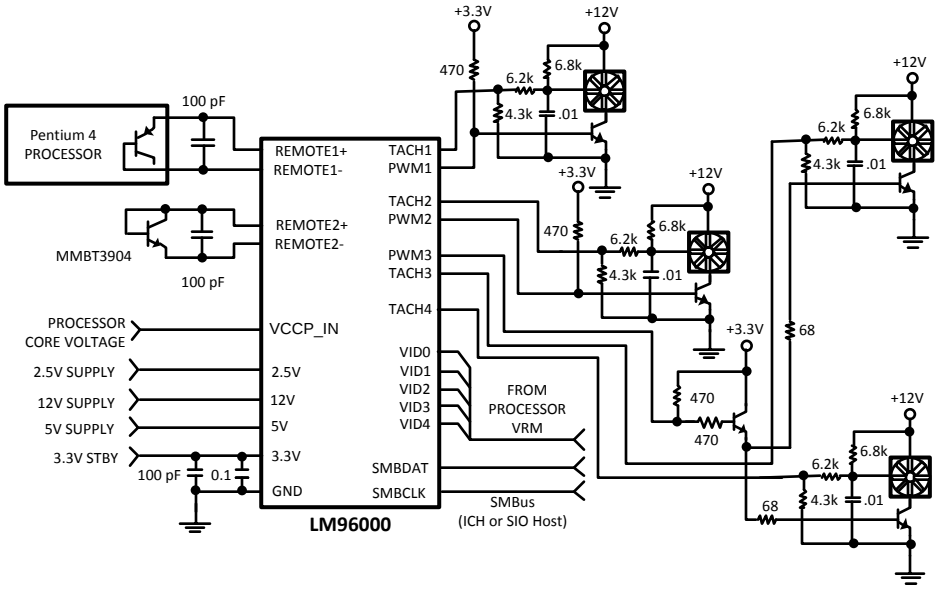


Figure 11. Typical Applications Schematic

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	33

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM96000CIMT/NOPB	Obsolete	Production	TSSOP (PW) | 24	-	-	Call TI	Call TI	0 to 125	LM96000 CIMT
LM96000CIMTX/NOPB	Active	Production	TSSOP (PW) | 24	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM96000 CIMT
LM96000CIMTX/NOPB.A	Active	Production	TSSOP (PW) | 24	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 125	LM96000 CIMT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

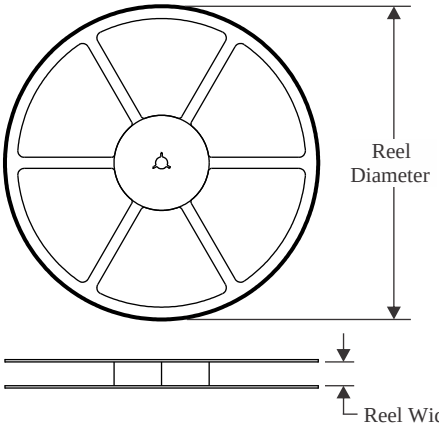
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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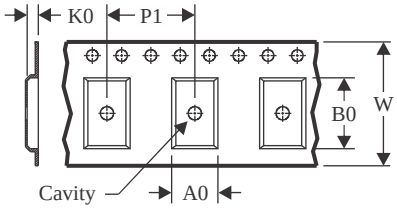
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

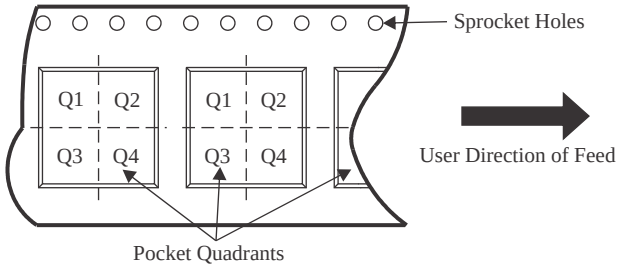


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

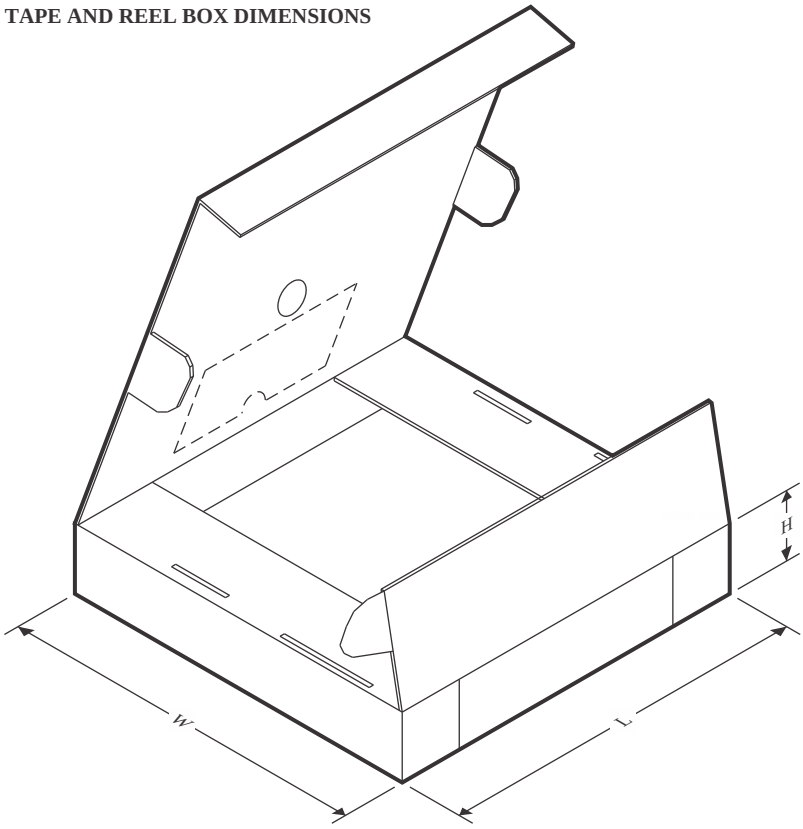
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM96000CIMTX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

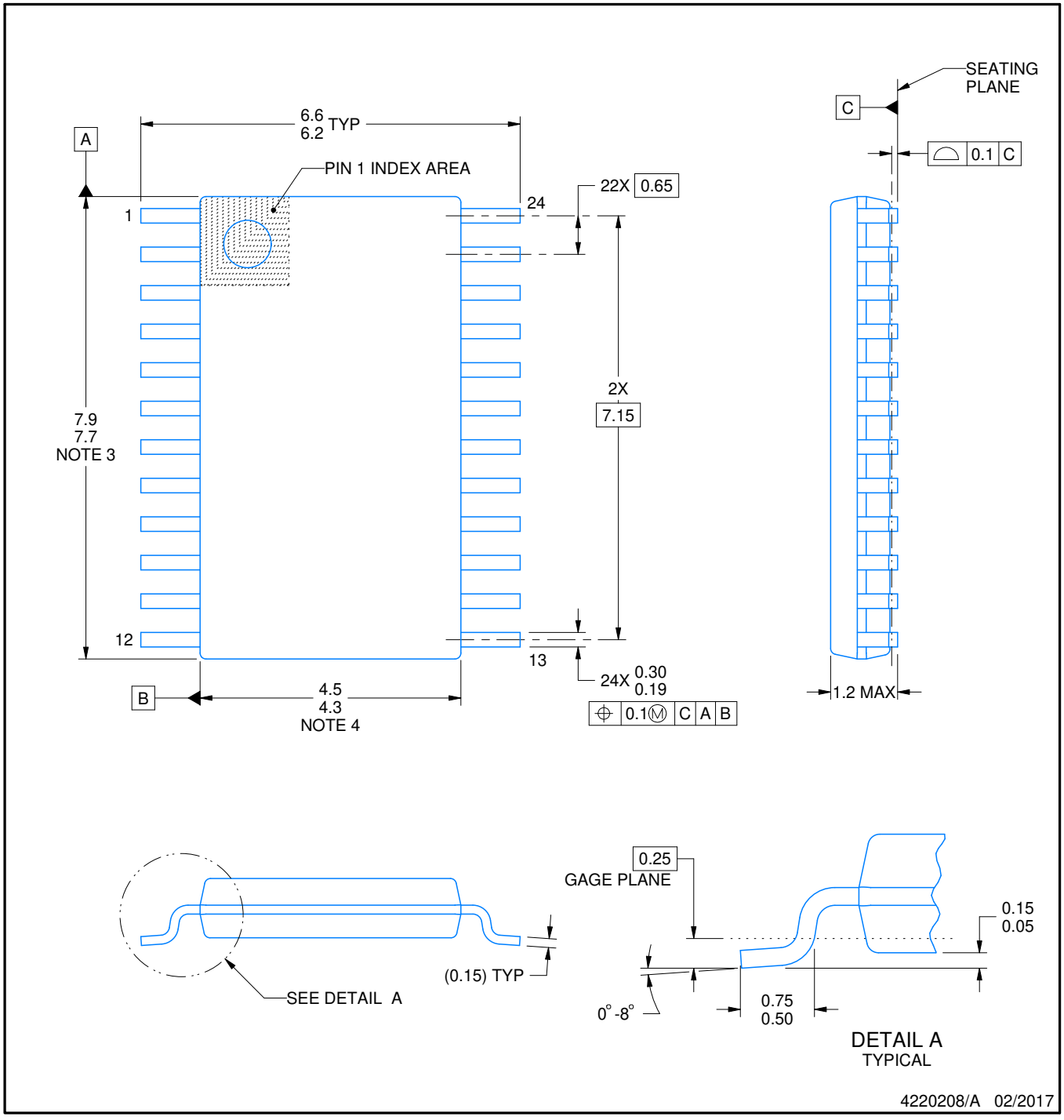
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM96000CIMTX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PW0024A

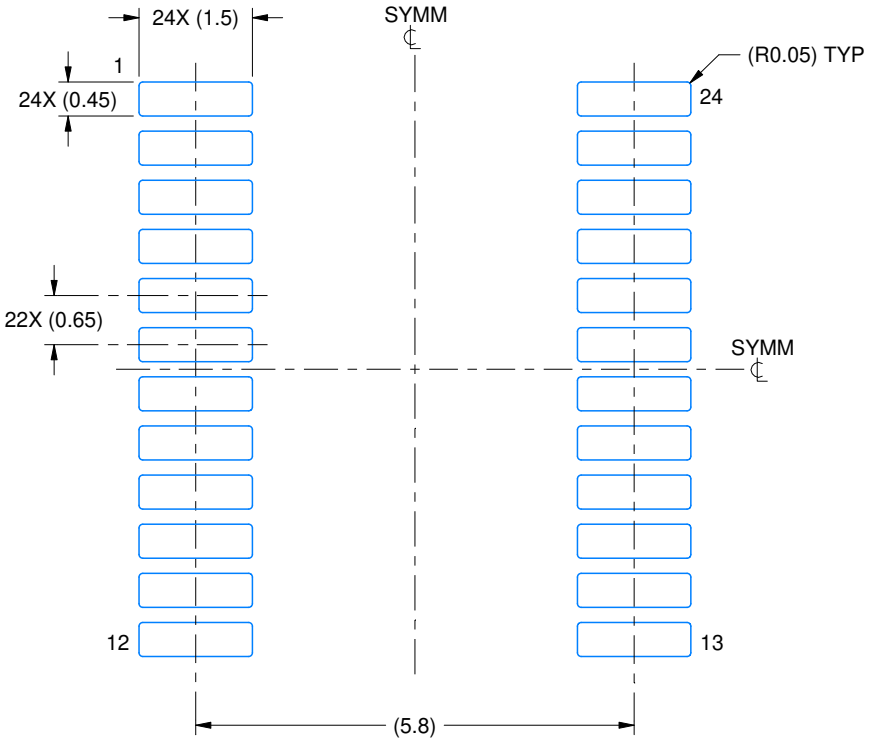
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

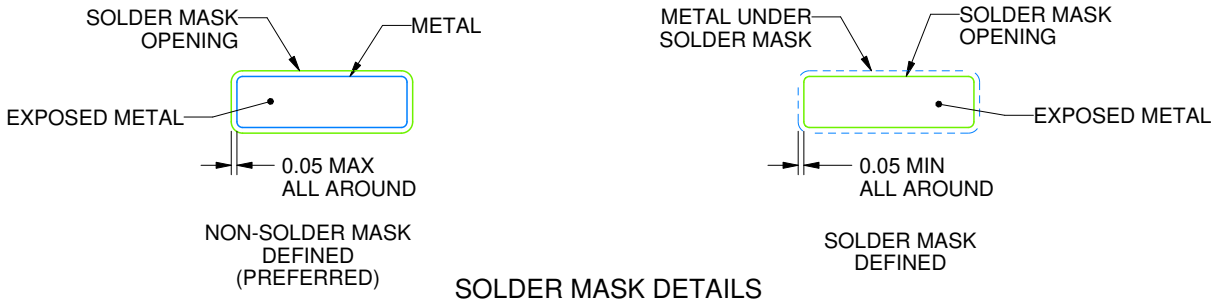


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

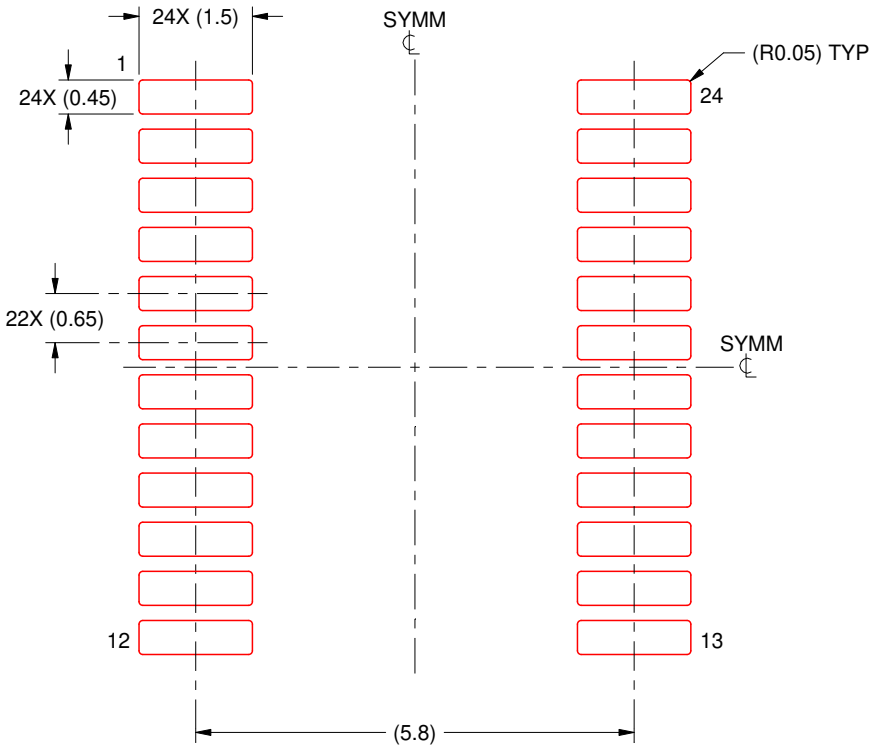


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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