LMC6024 Low Power CMOS Quad Operational Amplifier

Check for Samples: LMC6024

FEATURES

- **Specified for 100 kΩ and 5 kΩ Loads**
- **High Voltage Gain 120 dB**
- **Low Offset Voltage Drift 2.5 µV/°C**
- **Ultra Low Input Bias Vurrent 40 fA**
- **Input Common-mode Range Includes V^-**
- **Operating Range from +5V to +15V Supply**
- **Low Distortion 0.01% at 1 kHz**
- **Slew Rate 0.11 V/µs**
- **Micropower Operation 1 mW**

APPLICATIONS

- **High-impedance Buffer or Preamplifier**
- **Current-to-voltage Converter**
- **Long-term Integrator**
- **Sample-and-hold Circuit**
- **Peak Detector**
- **Medical Instrumentation**
- **Industrial Controls**

DESCRIPTION

The LMC6024 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^-, low input bias current and voltage gain (into 100 kΩ and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 1 mW.

This chip is built with Texas Instrument's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6022 datasheet for a CMOS dual operational amplifier with these same features.

Connection Diagram

Top View

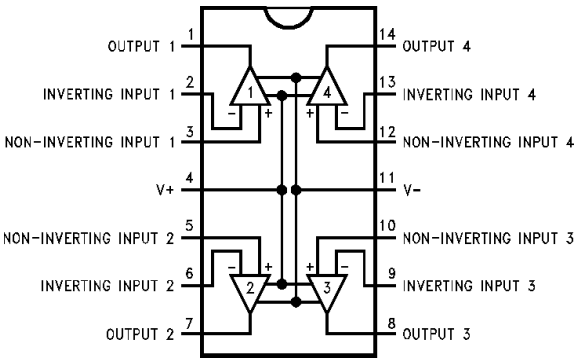

Figure 1. 14-Pin DIP and SOIC Package
See Package Number D0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Absolute Maximum Ratings (1)(2)

Differential Input Voltage		±Supply Voltage
Supply Voltage ($V^+ - V^-$)		16V
Lead Temperature	Soldering, 10 sec.	260°C
Storage Temperature Range		−65°C to +150°C
Voltage at Output/Input Pin		(V^+) + 0.3V, (V^-) − 0.3V
Current at Input Pin		±5 mA
Current at Output Pin		±18 mA
Current at Power Supply Pin		35 mA
Output Short Circuit to V^+		See (3)
Output Short Circuit to V^-		See (4)
Junction Temperature		150°C
ESD Tolerance (5)		1000V
Power Dissipation		See (6)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversly affect reliability.
(5) Human body model, 100 pF discharge through a 1.5 kΩ resistor.
(6) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Operating Ratings

Temperature Range		$-40°C \le T_J \le +85°C$
Supply Voltage Range		4.75V to 15.5V
Power Dissipation		See (1)
Thermal Resistance (θ_{JA}) (2)	14-Pin DIP	85°C/W
	14-Pin SOIC	115°C/W

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
(2) All numbers apply for packages soldered directly into a PC board.

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DC Electrical Characteristics

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Parameter		Test Conditions		Typical[1]	LMC6024I Limit[2]	Units
V_{OS}	Input Offset Voltage			1	9	mV
					11	Max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift			2.5		µV/°C
I_B	Input Bias Current			0.04		pA
					200	Max
I_{OS}	Input Offset Current			0.01	**100**	pA Max
R_{IN}	Input Resistance			>1		TeraΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12V		83	63	dB Min
		V^+ = 15V			**61**	
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V		83	63	dB Min
					61	
−PSRR	Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V		94	74	dB Min
					73	
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V For CMRR ≥ 50 DB		−0.4	−0.1	V Max
					0	
				V^+ − 1.9	V^+ − 2.3	V Min
					V^+ − 2.5	
A_V	Large Signal Voltage Gain	R_L = 100 kΩ[3]	Sourcing	1000	200	V/mV Min
					100	
			Sinking	500	90	V/mV Min
					40	
		R_L = 5 kΩ[3]	Sourcing	1000	100	V/mV Min
					75	
			Sinking	250	50	V/mV Min
					20	
V_O	Output Voltage Swing	V^+ = 5V R_L = 100 kΩ to 2.5V		4.987	4.40	V Min
					4.43	
				0.004	0.06	V Max
					0.09	
		V^+ = 5V R_L = 5 kΩ to 2.5V		4.940	4.20	V Min
					4.00	
				0.040	0.25	V Max
					0.35	
		V^+ = 15V R_L = 100 kΩ to 7.5V		14.970	14.00	V Min
					13.90	
				0.007	0.06	V Max
					0.09	
		V^+ = 15V R_L = 5 kΩ to 7.5V		14.840	13.70	V Min
					13.50	
				0.110	0.32	V Max
					0.40	

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or correlation.
(3) V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

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DC Electrical Characteristics (continued)

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Parameter		Test Conditions	Typical[1]	LMC6024I Limit[2]	Units
I_O	Output Current	V^+ = 5V Sourcing, V_O = 0V Sinking V_O = 5V [4]	22	13	mA Min
				9	
			21	13	mA Min
				9	
		V^+ = 15V Sourcing, V_O = 0V Sinking, V_O = 13V [5]	40	23	mA Min
				15	
			39	23	mA Min
				15	
I_S	Supply Current	All Four Amplifiers V_O = 1.5V	160	240	µA Max
				280	

(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(5) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

AC Electrical Characteristics

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Parameter		Test Conditions	Typical[1]	LMC6024I Limit[2]	Units
SR	Slew Rate	See[3]	0.11	0.05	V/µs Min
				0.03	
GBW	Gain-Bandwidth Product		0.35		MHz
θ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	See[4]	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/$\sqrt{Hz}$

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or correlation.
(3) V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

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Typical Performance Characteristics

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Supply Current vs Supply Voltage

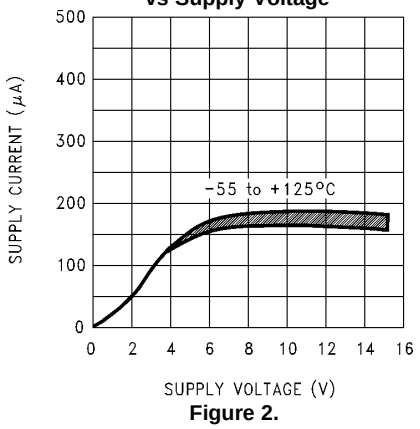

Figure 2.

Input Bias Current vs Temperature

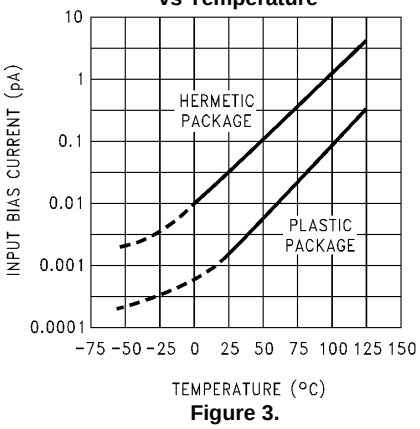

Figure 3.

Common-Mode Voltage Range vs Temperature

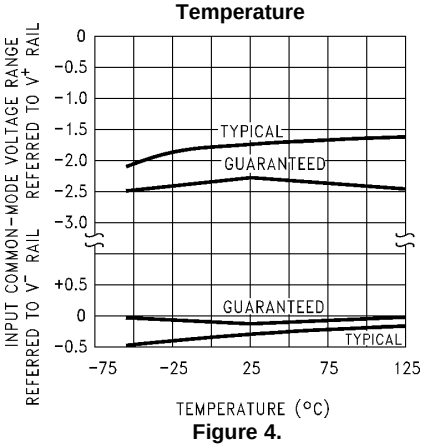

Figure 4.

Output Characteristics Current Sinking

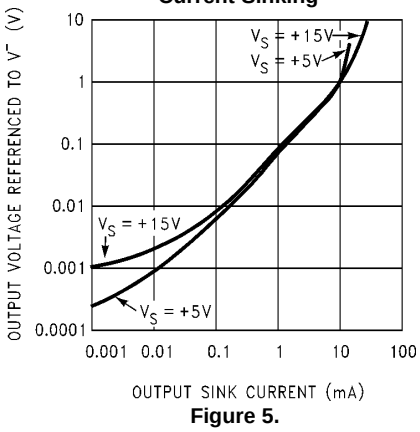

Figure 5.

Output Characteristics Current Sourcing

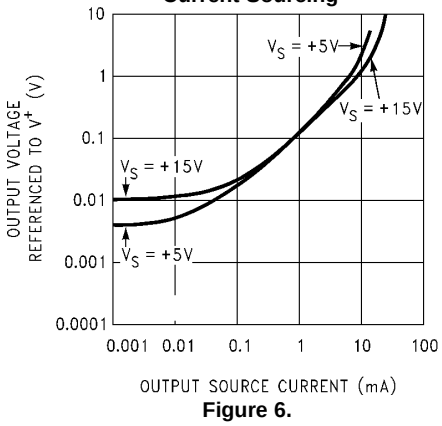

Figure 6.

Input Voltage Noise vs Frequency

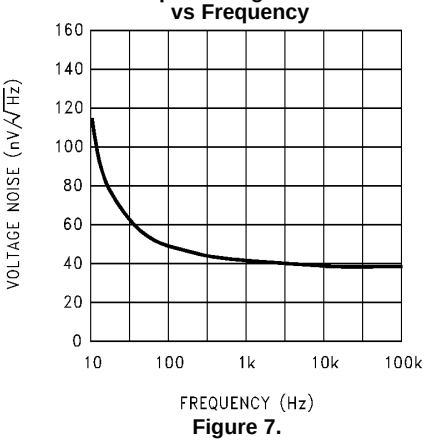

Figure 7.

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Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Crosstalk Rejection vs Frequency

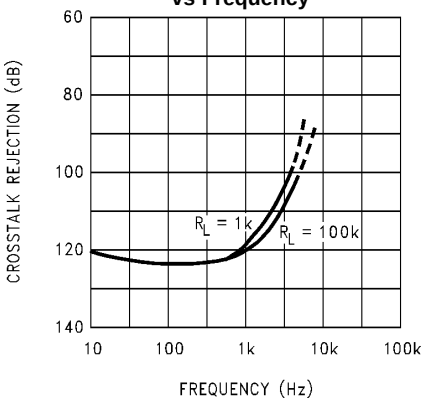

Figure 8.

CMRR vs Frequency

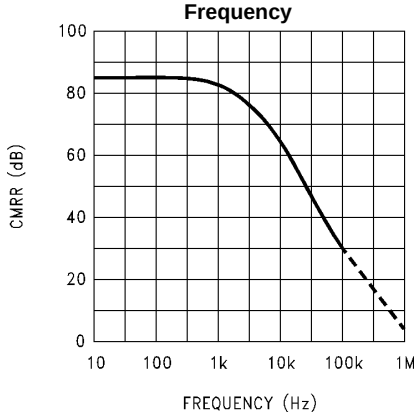

Figure 9.

CMRR vs Temperature

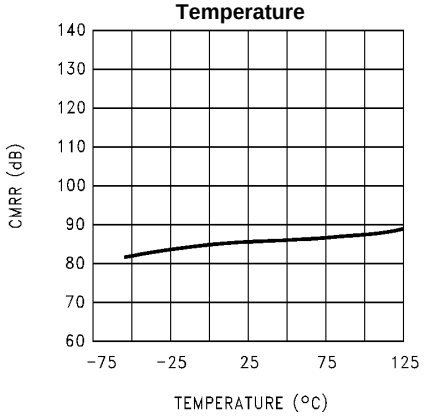

Figure 10.

Power Supply Rejection Ratio vs Frequency

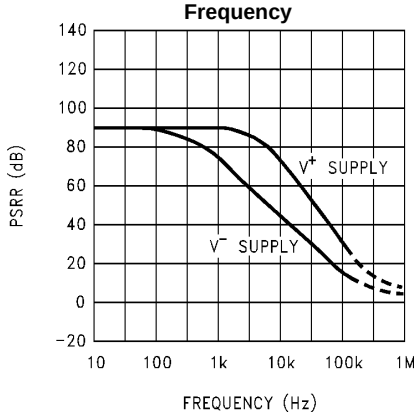

Figure 11.

Open-Loop Voltage Gain vs Temperature

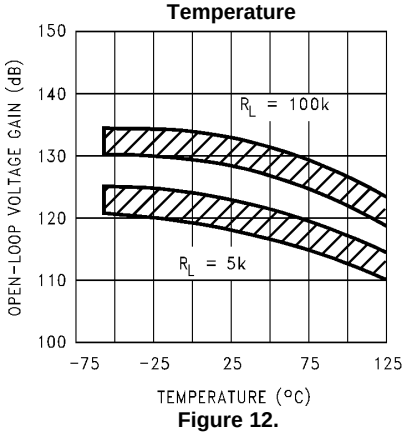

Figure 12.

Open-Loop Frequency Response

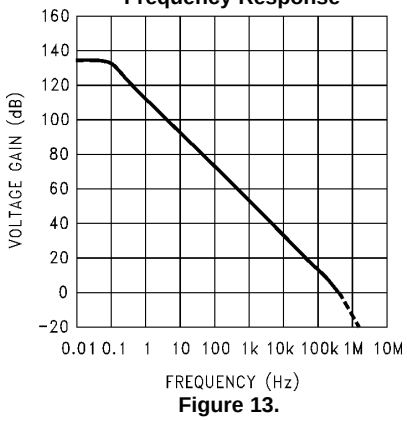

Figure 13.

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Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Gain and Phase Responses vs Load Capacitance

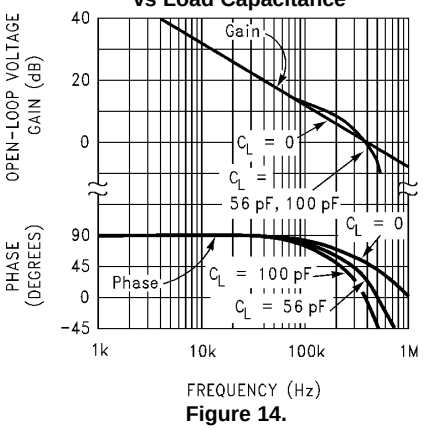

Figure 14.

Gain and Phase Responses vs Temperature

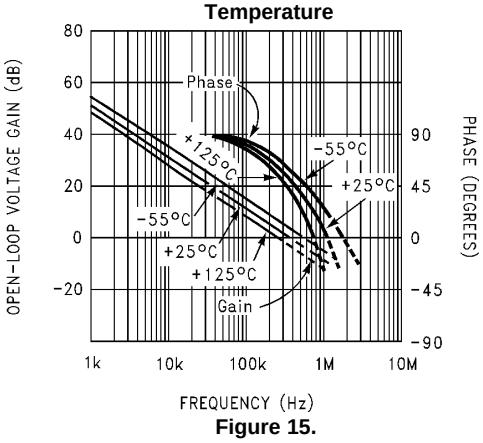

Figure 15.

Gain Error (V_{OS} vs V_{OUT})

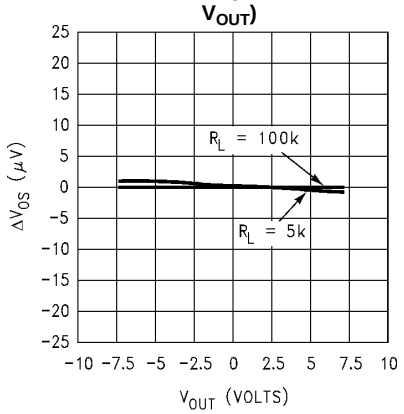

Figure 16.

Non-Inverting Slew Rate vs Temperature

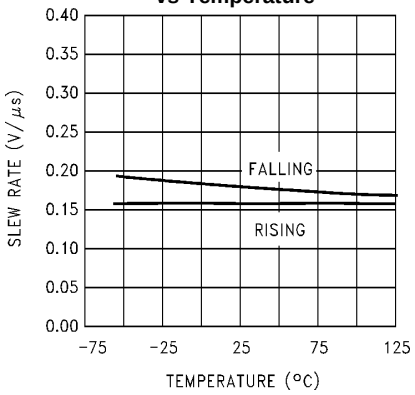

Figure 17.

Inverting Slew Rate vs Temperature

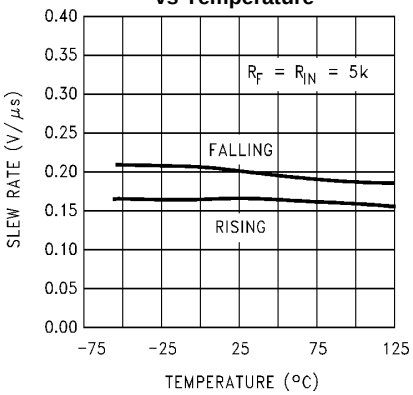

Figure 18.

Large-Signal Pulse Non-Inverting Response (A_V = +1)

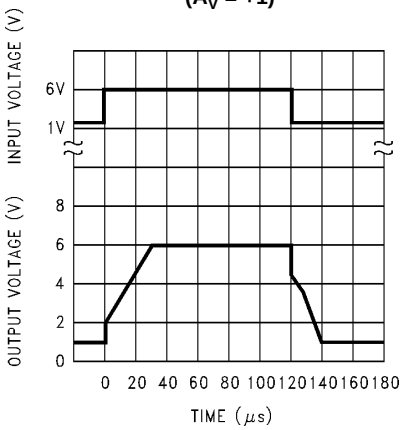

Figure 19.

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Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Non-Inverting Small Signal Pulse Response (A_V = +1)

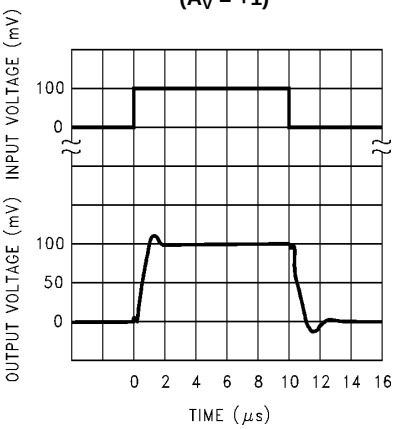


Figure 20.

Inverting Large-Signal Pulse Response

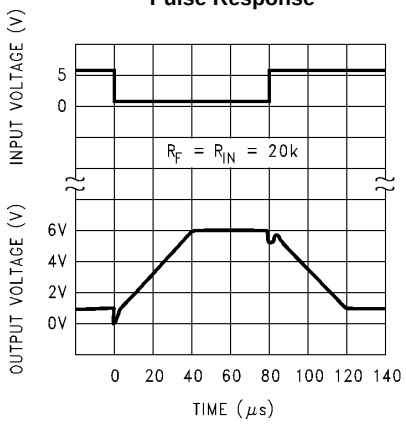


Figure 21.

Inverting Small-Signal Pulse Response

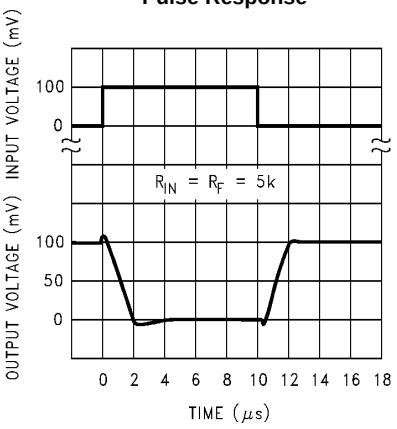
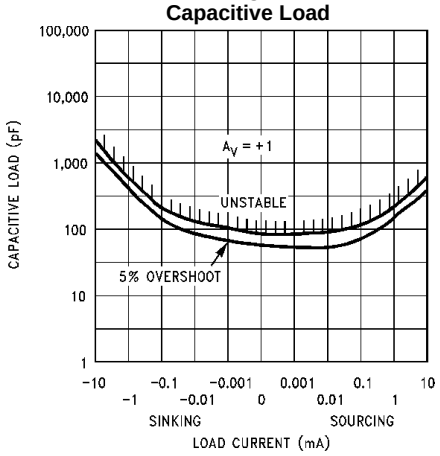


Figure 22.

Stability vs Capacitive Load



Avoid resistive loads of less than 500Ω, as they may cause instability.

Figure 23.

Stability vs Capacitive Load

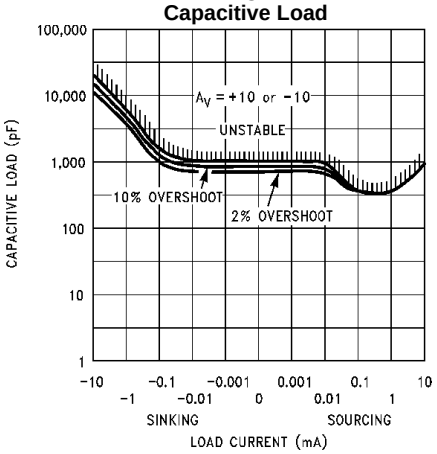


Figure 24.

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APPLICATION HINTS

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6024 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

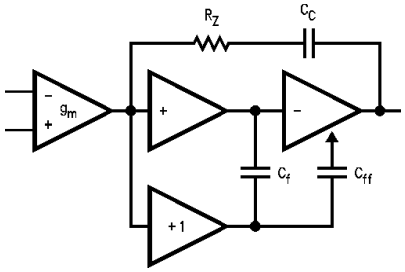

Figure 25. LMC6024 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characterisitics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6024 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capcitance is near the threshold for oscillation.

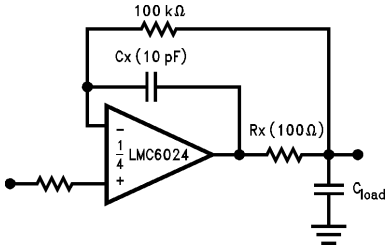

Figure 26. Rx, Cx Improve Capacitive Load Tolerance

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Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 27). Typically a pull up resistor conducting 50 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see DC Electrical Characteristics).

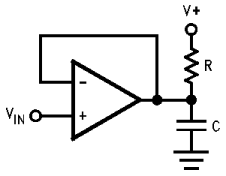

Figure 27. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6024, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6024's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 28. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6024's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 28, Figure 30, and Figure 31 for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 32.

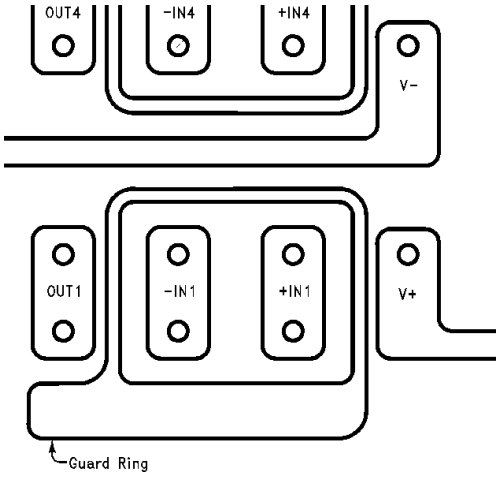

Figure 28. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)

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Guard Ring Connections

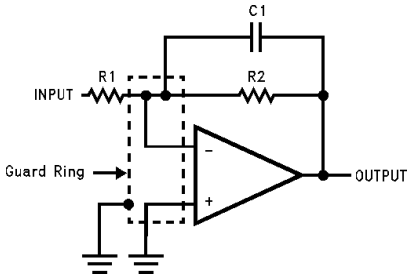


Figure 29. Inverting Amplifier Guard Ring Connections

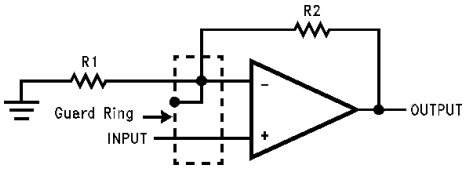


Figure 30. Non-Inverting Amplifier Guard Ring Connections

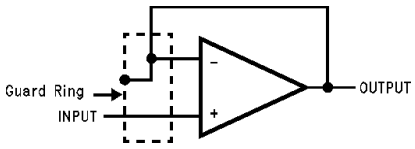


Figure 31. Follower Guard Ring Connections

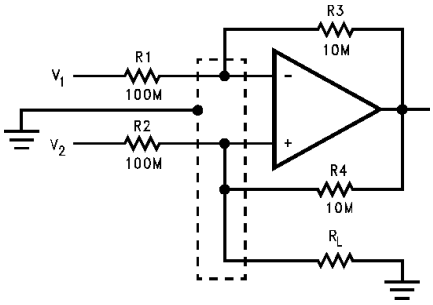
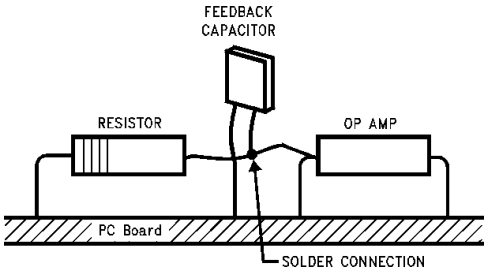


Figure 32. Howland Current Pump Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 33.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 33. Air Wiring

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BIAS CURRENT TESTING

The test method of Figure 34 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2. \quad (1)$$

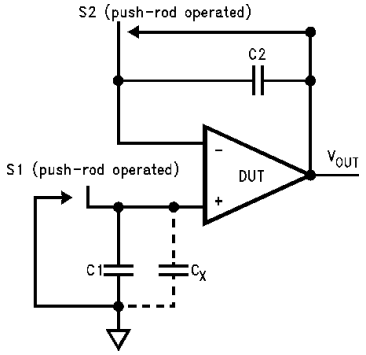


Figure 34. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

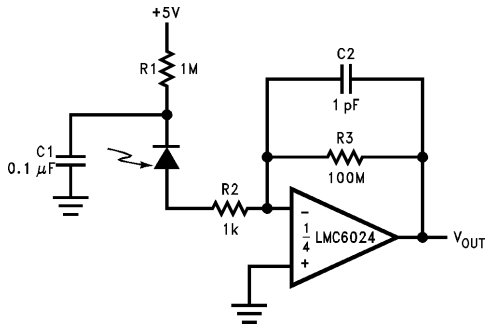
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X) \quad (2)$$

where C_X is the stray capacitance at the +input.

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)



A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Figure 35. Photodiode Current-to-Voltage Converter

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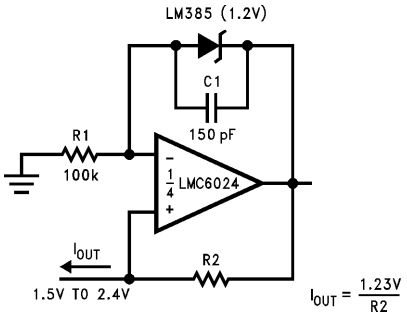
(V^+ = 5.0 V_{DC})

Figure 36.



(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Figure 37. Micropower Current Source

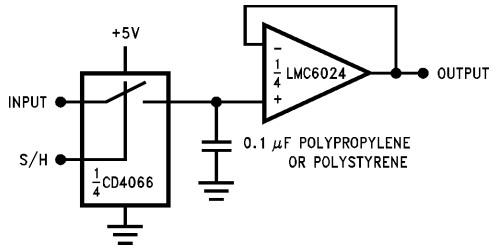
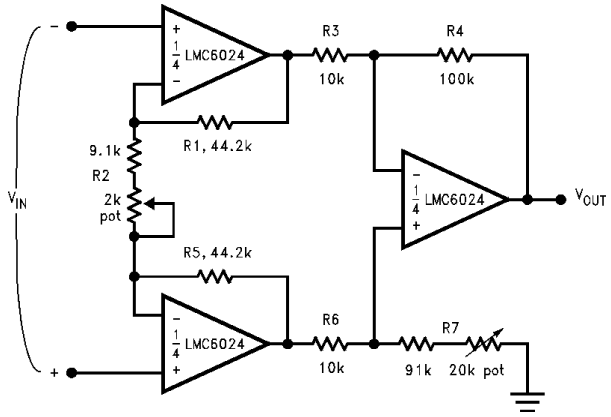


Figure 38. Low-Leakage Sample-and-Hold



If R1 = R5, R3 = R6, and R4 = R7;
Then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}.$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Figure 39. Instrumentation Amplifier

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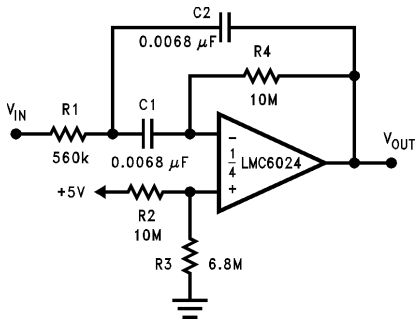
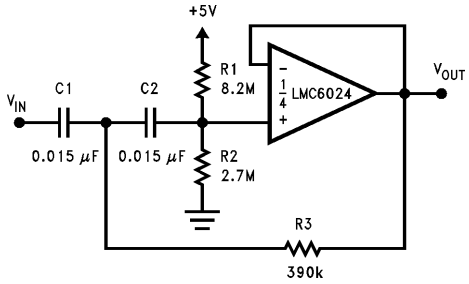
(V^+ = 5.0 V_{DC})



f_O = 10 Hz
Q = 2.1
Gain = −8.8

Figure 40. 10 Hz Bandpass Filter



f_c = 10 Hz
d = 0.895
Gain = 1

Figure 41. 10 Hz High-Pass Filter (2 dB Dip)

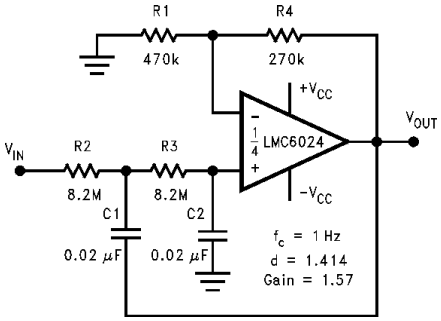


Figure 42. 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)

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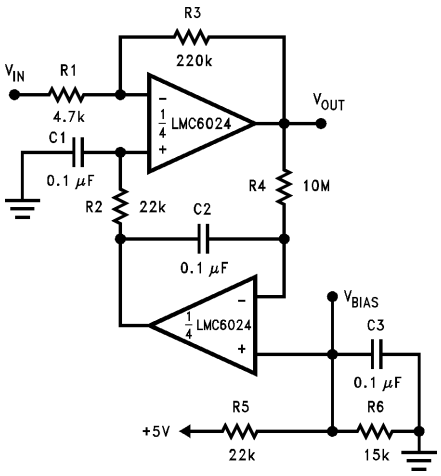
(V^+ = 5.0 V_{DC})



Gain = −46.8
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

Figure 43. High Gain Amplifier with Offset Voltage Reduction

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6024IM/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6024IM
LMC6024IM/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6024IM
LMC6024IM/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6024IM
LMC6024IMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6024IM
LMC6024IMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6024IM
LMC6024IMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6024IM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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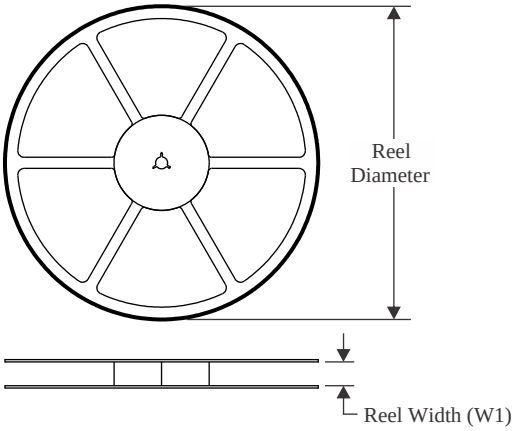
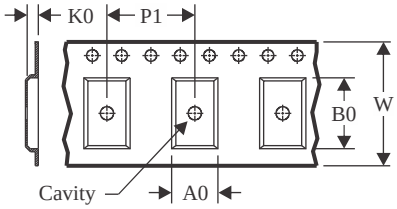
TAPE AND REEL INFORMATION

REEL DIMENSIONS

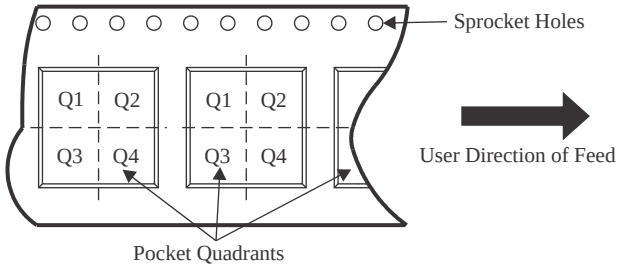


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

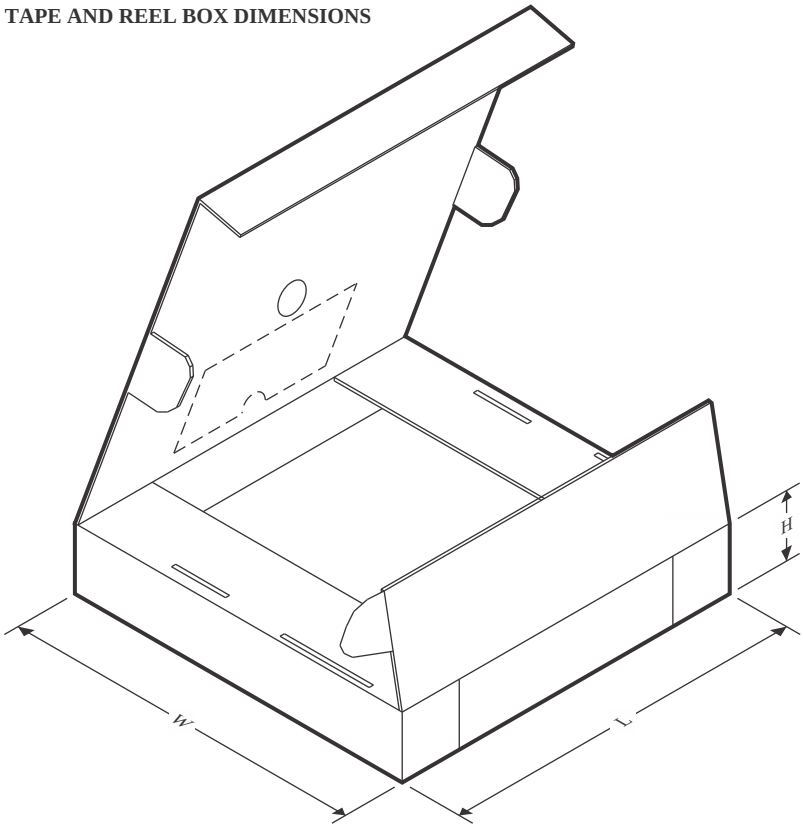
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6024IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

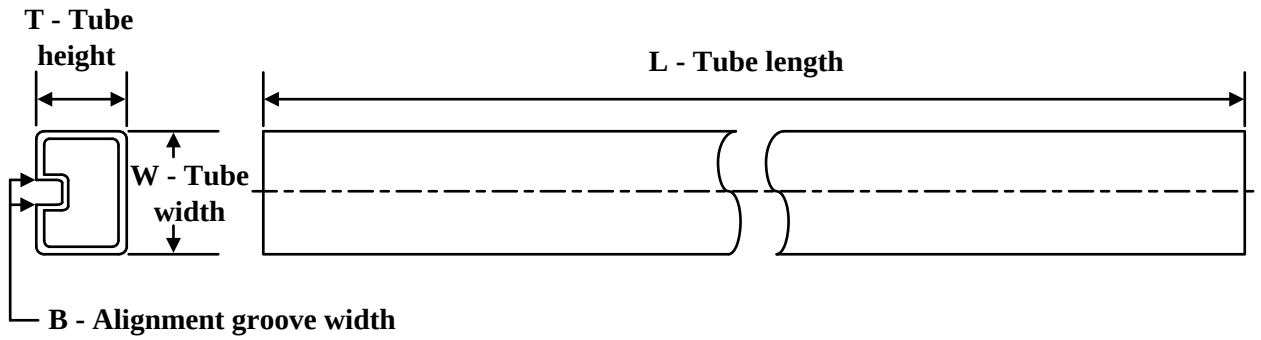
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6024IMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6024IM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMC6024IM/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
LMC6024IM/NOPB.B	D	SOIC	14	55	495	8	4064	3.05

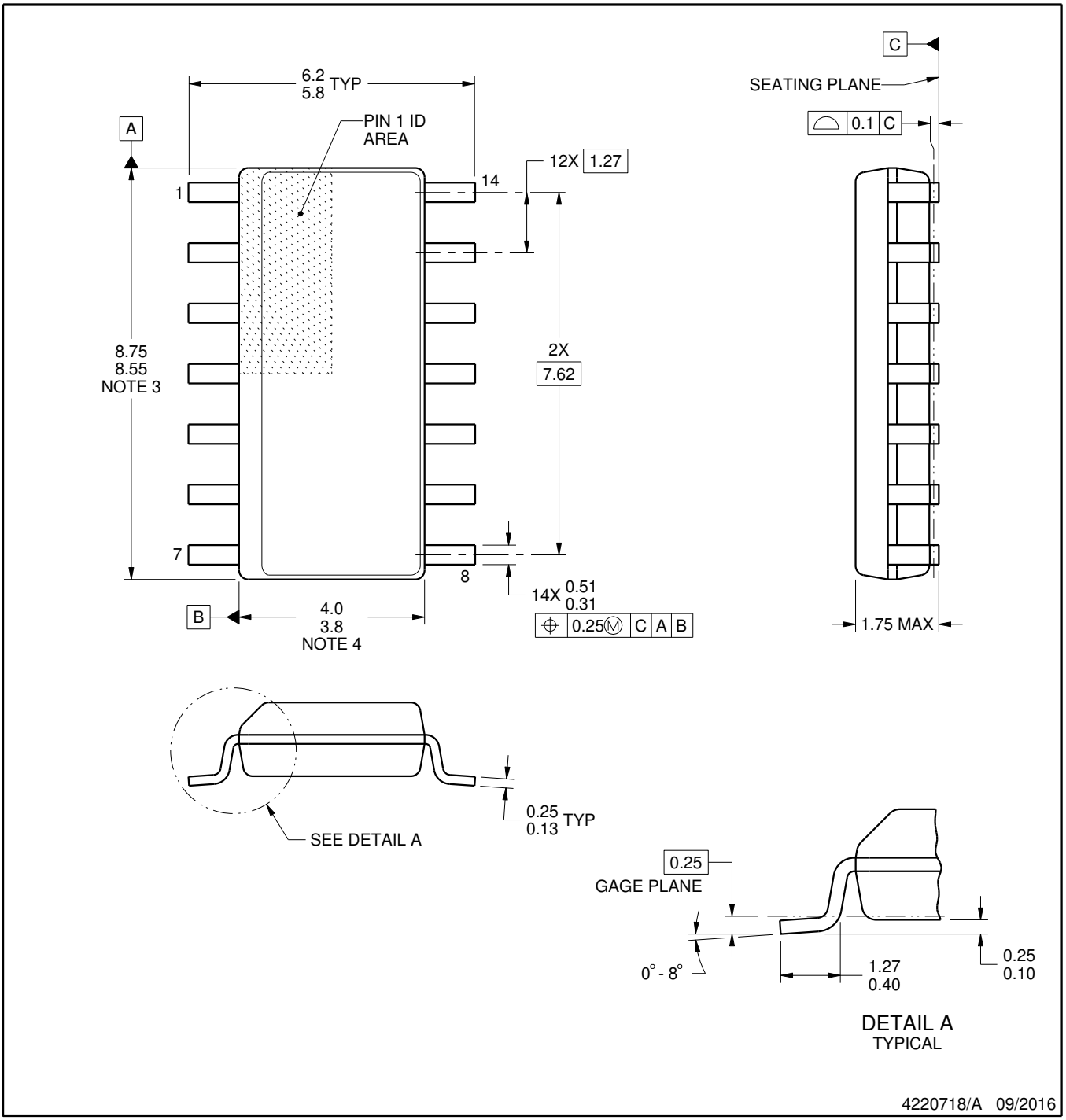


PACKAGE OUTLINE

D0014A

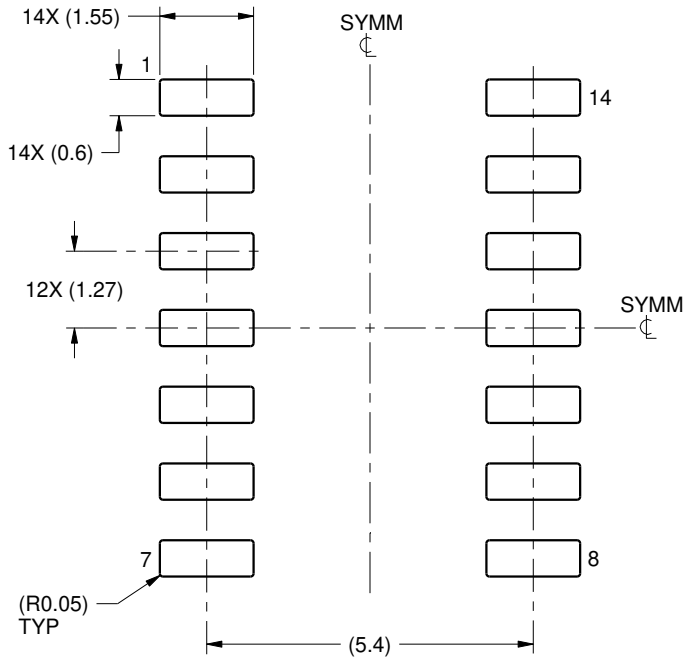
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

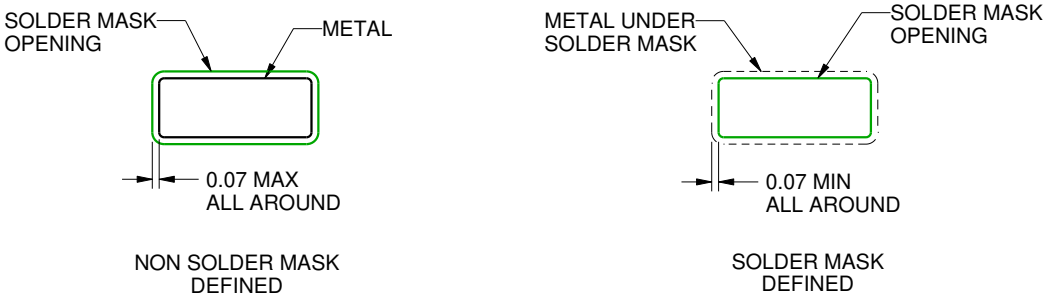


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

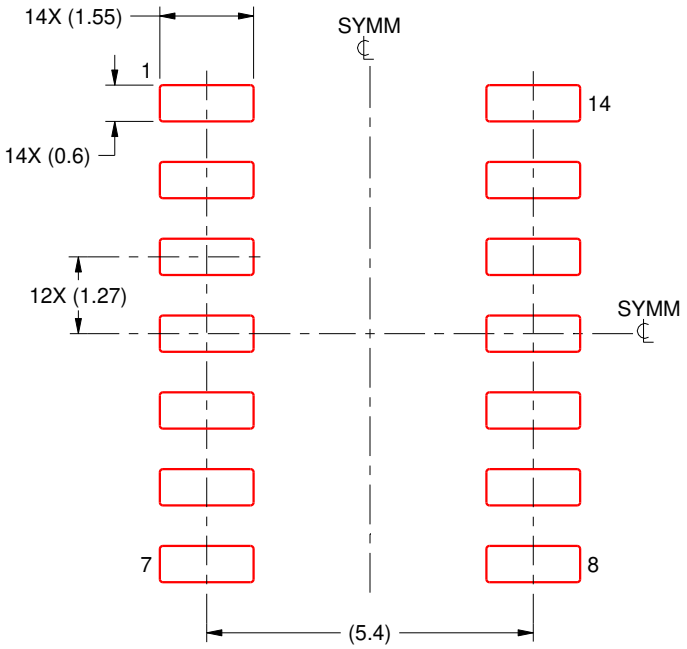
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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