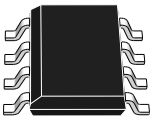
LMC6482

Datasheet

16 V CMOS dual rail-to-rail input and output, operational amplifiers



MiniSO8



SO8

Features

- Low input offset voltage: 2 mV max.
- Rail-to-rail input and output
- Excellent CMRR : 98 dB @ 16 V
- Low current consumption: 900 µA max.
- Gain bandwidth product: 2.7 MHz
- Low supply voltage: 2.7 - 16 V
- Unity gain stable
- Low input bias current: 50 pA max.
- High ESD tolerance: 4 kV HBM
- Extended temp. range: -40 °C to +125 °C

Application

- Data acquisition systems
- Battery-powered instrumentation
- Instrumentation amplifier
- Active filtering
- DAC buffer
- High-impedance sensor interface
- Current sensing (high and low side)

Maturity status link
LMC6482

Description

The LMC6482 offer rail-to-rail input and output functionality allowing this product to be used on full range input and output without limitation.

This rail to rail capability combined with excellent accuracy makes this device ideal for systems such as data acquisition, that require wide input signal range.

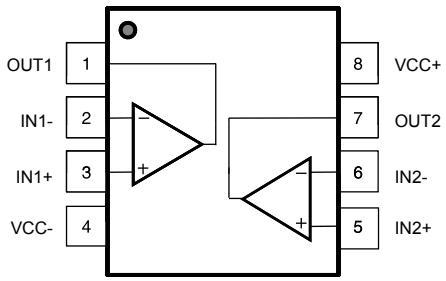
This is particularly useful for a low-voltage supply such as 2.7 V that the LMC6482 is able to operate with.

Thus, the LMC6482 has the great advantage of offering a large span of supply voltages, ranging from 2.7 V to 16 V. It can be used in multiple applications with a unique reference.

Low input bias current performance makes the LMC6482 perfect when used for signal conditioning in sensor interface applications. In addition, low- side and high-side current measurements can be easily made thanks to rail-to-rail functionality.

1 Pin configuration

Figure 1. **Pin connection (top view)**



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		18	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	mV
V_{in}	Input voltage		(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	V
I_{in}	Input current (3)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient (4)(5)	MiniSO8	190	°C/W
		SO-8	125	
T_j	Maximum junction temperature		150	°C
ESD	HBM: Human body model (6)		4000	V
	MM: machine model (7)		100	
	CDM: charged device model (8)		1500	
	Latch-up immunity		200	mA

1. *All voltage values, except the differential voltage are with respect to the network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. See for the precautions to follow when using LMC6482 with a high differential input voltage.*
3. *Input current must be limited by a resistor in series with the inputs.*
4. *R_{th} are typical values.*
5. *Short-circuits can cause excessive heating and destructive dissipation.*
6. *According to JEDEC standard JESD22-A114F.*
7. *According to JEDEC standard JESD22-A115A.*
8. *According to ANSI/ESD STM5.3.1.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. Electrical characteristics V_{CC+} = +4 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 ° C, and R_L > 10 kΩ connected to V_{CC}/2 (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Vio	Input offset voltage	V_{icm} = V_{CC}/2			2	mV
		T_{min} < T_{op} < T_{max}			2.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				5	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		1		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current (1)	V_{out} = V_{CC}/2		1	50	pA
		T_{min} < T_{op} < T_{max}			200	
I_{io}	Input offset current (1)	V_{out} = V_{CC}/2		1	50	
		T_{min} < T_{op} < T_{max}			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 4.1 V, V_{out} = V_{CC}/2	65	85		dB
		T_{min} < T_{op} < T_{max}	60			
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out}= 0.3 to 3.7 V	85	136		
		T_{min} < T_{op} < T_{max}	80			
		R_L = 10 kΩ, V_{out} = 0.2 to 3.8 V	85	140		
		T_{min} < T_{op} < T_{max}	80			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L=2 kΩ to V_{CC}/2		28	50	mV
		T_{min} < T_{op} < T_{max}			60	
		R_L = 10 kΩ to V_{CC}/2		6	15	
		T_{min} < T_{op} < T_{max}			20	
V_{OL}	Low level output voltage	R_L = 2 kΩ to V_{CC}/2		23	50	mV
		T_{min} < T_{op} < T_{max}			60	
		R_L = 10 kΩ to V_{CC}/2		5	15	
		T_{min} < T_{op} < T_{max}			20	
I_{out}	I_{sink}	V_{out} = V_{CC}	25	37		mA
		T_{min} < T_{op} < T_{max}	15			
	I_{source}	V_{out} = 0 V	35	45		
		T_{min} < T_{op} < T_{max}	20			
I_{CC}	Supply current per amplifier	No load, V_{out} = V_{CC}/2		570	800	µA
		T_{min} < T_{op} < T_{max}			900	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.9	2.7		MHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		50		Degrees
Gm	Gain margin	R_L = 10 kΩ, C_L = 100 pF		15		dB
SRn	Negative slew rate	Av = 1, V_{out} = 3 V_{PP}, 10 % to 90%	0.6	0.85		V/µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SRn	Negative slew rate	$T_{min} < T_{op} < T_{max}$	0.5			V/µs
SRp	Positive slew rate	Av = 1, V_{out} = 3 V_{PP}, 10 % to 90%	1.0	1.4		
		$T_{min} < T_{op} < T_{max}$	0.9			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, BW = 22 kHz, V_{in} = 0.8 V_{PP}		0.001		%

1. *Maximum values are guaranteed by design.*
2. *Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see Section 5.6 Long term input offset voltage drift).*

Table 4. Electrical characteristics V_{CC+} = +10 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 ° C, and R_L > 10 kΩ connected to V_{CC}/2 (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Vio	Input offset voltage	V_{icm} = V_{CC}/2			2	mV
		T_{min} < T_{op} < T_{max}			2.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				5	µV/°C
ΔV_{io}	Longterm input offset voltage drift (2)	T = 25 °C		25		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current (1)	V_{out} = V_{CC}/2		1	50	pA
		T_{min} < T_{op} < T_{max}			200	
I_{io}	Input offset current (1)	V_{out} = V_{CC}/2		1	50	
		T_{min} < T_{op} < T_{max}			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR	Common mode rejectionratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 10.1 V, V_{out} = V_{CC}/2	72	92		dB
		T_{min} < T_{op} < T_{max}	67			
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out}= 0.3 to 9.7 V	90	140		
		T_{min} < T_{op} < T_{max}	85			
		R_L = 10 kΩ, V_{out} = 0.2 to 9.8 V	90			
		T_{min} < T_{op} < T_{max}	85			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L=2 kΩ to V_{CC}/2		45	70	mV
		T_{min} < T_{op} < T_{max}			80	
		R_L = 10 kΩ to V_{CC}/2		10	30	
		T_{min} < T_{op} < T_{max}			40	
V_{OL}	Low level output voltage	R_L = 2 kΩ to V_{CC}/2		42	70	mV
		T_{min} < T_{op} < T_{max}			80	
		R_L = 10 kΩ to V_{CC}/2		9	30	
		T_{min} < T_{op} < T_{max}			40	
I_{out}	I_{sink}	V_{out} = V_{CC}	30	39		mA
		T_{min} < T_{op} < T_{max}	15			
	I_{source}	V_{out} = 0 V	50	69		
		T_{min} < T_{op} < T_{max}	40			
I_{CC}	Supply current per amplifier	No load, V_{out} = V_{CC}/2		630	850	µA
		T_{min} < T_{op} < T_{max}			1000	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.9	2.7		MHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		53		Degrees
Gm	Gain margin	R_L = 10 kΩ, C_L = 100 pF		15		dB
SRn	Negative slew rate	Av = 1, V_{out} = 8 V_{PP}, 10 % to 90%	0.8	1		V/µs
		T_{min} < T_{op} < T_{max}	0.7			
SRp	Positive slew rate	Av = 1, V_{out} = 8 V_{PP}, 10 % to 90%	1.0	1.3		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SRp	Positive slew rate	$T_{min} < T_{op} < T_{max}$	0.9			V/µs
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, BW = 22 kHz, V_{in} = 5 V_{PP}		0.0003		%

1. *Maximum values are guaranteed by design.*
2. *Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see Section 5.6 Long term input offset voltage drift).*

Table 5. Electrical characteristics V_{CC+} = +16 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 ° C, and R_L > 10 kΩ connected to V_{CC}/2 (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Vio	Input offset voltage	V_{icm} = V_{CC}/2			2	mV
		T_{min} < T_{op} < T_{max}			2.5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				5	µV/°C
ΔV_{io}	Longterm input offset voltage drift (2)	T = 25 °C		500		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current (1)	V_{out} = V_{CC}/2		1	50	pA
		T_{min} < T_{op} < T_{max}			200	
I_{io}	Input offset current (1)	V_{out} = V_{CC}/2		1	50	
		T_{min} < T_{op} < T_{max}			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 16.1 V, V_{out} = V_{CC}/2	75	98		dB
		T_{min} < T_{op} < T_{max}	70			
SVRR	Supply voltage rejection ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{cc} = 4 to 16 V	100	131		
		T_{min} < T_{op} < T_{max}	90			
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out}= 0.3 to 15.7 V	90	146		
		T_{min} < T_{op} < T_{max}	85			
		R_L = 10 kΩ, V_{out} = 0.2 to 15.8 V	90	149		
		T_{min} < T_{op} < T_{max}	85			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L = 2 kΩ to V/2		70	130	mV
		T_{min} < T_{op} < T_{max}			150	
		R_L = 10 kΩ		16	40	
		T_{min} < T_{op} < T_{max}			50	
V_{OL}	Low level output voltage	R_L = 2 kΩ		70	130	mV
		T_{min} < T_{op} < T_{max}			150	
		R_L = 10 kΩ		15	40	
		T_{min} < T_{op} < T_{max}			50	
I_{out}	I_{sink}	V_{out} = V_{CC}	30	40		mA
		T_{min} < T_{op} < T_{max}	15			
	I_{source}	V_{out} = 0 V	50	68		
		T_{min} < T_{op} < T_{max}	45			
I_{CC}	Supply current per amplifier	No load, V_{out} = V_{CC}/2		660	900	µA
		T_{min} < T_{op} < T_{max}			1000	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.9	2.7		MHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		Degrees
Gm	Gain margin	R_L = 10 kΩ, C_L = 100 pF		15		dB
SRn	Negative slew rate	Av = 1, V_{out} = 10 V_{PP}, 10 % to 90%	0.7	0.95		V/µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SRn	Negative slew rate	$T_{min} < T_{op} < T_{max}$	0.6			V/µs
SRp	Positive slew rate	Av = 1, V_{out} = 10 V_{PP}, 10 % to 90%	1	1.4		
		$T_{min} < T_{op} < T_{max}$	0.9			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, BW = 22 kHz, V_{in} = 10 V_{PP}		0.0002		%

1. *Maximum values are guaranteed by design.*
2. *Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see Section 5.6 Long term input offset voltage drift).*

4 Electrical characteristic curves

Figure 2. Supply current vs. supply voltage

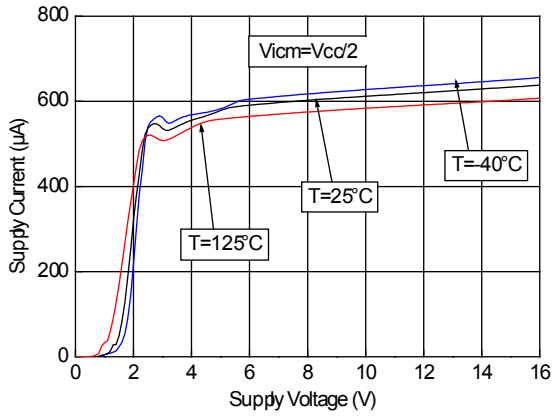


Figure 3. Input offset voltage distribution at V_{CC} = 16 V

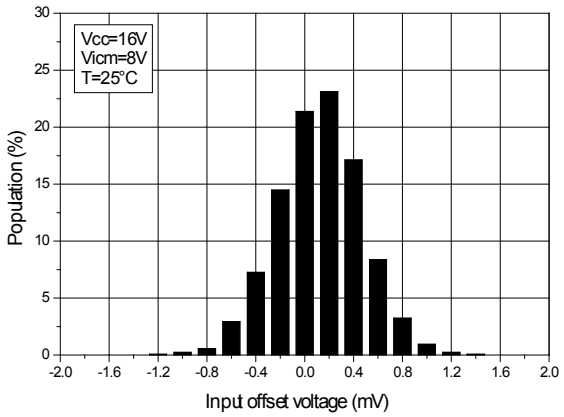


Figure 4. Input offset voltage distribution at V_{CC} = 4 V

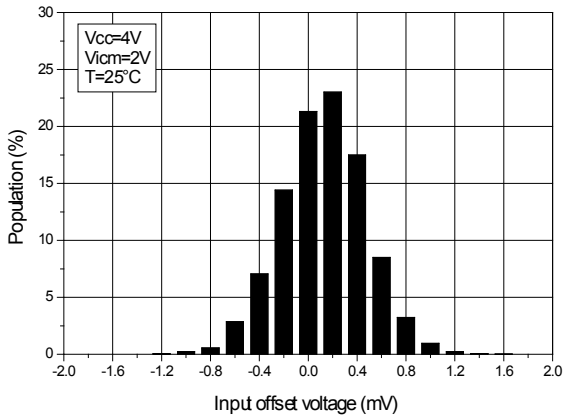


Figure 5. Channel separation

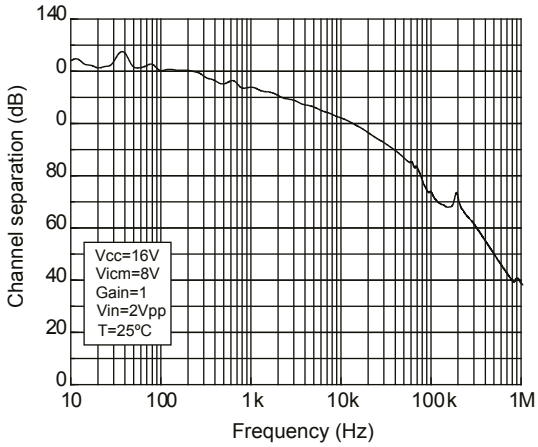


Figure 6. Output current vs. output voltage at V_{CC} = 2.7 V

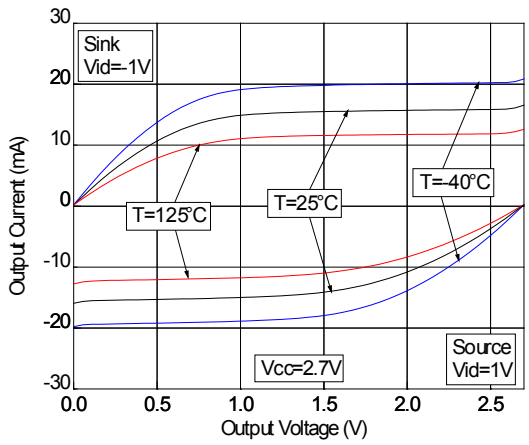


Figure 7. Output current vs. output voltage at V_{CC} = 16 V

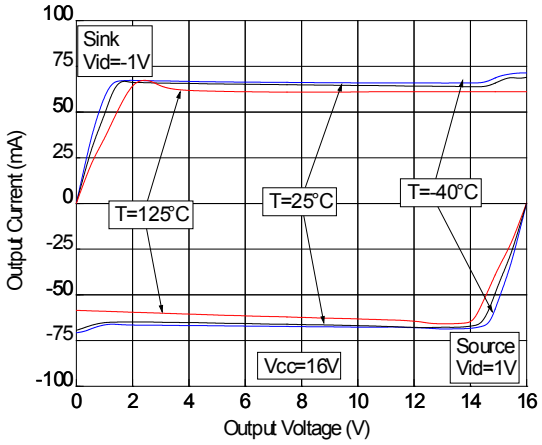


Figure 8. Output low voltage vs. supply voltage

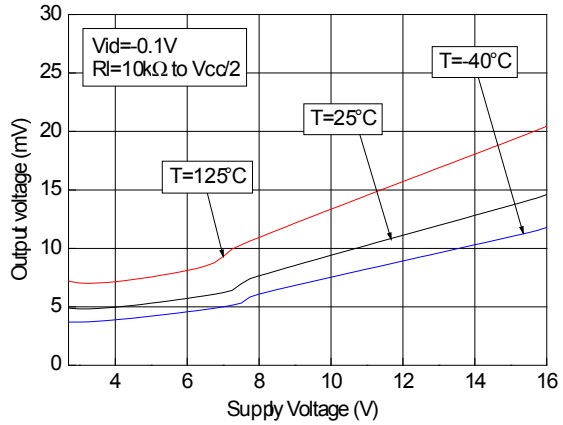


Figure 9. Output high voltage (drop from V_{CC+}) vs. supply voltage

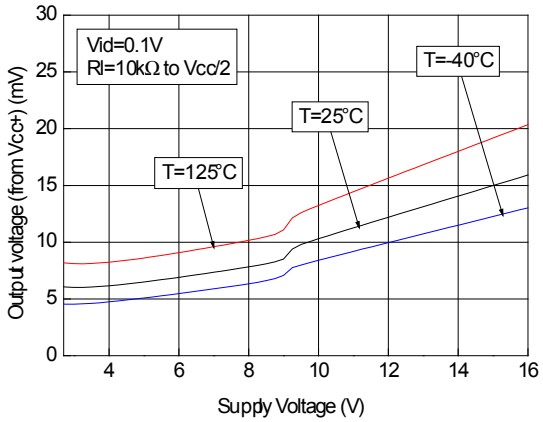


Figure 10. Output voltage vs. input voltage close to the rail at V_{CC} = 16 V

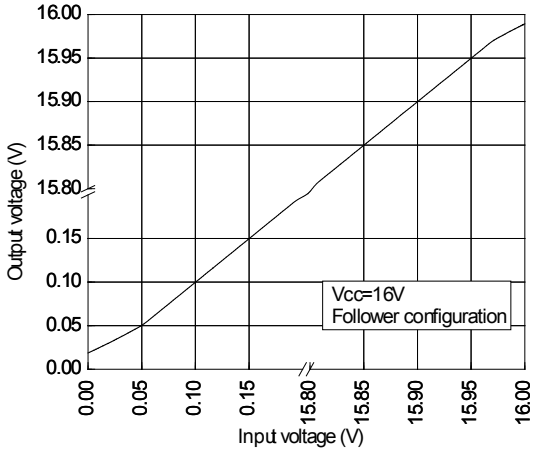


Figure 11. Slew rate vs. supply voltage

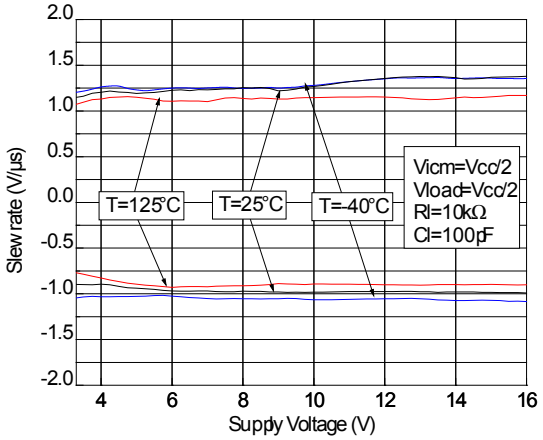


Figure 12. Negative slew rate at V_{CC} = 16 V

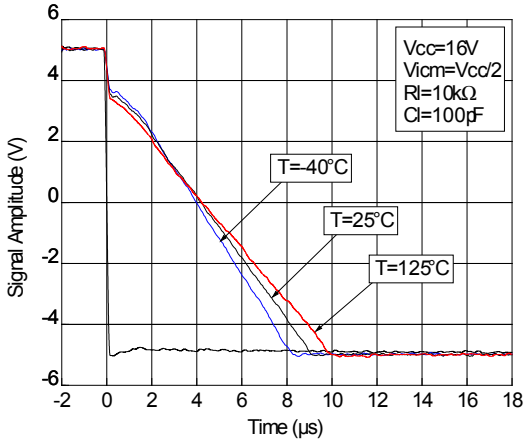


Figure 13. Positive slew rate at V_{CC} = 16 V

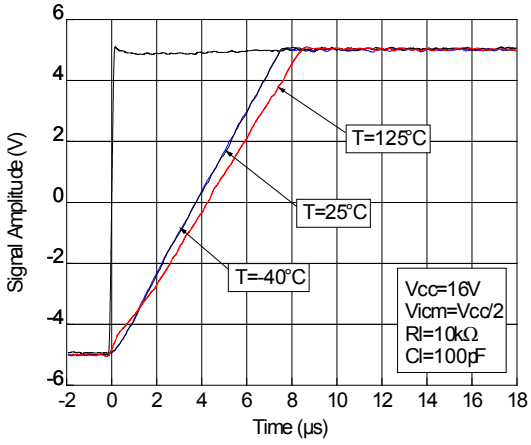


Figure 14. Response to a small input voltage step

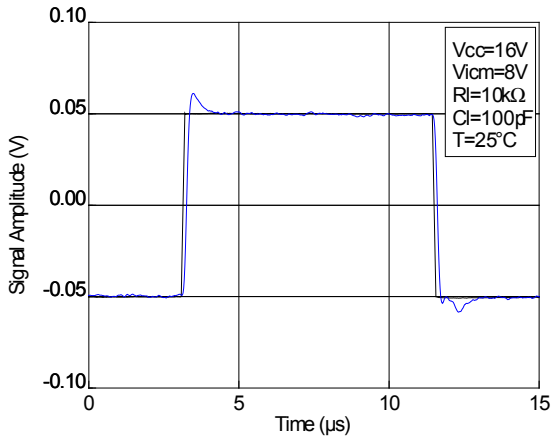


Figure 15. Recovery behavior after a negative step on the input

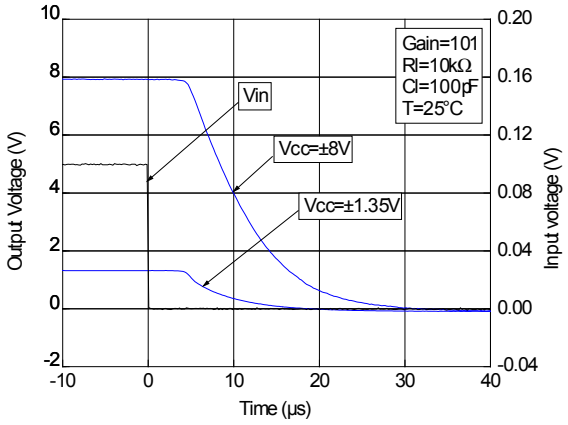


Figure 16. Recovery behavior after a positive step on the input

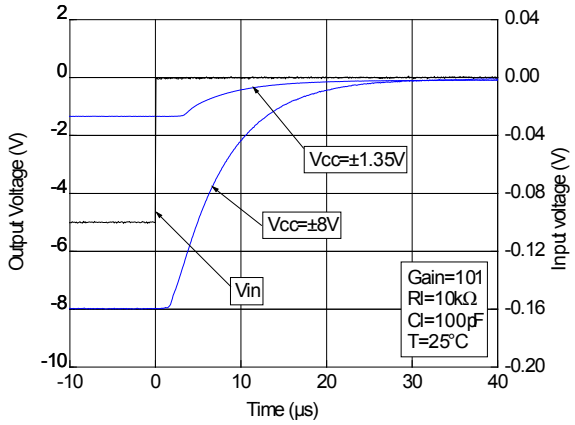


Figure 17. Bode diagram at V_{CC} = 2.7 V

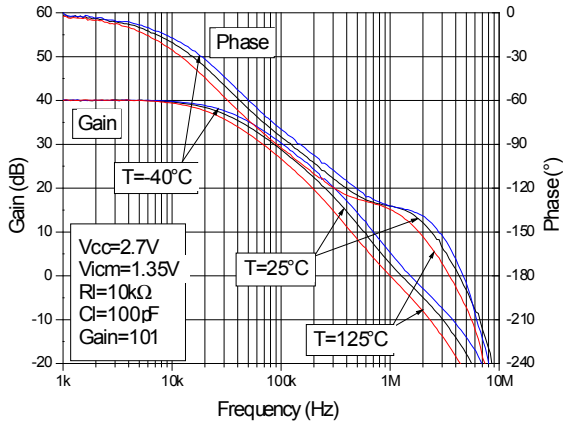


Figure 18. Bode diagram at V_{CC} = 16 V

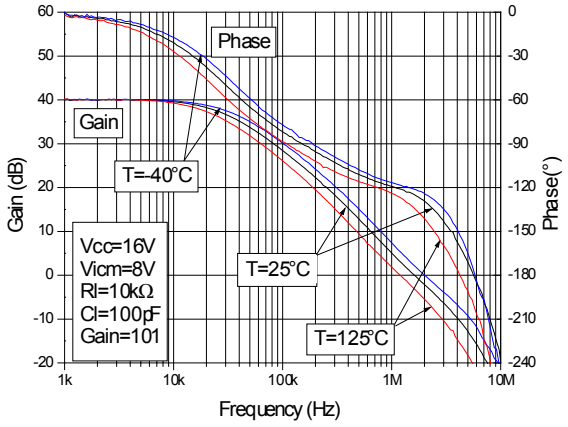


Figure 19. Power supply rejection ratio (PSRR) vs. frequency

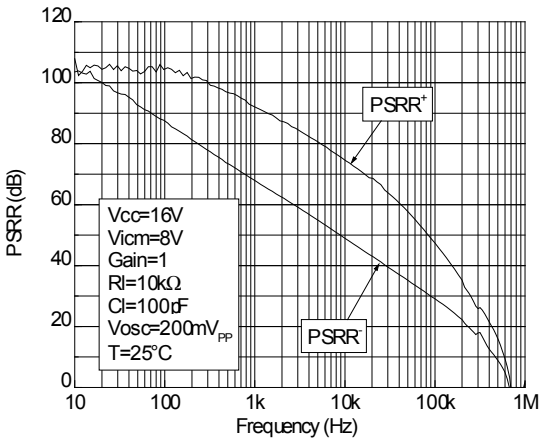


Figure 20. Output overshoot vs. capacitive load

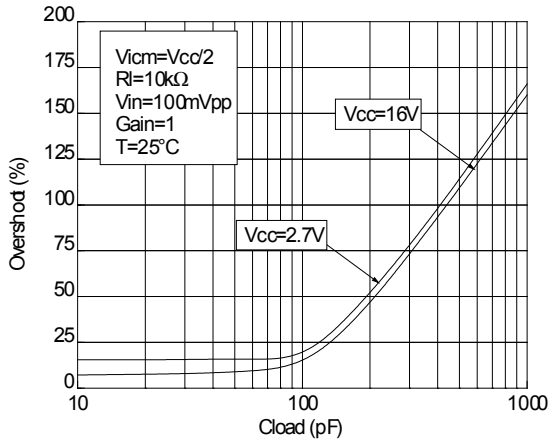


Figure 21. Output impedance vs. frequency in closed loop configuration

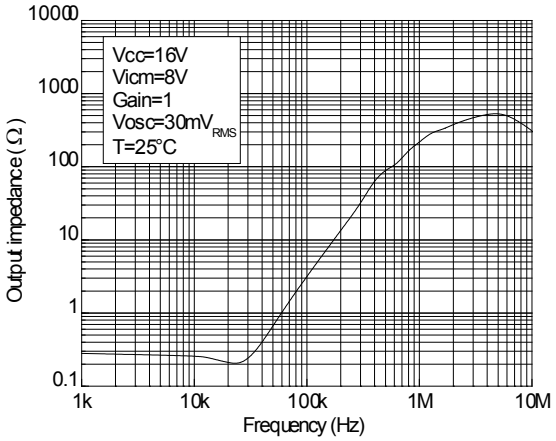


Figure 22. THD + N vs. frequency

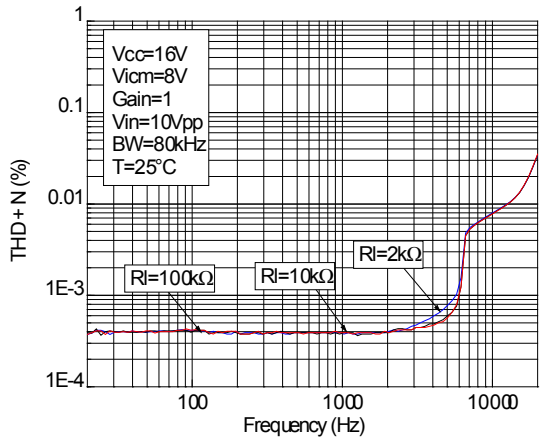


Figure 23. THD + N vs. output voltage

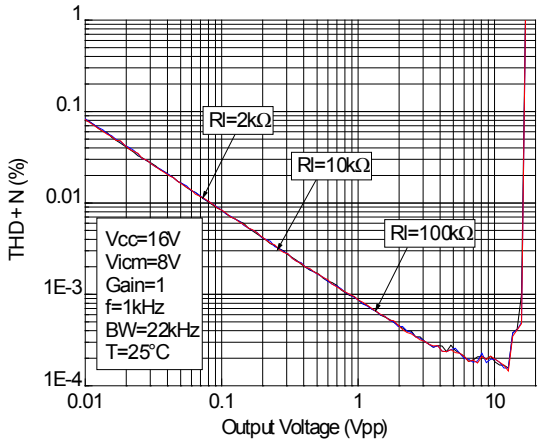


Figure 24. Noise vs. frequency

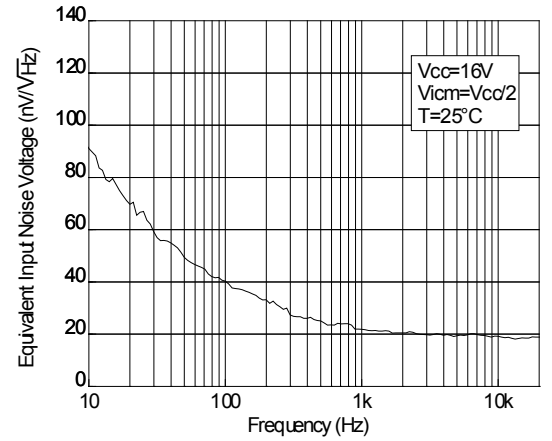
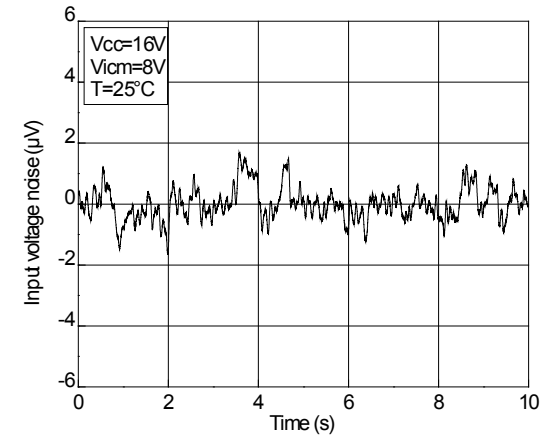


Figure 25. 0.1 to 10 Hz noise



5 Application information

5.1 Operating voltages

The LMC6482 device can operate from 2.7 to 16 V. The parameters are fully specified for 4 V, 10 V, and 16 V power supplies. However, the parameters are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to 125 °C.

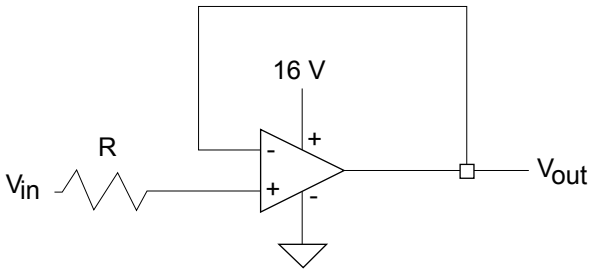
5.2 Input pin voltage ranges

The LMC6482 device have internal ESD diode protection on the inputs. These diodes are connected between the input and each supply rail to protect the input MOSFETs from electrical discharge.

If the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current can flow through them. Without limitation this over current can damage the device.

In this case, it is important to limit the current to 10 mA, by adding resistance on the input pin, as described in figure below.

Figure 26. Input current limitation



5.3 Rail-to-rail input

The LMC6482 device have a rail-to-rail input, and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V.

5.4 Rail-to-rail output

The operational amplifier output levels can go close to the rails: to a maximum of 40 mV above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

5.5 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using Equation 1.

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right| \quad (1)$$

where T = -40 °C and 125 °C.

The LMC6482 datasheet maximum values are guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.6 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

Voltage acceleration, by changing the applied voltage

Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using

Equation 2

$$A_{FV} = \epsilon^{\beta.V_S - V_U} \quad (2)$$

where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in

Equation 3

$$A_{FT} = e^{\frac{E_a}{k}\cdot\left(\frac{1}{T_U} - \frac{1}{T_S}\right)} \quad (3)$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate k is the Boltzmann constant (8.6173 x 10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (Equation 4)

$$A_F = A_{FT} \times A_{FV} \quad (4)$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The AF value can then be used in to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

$$Months = A_F \times 1000\,h \times 12\,months / 24\,h \times 365.25\,days \quad (5)$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see equation 6)

$$V_{CC} = \max V_{PP}\ with\ V_{icm} = V_{CC}/2 \quad (6)$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (Equation 7)

$$\Delta V_{io} = \frac{V_{io}\,drift}{\sqrt{months}} \quad (7)$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

5.7 High values of input differential voltage

In a closed loop configuration, which represents the typical use of an op amp, the input differential voltage is low (close to V_{io}). However, some specific conditions can lead to higher input differential values, such as:

operation in an output saturation state

operation at speeds higher than the device bandwidth, with output voltage dynamics limited by slew rate.

use of the amplifier in a comparator configuration, hence in open loop

Use of the LMC6482 in comparator configuration, especially combined with high temperature and long duration can create a permanent drift of V_{io}.

5.8 Capacitive load

Driving large capacitive loads can cause stability problems. Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB an op amp might become unstable.

Generally, the unity gain configuration is the worst case for stability and the ability to drive large capacitive loads.

Figure below "Stability criteria with a serial resistor at different supply voltage" shows the serial resistor that must be added to the output, to make a system stable. The Figure 28. Test configuration for Riso shows the test configuration using an isolation resistor, Riso.

Figure 27. Stability criteria with a serial resistor at different supply voltage

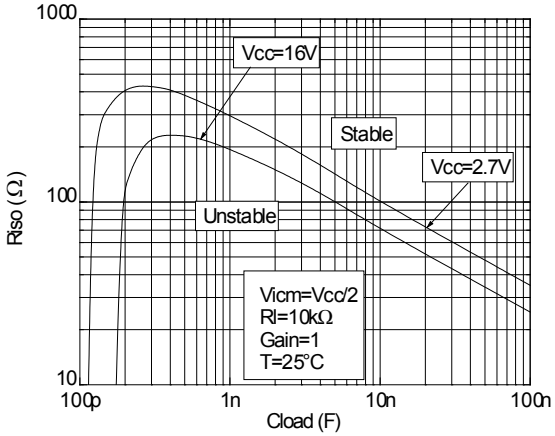
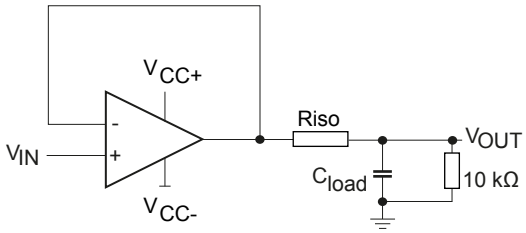


Figure 28. Test configuration for Riso



5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB, tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.10 Optimized application recommendation

It is recommended to place a 22 nF capacitor as close as possible to the supply pin. A good decoupling will help to reduce electromagnetic interference impact.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 MiniSO8 package information

Figure 29. MiniSO8 package outline

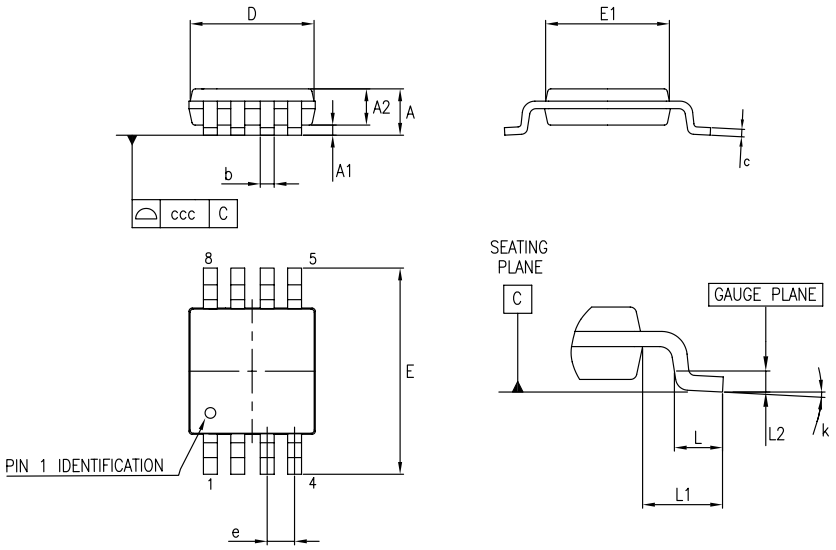


Table 6. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

6.2 SO8 package information

Figure 30. **SO8 package outline**

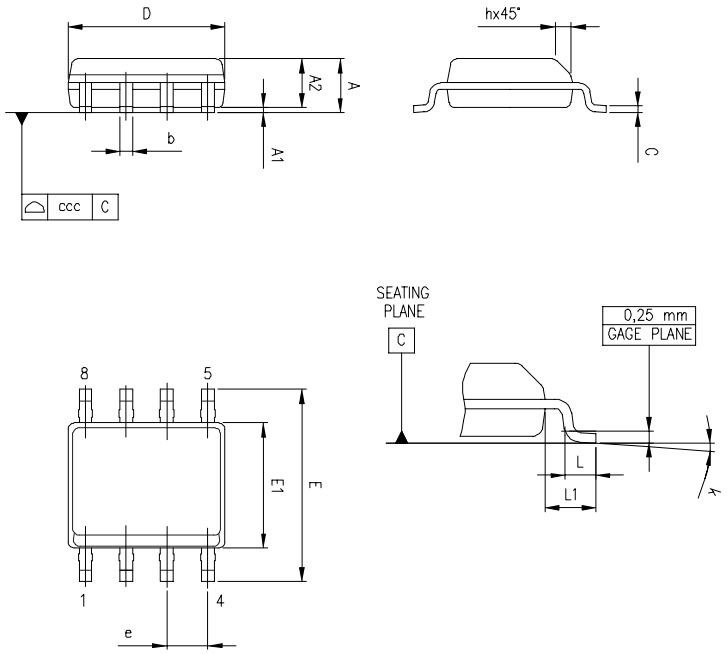


Table 7. **SO-8 mechanical data**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

7 Ordering information

Table 8. **Order code**

Order code	Temperature range	Package	Packing	Marking
LMC6482IDT	-40 ° to +125 °C	SO8	Tape and reel	LMC6482
LMC6482IST		MiniSO8		6482

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
24-Jul-2018	1	Initial release.
12-Sep-2018	2	Updated the temperature range value in Table 8. Order code.
26-Oct-2021	3	Added Marking column in Table 8. Order code.

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