

LMH2180 75 MHz Dual Clock Buffer

Check for Samples: [LMH2180](#)

FEATURES

- (Typical Values are: $V_{\text{SUPPLY}} = 2.7\text{V}$ and $C_L = 10\text{ pF}$, unless Otherwise Specified.)
- Small Signal Bandwidth 78 MHz
- Supply Voltage Range 2.4V to 5V
- Phase Noise ($V_{\text{IN}} = 1\text{ V}_{\text{PP}}$, $f_C = 38.4\text{ MHz}$, $\Delta f = 1\text{ kHz}$) -123 dBc/Hz
- Slew Rate 106 V/ μs
- Total Supply Current 2.3 mA
- Shutdown Current 30 μA
- Rail-to-Rail Input and Output
- Individual Buffer Enable Pins
- Rapid T_{on} Technology
- Crosstalk Rejection Circuitry
- Packages:
 - 8-Pin WSON, Solder Bump and no Pullback
 - 8-Bump DSBGA
- Temperature Range -40°C to 85°C

APPLICATIONS

- 3G Mobile Applications
- WLAN–WiMAX Modules
- TD_SCDMA Multi-Mode MP3 and Camera
- GSM Modules
- Oscillator Modules

DESCRIPTION

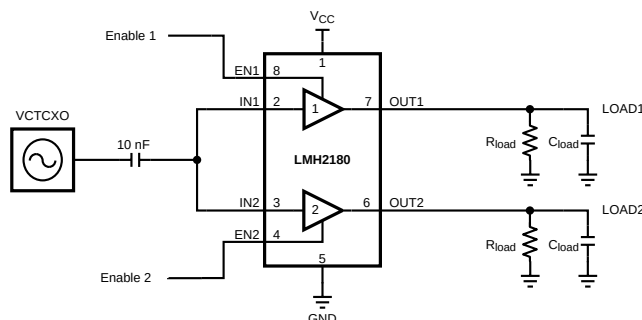
The LMH2180 is a high speed dual clock buffer designed for portable communications and applications requiring multiple accurate multi-clock systems. The LMH2180 integrates two 75 MHz low noise buffers with independent shutdown pins into a small package. The LMH2180 ensures superb system operation between the baseband and the oscillator signal path by eliminating crosstalk between the multiple clock signals.

Unique technology and design provides the LMH2180 with the ability to accurately drive both large capacitive and resistive loads. Low supply current combined with shutdown pins for each channel means the LMH2180 is ideal for battery powered applications. This part does not use an internal ground reference, thus providing additional system flexibility.

The flexible buffers provide system designers the capacity to manage complex clock signals in the latest wireless applications. Each buffer delivers 106 V/ μs internal slew rate with independent shutdown and duty cycle precision. Each input is internally biased to 1V, removing the need for external resistors. Both channels have rail-to-rail inputs and outputs, a gain of one, and are AC coupled with the use of one capacitor.

Replacing a discrete buffer solution with the LMH2180 provides many benefits: simplified board layout, minimized parasitic components, simplified BOM, design durability across multiple applications, simplification of clock paths, and the ability to reduce the number of clock signal generators in the system. The LMH2180 is produced in the tiny packages minimizing the required PCB space.

TYPICAL APPLICATION



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CONNECTION DIAGRAMS

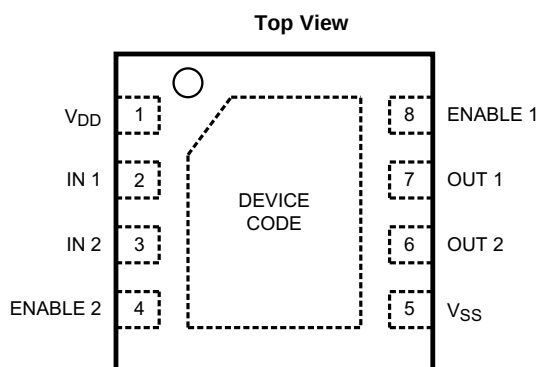


Figure 1. 8-Pin WSON Package
See Package Number NGW0008A or NGQ0008A

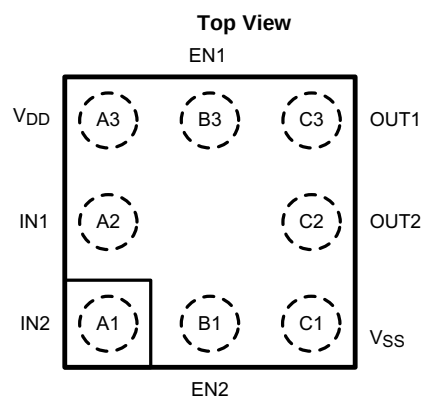


Figure 2. 8-Bump DSBGA Package
See Package Number YFQ0008AAA

PIN DESCRIPTIONS

Pin No. WSN	Pin No. DSBGA	Pin Name	Description
1	A3	V _{DD}	Voltage supply connection
2	A2	IN 1	Input 1
3	A1	IN 2	Input 2
4	B1	ENABLE 2	Enable buffer 2
5	C1	V _{SS}	Ground connection
6	C2	OUT 2	Output 2
7	C3	OUT 1	Output 1
8	B3	ENABLE 1	Enable buffer 1



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

Supply Voltages (V ⁺ – V [–])	5.5V
ESD Tolerance	
Human Body ⁽³⁾	2000V
Machine Model ⁽⁴⁾	200V
Charged Device Model	1000V
Storage Temperature Range	–65°C to 150°C
Junction Temperature ⁽⁵⁾	150°C
Soldering Information	
Infrared or Convection (35 sec.)	235°C

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, applicable std. JESD22–A114C.
- (4) Machine model, applicable std. JESD22–A115–A.
- (5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{J(MAX)}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is P_{DMAX} = (T_{JMAX} – T_A) / θ_{JA} or the number given in the *Absolute Maximum Ratings*, whichever is lower.

OPERATING RATINGS ⁽¹⁾

Supply Voltage ($V^+ - V^-$)	2.4V to 5.0V
Temperature Range ⁽²⁾⁽³⁾	-40°C to 85°C
Package Thermal Resistance ⁽²⁾⁽³⁾	
8-Pin WSON (θ_{JA})	217°C/W
8-Bump DSBGA (θ_{JA})	90°C/W

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables show performance under the specified Recommended Operating Conditions except as otherwise modified by the Electrical Characteristics Conditions and/or Notes. Typical values represent typical performance as measured by production tests. Individual parts may vary.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.

2.7V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified for $T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $V_{CM} = 1\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{pF}$, $R_L = 30\text{k}\Omega$, Load is connected to V_{SS} , $C_{COUPLING} = 10\text{nF}$. **Boldface** limits apply at temperature range extremes of operating condition. ⁽¹⁾

Parameter		Test Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	$V_{IN} = 100\text{mV}_{PP}$; -3 dB		78		MHz
LSBW	Large Signal Bandwidth	$V_{IN} = 1.0\text{V}_{PP}$; -3 dB		60		MHz
GFN	Gain Flatness < 0.1 dB	$f > 100\text{kHz}$		4.9		MHz
Distortion and Noise Performance						
Φ_n	Phase Noise	$V_{IN} = 1\text{V}_{PP}$, $f_C = 38.4\text{MHz}$, $\Delta f = 1\text{kHz}$		-123		dBc/Hz
		$V_{IN} = 1\text{V}_{PP}$, $f_C = 38.4\text{MHz}$, $\Delta f = 10\text{kHz}$		-132		dBc/Hz
e_n	Input-Referred Voltage Noise	$f = 1\text{MHz}$, $R_{SOURCE} = 50\Omega$		13		nV/ $\sqrt{\text{Hz}}$
$I_{ISOLATION}$	Output to Input	$f = 1\text{MHz}$, $R_{SOURCE} = 50\Omega$		84		dB
CT	Crosstalk Rejection	$f = 38.4\text{MHz}$, $V_{IN} = 1\text{V}_{PP}$		41		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%)		6		ns
t_f	Fall Time			5		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step		120		ns
OS	Overshoot	0.1 V_{PP} Step		37		%
SR	Slew Rate ⁽⁴⁾	$V_{IN} = 2\text{V}_{PP}$		106		V/ μs
Static DC Performance						
I_S	Supply Current	$\text{Enable}_{1,2} = V_{DD}$; No Load		2.3	2.7 2.9	mA
		$\text{Enable}_1 = V_{DD}$, $\text{Enable}_2 = V_{SS}$, No Load		1.3	1.5 1.6	mA
		$\text{Enable}_{1,2} = V_{SS}$; No Load		30	41 46	μA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	65 64	68		dB

- (1) The Electrical Characteristics tables show performance under the specified Recommended Operating Conditions except as otherwise modified by the Electrical Characteristics Conditions and/or Notes. Typical values represent typical performance as measured by production tests. Individual parts may vary.
- (2) Datasheet min/max limits are specified by test or statistical analysis.
- (3) Typical values represent the most likely parametric norms at $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization.
- (4) Slew rate is the average of the rising and falling slew rates.

2.7V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified for $T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $V_{CM} = 1\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$, Load is connected to V_{SS} , $C_{COUPLING} = 10\text{ nF}$. **Boldface** limits apply at temperature range extremes of operating condition.⁽¹⁾

Parameter		Test Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
A _{CL}	Small Signal Voltage Gain	V _{IN} = 0.2 V _{PP}	0.95	1.0	1.05	V/V
V _{OS}	Output Offset Voltage			-0.5	17 18	mV
TC V _{OS}	Temperature Coefficient Output Offset Voltage ⁽⁵⁾			2.8		μV/°C
R _{OUT}	Output Resistance	f = 100 kHz		0.6		Ω
		f = 38.4 MHz		166		
		disabled		High Impedance		
Miscellaneous Performance						
R _{IN}	Input Resistance per Buffer	Enable = V _{DD}		137		kΩ
		Enable = V _{SS}		137		
C _{IN}	Input Capacitance per Buffer	Enable = V _{DD}		1.3		pF
		Enable = V _{SS}		1.3		
Z _{IN}	Input Impedance	f = 38.4 MHz, Enable = V _{DD}		4.5		kΩ
		f = 38.4 MHz, Enable = V _{SS}		4.2		
V _O	Output Swing Positive	V _{IN} = V _{DD}	2.66 2.65	2.69		V
	Output Swing Negative	V _{IN} = V _{SS}		19	35 37	mV
I _{SC}	Output Short-Circuit Current ⁽⁶⁾⁽⁷⁾	Sourcing, V _{IN} = V _{DD} , V _{OUT} = V _{SS}	-21 -18	-25		mA
		Sinking, V _{IN} = V _{SS} , V _{OUT} = V _{DD}	23 15	25		
V _{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V _{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

(5) Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.

(6) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

(7) Positive current corresponds to current flowing into the device.

5V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified for $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$, $V_{CM} = 1\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$, Load is connected to V_{SS} , $C_{COUPLING} = 10\text{ nF}$. **Boldface** limits apply at temperature range extremes of operating condition.⁽¹⁾

Parameter		Test Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	$V_{IN} = 100\text{ mV}_{PP}$; -3 dB		87		MHz
LSBW	Large Signal Bandwidth	$V_{IN} = 1.0\text{ V}_{PP}$; -3 dB		68		MHz
GFN	Gain Flatness < 0.1 dB	$f > 100\text{ kHz}$		25		MHz
Distortion and Noise Performance						
Φ_n	Phase Noise	$V_{IN} = 1\text{ V}_{PP}$, $f_C = 38.4\text{ MHz}$, $\Delta f = 1\text{ kHz}$		-123		dBc/Hz
		$V_{IN} = 1\text{ V}_{PP}$, $f_C = 38.4\text{ MHz}$, $\Delta f = 10\text{ kHz}$		-132		dBc/Hz

(1) The Electrical Characteristics tables show performance under the specified Recommended Operating Conditions except as otherwise modified by the Electrical Characteristics Conditions and/or Notes. Typical values represent typical performance as measured by production tests. Individual parts may vary.

(2) Datasheet min/max limits are specified by test or statistical analysis.

(3) Typical values represent the most likely parametric norms at $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization.

5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified for $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$, $V_{CM} = 1\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$, Load is connected to V_{SS} , $C_{COUPLING} = 10\text{ nF}$. **Boldface** limits apply at temperature range extremes of operating condition.⁽¹⁾

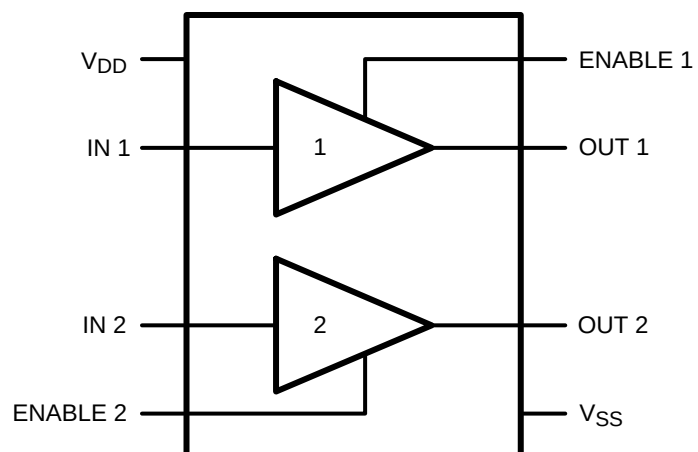
Parameter		Test Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
e _n	Input-Referred Voltage Noise	f = 1 MHz, R _{SOURCE} = 50Ω		12		nV/√Hz
I _{SOLATION}	Output to Input	f = 1 MHz, R _{SOURCE} = 50Ω		84		dB
CT	Crosstalk Rejection	f = 38.4 MHz, P _{IN} = 0 dBm		59		dB
Time Domain Response						
t _r	Rise Time	0.1 V _{PP} Step (10-90%)		6		ns
t _f	Fall Time			6		ns
t _s	Settling Time to 0.1%	1 V _{PP} Step		70		ns
OS	Overshoot	0.1V _{PP} Step		13		%
SR	Slew Rate ⁽⁴⁾	V _{IN} = 2 V _{PP}		124		V/μs
Static DC Performance						
I _S	Supply Current	Enable _{1,2} = V _{DD} ; No Load		3.4	4.0 4.1	mA
		Enable ₁ = V _{DD} , Enable ₂ = V _{SS} ; No Load		1.8	2.2 2.3	mA
		Enable _{1,2} = V _{SS} ; No Load		32	43 49	μA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	65 64	68		dB
A _{CL}	Small Signal Voltage Gain	V _{IN} = 0.2 V _{PP}	0.95	1.0	1.05	V/V
V _{OS}	Output Offset Voltage			-1.4	21 22	mV
TC V _{OS}	Temperature Coefficient Output Offset Voltage ⁽⁵⁾			2.4		μV/°C
R _{OUT}	Output Resistance	f = 100 kHz		0.5		Ω
		f = 38.4 MHz		126		
		disabled	High Impedance			
Miscellaneous Performance						
R _{IN}	Input Resistance per Buffer	Enable = V _{DD}		138		kΩ
		Enable = V _{SS}		138		
C _{IN}	Input Capacitance per Buffer	Enable = V _{DD}		1.3		pF
		Enable = V _{SS}		1.3		
Z _{IN}	Input Impedance	f = 38.4 MHz, Enable = V _{DD}		4.3		kΩ
		f = 38.4 MHz, Enable = V _{SS}		4.2		
V _O	Output Swing Positive	V _{IN} = V _{DD}	4.96 4.95	4.99		V
	Output Swing Negative	V _{IN} = V _{SS}		10	35 50	mV
I _{SC}	Output Short-Circuit Current ⁽⁶⁾⁽⁷⁾	Sourcing, V _{IN} = V _{DD} , V _{OUT} = V _{SS}	-80 -62	-90		mA
		Sinking, V _{IN} = V _{SS} , V _{OUT} = V _{DD}	60 43	65		
V _{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V _{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

(4) Slew rate is the average of the rising and falling slew rates.

(5) Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.

(6) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

(7) Positive current corresponds to current flowing into the device.

BLOCK DIAGRAM

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$ and $C_{\text{COUPLING}} = 10\text{ nF}$, unless otherwise specified.

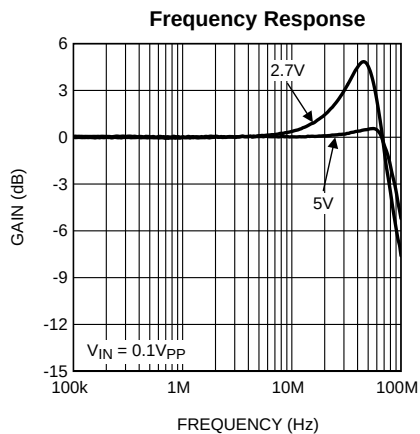


Figure 3.

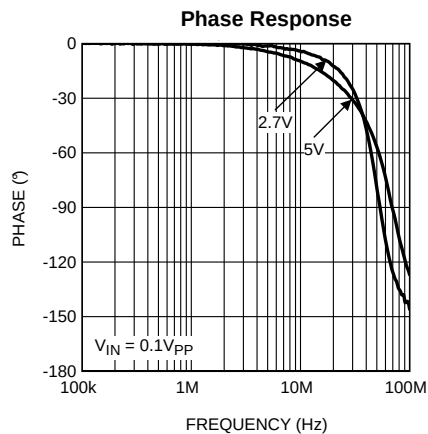


Figure 4.

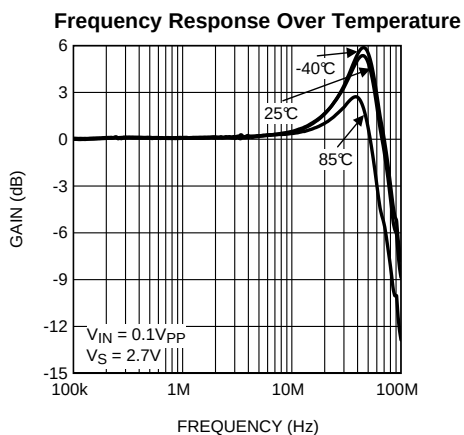


Figure 5.

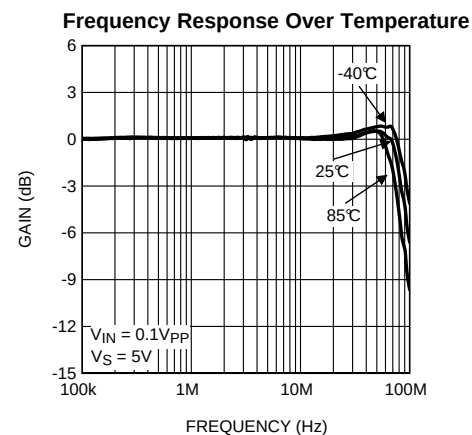


Figure 6.

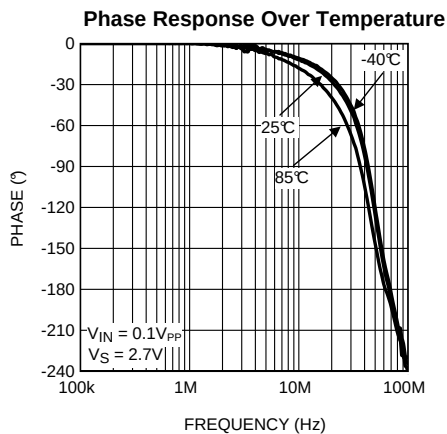


Figure 7.

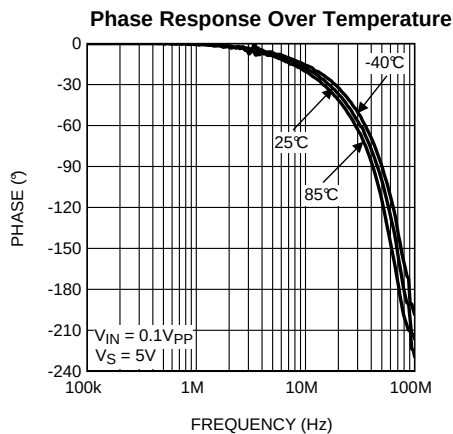


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$ and $C_{\text{COUPLING}} = 10\text{ nF}$, unless otherwise specified.

Large Signal Bandwidth

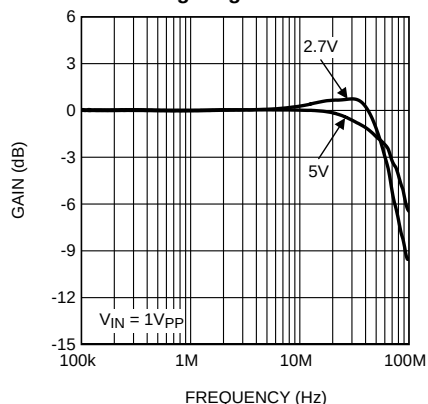


Figure 9.

Gain Flatness < 0.1 dB (GFN)

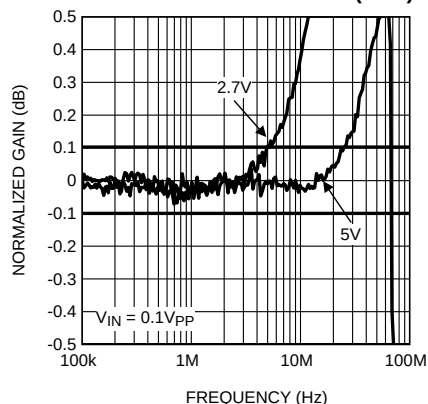


Figure 10.

Voltage Noise

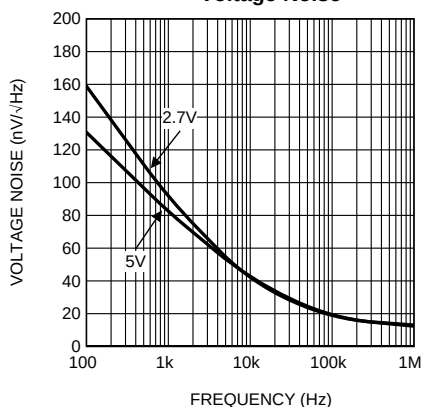


Figure 11.

Phase Noise

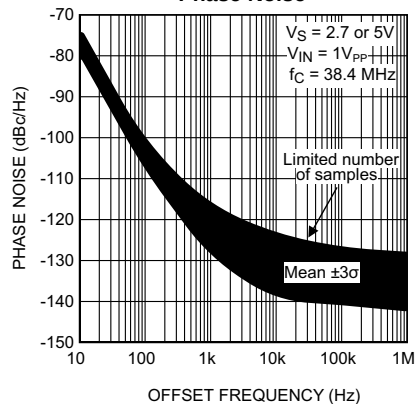


Figure 12.

**Isolation Output to Input
vs.
Frequency**

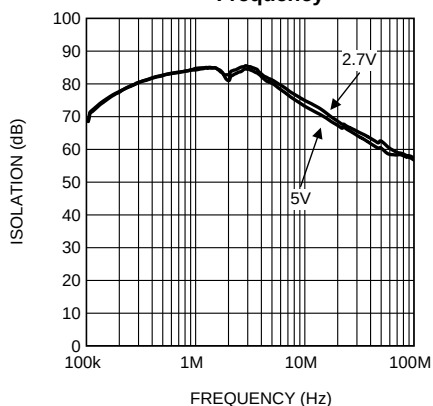


Figure 13.

**Crosstalk Rejection
vs.
Frequency**

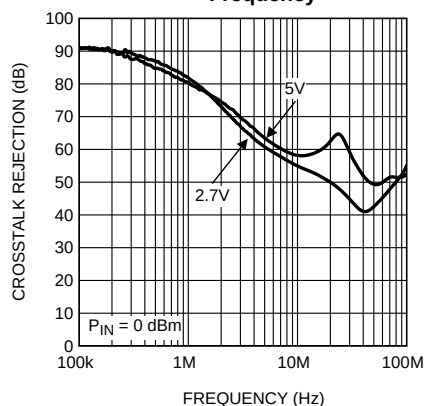


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$ and $C_{\text{COUPLING}} = 10\text{ nF}$, unless otherwise specified.

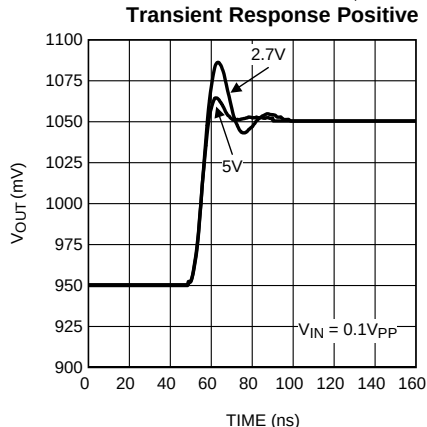


Figure 15.

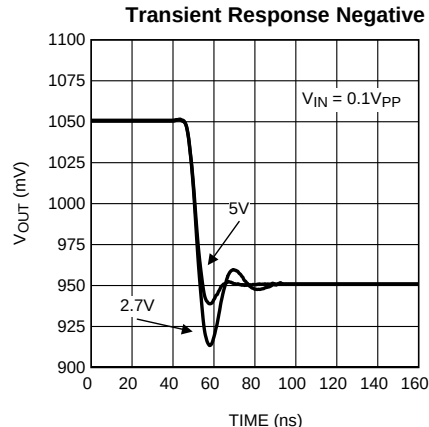


Figure 16.

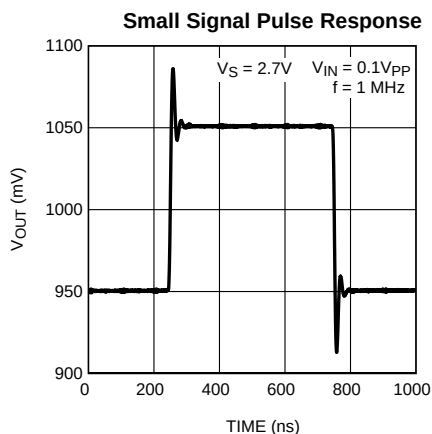


Figure 17.

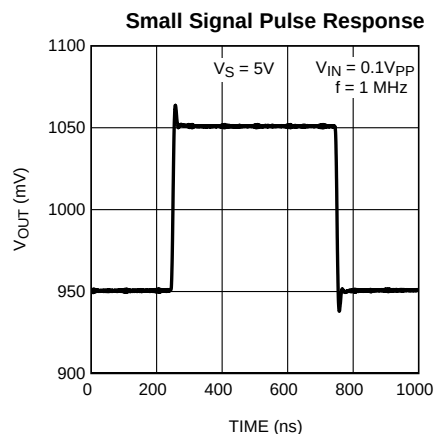


Figure 18.

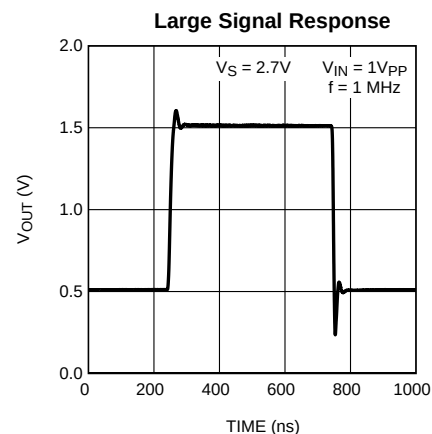


Figure 19.

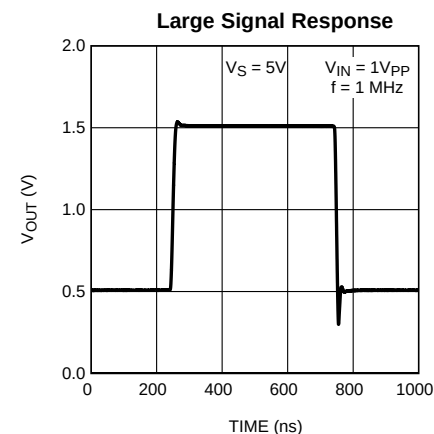


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$ and $C_{\text{COUPLING}} = 10\text{ nF}$, unless otherwise specified.

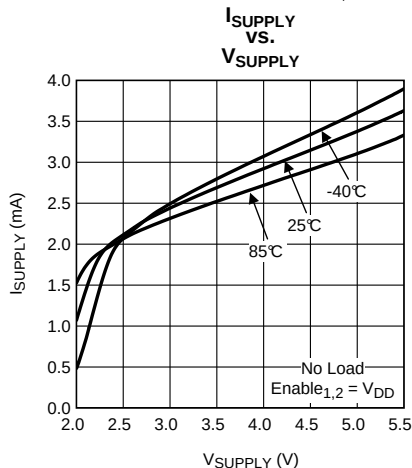


Figure 21.

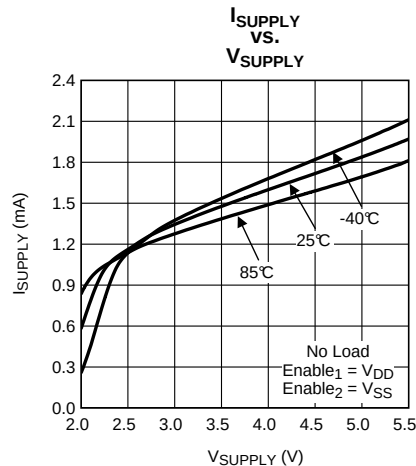


Figure 22.

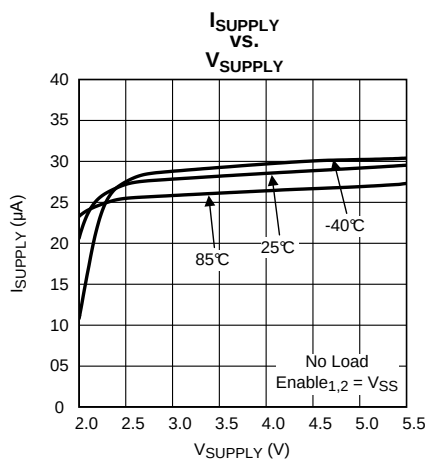


Figure 23.

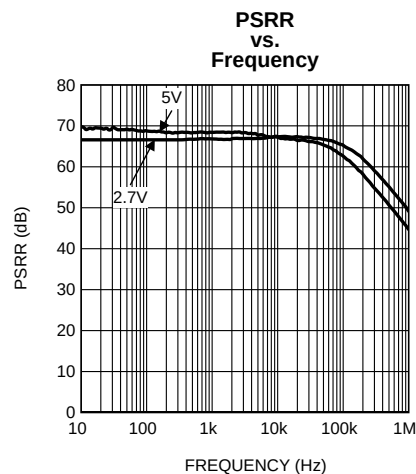


Figure 24.

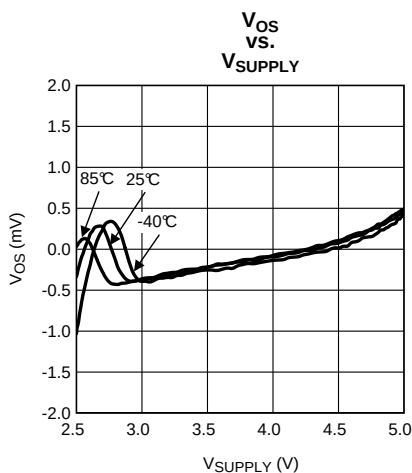


Figure 25.

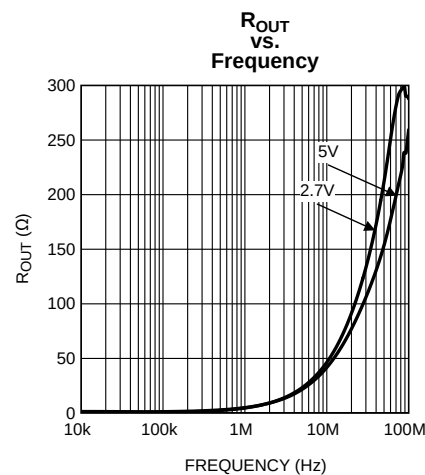


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$ and $C_{\text{COUPLING}} = 10\text{ nF}$, unless otherwise specified.

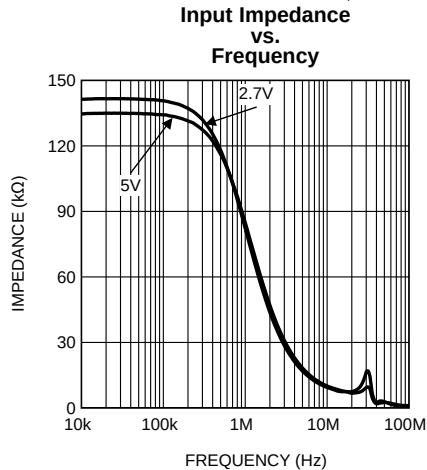


Figure 27.

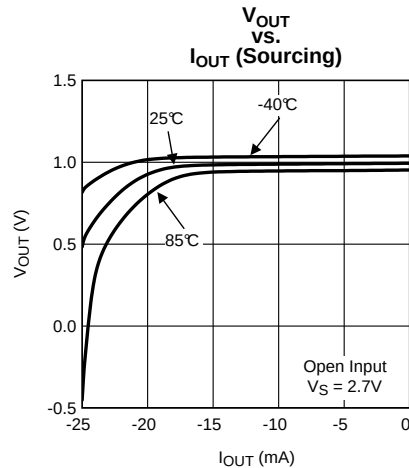


Figure 28.

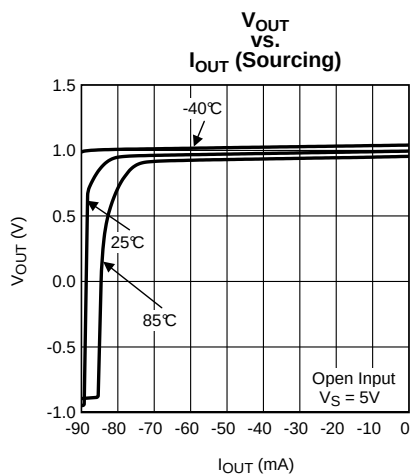


Figure 29.

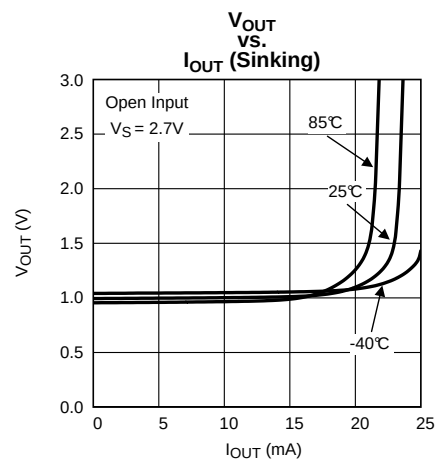


Figure 30.

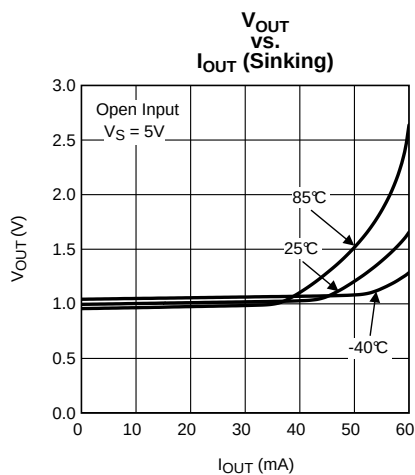


Figure 31.

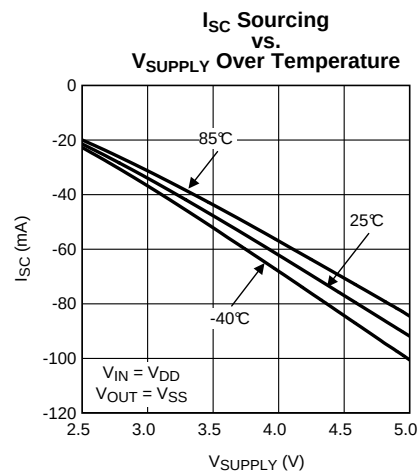
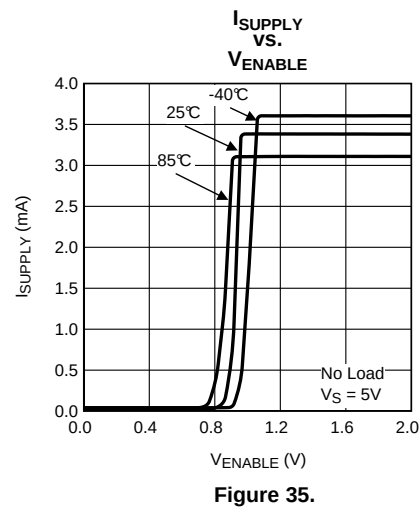
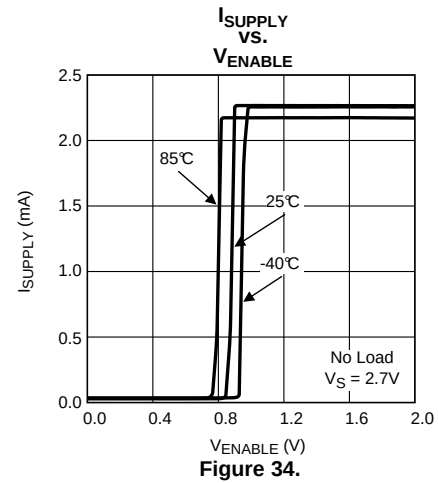
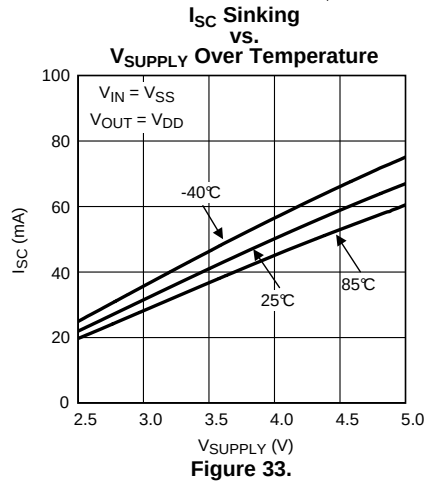


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{V}$, $V_{SS} = 0\text{V}$, $\text{Enable}_{1,2} = V_{DD}$, $C_L = 10\text{ pF}$, $R_L = 30\text{ k}\Omega$ and $C_{\text{COUPLING}} = 10\text{ nF}$, unless otherwise specified.



APPLICATION INFORMATION

GENERAL

The LMH2180 is designed to minimize the effects of spurious signals from the base chip to the oscillator. Also the influence of varying load resistance and capacitance to the oscillator is minimized, while the drive capability is increased.

The inputs of the LMH2180 are internally biased at 1V, making AC coupling possible without external bias resistors.

To optimize current consumption, a buffer that is not in use can be disabled by connecting its enable pin to V_{SS} .

The LMH2180 has no internal ground reference; therefore, either single or split supply configurations can be used.

The LMH2180 is an easy replacement for discrete circuitry. It simplifies board layout and minimizes the effect of layout related parasitic components.

INPUT CONFIGURATION

The internal 1V input biasing allows AC coupling of the input signal. This biasing avoids the use of external resistors, as depicted in [Figure 36](#). The biasing prevents a large DC load at the oscillator's output that creates a load impedance and may affect its oscillating frequency. As a result of this biasing, the maximum amplitude of the AC signal is $2V_{PP}$.

The coupling capacitance $C1$ should be large enough to let the AC signal pass. This is a unity gain buffer with rail-to-rail inputs and outputs.

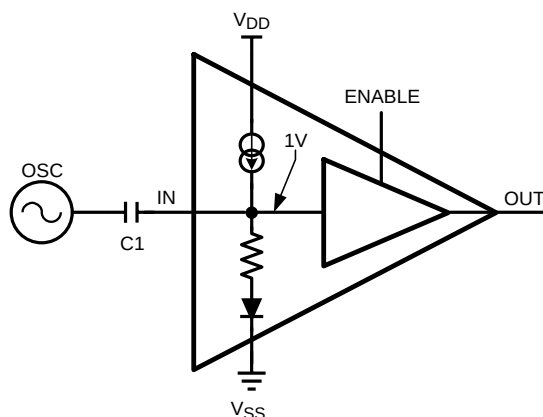


Figure 36. Input Configuration

FREQUENCY PULLING

Frequency pulling is the frequency variation of an oscillator caused by a varying load. In the typical application, the load of the oscillator is a fixed capacitor ($C1$) in series with the input impedance of the buffer.

To keep the input impedance as constant as possible, the input is biased at 1V, even when the part is disabled. A simplified schematic of the input configuration is shown in [Figure 36](#).

ISOLATION AND CROSSTALK

Output to input isolation prevents the clock signal of the oscillator from being affected by spurious signals generated by the digital blocks behind the output buffer. See [Figure 13](#).

A block diagram of the isolation is shown in [Figure 37](#). Crosstalk rejection between buffers prevents signals from affecting each other. [Figure 37](#) shows a Baseband IC and a Bluetooth module as an example. See [Figure 14](#) for more information.

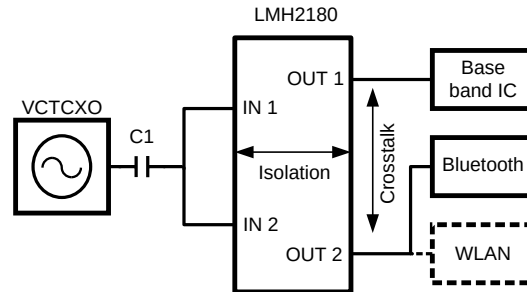


Figure 37. Isolation Block Diagram

DRIVING CAPACITIVE LOADS

Each buffer can drive a capacitive load. Be aware that every capacitor directly connected to the output becomes part of the loop of the buffer. In most applications the load consists of the capacitance of copper tracks and the input capacitance of the application blocks. Capacitance reduces the gain/phase margin and decreases the stability. This leads to peaking in the frequency response and in extreme situations oscillations can occur. To drive a large capacitive load it is recommended to include a series resistor between the buffer and the load capacitor. The best value for this isolation resistance can be found by experimentation.

The LMH2180 datasheet reflects measurements with capacitive loads of 10 pF at the output of the buffers. Most common applications will probably use a lower capacitive load, which will result in lower peaking and significantly greater bandwidth, see Figure 38.

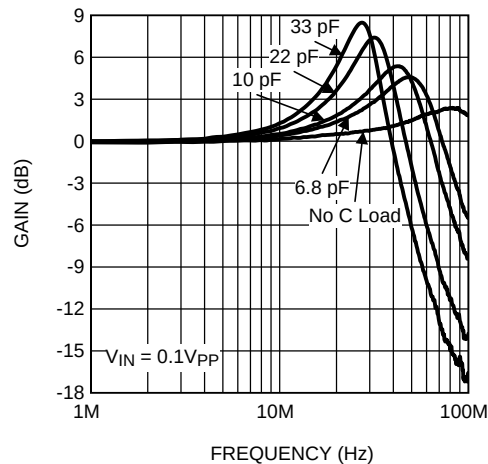


Figure 38. Bandwidth and Peaking

PHASE NOISE

A clock buffer adds noise to the clock signal. This noise causes uncertainty in the phase of the clock signal. This uncertainty is described by jitter (time domain) or phase noise (frequency domain). Communication systems, such as Wireless LAN, require a low jitter/phase noise clock signal to obtain a low Bit Error Rate. Figure 39 shows the frequency domain representation of a clock signal with frequency f_c . Without Phase Noise the entire signal power would only be located at the frequency f_c . Phase Noise spreads some of the power to adjacent frequencies. Phase Noise is usually specified in dBc/Hz at a given frequency offset Δf from the carrier, where dBc is the power level in dB relative to the carrier. The noise power is measured within a 1 Hz bandwidth.

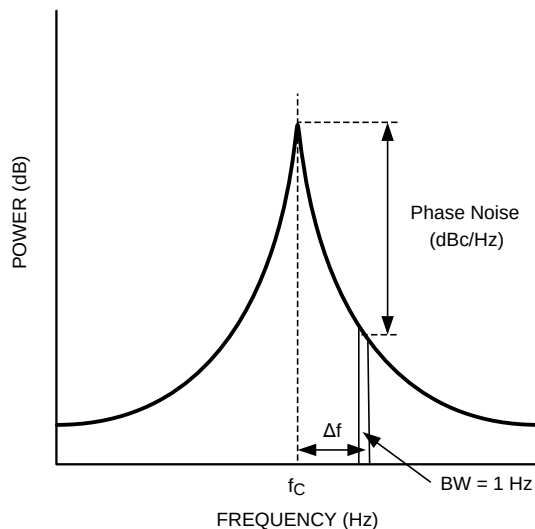


Figure 39. Phase Noise

Figure 40 shows the setup used to measure the LMH2180 phase noise. The clock driving the LMH2180 is a state of the art 38.4MHz TCXO. Both the TCXO phase noise and the phase noise at the LMH2180 output were measured. At offset frequencies of 1 kHz and higher from the carrier, the TCXO phase noise is sufficiently low to accurately calculate the LMH2180 contribution to the phase noise at the output. The LMH6559, whose phase noise contribution can be neglected, is used to drive the 50Ω input impedance of the Signal Source Analyzer.

LAYOUT DESIGN RECOMMENDATION

Careful consideration during circuit design and PCB layout will eliminate problems and will optimize the performance of the LMH2180. It is best to have the same ground plane on the PCB for all decoupling and other ground connections.

To ensure a clean supply voltage it is best to place decoupling capacitors close to the LMH2180, between V_{DD} and V_{SS} .

Another important issue is the value of the components, because this also determines the sensitivity to disturbances. Resistor values have to be low enough to avoid a significant noise contribution and large enough to avoid a significant increase in power consumption while loading inputs or outputs to heavily.

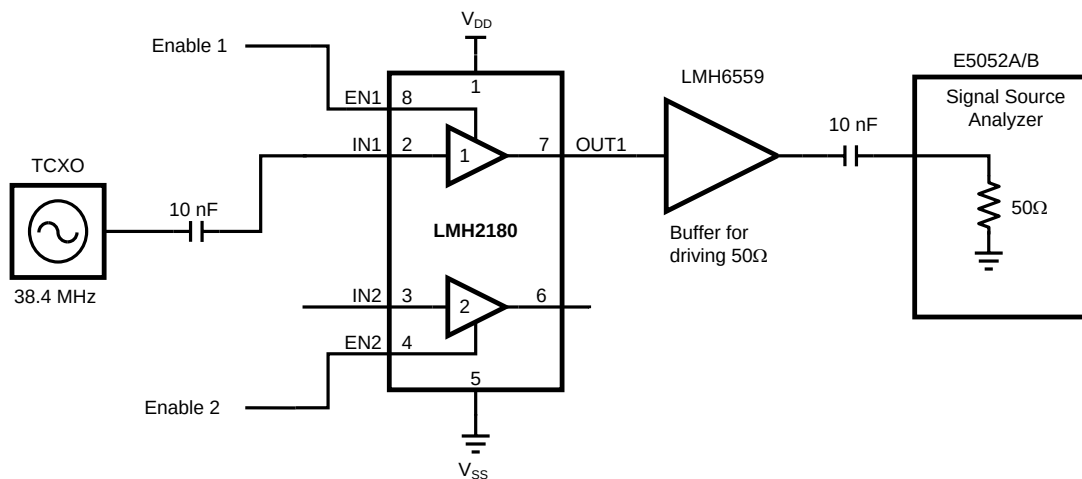


Figure 40. Measurement Setup

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D

Page

- Changed layout of National Data Sheet to TI format [15](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH2180SD/NOPB	Active	Production	WSO (NGQ) 8	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2180S
LMH2180SD/NOPB.A	Active	Production	WSO (NGQ) 8	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2180S
LMH2180SDE/NOPB	Active	Production	WSO (NGQ) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2180S
LMH2180SDE/NOPB.A	Active	Production	WSO (NGQ) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2180S
LMH2180TM/NOPB	Active	Production	DSBGA (YFQ) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	A
LMH2180TM/NOPB.A	Active	Production	DSBGA (YFQ) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A
LMH2180TMX/NOPB	Active	Production	DSBGA (YFQ) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	A
LMH2180TMX/NOPB.A	Active	Production	DSBGA (YFQ) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

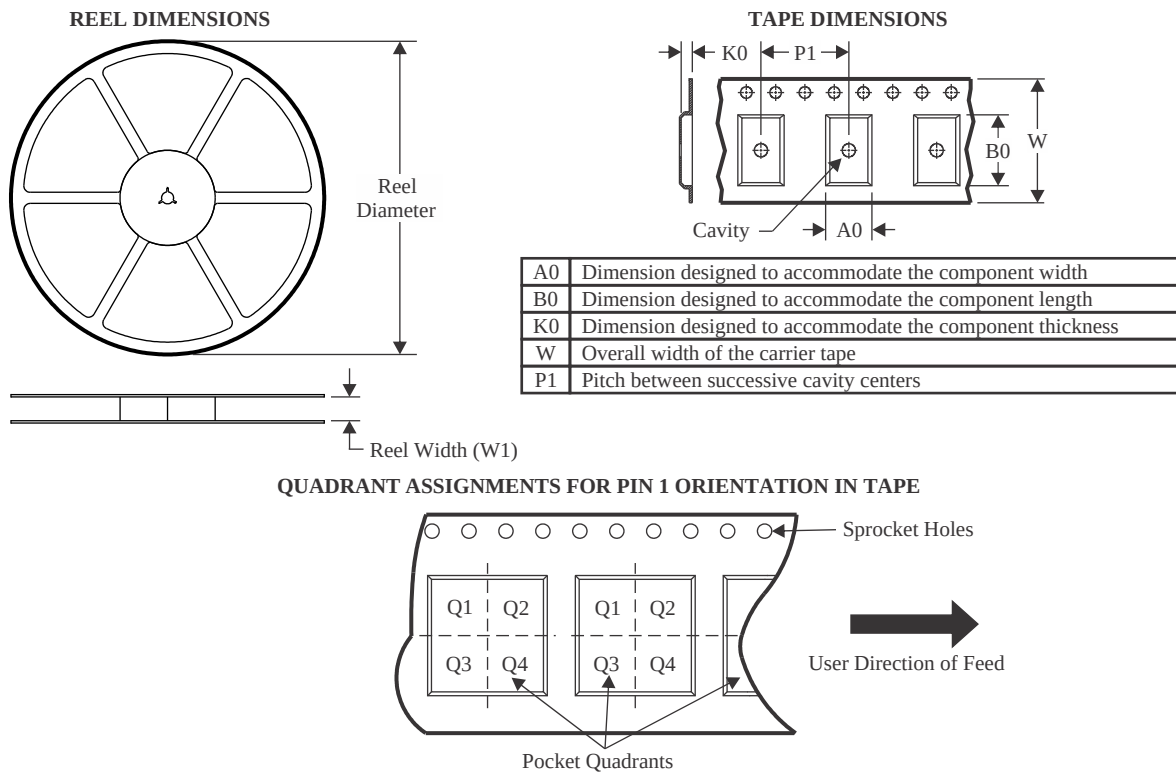
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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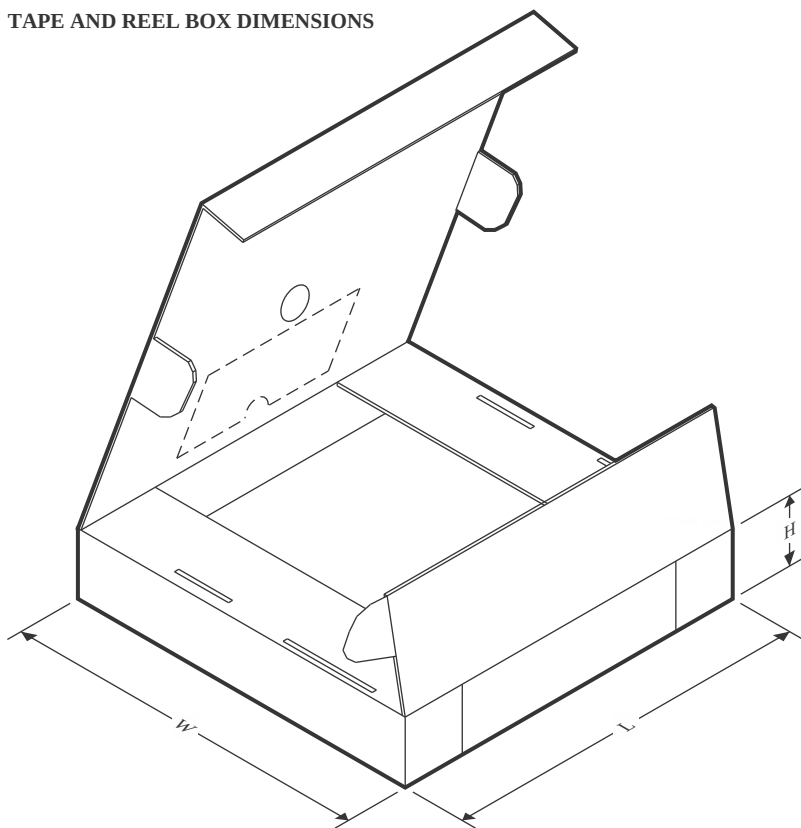
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH2180SD/NOPB	WSO	NGQ	8	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH2180SDE/NOPB	WSO	NGQ	8	250	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH2180TM/NOPB	DSBGA	YFQ	8	250	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1
LMH2180TMX/NOPB	DSBGA	YFQ	8	3000	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1

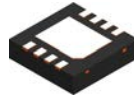
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH2180SD/NOPB	WSO	NGQ	8	1000	208.0	191.0	35.0
LMH2180SDE/NOPB	WSO	NGQ	8	250	208.0	191.0	35.0
LMH2180TM/NOPB	DSBGA	YFQ	8	250	208.0	191.0	35.0
LMH2180TMX/NOPB	DSBGA	YFQ	8	3000	208.0	191.0	35.0

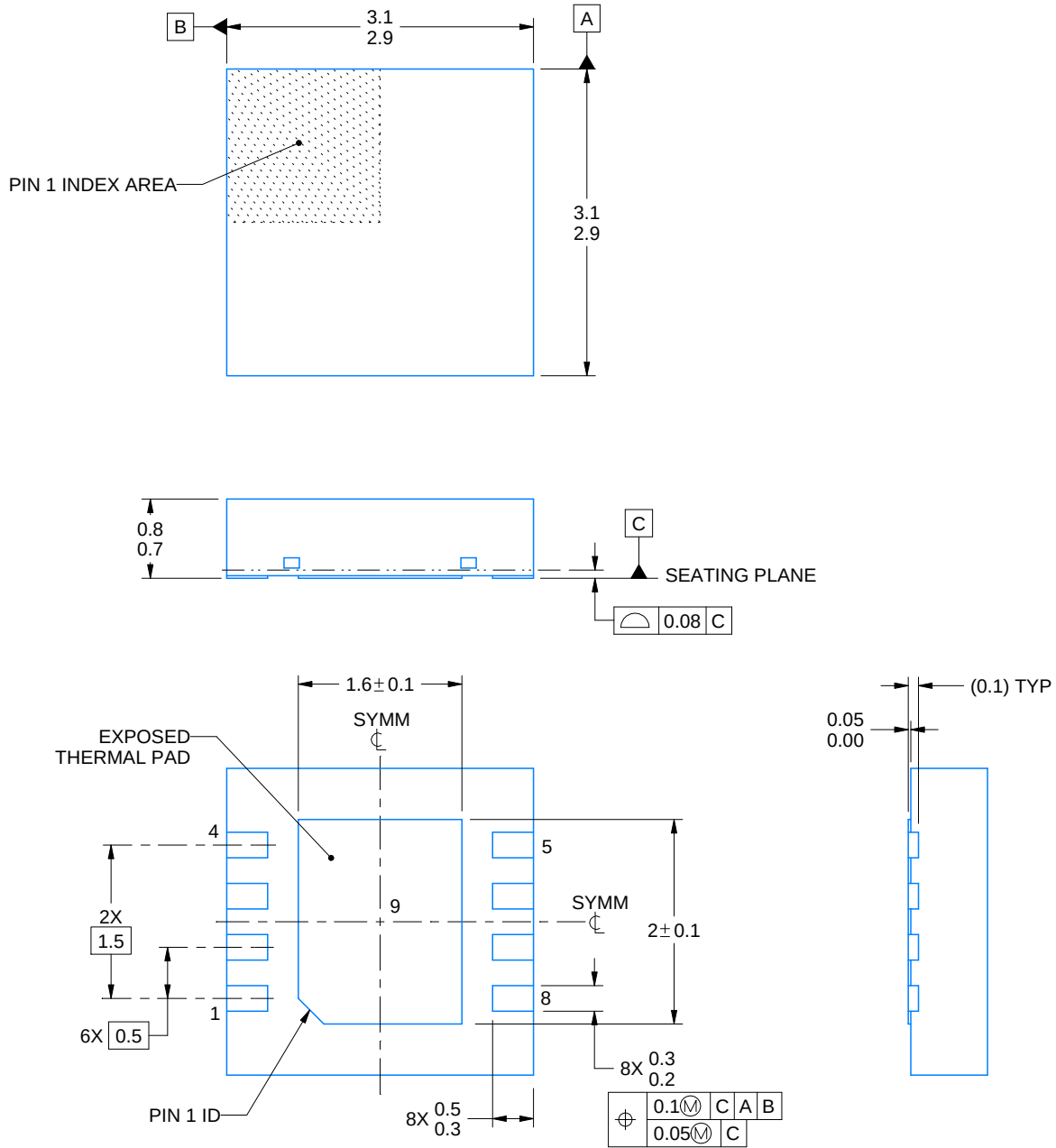
NGQ0008A



PACKAGE OUTLINE

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4214922/A 03/2018

NOTES:

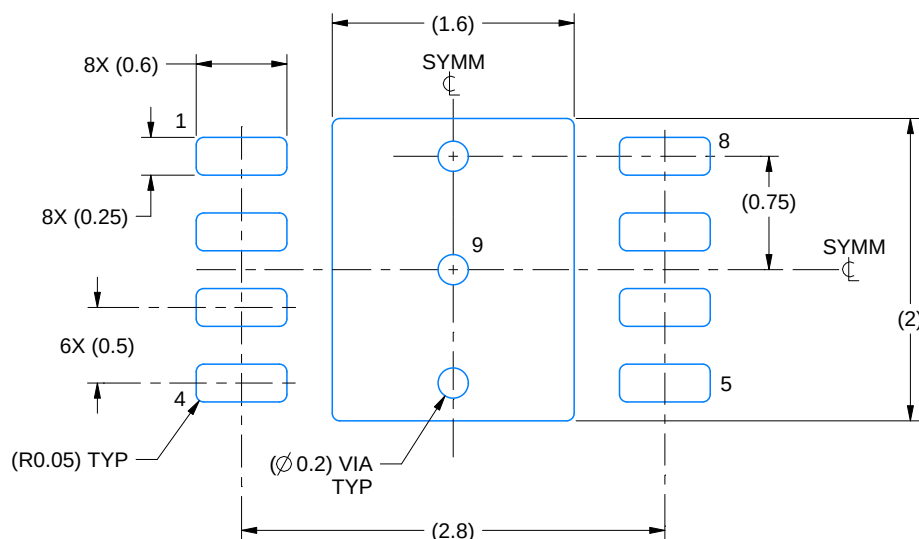
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

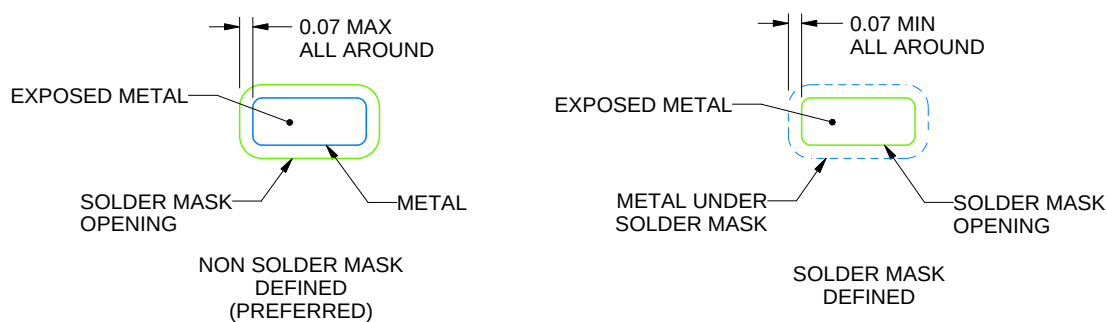
NGQ0008A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4214922/A 03/2018

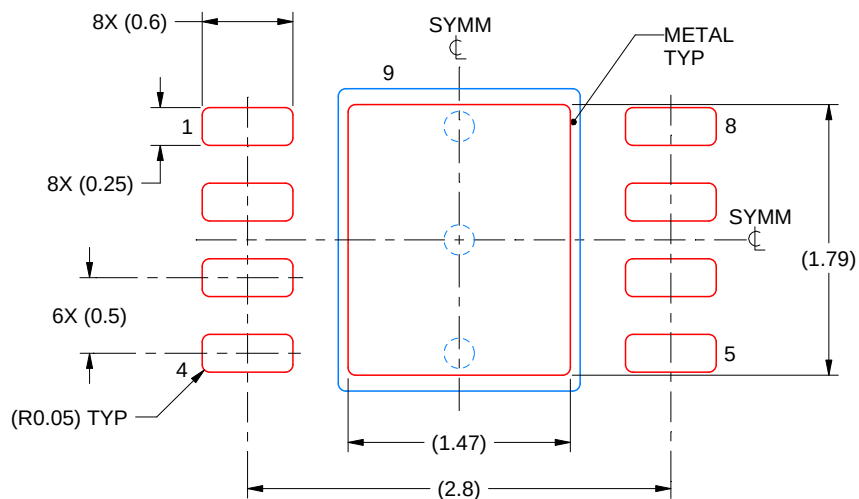
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

NGQ0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

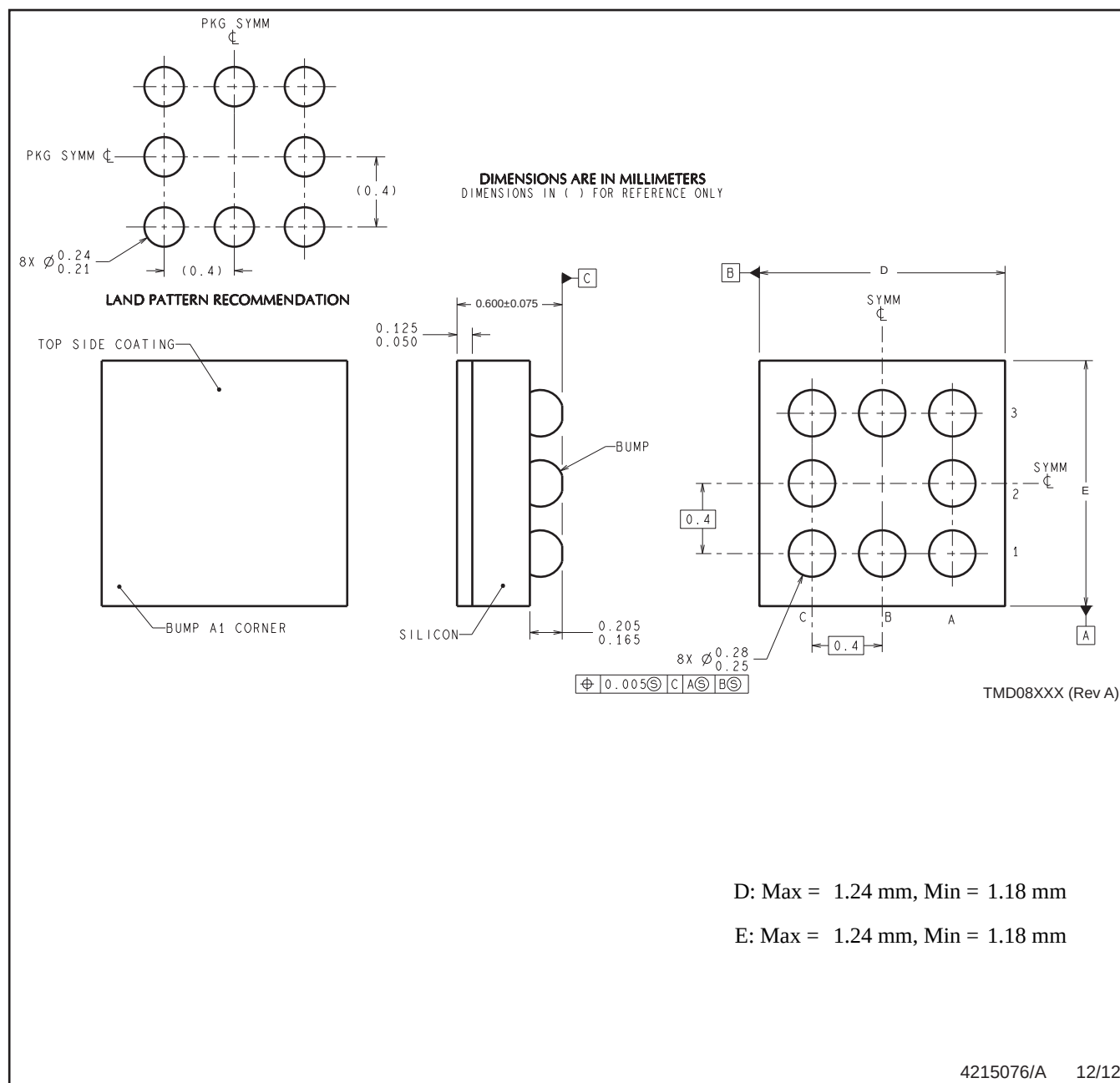
EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YFQ0008



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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