LMX2820 22.6-GHz Wideband PLLatinum™ RF Synthesizer With Phase Synchronization and JESD204B Support

1 Features

- Output frequency: 45 MHz to 22.6 GHz
- 36-fs rms jitter (12 kHz – 95 MHz) at 6 GHz
- High-performance PLL
  - Figure of merit: –236 dBc/Hz
  - Normalized 1/f noise: –134 dBc/Hz
  - -95 dBc Integer Mode Spurs (f_{PD}=100 MHz)
  - High phase detector frequency
    - 400-MHz integer mode
    - 300-MHz fractional mode
  - Programmable input multiplier
  - Direct PFD input for offset mixing support allowing PLL N divider to be one for ultra-low jitter
- 2.5-µs fast VCO calibration time
- Mute pin with 200-ns mute/unmute time
- –45-dBc VCO leakage with doubler enabled
- Support for external VCO up to 22.6-GHz
- Synchronization of output phase across multiple devices
- Two differential RF outputs and one differential SYSREF output for JESD204B support

2 Applications

- Radar and electronic warfare
- 5G and mm-Wave wireless infrastructure
- Microwave backhaul
- Test and measurement equipment
- High-speed data converter clocking

3 Description

The LMX2820 is a high-performance, wideband synthesizer that can generate any frequency in the range of 45 MHz to 22.6 GHz. The high performance PLL with figure of merit of –236 dBc/Hz and high phase detector frequency can attain very low in-band noise and integrated jitter. The high-speed N-divider has no pre-divider, thus significantly reducing the amplitude and number of spurs. There is also a programmable input multiplier to mitigate integer boundary spurs.

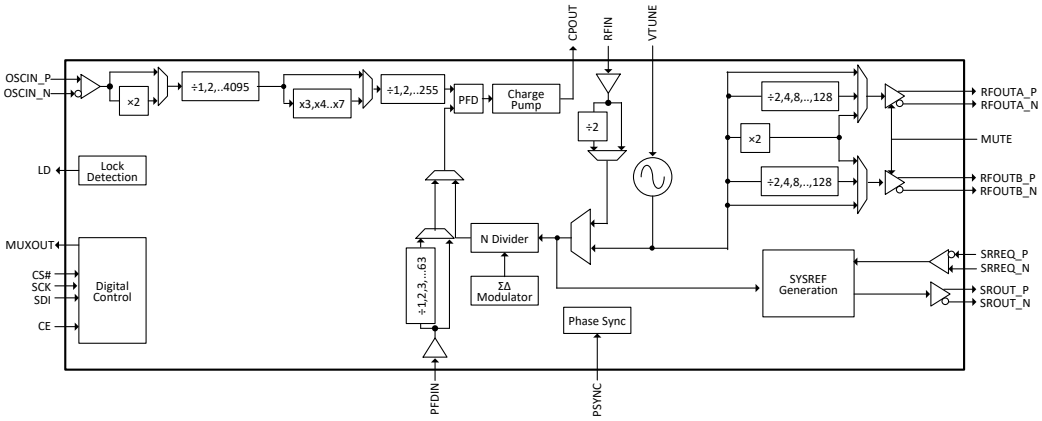
The LMX2820 allows users to synchronize the output of multiple devices and also enables applications that need deterministic delay between input and output. The fast calibration algorithm greatly reduces the VCO calibration time, enabling systems requiring fast frequency hopping. The LMX2820 can generate or repeat SYSREF that is compliant to the JESD204B standard, allowing for its use as a low-noise clock source for high-speed data converters. This synthesizer can also be used with an external VCO. A direct PFD input pin is provided to support offset mixing for low spurious transmission.

The device runs from a single 3.3-V supply and has integrated LDOs that eliminate the need for onboard low-noise LDOs.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMX2820	VQFN (48)	7 mm x 7 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2020) to Revision C (February 2021)	Page
• Changed data sheet origin data from December 2018 to June 2020	1

Changes from Revision A (November 2020) to Revision B (December 2020)	Page
• Changed PSYNC pin description	3
• Changed from V to Vpp. Therefore numbers double, but actual voltage is the same	7
• Changed PFDIN sensitivity graph	11

Changes from Revision * (June 2020) to Revision A (November 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed data sheet status from: Advanced Information to: Production Data	1

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5 Pin Configuration and Functions

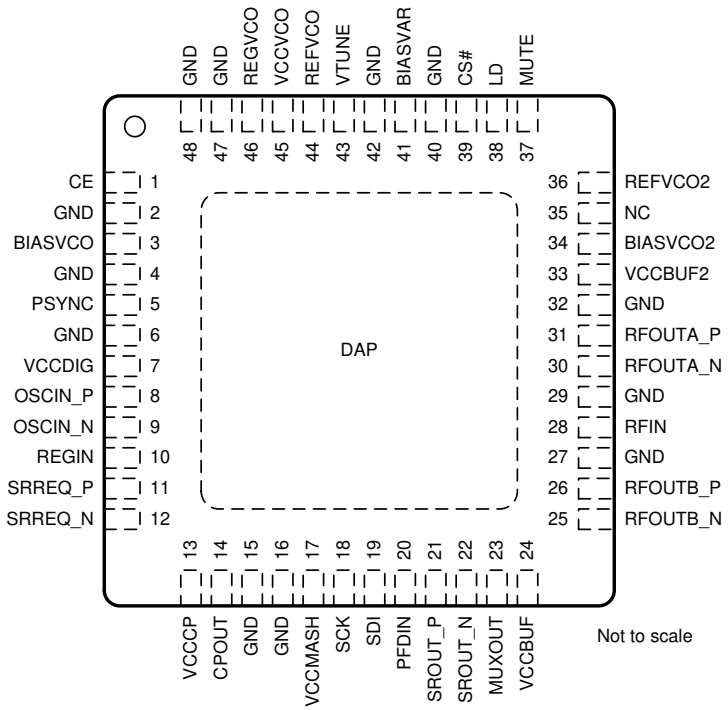

Figure 5-1. RTC Package 48-Pin VQFN Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.[1]		
SUPPLY AND GROUND			
VCCBUF	24	P	Output buffer supply. Connect to 3.3-V with a low-ESR, 0.1-µF and a 1-µF decoupling capacitor to ground.
VCCBUF2	33	P	Buffer supply. Connect to 3.3-V with a low-ESR, 0.1-µF and a 1-µF decoupling capacitor to ground.
VCCCP	13	P	Charge pump supply. Connect to 3.3-V with a 1-µF decoupling capacitor to ground.
VCCDIG	7	P	Digital supply. Connect to 3.3-V with a low-ESR, 0.1-µF and a 1-µF decoupling capacitor to ground.
VCCMASH	17	P	Digital supply. Connect to 3.3-V with a low-ESR, 0.1-µF and a 1-µF decoupling capacitor to ground.
VCCVCO	45	P	VCO supply. Connect to 3.3-V with a low-ESR, 0.1-µF and a 1-µF decoupling capacitor to ground.

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Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.[1]		
GND	2	G	Ground
	4		
	6		
	15		
	16		
	27		
	29		
	32		
	40		
	42		
	47		
	48		
DAP	—	—	Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.
NC	35	NC	Connect to ground.
BIAS/LDO BYPASS			
BIASVAR	41	B	VCO varactor bias. Connect a 1-µF decoupling capacitor to ground.
BIASVCO	3	B	VCO bias. Connect a low-ESR capacitor in the range of 0.47-µF (for fastest calibration time) to 4.7-µF (for optimal in-band phase noise)
BIASVCO2	34	B	VCO bias. Connect a 1-µF decoupling capacitor to ground. Place close to pin.
REFVCO2	36	B	VCO supply reference. Connect a 1-µF decoupling capacitor to ground.
REGIN	10	B	Input reference path regulator decoupling. Connect a 1-µF decoupling capacitor to ground. Place close to pin. An additional low-ESR, 0.1-µF decoupling capacitor is recommended for high-frequency noise filtering.
REGVCO	46	B	VCO regulator node. Connect a 1-µF decoupling capacitor to ground.
REFVCO	44	B	VCO supply reference. Connect a 10-µF decoupling capacitor to ground.
DIGITAL INPUTS			
CE	1	I	Chip Enable. High-impedance CMOS input. 1.8-V to 3.3-V logic. Active HIGH powers on the device.
MUTE	37	I	Buffer mute control. High-impedance CMOS input. 1.8-V to 3.3-V logic.
PSYNC	5	I	Phase synchronization with configurable input signal level. Connect with series 100 Ω to PSYNC signal, or to GND if not used.
CS#	39	I	SPI latch. High-impedance CMOS input. 1.8-V to 3.3-V logic.
SCK	18	I	SPI clock. High-impedance CMOS input. 1.8-V to 3.3-V logic.
SDI	19	I	SPI data. High-impedance CMOS input. 1.8-V to 3.3-V logic.
ANALOG INPUTS			
OSCIN_P	8	I	Reference input clock (+). High impedance self-biasing pin. Requires AC coupling. If not being used, AC-couple it to ground through a 50-Ω resistor.
PFDIN	20	I	External PFD input. Self-biasing pin. Requires AC coupling and an external 50-Ω resistor to ground.
RFIN	28	I	External VCO input. Internal 50 Ω terminated. Requires AC coupling.
OSCIN_N	9	I	Reference input clock (–). High impedance self-biasing pin. Requires AC coupling. If not being used, AC-couple it to ground through a 50-Ω resistor.
SRREQ_P	11	I	Differential SYSREF input clock (+). Supports AC and DC coupling.
VTUNE	43	I	VCO tuning voltage input. Connect a 1.5-nF or more capacitor to VCO ground.
SRREQ_N	12	I	Differential SYSREF input clock (–). Supports AC and DC coupling.

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Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.[1]		
OUTPUTS			
CPOUT	14	O	Charge pump output. Recommend connecting C1 of loop filter close to this pin.
LD	38	O	Lock detect output. 3.3-V logic.
MUXOUT	23	O	SPI readback output. 3.3-V logic. High impedance when CE = LOW.
RFOUTA_N	30	O, PU	Differential output A (–). Internal 50-Ω pullup. Requires AC coupling.
RFOUTA_P	31	O, PU	Differential output A (+). Internal 50-Ω pullup. Requires AC coupling.
RFOUTB_N	25	O, PU	Differential output B (–). Internal 50-Ω pullup. Requires AC coupling.
RFOUTB_P	26	O, PU	Differential output B (+). Internal 50-Ω pullup. Requires AC coupling.
SROUT_N	22	O, PU	Differential SYSREF output (–). Internal 50-Ω pullup.
SROUT_P	21	O, PU	Differential SYSREF output (+). Internal 50-Ω pullup.

(1) The definitions below define the I/O type for each pin.
- P = Power supply
- G = Ground
- NC = No connect. Pin may be grounded or left unconnected.
- B = Bias/LDO Bypass
- I = Input
- O = Output
- PU = Pullup

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	–0.3	3.6	V
V_{IN}	IO input voltage		V_{CC}+0.3	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature			125	°C
V_{CC}	Supply voltage	3.15	3.3	3.45	V

6.4 Thermal Information

THERMAL METRIC[1]		LMX2820 RTC (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85 °C. Typical values are at V_{CC} = 3.3 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{CC}	Supply current	One direct RF output[1]		500		mA
		One divided down RF output[2]		580		
		One RF output with VCO doubler enabled[3]		590		
		RFIN External Feedback Mode, Internal VCO		530		
		PFDIN External Feedback Mode, Internal VCO[5]		455		
		External VCO Mode[4]		290		
I_{CC}POR	Power-on-reset current			234		
I_{CC}PD	Power-down current			10		
INPUT SIGNAL PATH						
f_{OSCin}	OSCin input frequency	OSC_2X = 0 (Doubler bypassed)	5		1400	MHz
		OSC_2X = 1 (Doubler enabled); Single-ended input buffer	5		250	
V_{OSCin}	OSCin input voltage[6]	Single-ended input buffer	0.3		3.6	Vpp
		Differential input buffer	0.1		1	
f_{MULTin}	Multiplier input frequency	MULT ≥ 3	30		70	MHz
$f_{MULTout}$	Multiplier output frequency		180		250	
PLL						
f_{PD}	Phase detector frequency[7]	Integer channel	5		400	MHz
		1st and 2nd order modulator	5		300	
		3rd order modulator	5		225	
I_{CPout}	Charge pump current	CPG = 1		1.4		mA
		CPG = 8		2.8		
		CPG = 4		5.6		
		CPG = 12		8.4		
		CPG = 15		15.4		
$PN_{PLL_1/f}$	Normalized PLL 1/f noise[8]			–134		dBc/Hz
PN_{PLL_Flat}	Normalized PLL noise floor[8]	Integer channel[9]		–236		
		Fractional channel[10]		–236		
f_{RFIN}	RFin input frequency		1000		22600	MHz
P_{RFIN}	RFin input power		–10		5	dBm
RL_{RFIN}	RFin return loss	2 GHz ≤ f_{RFin} ≤ 22 GHz		−8		dB
f_{PFDIN}	PFDin input frequency		20		2000	MHz
v_{PFDIN}	PFDin input voltage		0.2		2	Vpp
VCO						
f_{VCO}	VCO frequency		5650		11300	MHz

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3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85 °C. Typical values are at V_{CC} = 3.3 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PN_{VCO}	Open-loop VCO phase noise	f_{VCO} = 6.0 GHz	10 kHz		-77.0		dBc/Hz
			100 kHz		-110.3		
			1 MHz		-131.9		
			10 MHz		-151.0		
			100 MHz		-159.5		
		f_{VCO} = 6.8 GHz	10 kHz		-76.5		
			100 kHz		-109.3		
			1 MHz		-130.7		
			10 MHz		-149.8		
			100 MHz		-159.3		
		f_{VCO} = 7.6 GHz	10 kHz		-75.8		
			100 kHz		-108.5		
			1 MHz		-130.2		
			10 MHz		-149.2		
			100 MHz		-159.2		
		f_{VCO} = 8.4 GHz	10 kHz		-74.7		
			100 kHz		-107.6		
			1 MHz		-129.4		
			10 MHz		-148.8		
			100 MHz		-159.0		
		f_{VCO} = 9.4 GHz	10 kHz		-76.0		
			100 kHz		-105.5		
			1 MHz		-128.0		
			10 MHz		-147.4		
			100 MHz		-157.9		
		f_{VCO} = 10.2 GHz	10 kHz		-75.9		
			100 kHz		-105.6		
			1 MHz		-127.5		
			10 MHz		-146.8		
			100 MHz		-157.6		
		f_{VCO} = 11.2 GHz	10 kHz		-75.4		
			100 kHz		-104.4		
			1 MHz		-126.4		
			10 MHz		-145.8		
			100 MHz		-156.5		
K_{VCO}	VCO gain	f_{VCO} = 6.0 GHz			95		MHz/V
		f_{VCO} = 6.8 GHz			108		
		f_{VCO} = 7.6 GHz			131		
		f_{VCO} = 8.4 GHz			140		
		f_{VCO} = 9.4 GHz			149		
		f_{VCO} = 10.2 GHz			156		
		f_{VCO} = 11.2 GHz			139		
t_{VCOcal}	VCO calibration time	f_{OSCin} = f_{PD} = 100 MHz; Switch between 5.65 GHz and 11.3 GHz; Using Instant Calibration 0.47 µF capacitor at VbiasVCO pin			2.5		µs

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3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85 °C. Typical values are at V_{CC} = 3.3 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert\Delta_{TC}L\rvert$	Allowable temperature drift(11)	VCO not being recalibrated; –40 °C ≤ T_A ≤ 85 °C				125	°C
RF OUTPUT							
f_{OUT}	RF output frequency			45		22600	MHz
P_{OUT}	Single-ended output power(12)	OUTx_PWR=7	f_{OUT} = 22 GHz		3		dBm
			f_{OUT} = 11 GHz		5		
			f_{OUT} ≤ 5.5 GHz		6		
$H_{1/2}$	1/2 harmonic(13)		f_{OUT} = 2 x f_{VCO} = 22 GHz		−45		dBc
$H_{3/2}$	3/2 harmonic		f_{OUT} = 2 x f_{VCO} = 11.3 GHz to 22.6 GHz		−65		
H2	Second harmonic		f_{VCO} = f_{OUT} = 11 GHz		−20		
			f_{VCO} = 11 GHz; f_{OUT} = 5.5 GHz		−35		
			f_{OUT} = 2 x f_{VCO} = 11.3 GHz to 22.6 GHz		−25		
H3	Third harmonic		f_{VCO} = f_{OUT} = 11 GHz		−20		
			f_{VCO} = 11 GHz; f_{OUT} = 5.5 GHz		−10		
P_{MUTE}	Single-ended output power when output is muted(12)	f_{OUT} = 22 GHz			−32		dBm
		f_{OUT} = 11 GHz			−32		
		f_{OUT} = 5.5 GHz			−53		
t_{MUTE}	Mute enable time	f_{OUT} = 11 GHz			200		ns
t_{unMUTE}	Mute disable time	f_{OUT} = 11 GHz			200		
isoCH	Channel to channel isolation	$f_{OUT}A$ = 11 GHz; $f_{OUT}B$ = 5.5 GHz; OUTx_PWR=7			–40		dBc
PHASE SYNCHRONIZATION							
$f_{OSCin}SYNC$	OSCin input frequency with SYNC	Category 3		5		200	MHz
DIGITAL INTERFACE (CE, SCK, SDI, CS#, PSYNC, MUTE)							
V_{IH}	High-level input voltage			1.2		V_{CC}	V
V_{IL}	Low-level input voltage					0.6	
I_{IH}	High-level input current	CS#, MUTE, CE				25	µA
		SCK, SDI, PSYNC				70	
I_{IL}	Low-level input current			−1			
V_{OH}	High-level output voltage	MUXout, LD	Load current = –3 mA	V_{CC}–0.5			V
V_{OL}	Low-level output voltage		Load current = 3 mA			0.4	

(1) f_{OSCin} = f_{PD} = 100 MHz; f_{VCO} = f_{OUT} = 11 GHz; P_{OUT} = 0 dBm; OSC_2X = 0; MULT = 1.
(2) f_{OSCin} = f_{PD} = 100 MHz; f_{VCO} = 11 GHz; f_{OUT} = 5.5 GHz; P_{OUT} = 0 dBm; OSC_2X = 0; MULT = 1.
(3) f_{OSCin} = f_{PD} = 100 MHz; f_{VCO} = 11 GHz; f_{OUT} = 22 GHz; P_{OUT} = 0 dBm; OSC_2X = 1; MULT = 1.
(4) f_{OSCin} = f_{PD} = 100 MHz; f_{RFin} = 11 GHz; f_{OUT} = 11 GHz (from external VCO); OSC_2X = 0; MULT = 1.
(5) f_{OSCin} = f_{PD} = 100 MHz; f_{PFDin} = 2 GHz; f_{OUT} = 11 GHz (from external VCO); OSC_2X = 0; MULT = 1.
(6) See applications section for definition of OSCin input voltage.
(7) For lower VCO frequencies, the N-divider minimum value can limit the phase detector frequency.
(8) Measured with a clean OSCin signal with a high slew rate using a wide loop bandwidth. The noise metrics model the PLL noise for an infinite loop bandwidth as: PLL_Total = $10\cdot\log[10^{(PLL_Flat/10)}+10^{(PLL_Flicker/10)}]$; PLL_Flat = PN1 Hz + $20\cdot\log(N) + 10*\log(f_{PD})$; PLL_Flicker = PN10 kHz - $10\cdot\log(\text{Offset}/10\text{ kHz}) + 20\cdot\log(f_{OUT}/1\text{ GHz})$.
(9) f_{OSCin} = 100 MHz, f_{PD} = 200 MHz; f_{VCO} = f_{OUT} = 11 GHz.
(10) f_{OSCin} = f_{PD} = 100 MHz; f_{VCO} = f_{OUT} = 10.999 GHz; Fractional denominator = 1000.
(11) Not tested in production. Ensured by characterization. Allowable temperature drift refers to programming the device at an initial temperature and allowing this temperature to drift WITHOUT reprogramming the device, and still have the device stay at lock. This change could be up or down in temperature and the specification does not apply to temperatures that go outside the recommended operating temperatures of the device.

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(12) Measured with one of the RF output differential pair pins, the unused pin is 50-Ω terminated. See applications section for details.
(13) One RF output is active. Measured differentially with JSO-51-471/6S balun. Consult typical performance plots to see how this varies over conditions.

6.6 Timing Requirements

3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85 °C. Typical values are at V_{CC} = 3.3 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SERIAL INTERFACE WRITE TIMING						
f_{SCK}	SCK frequency	1 / (t_{CWL}+t_{CWH})			40	MHz
t_{CE}	SCK to CSB low time		5			ns
t_{CS}	SDI to SCK setup time		2			ns
t_{CH}	SDI to SCK hold time		2			ns
t_{CWH}	SCK pulse width high		10			ns
t_{CWL}	SCK pulse width low		10			ns
t_{CES}	CSB to SCK setup time		10			ns
t_{EWH}	CSB pulse width high		3			ns
SERIAL INTERFACE READ TIMING						
f_{SCK}	SCK frequency	1 / (t_{CWL}+t_{CWH})			40	MHz
t_{CE}	SCK to CSB low time		5			ns
t_{CS}	SDI to SCK setup time		2			ns
t_{CH}	SDI to SCK hold time		2			ns
t_{CWH}	SCK pulse width high		10			ns
t_{CWL}	SCK pulse width low		10			ns
t_{CES}	CSB to SCK setup time		10			ns
t_{EWH}	CSB pulse width high		3			ns
t_{OD}	SCK to MUXout delay time				10	ns
SYNC AND SYSREFREQ TIMING						
t_{CS}	Pin to OSCin setup time		2.5			ns
t_{CH}	Pin to OSCin hold time		2			ns

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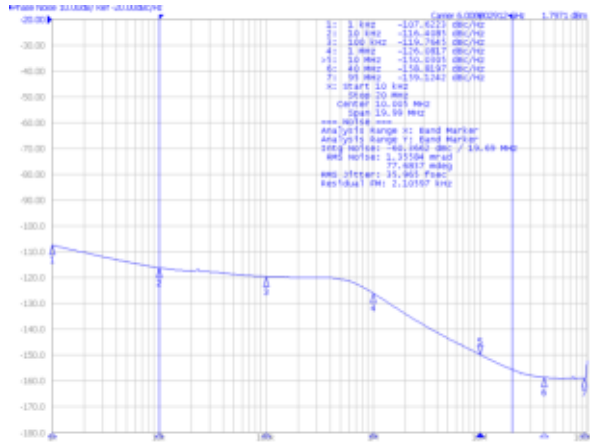
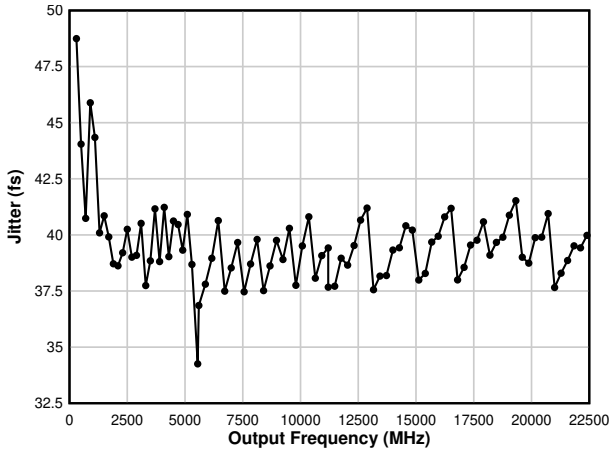
6.7 Typical Characteristics



f_{OUT} = 6 GHz, f_{PD}=200 MHz,Jitter=36 fs 12k-20 MHz

Figure 6-1. Closed-Loop Noise



Integration Range is 12k-20 MHz

Figure 6-2. Integrated Jitter

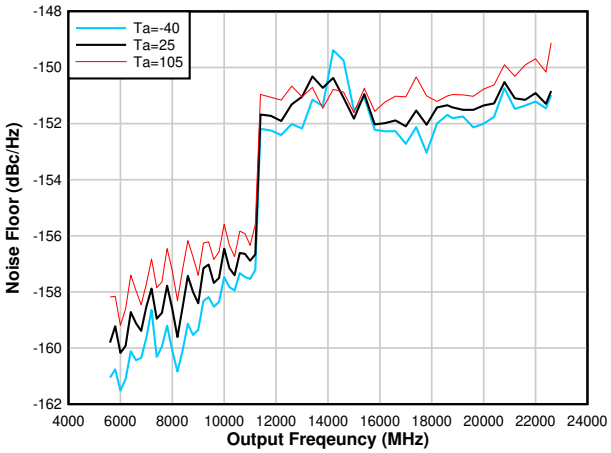
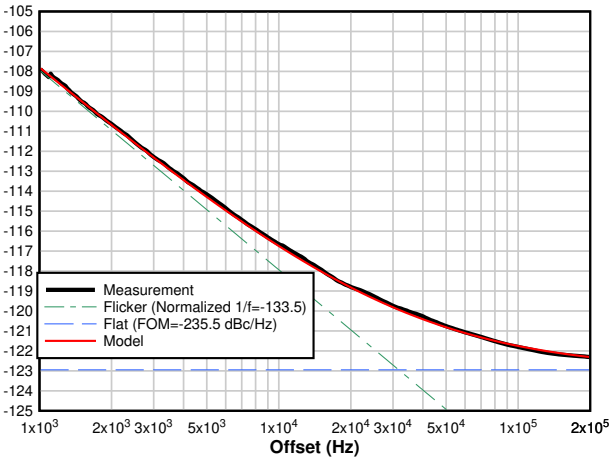


Figure 6-3. Noise Floor



f_{OSC}=100 MHz, f_{PD}=200 MHz, f_{OUT}=6 GHz, OSC_2X=1
Use of input doubler slightly degrades PLL noise metrics.

Figure 6-4. PLL Noise Metrics

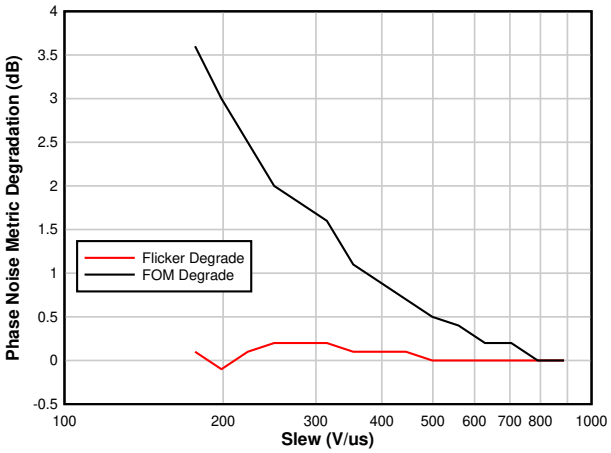


Figure 6-5. PLL Noise Metric Degradation vs. OSCin Slew Rate

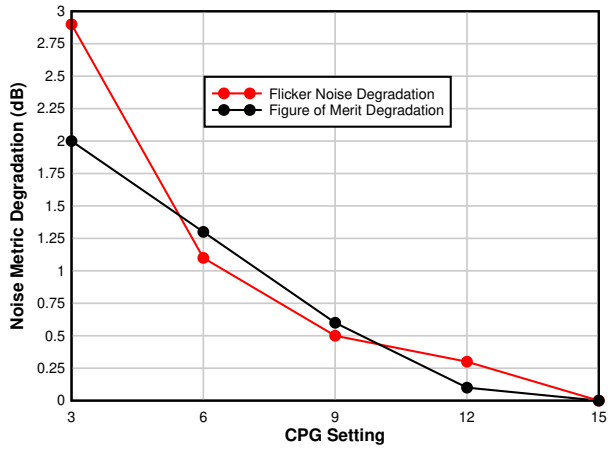
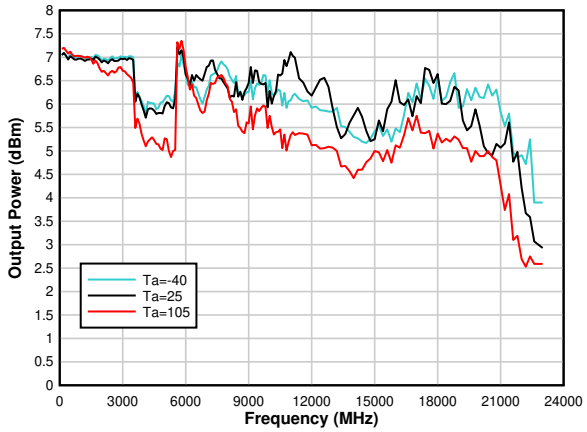


Figure 6-6. IPLL Noise Metric Degradation vs. Charge Pump Gain



Single-ended, OUTx_PWR=7, board losses de-embedded

Figure 6-7. Output Power vs. Temperature

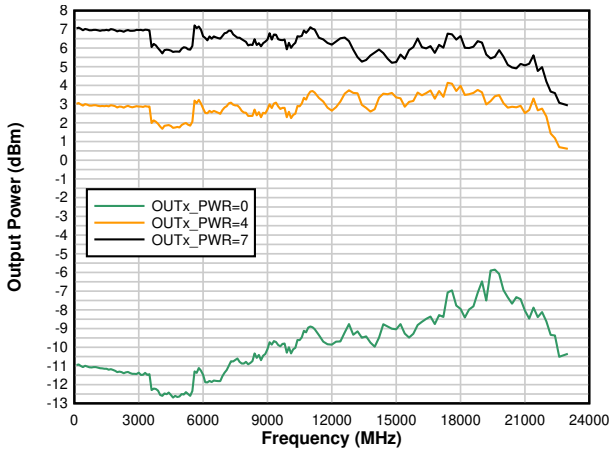


Figure 6-8. Output Power vs. OUTx_PWR

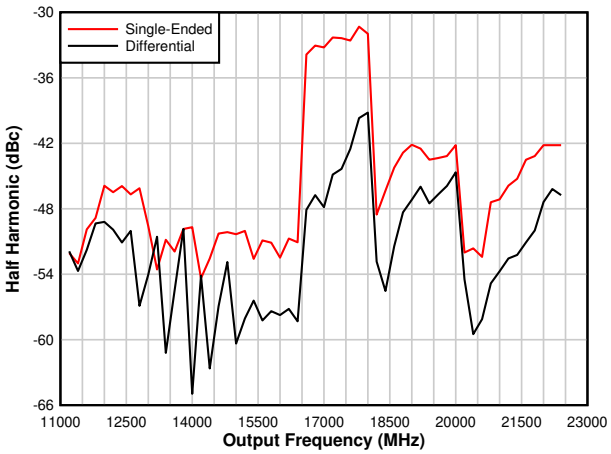


Figure 6-9. Output Half Harmonic with Doubler Enabled

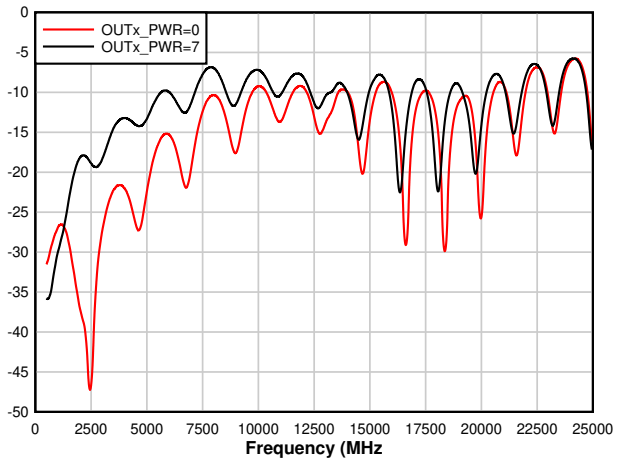


Figure 6-10. RF Output Return Loss

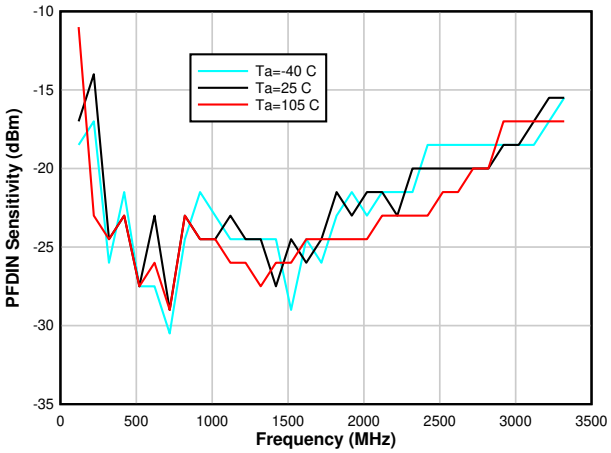


Figure 6-11. PFDIN Pin Input Sensitivity

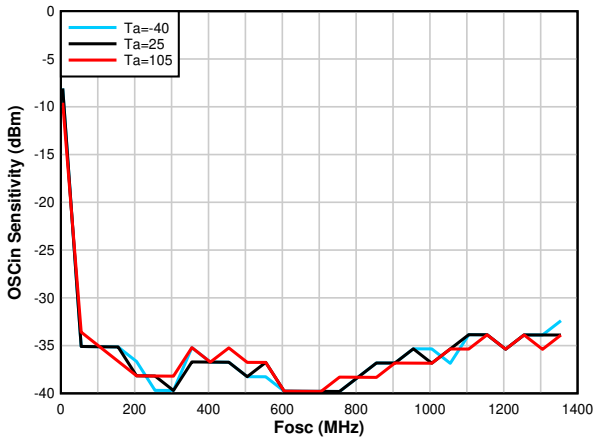


Figure 6-12. OSCin Input Sensitivity

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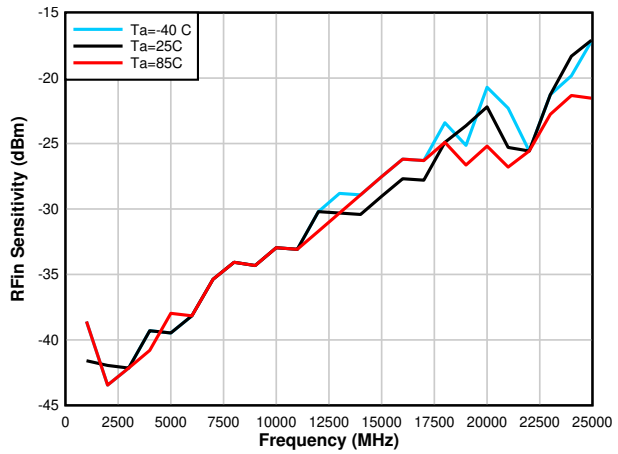


Figure 6-13. RFIN Input Sensitivity

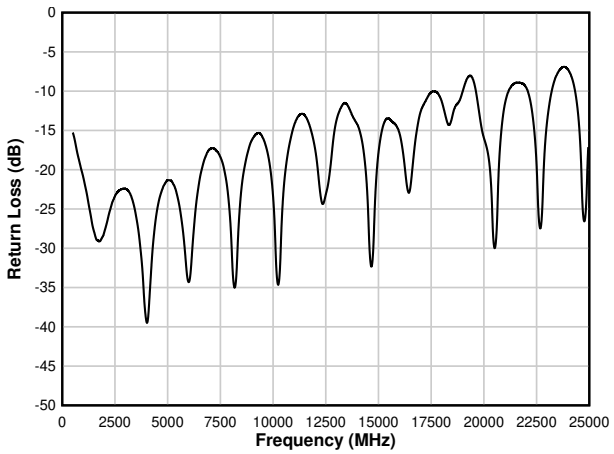
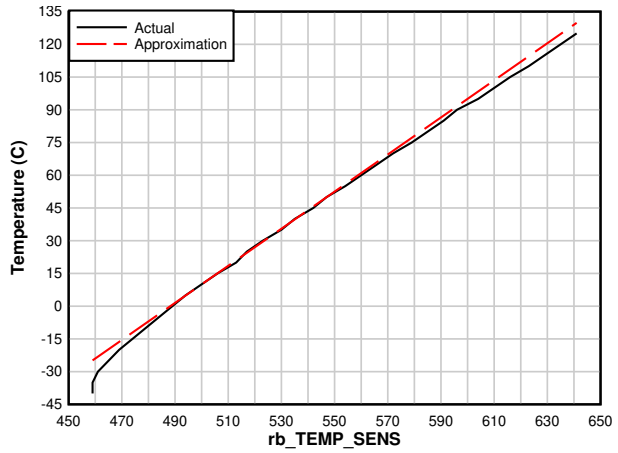
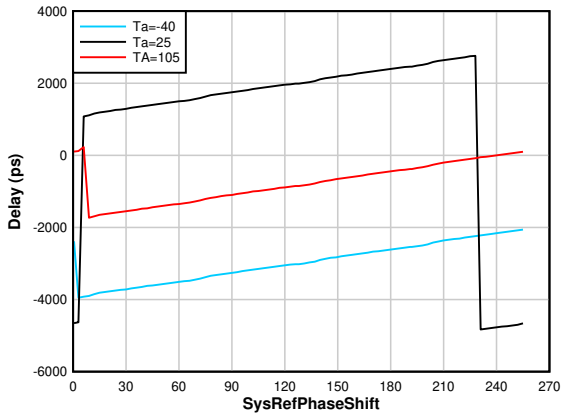


Figure 6-14. RFIN Return Loss



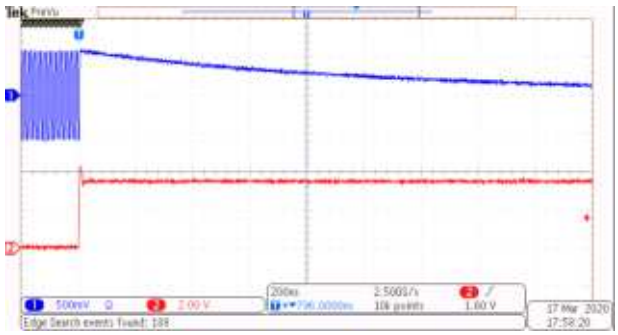
Approximation = 0.85*rb_TEMP_SENS - 415

Figure 6-15. Temperature Sensor Readback



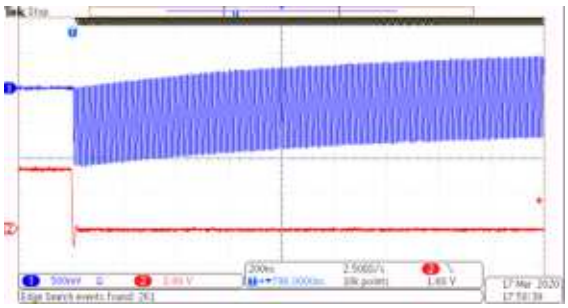
f_{VCO}=8.4 GHz, SYSREF_DIV_PRE=8,Step Size=7.6 ps

Figure 6-16. SysRef Delays vs Temperature



This is showing the output is muted in well under 200 ns

Figure 6-17. Mute Pin Disable Output Time



Output is unmuted in under 200 µs. DC bias level can stabilize faster if smaller AC-coupling capacitor is used.

Figure 6-18. Mute Pin Enable Output Time

7 Detailed Description

7.1 Overview

The LMX2820 is a high-performance, wideband frequency synthesizer with an integrated VCO and output divider. The VCO operates from 5.65 GHz to 11.3 GHz, and this can be combined with the output divider and doubler to produce any frequency in the range of 45 MHz to 22.6 GHz. Within the input path, there are two dividers and a multiplier for flexible frequency planning. The multiplier also allows the reduction of spurs by moving the frequencies away from the integer boundary. The PLL is fractional-N PLL with a programmable delta-sigma modulator up to third order. The fractional denominator is a programmable 32-bit long, which can easily provide fine frequency steps below 1-Hz resolution, or be used to do exact fractions like 1/3, 7/1000, and many others. The phase frequency detector goes up to 300 MHz in fractional mode or 400 MHz in integer mode, although minimum N-divider values must also be taken into account. For applications where deterministic or adjustable phase is desired, the PSYNC Pin can be used to get the phase relationship between the OSCIN and RFOUT pins deterministic. When this is done, the phase can be adjusted in very fine steps of the VCO period divided by the fractional denominator. The ultra-fast VCO calibration is designed for applications where the frequency must be swept or abruptly changed. The JESD204B support includes using the SROUT output to create a differential SYSREF output that can be either a single pulse or a series of pulses that occur at a programmable distance away from the rising edges of the output signal. The LMX2820 device requires only a single 3.3-V power supply. The internal power supplies are provided by integrated LDOs, eliminating the need for high-performance external LDOs. The digital logic for the SPI interface and is compatible with voltage levels from 1.8 V to 3.3 V. Table 7-1 shows the range of several of the dividers, multipliers, and fractional settings.

Table 7-1. Dividers, Multipliers, and Fractional Settings

BLOCK	SUB-BLOCK	FIELD	MIN	MAX	COMMENTS
Input Path	Doubler	OSC_2X	0 (= 1X)	1 (= 2X)	The low noise doubler can be used to increase the phase detector frequency to improve phase noise and avoid spurs.
	Pre-R Divider	PLL_R_PRE	1	4095	Only use the Pre-R divider if the frequency is too high for the input multiplier or for the Post-R divider.
	Input Multiplier	MULT	3	7	The input multiplier is effective for spur avoidance, increases PLL noise.
	Post-R Divider	PLL_R	1	255	The maximum input frequency for this divider is 500 MHz for PLLR=2 and 250 MHz for PLL_R>2. Use the Pre-R divider if necessary.
N Divider	N Divider	PLL_N	≥ 12	32767	The minimum divide depends on the modulator order, VCO frequency/core, and choice of internal/external VCO.
	Fractional numerator	PLL_NUM	1	$2^{32} – 1$ = 4294967295	PLL_NUM should be smaller than PLL_DEN
	Fractional Denominator	PLL_DEN	0	$2^{32} – 1$ = 4294967295	The fractional denominator is programmable and can assume any value between 1 and $2^{32} – 1$; it is not a fixed denominator.
	Fractional Order	MASH_ORDER	0	3	The fractional order is programmable from 0 to 3; 0 is integer mode.
PFDIN Path	PFD Input Divider	EXTPFD_DIV	1	63	
External VCO	External VCO Divider	EXTVCO_DIV	1	2	If the VCO frequency exceeds 11.3 GHz, then use divide by 2, otherwise use divide by 1 (bypass).
SYSREF	Pre-Divider	SYSREF_DIV_PRE	1	4	Supports 1, 2 and 4 ONLY. There is an additional divide-by-2 in this block. The total pre-divider value is 2 × SYSREF_DIV_PRE.
	Divider	SYSREF_DIV	0	2047	Total divider value is 2 + SYSREF_DIV.
	Extra Divide	None	4	4	This is a fixed divide-by-4 divider.

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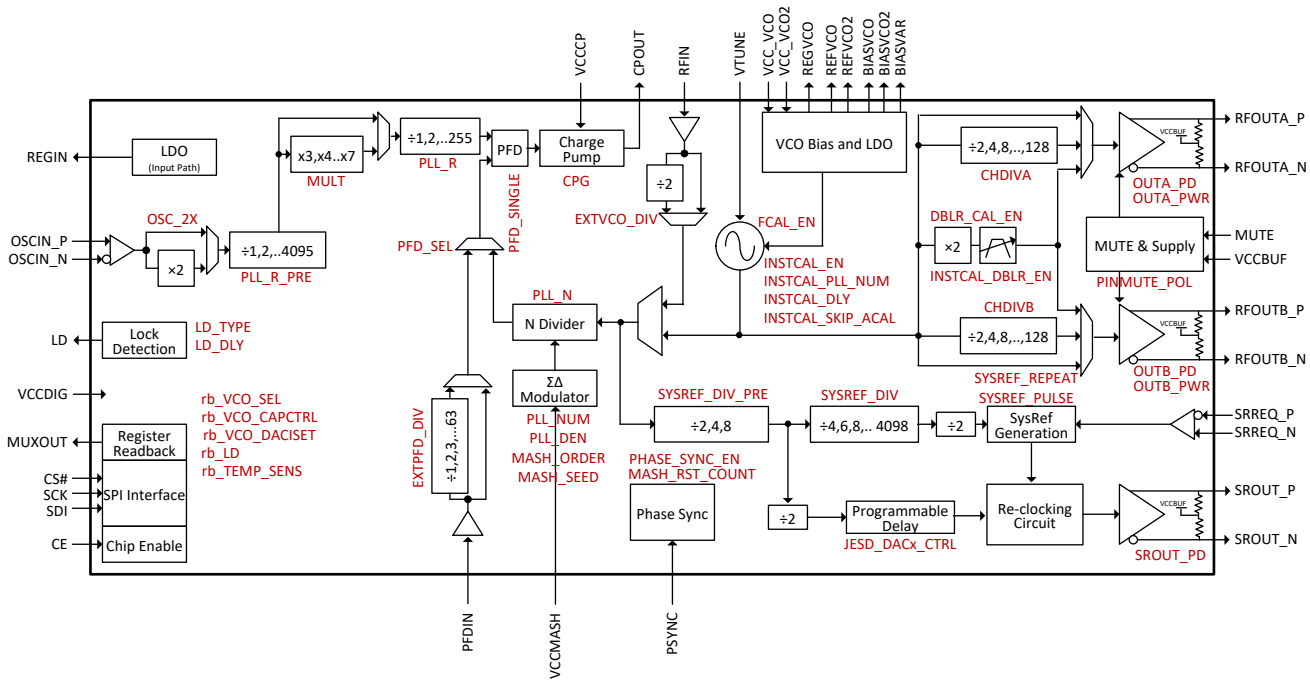
Table 7-1. Dividers, Multipliers, and Fractional Settings (continued)

BLOCK	SUB-BLOCK	FIELD	MIN	MAX	COMMENTS
Outputs	OUTA Divider	CHDIVA	2	128	This is a power-of-2 divider that supports 2, 4, 8, 16, 32, 64 and 128.
	OUTB Divider	CHDIVB	2	128	This is a power-of-2 divider that supports 2, 4, 8, 16, 32, 64 and 128.
	Output Frequency	n/a	45	22600	Below 5.65 GHz, the channel divider is used. 5.65 - 11.23 GHz is direct VCO. 11.3 - 22.6 GHz is using the output doubler.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference Oscillator Input

The OSCIN pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling caps at the pin. A CMOS clock or XO can drive the single-ended OSCIN pins. Differential clock input is also supported, making it easier to interface with high-performance system clock devices such as TI's LMK series clock devices. As the OSCIN signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCIN pin at the time of the VCO needs to calibrate.

7.3.2 Input Path

The reference path consists of an OSCIN doubler (OSC_2X), Pre-R divider, multiplier (MULT) and a Post-R divider. The OSCIN doubler (OSC_2X) can double up low OSCIN frequencies. Pre-R (PLL_R_PRE) and Post-R (PLL_R) dividers both divide frequency down while the multiplier (MULT) multiplies frequency up. The purposes of adding a multiplier is to reduce integer boundary spurs or to increase the phase detector frequency. Use Equation 1 to calculate the phase detector frequency, f_{PD}:

$$f_{PD} = f_{OSC} \times OSC_2X \times MULT / (PLL_R_PRE \times PLL_R) \quad (1)$$

7.3.2.1 Input Path Doubler (OSC_2X)

The OSCIN doubler allows one to double the input reference frequency up to 500 MHz. This doubler adds minimal noise and is useful for raising the phase detector frequency for better phase noise and also to avoid

spurs. When the phase-detector frequency is increased, the flat portion of the PLL phase noise improves. There are a few considerations when using the Input Path Doubler:

- The doubler works by acting on both the rising and falling edges of the input signal.
- The duty cycle needs to be close to 50%, or else the spurs will be very high.
- Using the Input Path Doubler degrades the PLL flicker noise and figure of merit by about 1 dB. However, the benefit of the higher phase detector frequency outweighs this.

7.3.2.2 Pre-R Divider (PLL_R_PRE)

The Pre-R divider serves the purpose of reducing the input frequency if it is too high for the input of the programmable multiplier (MULT) or post R divider.

7.3.2.3 Programmable Input Multiplier (MULT)

The MULT is useful for shifting the phase-detector frequency to avoid integer boundary spurs. The multiplier allows a multiplication of 3, 4, 5, 6, or 7. There are some considerations when using the input multiplier:

- The programmable input multiplier cannot be used at the same time that the Input Path Doubler is used.
- The programmable input multiplier degrades the PLL figure of merit by about 8 dB; it is for spur mitigation, not PLL noise improvement.
- The programmable input multiplier is most effective when VCO frequency is not close to a multiple of the OSCIN frequency.

7.3.2.4 R Divider (PLL_R)

The Post-R divider further divides down the frequency to the phase detector frequency. When it is used with PLL_R=2, the maximum input frequency to this divider is limited to 500 MHz. When it is used with PLL_R>2 then the maximum frequency to this divider is limited to 250 MHz.

7.3.3 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the R divider and N-divider, and generates a correction current corresponding to the phase error until the two signals are aligned in-phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed-loop bandwidth of the PLL. See Section 8.1 for more information. The polarity of the phase detector is configurable in order to suit for active loop filter application.

7.3.4 N Divider and Fractional Circuitry

The complete N divider divides down the VCO frequency to the phase detector frequency (f_{PD}). The output frequency of the VCO is changed by changing this total N divider value. The total N divider value consists of an integer portion and a fractional portion as shown in Equation 2:

$$N_{Total} = N_{Integer} + N_{Fractional} = PLL_N + (PLL_NUM / PLL_DEN) \quad (2)$$

7.3.4.1 Integer N Divide Portion (PLL_N)

Due to the requirements of the total N divider value to handle fractions and also high frequency, there are limitations based the modulator order and VCO frequency.

When using the internal VCO, the true minimum N divide is based on the VCO core. The VCO core frequencies may shift some with process, so the most reasonable thing to do is based this on worst case assumption for the VCO Core.

Table 7-2. Minimum N Divider Value for Internal VCO

f_{VCO}	WORST CASE CORE	MASH_ORDER = 0	MASH_ORDER = 1	MASH_ORDER = 2	MASH_ORDER = 3
5.65 - 6.35 GHz	VCO1	12	18	19	24
6.35 - 7.3 GHz	VCO2	14	21	22	26
7.3 - 8.1 GHz	VCO3	16	23	24	26
8.1 - 9.0 GHz	VCO4	16	26	27	29

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Table 7-2. Minimum N Divider Value for Internal VCO (continued)

f_{VCO}	WORST CASE CORE	MASH_ORDER = 0	MASH_ORDER = 1	MASH_ORDER = 2	MASH_ORDER = 3
9.0 - 9.8 GHz	VCO5	18	28	29	31
9.8 - 10.6 GHz	VCO6	18	30	31	33
10.6 - 11.3 GHz	VCO7	20	33	34	36

For the external VCO, the minimum N divides are slightly different. In cases where the VCO frequency is higher than 11.3 GHz, the VCO frequency must divided by 2 by setting EXTVCO_DIV bit.

Table 7-3. Minimum N Divider for External VCO

f_{RFIN} / (RFIN Divider)	MASH_ORDER = 0	MASH_ORDER = 1	MASH_ORDER = 2	MASH_ORDER = 3
0.5 - 4 GHz	12	12	14	20
4 - 5.5 GHz	12	15	18	24
5.5 - 7 GHz	14	18	20	26
7 - 8.5 GHz	16	23	24	26
8.5 - 10 GHz	20	28	29	35
10 GHz - 11.3 GHz	20	32	33	35

7.3.4.2 Fractional N Divide Portion (PLL_NUM and PLL_DEN)

The N-divider includes fractional compensation and can achieve any fractional denominator from 1 to (2^{32} – 1). The fractional portion of the total N divide value is $N_{Fractional}$ = PLL_NUM / PLL_DEN. The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200 MHz, the output can increment in steps of 200 MHz / (2^{32} – 1) = 0.047 Hz.

7.3.4.3 Modulator Order (MASH_ORDER)

The fractional modulator order is programmable and has an impact on spurs. Theoretically, the higher order the fractional modulator order, the more it pushes the lower frequency spur energy to higher frequency. However, higher order modulators add more noise and increase the minimum N divide ratio. Modulator orders higher than one can create sub-fractional spurs, depending on the value of FDEN, which is the value of the denominator of the fraction PLL_NUM / PLL_DEN, after it is reduced to the lowest terms.

Table 7-4. Rough Guidelines for Choosing MASH_ORDER

MASH_ORDER	WHEN TO USE
Integer Mode	Integer mode (MASH_ORDER = 0) is good when the fractional circuitry is not needed. It has the advantage that it allows the lowest N divider value. Be aware that the output phase cannot be shifted with MASH_SEED in integer mode.
1st Order Modulator	The first order modulator is good for situations where the fractional denominator is small. Theoretically, if FDEN < 7, then all the fractional spurs will be lowest with the first order modulator. If the fraction is divisible by 2, then there will be sub-fractional spurs which one has to trade-off with the primary spur level. If the primary fractional spur at offset of f_{PD} / FDEN is far outside the loop bandwidth, this is often a good choice.
2nd Order Modulator	The second order modulator gives good spurs. If FDEN is odd, then there are no sub-fractional spurs, so situations where FDEN > 8 and FDEN is odd, this might make sense. If FDEN is very large, like 1000000, then the fraction is likely well-randomized and one might consider a third-order modulator, if it does not overly restrict the N divider value.
3rd Order Modulator	The third-order modulator is a good general purpose starting point if FDEN > 9 and FDEN is not divisible by 3.

7.3.5 LD Pin Lock Detect

Lock detect gives a rough indication of whether or not the PLL is in lock. There are two general types of lock detect supported: calibration status and indirect vtune. The calibration status lock detect starts low when the VCO begins cailbration. If LD_VTUNE_EN=1, then an additional 4xLD_DLY phase detector cycles is added to this delay. The indirect vtune lock detect works by creating an indirect internal voltage that is intended to mimic

the actual voltage at the VTUNE pin. When this voltage goes out of range, the Vtune lock detect is low. The calibration status and Vtune lock detect can be combined as well. In situations where the VCO calibration is bypassed, such as full assist mode or instant calibration, then this lock detect serves just the Vtune function.

7.3.6 MUXOUT Pin and Readback

Readback is useful for getting information regarding the device status. Fields that can be read back are:

1. Raw register values to confirm programming.
2. VCO lock detect status (rb_LD).
3. VCO calibration information (rb_VCO_SEL; rb_VCO_CAPCTRL; rb_VCO_DACISET).
4. Die temperature (rb_TEMP_SENS). To use this feature, set TEMPSENSE = 1. Equation 3 calculates the readback temperature:

$$\text{Temperature [°C]} = 0.85 \times \text{rb_TEMP_SENSE} - 415 \quad (3)$$

Measurement accuracy is ± 5 °C.

7.3.7 Internal VCO

The LMX2820 includes a fully integrated VCO. The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies as $f_{VCO} = f_{PD} \times (PLL_N + PLL_NUM / PLL_DEN)$.

7.3.7.1 VCO Calibration

To reduce the VCO tuning gain and therefore improve the VCO phase-noise performance, the VCO frequency range is divided into several different frequency bands. The entire range, 5.65 to 11.3 GHz covers an octave that allows the divider to take care of frequencies below the lower bound. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. It is important that a valid OSCIN signal must present before VCO calibration begins. The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed. The optimum internal settings for this are temperature dependent. The maximum allowable drift for continuous lock, ΔTCL, is stated in the electrical specifications. For this device, a number of 125 °C means the device never loses lock if the device is operated under the *Recommended Operating Conditions*.

7.3.7.1.1 Determining the VCO Gain and Ranges

VCO gain can vary based on core, and this can vary over temperature and process, but Table 7-5 gives a rough guideline of what VCO gain to expect.

Table 7-5. Approximate VCO Gain and Ranges

VCO CORE	Fmin (MHz)	Fmax (MHz)	KvcoMax	KvcoMin
VCO1	5650	6350	84	115
VCO2	6350	7300	94	131
VCO3	7300	8100	123	156
VCO4	8100	9000	132	169
VCO5	9000	9800	131	163
VCO6	9800	10600	152	185
VCO7	10600	11300	130	151

7.3.8 Channel Divider

The channel divider is actually a single divider with multiple segments and tap points that is shared between RFOUTA and RFOUTB. In general, this can operate as independent divider values with the one exception that if a divide value of 128 is chosen for one output, then this divide must be chosen for the other output (although the channel divider can still be bypassed). Note that when the output frequencies are not the same, the higher frequency output will have sub-harmonic spurs at frequency offset equal to other output.

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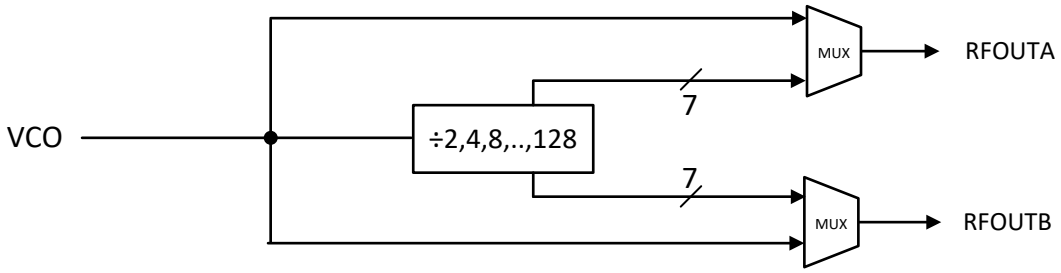

Figure 7-1. Channel Divider

7.3.9 Output Frequency Doubler

The frequency doubler is used to produce an output frequency that is twice the VCO frequency and is selected when OUTx_MUX = 2. When the VCO frequency is doubled, the fundamental (non-doubled) VCO frequency does leak to the output and this is the sub-harmonic (0.5X). To minimize these sub-harmonics, there is tunable filter that tracks the output frequency and filters out this sub-harmonic as well as other undesired harmonics (1.5X, 2X, 3X, ...). The calibration for this tunable filter is automatically triggered whenever the VCO calibration is done.

7.3.10 Output Buffer

The output buffer is an open-collector architecture, but the 50-Ω pullup resistor is integrated within the device. At lower frequencies, it is fair to assume the output impedance is 50 Ω, but at higher frequencies, parasitic can cause the output impedance to be different. The OUTx_PWR programming fields set the emitter current and adjust the power level.

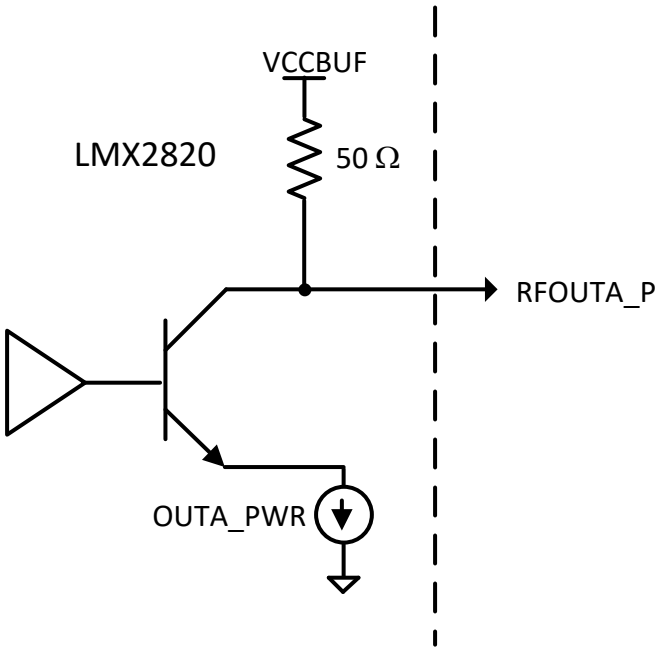

Figure 7-2. Output Buffer Structure

7.3.11 Power-Down Modes

The LMX2820 can be powered up and down using the CE pin or the POWERDOWN bit. In power-down mode, the majority of the device is shut down. However, in power-down mode, the device retains its programming information and can still be programmed, provided that the supply pins still have power applied to them. As this also powers down the internal LDOs, be aware that programming register R0 with POWERDOWN will re-calibrate the VCO if FCAL_EN = 1. In this case, one should re-program register R0 with FCAL_EN = 1 to ensure

that this happens with the LDOs at their proper bias level. If the instant calibration is used, then this extra programming of register R0 is unnecessary.

7.3.12 Phase Synchronization for Multiple Devices

In many situations, a synchronization pulse is needed to ensure that the device has deterministic phase. The requirements for phase synchronization depend on certain setup conditions. In cases that the timing of the synchronization pulse is not critical, it can be done through software by toggling the INPIN_IGNORE bit. When it is timing critical, then it must be done through the pin and the setup and hold times for the OSCIN pin are critical. The following section gives categories for phase sync based on the input and output frequencies.

7.3.12.1 SYNC Categories

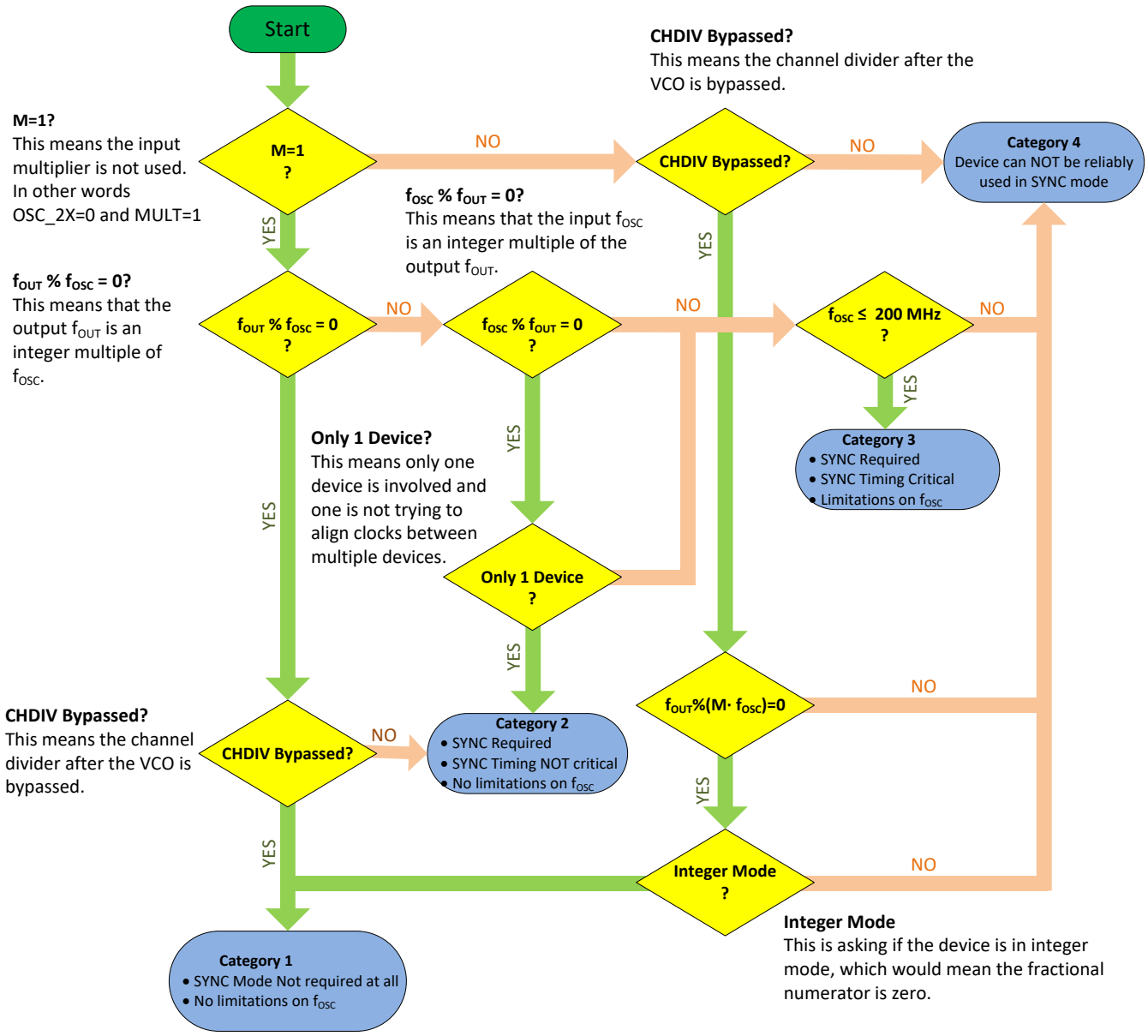

Figure 7-3. Synchronization Flowchart

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7.3.12.2 Phase Adjust

7.3.12.2.1 Using MASH_SEED to Create a Phase Shift

The MASH_SEED word can use the sigma-delta modulator to shift output signal phase with respect to the input reference. If a SYNC pulse is sent (software or pin) or the MASH is reset with MASH_RST_N, then this phase shift is from the initial phase of zero. The phase shift can be calculated based on the MASH_SEED.

$$\text{Phase shift in degrees} = 360 \times (\text{MASH_SEED} / \text{PLL_DEN} / \text{CHDIV}) \quad (4)$$

There are a few considerations with MASH_SEED:

- Phase shift can be done with a PLL_NUM = 0, but MASH_ORDER must be greater than zero.
- For MASH_ORDER = 1, the phase shifting only occurs when MASH_SEED is a multiple of PLL_DEN.
- Setting MASH_SEED > 0 can impact fractional spurs. If used with a PLL_NUM = 0, it can create fractional spurs. If used with a non-zero numerator, it can either help or hurt spurs and this effect can be simulated with the TI PLLatinum Sim tool.

7.3.12.2.2 Static vs. Dynamic Phase Adjust

The programming of the MASH_SEED word is cumulative. By that it means that the programmed value is added to the current value. Whenever the MASH_RST_N bit or the VCO is re-calibrated, the current value is set to MASH_SEED. Static phase adjust would involve setting the MASH_SEED word to the desired value and toggling the MASH_RST_N bit to force this value. Dynamic phase adjust involves setting MASH_SEED to a smaller value and repetitively program the MASH_SEED word to add to the cumulative value for MASH_SEED.

7.3.12.2.3 Fine Adjustments to Phase Adjust

Phase SYNC refers to the process of getting the same phase relationship for every power-up cycle and each time assuming that a given programming procedure is followed. However, in cases of higher output frequencies which have shorter periods, there are some adjustments that may be necessary to achieve the most accurate results.. As for the consistency of the phase SYNC, the only source of variation could be if the VCO calibration chooses a different VCO core and capacitor, which can introduce a bimodal distribution with about 10 ps of variation. If this 10 ps is not desirable, then it can be eliminated by either using the instant calibration based VCO calibration or Full assist VCO calibration.

The delay through the device varies from part to part and can be on the order of 60 ps. This part to part variation can be calibrated out with the MASH_SEED. The variation in delay through the device also changes on the order of +2.5 ps/°C, but devices on the same board likely have similar temperatures, so this will somewhat track. In summary, the device can be made to have consistent delay through the part and there are means to adjust out any remaining errors with the MASH_SEED. This tends only to be an issue at higher output frequencies when the period is shorter.

7.3.13 SYSREF

The LMX2820 can generate a SYSREF output signal that is synchronized to f_{OUT} with a programmable delay. This output can be a single pulse, series of pulses, or a continuous stream of pulses. To use the SYSREF capability, the PLL must first be placed in SYNC mode with PHASE_SYNC_EN = 1.

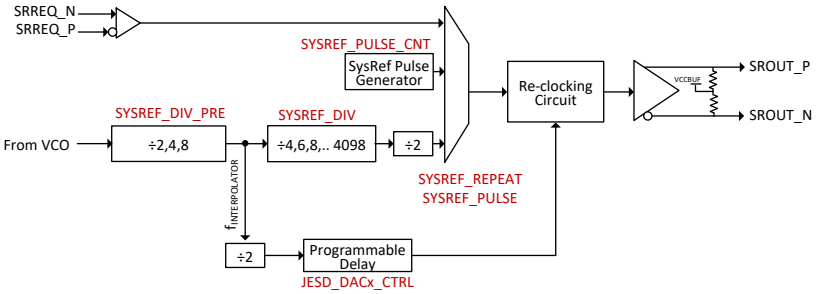

Figure 7-4. SYSREF Functional Diagram

The SYSREF feature uses SYSREF_DIV_PRE divider to generate $f_{INTERPOLATOR}$. This frequency is used for reclocking of the rising and falling edges at the SRREQ pin. In master mode, the $f_{INTERPOLATOR}$ is further divided by 2 × SYSREF_DIV to generate finite series or continuous stream of pulses.

The delay can be programmed using the JESD_DAC1_CTRL, JESD_DAC2_CTRL, JESD_DAC3_CTRL, and JESD_DAC4_CTRL words. By concatenating these words into a larger word called "SysRefPhaseShift", the relative delay can be found. The sum of these words should always be 63. The size of the delay step is:

SysRefDelayStepSize = SYSREF_DIV_PRE/(126*f_{VCO})

Table 7-6. SysRefPhaseShift vs. JESD_DACx_CTRL

SysRefPhaseShift	JESD_DAC1_CTRL	JESD_DAC2_CTRL	JESD_DAC3_CTRL	JESD_DAC4_CTRL
0	63	0	0	0
1	62	1	0	0
…	…	…	0	0
62	1	62	0	0
63	0	63	0	0
64	0	62	1	0
…	0	…	…	0
125	0	1	62	0
126	0	0	63	0
127	0	0	62	1
…	0	0	…	…
188	0	0	1	62
189	0	0	0	63
190	1	0	0	62
…	…	0	0	…
251	62	0	0	1

One cannot always assume that the lowest value of SysRefPhaseShift gives the lowest delay. In other words, there could be a wrap around effect where there is an abrupt transition from the longest delay to the shortest delay. The code where this abrupt transition happens is mainly dependent on f_{VCO} and SYSREF_DIV_PRE.

7.3.14 Fast VCO Calibration

The time that it takes the VCO to calibrate can be reduced. Table 7-7 shows the general methods of VCO Calibration.

Table 7-7. Types of VCO Calibration

CALIBRATION TYPE	DESCRIPTION
No Assist	User does nothing to improve VCO calibration speed, but the user-specified VCO_SEL, VCO_DACISET and VCO_CAPCTRL values do affect the starting point of VCO calibration.
Partial Assist	Upon every frequency change, before the FCAL_EN bit is checked, the user provides the initial starting point for the VCO core (VCO_SEL), band (VCO_CAPCTRL), and amplitude (VCO_DACISET) based on values specified in the datasheet.
Full Assist	The user forces the VCO core (VCO_SEL), amplitude settings (VCO_DACISET), and frequency band (VCO_CAPCTRL) and manually sets the value. If the two frequency points are no more than 5 MHz apart and on the same VCO core, the user can set the VCO amplitude and capcode for any frequency between those two points using linear interpolation.
Instant Calibration	The user initializes the device to generate a instant calibration. For as long as power is applied to the device, the instant calibration can be used to make ultra-fast VCO Calibration

7.3.15 Double Buffering (Shadow Registers)

Double buffering—also known as "shadow registers"—allows the user to program multiple registers without having them actually take effect. Then when the R0 register is programmed, then these registers take effect.

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This is especially useful if one wants to change frequencies quickly and multiple register writes are required. When DBLBUF_EN = 1, the double buffering is enabled for the following registers: PLL_N, PLL_NUM, PLL_DEN, MULT, PLL_R, PLL_R_PRE, MASH_ORDER, and PFD_DLY.

7.3.16 Output Mute Pin and Ping Pong Approaches

The output buffer can be muted or unmuted using the MUTE pin. The polarity of this pin is programmable with the PINMUTE_POL bit. When the output is muted, the PLL stays in lock, so this can be used to combine multiple synthesizers for faster lock time. The PLL with the muted output can be accepting programming commands or even locking to a new frequency. As the output is muted, the unwanted signal is greatly attenuated and can be further attenuated with an RF switch.

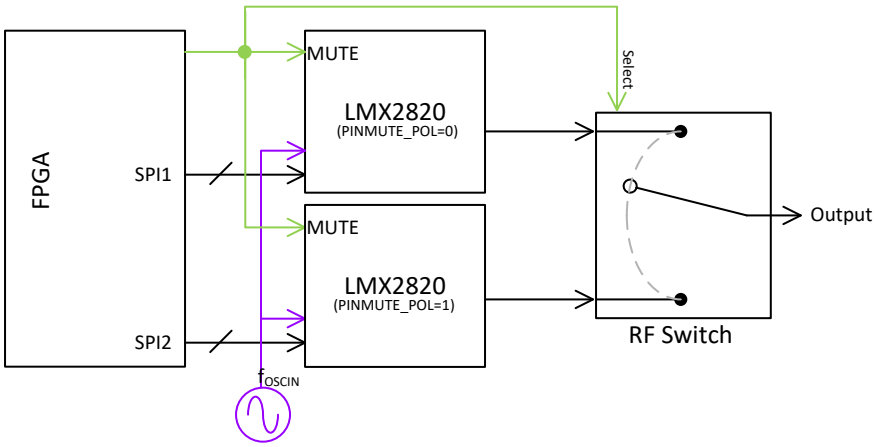

Figure 7-5. Output Mute Pins

7.4 Device Functional Modes

There are six basic modes of the LMX2820 that allow the choices of the use of internal vs. external VCO and three different ways that the output of the VCO can be sent to the phase detector.

Table 7-8. Summary of Device Functional Modes

VCO MODE	FEEDBACK MODE	COMMENT
Internal	Internal Feedback	The internal VCO is used and the VCO is internally fed back to the phase detector.
	PFDIN External Feedback	The internal VCO is used, but the output is downconverted with an external mixer and fed to the PFDIN pin.
	RFIN External Feedback	The internal VCO is used and the output is downconverted with an external mixer and fed to the RFIN pin.
External	Internal Feedback	For some applications, especially if it is narrowband, an external VCO may be able to provide better phase noise performance than the internal VCO. There could be an advantage in phase noise and harmonics if the output divider or doubler can be avoided by using external VCO.
	PFDIN External Feedback	Theoretically, an external VCO can be used with the external phase detector for the ultimate in phase noise. This does require a high-performance source, mixer, and VCO to fully take advantage of this mode.
	RFIN External Feedback	An external VCO is used and the output is downconverted with an external mixer and fed to the RFIN pin.

7.4.1 External VCO Mode

An external VCO can also be used with the LMX2820, but note that the output buffers cannot be used while the SYSREF feature can. The charge pump voltage maximum output voltage is about 2.5 V, but this is not sufficient for most VCOs. For this reason, an active filter is recommended, which can keep the charge pump voltage

biased around 1.2 V and provide the higher output voltage. If the VCO frequency is higher than 11.3 GHz, the EXTVCODIV bit must be enabled, otherwise, it should be zero.

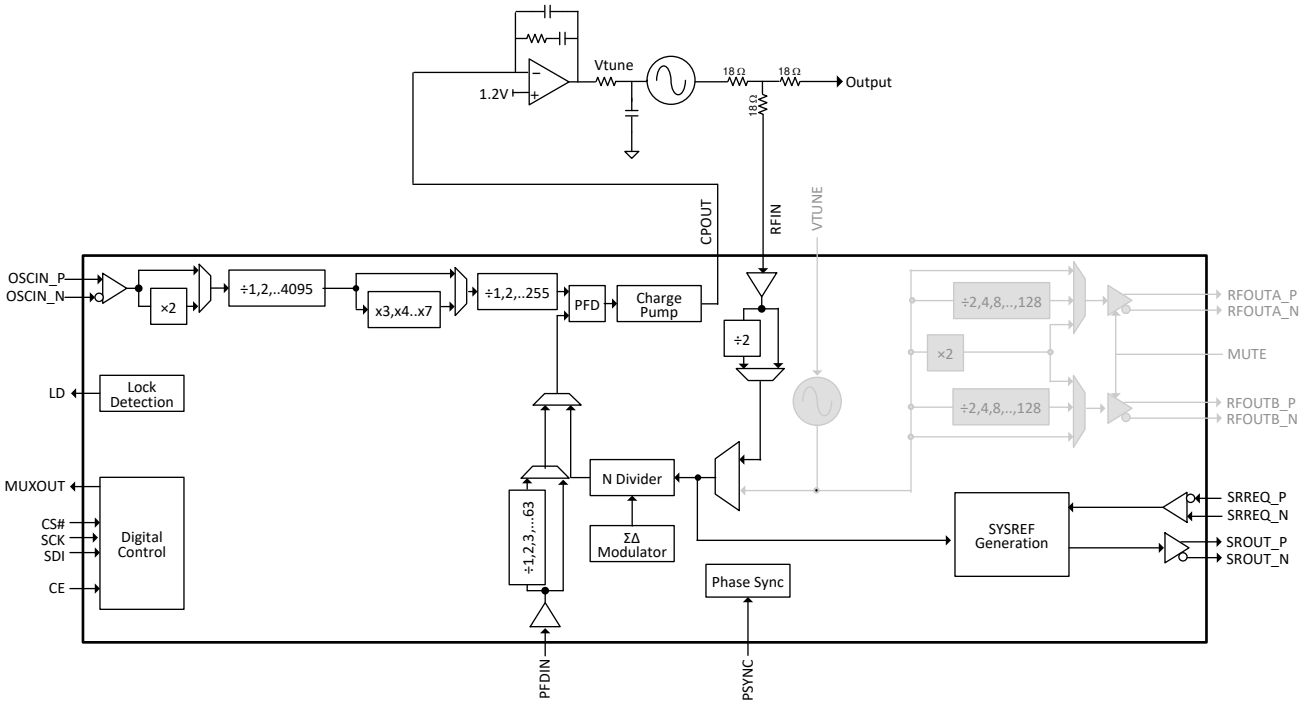

Figure 7-6. External VCO Mode

When using the external VCO, the PFD_DLY word must be set manually as shown in Table 7-9. For the case of an integrated VCO, it is not necessary to program this word. PFD_DLY_MANUAL = 1 is required to manually set the PFD_DLY.

Table 7-9. PFD_DLY_SEL Settings for External VCO Mode

f_{RFIN}/(RFIN Divider)	MASH_ORDER = 0	MASH_ORDER = 1	MASH_ORDER = 2	MASH_ORDER = 3
0.5 - 4 GHz	1	1	2	4
4 - 5.5 GHz	2	2	3	5
5.5 - 7 GHz	3	3	4	6
7 - 8.5 GHz	4	4	5	7
8.5 - 10 GHz	5	5	6	8
> 10 GHz	6	6	7	9

7.4.2 External Feedback Input Pins

The LMX2820 gives the user the option to downconvert the VCO frequency using an external mixer and clean source for improved PLL noise. This frequency can be input through the RFIN or PFDIN pins.

7.4.2.1 PFDIN External Feedback Mode

The PFDIN pin allows the VCO frequency to be downconverted externally with a mixer in order to get a much lower N divider value. The EXTPFD_DIV allows divide values down to one in order to get the lowest possible phase noise. When using the PFDIN pin, single PFD mode needs to be enabled by setting PFD_SINGLE = 3. This setting degrades the PLL figure of merit about 3 dB, but allows the feedback divider to go all the way down to one. If it is not possible to take advantage of the lowest N divider, consider using the approach using the RFIN pin, which has a higher minimum N divider value, but the PLL figure of merit is not degraded.

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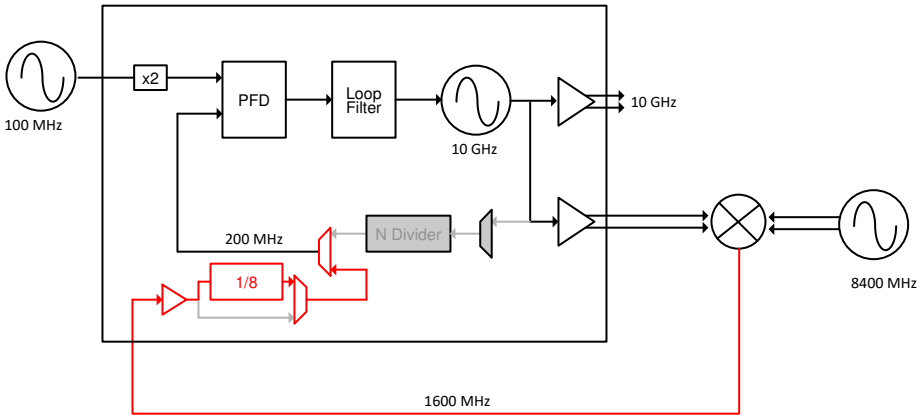

Figure 7-7. External Feedback Using PFDIN pin and Internal VCO

7.4.2.2 RFIN External Feedback Mode

The RFIN pin can also be used to allow a lower N divider value. This makes sense when the feedback divide value is higher or if the fractional circuitry is required. This does not require the use of the single PFD mode as is the case when the PFDIN pin is used for external fedback.

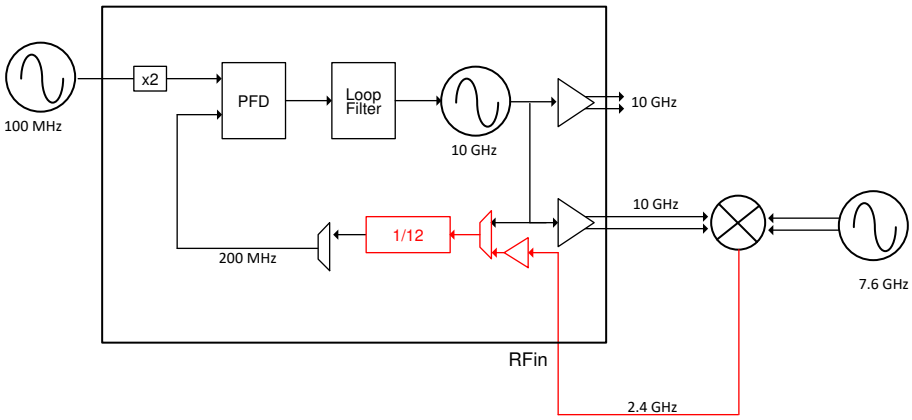

Figure 7-8. External Feedback Using the RFIN pin and Internal VCO

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Treatment of Unused Pins

In some applications, not all pins are needed. Table 8-1 discusses how to treat these unused pins.

Table 8-1. Treatment of Unused Pins

SITUATION	PINS APPLYING TO	COMMENT
Single-Ended Input	OSCIN_N	AC-couple this pin to GND through a 50-Ω resistor. For optimal spurs, the impedance seen looking out of OSCIN_P and OSCIN_N should be similar
Single-Ended Output	RFOUTA_N, RFOUTB_N	Terminate this pin to a load that looks similar to the output that is used. This is typically a 50-Ω resistor AC-coupled to ground. This is to minimize harmonics.
Unused Input	RFIN, PFDIN, SRREQ pins	This pin may be left floating. This feature can be powered down in software.
Unused Output	RFOUT Pins, SROUT pins	This pin may be left floating. This feature can be powered down in software.
Unused Digital Pin	Input pins	Ground this pin.

8.1.2 External Loop Filter

The LMX2820 requires an external loop filter that is application-specific and can be configured by PLLatinum Sim. For the LMX2820, it matters what impedance is seen from the VTUNE pin looking outwards. This impedance is dominated by the component C3 for a third order filter or C1 for a second order filter. If there is at least 1.5 nF for the capacitance that is shunt with this pin, the VCO phase noise will be as close to the best it can be. If the capacitance is less, the VCO phase noise in the 100-kHz to 1-MHz region will degrade. This capacitor should be placed close to the VTUNE pin.

8.1.3 Using Instant Calibration

Instant calibration allows the device to very quickly calibrate the VCO in 2.5 µs and choose the same calibration settings (rb_VCO_SEL, rb_VCO_DACISET, rb_VCO_CAPCTRL). Once this feature is initialized, then there is no overhead in changing the VCO frequency. This initialization is required when the device is initially powered up, but the settings are retained, provided power is not removed from the supply pins. The following procedure details how this is done:

1. Power up device Normally.
2. Program INSTCAL_DLY = $t_{DLY} \times f_{OSC}$ (in MHz)/ $2^{CAL_CLK_DIV}$. t_{DLY} is the required timeout count for instant calibration and is based on the bias capacitor at pin 3.

Table 8-2. Determining Instant Calibration Timeout

PIN 3 CAPACITANCE	PLL 1/f NOISE DEGRADATION	MINIMUM t_{DLY}
0.47 µF	1 dB	2.5 µs
C	0-1 dB	2.5 µs × C/(0.47 µF)
4.7 µF	0 dB	25 µs

3. Program register R1 for Instant Calibration.

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- Set INSTCAL_EN = 1. The action of toggling INSTCAL_EN from 0 to 1 resets the instant calibration settings and sets the part up to generate settings the next time that register R0 is programmed with FCAL_EN = 1.
- If the output doubler is used set INSTCAL_DBLR_EN = 1, otherwise set it to 0

4. Program the device to output 5.65 GHz.
5. Program INSTCAL_PLL_NUM = 2^{32} × (PLL_NUM / PLL_DEN).
6. Write R0 with FCAL_EN = 1 to generate the calibration settings.
7. Write R0 with FCAL_EN = 0 to have the device lock to 5.65 GHz
8. Wait for Lock Detect to go high.

Now the device is initialized for the particular phase detector frequency that this was done at. Provided that power is not removed from the device and then phase detector frequency does not change, subsequent frequency changes an be done using the instant cal. To change frequencies after the instant calibration is initialized:

1. Write the values for INSTCAL_PLL_NUM, PLL_N, PLL_NUM, PLL_DEN.
2. Write R0 to trigger Calibration (with DBLR_CAL_EN = 0, FCAL_EN = 0).

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8.2 Typical Application

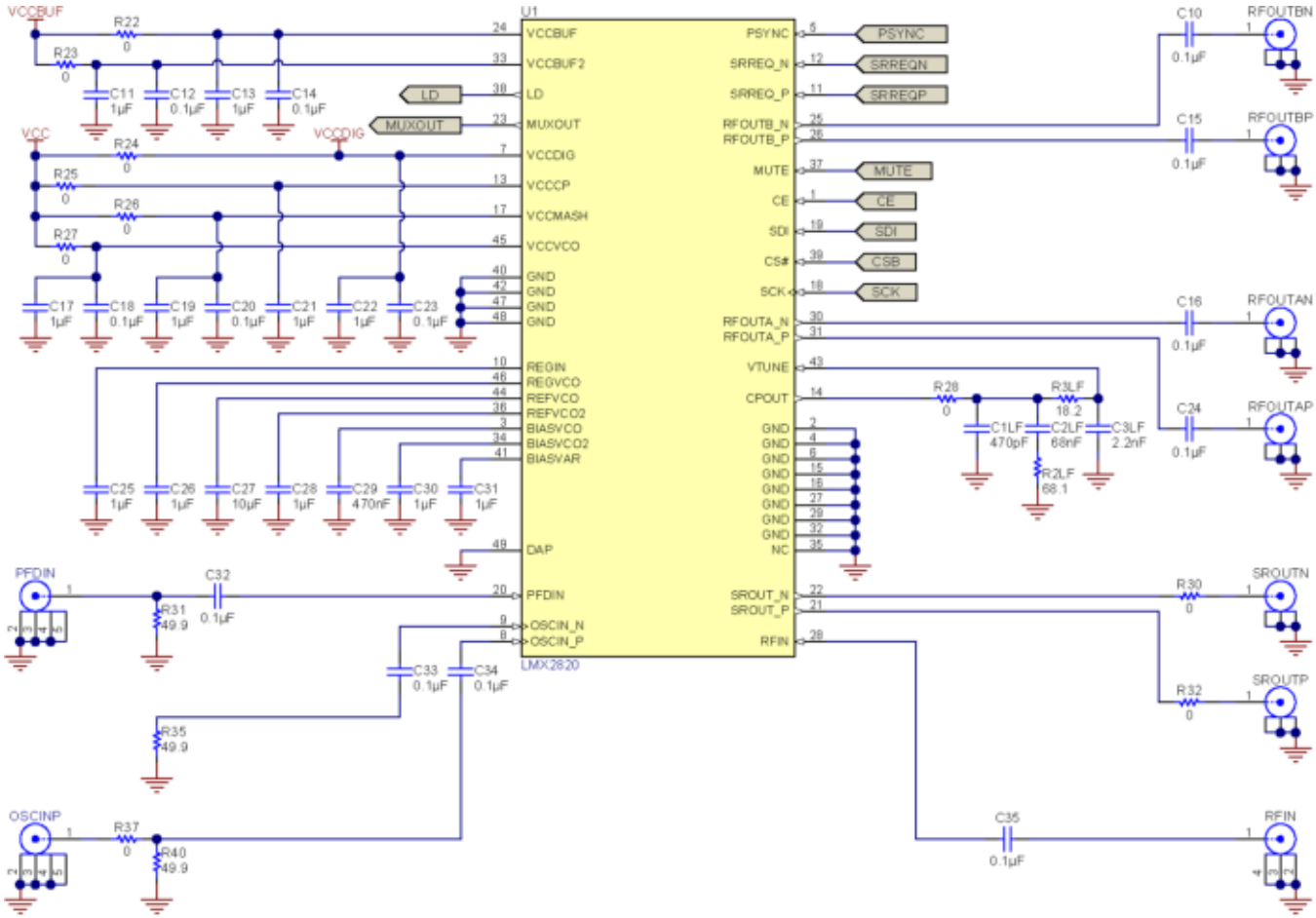

Figure 8-1. Typical Application Schematic

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8.2.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLATINUM Sim software is an excellent resource for doing this and the design and simulation. In this case, an integer design is assumed and this is being designed for optimal jitter, as would be the case for many clocking applications. For this example, it will be assumed that a 6-GHz output will be generated from a 100-MHz clock. From this, the engineer must choose a VCO frequency and phase detector before proceeding to the loop filter design.

The VCO frequency must be in the range of 5.65 to 11.3 GHz, the output frequency must either divide into this or double the VCO frequency selected (in the case that it is higher than 11.3 GHz). In this case, this implies the VCO frequency is 6 GHz. The next step is to choose the phase detector frequency. The phase detector frequency must either divide the input frequency, or it can be double this if the OSC_2X feature is used. Also, if the phase detector frequency divides the VCO frequency, the spur performance is much better. So by choosing a 200-MHz phase detector frequency and using the OSC_2X doubler, the device can be used in integer mode and the best phase noise performance can be achieved.

Table 8-3. Design Parameters

SYMBOL	DESCRIPTION	VALUE	UNITS
f_{OSC}	This is the input frequency that was given.	100	MHz
f_{OUT}	This is the output frequency that was given.	6000	MHz
f_{VCO}	This is the VCO frequency that was chosen to generate the output frequency.	6000	MHz
f_{PD}	This is the phase detector frequency that was chosen for the best noise performance.	200	MHz

8.2.2 Detailed Design Procedure

When the frequencies are known, the loop filter must be designed. The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO.

Generally, jitter is lowest if the loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The trade-off with this is that longer lock times and spurs must be considered in design as well.

The PLLatinum Sim software is very useful in designing the loop filter and is available on the TI website. Using this tool, the results in Table 8-4 were obtained.

Table 8-4. PLLatinum Sim Results

COMPONENT	VALUE	UNIT
C1	390	pF
C2	68	nF
C3	1.8	nF
R2	68	Ω
R3	18	Ω

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8.2.3 Application Curves

The actual phase noise result shows the outstanding result of 36 fs of jitter.

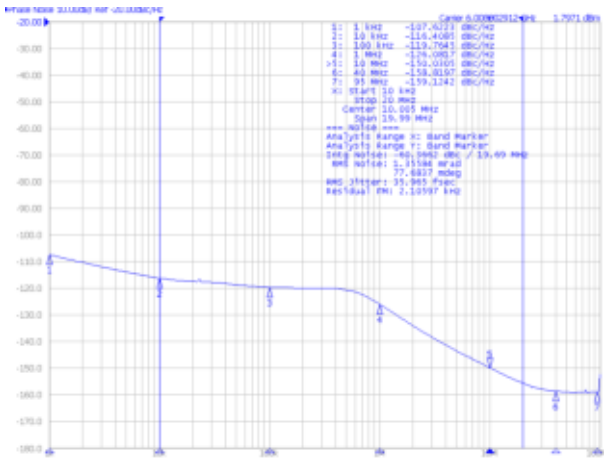

Figure 8-2. Measurement Plot

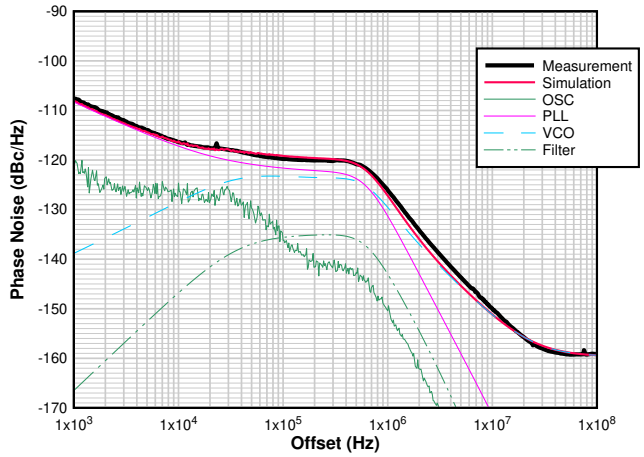

Figure 8-3. Measurement vs. Simulation

8.3 Initialization and Power-on Sequencing

To ensure the proper operation of the device, proper power on sequencing needs to be followed.

1. When power is initially applied, the Power-on Reset (POR) circuitry will reset the registers and state machines to a default state.
2. Before any programming is done, the voltages at VCC_CP, VCC_VCO, VCC_VCO2, VCC_MASH, and VCC_BUF are at lest above the minimum operating votlage of 3.15 V.
3. Although the POR circuitry does initialize the device, it is good practice to toggle the RESET bit from 1 to 0 to manually do a software reset. This is necessary to ensure that the internal state machines, bias levels, and overall device current reset to a stable starting condition. This reset takes less 1 µs.
4. Program the registers in descending order; R0 should be the last register programmed. This loads the device to the desired state.
5. Wait 10 ms to allow the internal LDOs to power up.
6. Program the R0 register one more time to activate the VCO calibration with the LDOs in a stable state. Even if this was done before, the calibration is not valid if it was done before the LDOs in the chip are at the proper levels. Also, it is important to have a stable and accurate input reference as the VCO calibration is based off of this. An input reference may be applied earlier to the device without damaging it. This applies to both the calibration methods with and without instant calibration.
7. After the VCO has calibrated, the frequency will be closer, but not exact. The frequency must settle out with the analog lock time, which adds to the VCO digital calibration.
8. After the analog PLL lock is done, the output is valid. There may be a signal that comes out of the output before this, but the frequency may not be valid.

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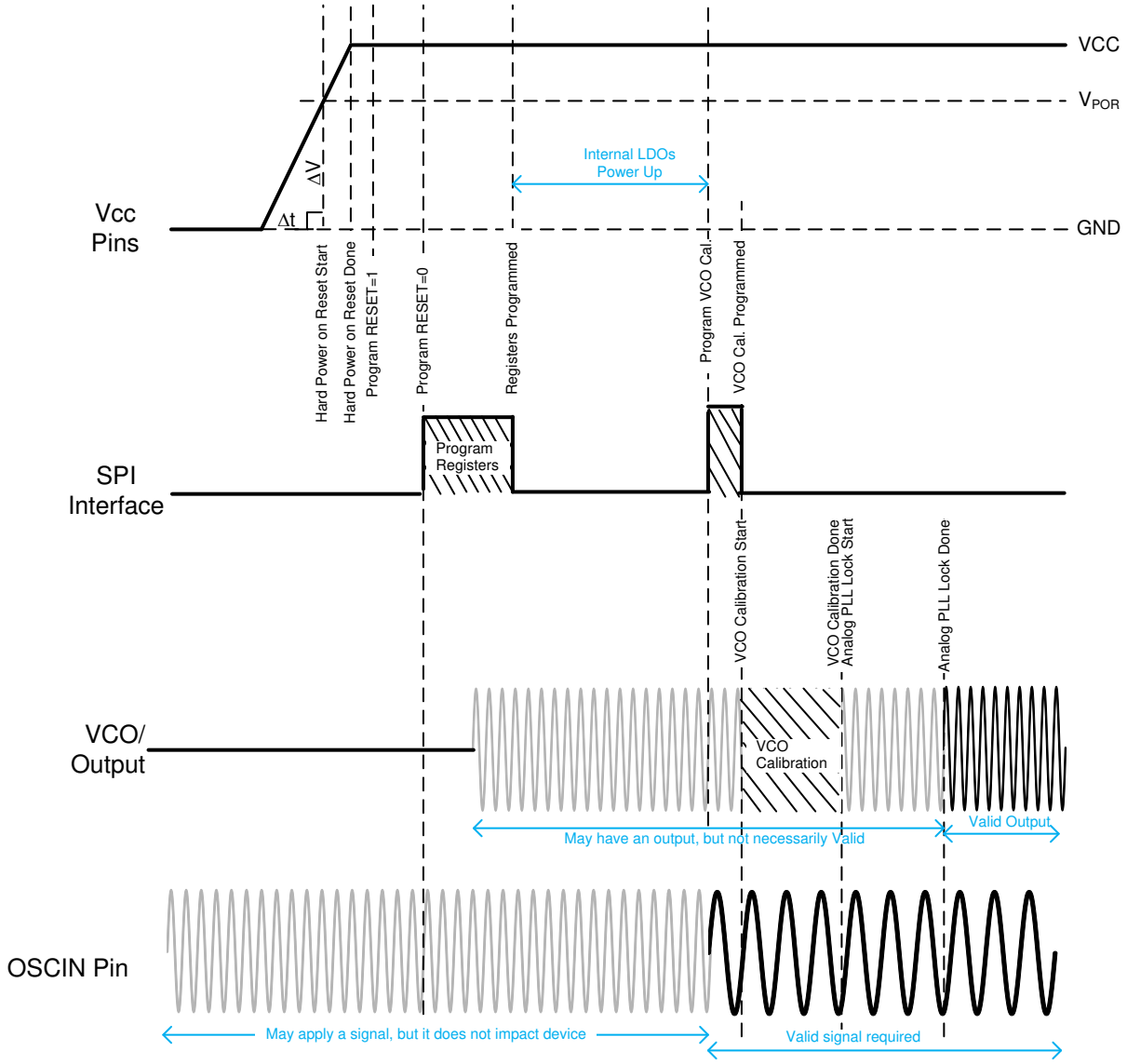
Figure 8-4. Power-on Sequencing



9 Power Supply Recommendations

If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise. This device can be powered by an external DC-DC buck converter, such as the TPS62150. For the purposes of power supply filtering, it is useful to have a general idea of how much current goes through different pins. This may change significantly with configuration, but the following table gives a good idea.

Table 9-1. Current Consumption per Pin in mA

Conditoin	Total	VCCDIG	VCCCP	VCCMASH	VCCBUF	VCCVCO
One direct RF Output	420	23	5	5	124	263
One divided RF Output	580	21	13	96	212	238
One RF output with VCO doubler enabled	590	20	12	89	238	231
RFIN External Feedback Mode, Internal VCO	530	18	12	90	170	240
PFDIN External Feedback Mode, Internal VCO	455	18	10	79	110	238
External VCO Mode	290	19	9	92	54	116
Power-on reset current	234	10	6	48	24	146
Power-down current	10	2	0	1	6	1

10 Layout

10.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines.

- GND pins may be routed on the package back to the DAP.
- The OSCIN pins, these are internally biased and must be AC coupled.
- If not used, the SRREQ pins may be grounded to the DAP.
- For optimal VCO phase noise in the 200 kHz to 1 MHz range, it is ideal that the capacitor closest to the VTUNE pin be at least 1.5 nF. As requiring this larger capacitor may restrict the loop bandwidth, this value can be reduced (to say 1 nF) at the expense of VCO phase noise.
- If a single-ended output is needed, the other side must have the same loading. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, make the load look equivalent to the side that is used.
- Ensure DAP on device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the LMX2820 exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.

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10.2 Layout Example

For this layout, all of the loop filter (C1LF, C2LF, C3LF, R2LF and R3LF) are on the top side of the board. C3LF is located right next to the VTUNE pin. In the event that this C3LF capacitor would be open, TI recommends to move one of loop capacitors in this spot. For instance, if a second order loop filter was used, technically C3LF would be open. However, for this layout example that is designed for a third order loop filter, it would be optimal to make C1LF = open, and C3LF to be whatever C1LF would have been.

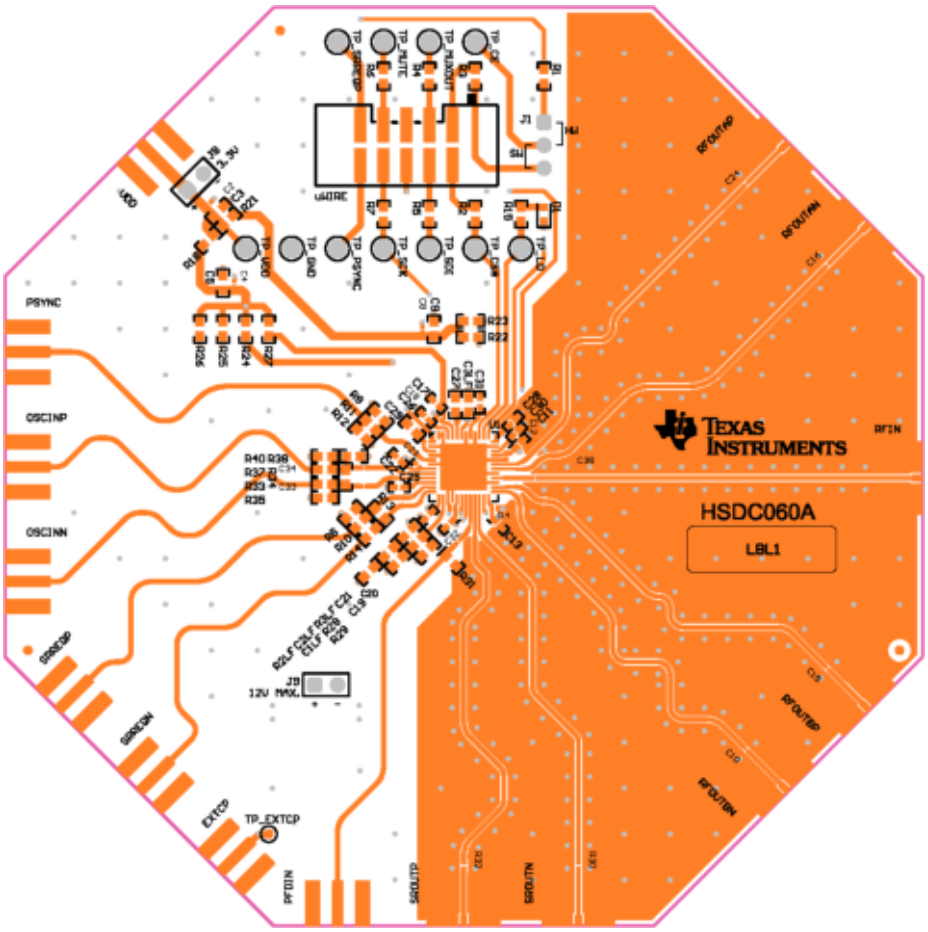

Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

PLLatinum™ are trademarks of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMX2820RTCR	Active	Production	VQFN (RTC) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2820
LMX2820RTCR.B	Active	Production	VQFN (RTC) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2820
LMX2820RTCT	Active	Production	VQFN (RTC) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2820
LMX2820RTCT.B	Active	Production	VQFN (RTC) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2820

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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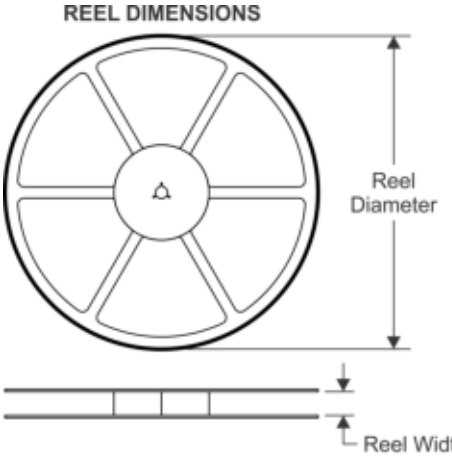
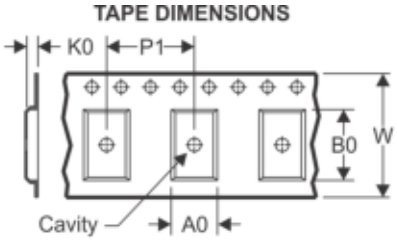
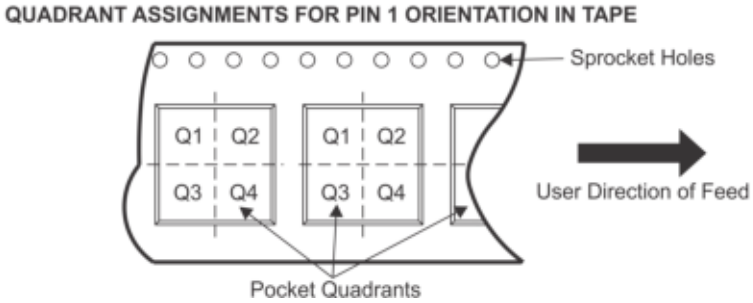
TAPE AND REEL INFORMATION





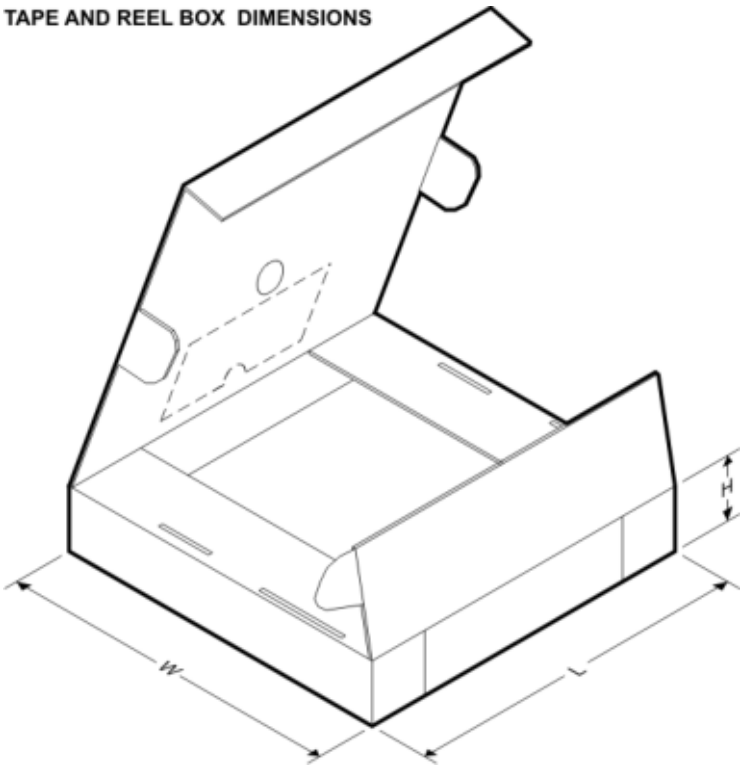
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2820RTCR	VQFN	RTC	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
LMX2820RTCT	VQFN	RTC	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2820RTCR	VQFN	RTC	48	2500	367.0	367.0	38.0
LMX2820RTCT	VQFN	RTC	48	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RTC 48

VQFNP - 0.9 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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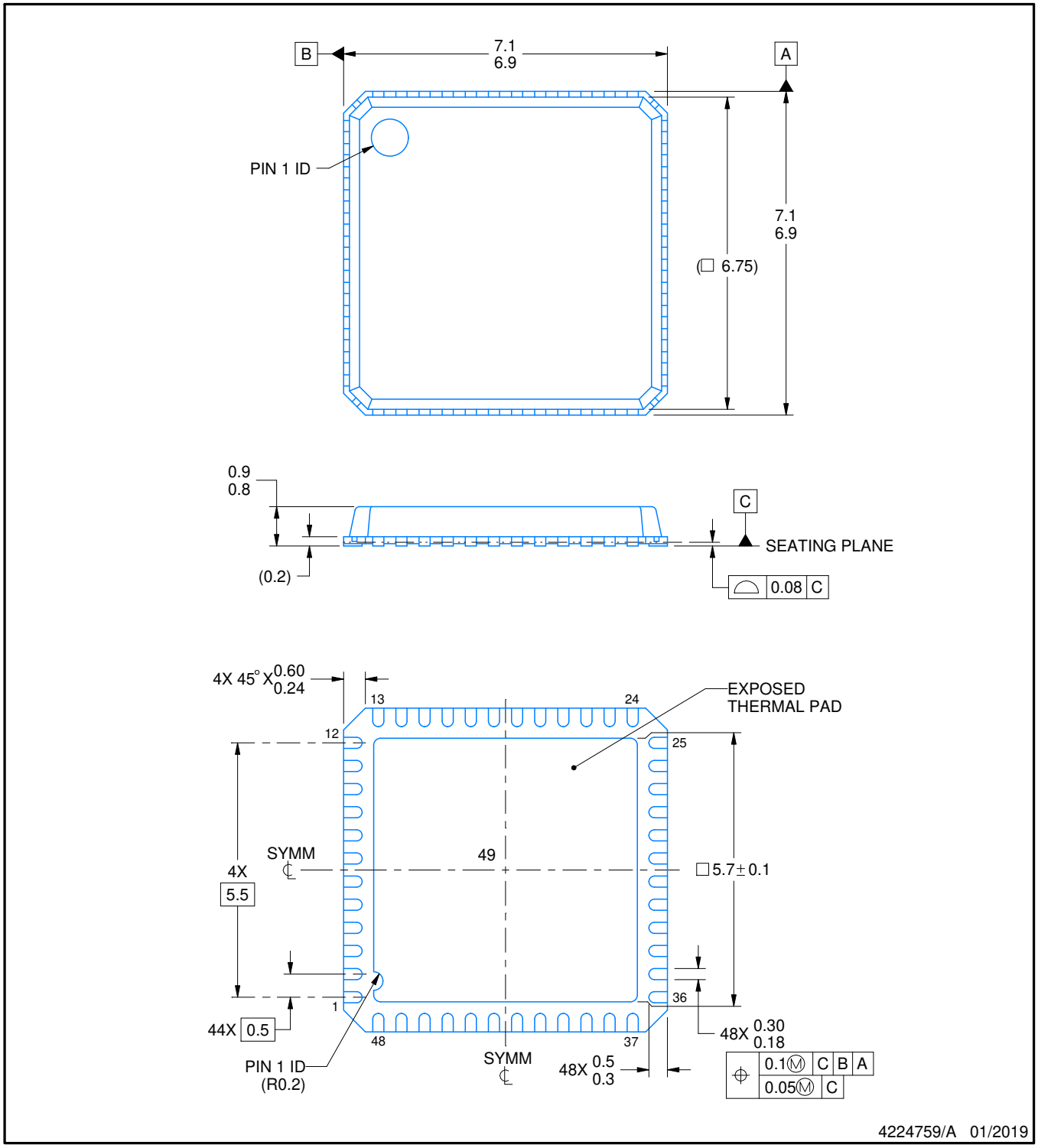
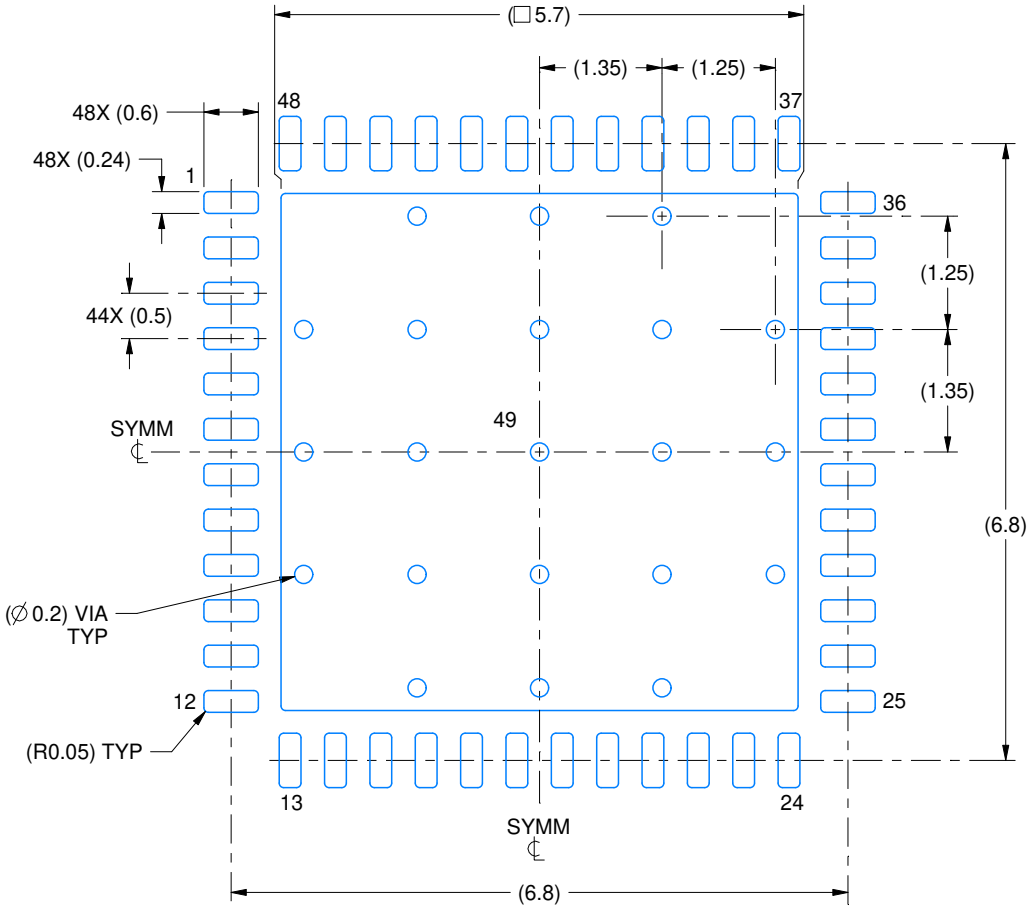
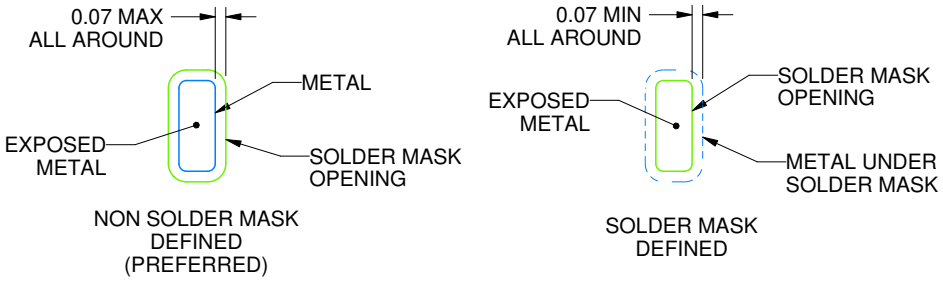


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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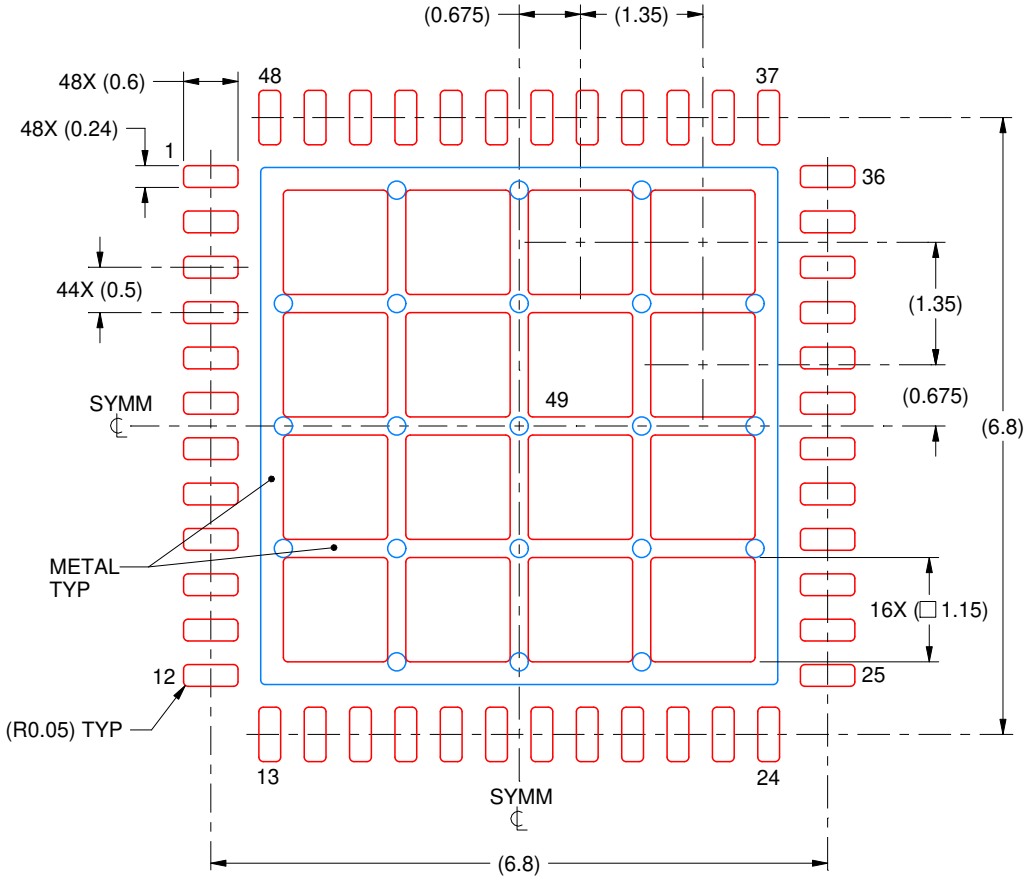
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49:
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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