LMZ14202H SIMPLE SWITCHER® 6V to 42V, 2A High Output Voltage Power Module

1 Features

- Integrated Shielded Inductor
- Simple PCB Layout
- Flexible Start-Up Sequencing Using External Soft-Start and Precision Enable
- Protection Against Inrush Currents
- Input UVLO and Output Short Circuit Protection
- –40°C to 125°C Junction Temperature Range
- Single Exposed Pad and Standard Pinout for Easy Mounting and Manufacturing
- Low Output Voltage Ripple
- Pin-to-Oin Compatible Family:
  - LMZ14203H/2H/1H (42 V Maximum 3-A, 2-A, 1-A)
  - LMZ14203/2/1 (42 V Maximum 3-A, 2-A, 1-A)
  - LMZ12003/2/1 (20 V Maximum 3-A, 2-A, 1-A)
- Fully Enabled for WEBENCH® Power Designer
- Electrical Specifications
  - Up to 2-A Output Current
  - Input Voltage Range 6 V to 42 V
  - Output Voltage as Low as 5 V
  - Efficiency up to 97%
- Performance Benefits
  - High Efficiency Reduces System Heat Generation
  - No Compensation Required
  - Low Package Thermal Resistance
  - Low Radiated EMI (EN 55022 Class B Tested)

NOTE: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007.

2 Applications

- Intermediate Bus Conversions to 12-V and 24-V Rail
- Time-Critical Projects
- Space Constrained / High Thermal Requirement Applications
- Negative Output Voltage Applications

3 Description

The LMZ14202H SIMPLE SWITCHER® power module is an easy-to-use step-down DC-DC solution capable of driving up to 2-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy. The LMZ14202H is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ14202H can accept an input voltage rail between 6 V and 42 V and deliver an adjustable and highly accurate output voltage as low as 5 V. The LMZ14202H only requires three external resistors and four external capacitors to complete the power solution. The LMZ14202H is a reliable and robust design with the following protection features: thermal shutdown, input undervoltage lockout, output overvoltage protection, short-circuit protection, output current limit, and allows start-up into a prebiased output. A single resistor adjusts the switching frequency up to 1 MHz.

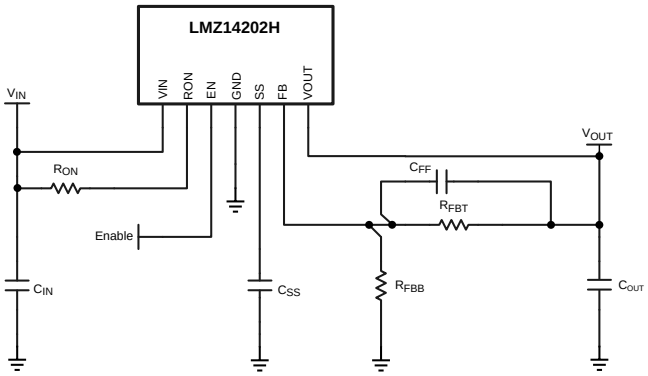
Device Information(1)(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMZ14202H	TO-PMOD (7)	10.16 mm × 9.85 mm

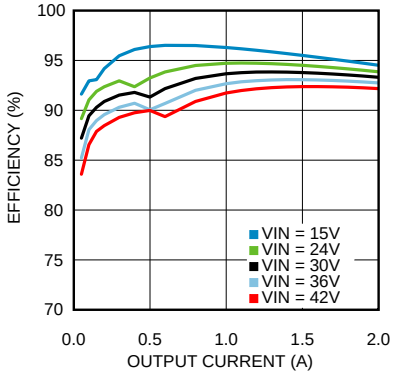
(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Peak reflow temperature equals 245°C. See SNAA214 for more details.

Simplified Application Schematic



Efficiency V_{OUT} = 12 V T_A = 25°C



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2015) to Revision H — **Page**

- Added the new bullet to the Power Module SMT Guidelines ... 22

Changes from Revision F (June 2015) to Revision G — **Page**

- Changed the title of the document ... 1

Changes from Revision E (October 2013) to Revision F — **Page**

- Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed Easy-to-Use PFM 7 Pin Package image ... 1

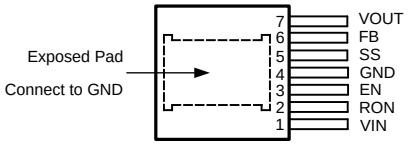
Changes from Revision D (February 2013) to Revision E — **Page**

- Changed 10 mils ... 21
- Added *Power Module SMT Guidelines* ... 21

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5 Pin Configuration and Functions

NDW Package
7-Lead PFM
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN	Power	Supply input — Additional external input capacitance is required between this pin and the exposed pad (EP).
2	RON	Analog	ON-time resistor — An external resistor from V_{IN} to this pin sets the ON-time and frequency of the application. Typical values range from 100 kΩ to 700 kΩ.
3	EN	Analog	Enable — Input to the precision enable comparator. Rising threshold is 1.18 V.
4	GND	Ground	Ground — Reference point for all stated voltages. Must be externally connected to EP.
5	SS	Analog	Soft-Start — An internal 8-µA current source charges an external capacitor to produce the soft-start function.
6	FB	Analog	Feedback — Internally connected to the regulation, overvoltage, and short-circuit comparators. The regulation reference point is 0.8 V at this input pin. Connect the feedback resistor divider between the output and ground to set the output voltage.
7	VOUT	Power	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and the EP.
—	EP	Ground	Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
VIN, RON to GND	–0.3	43.5	V
EN, FB, SS to GND	–0.3	7	V
Junction Temperature		150	°C
Peak Reflow Case Temperature (30 s)		245	°C
Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications, refer to the following document: SNOA549

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	6	42	V
EN	0	6.5	V
Operation Junction Temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]			LMZ14202H NDW (TO-PMOD) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	4-layer Printed-Circuit-Board, 7.62 cm × 7.62 cm (3 in × 3 in) area, 1-oz Copper, No air flow	16	°C/W
		4-layer Printed-Circuit-Board, 6.35 cm × 6.35 cm (2.5 in × 2.5 in) area, 1-oz Copper, No air flow	18.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	No air flow	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Limits are for T_J = 25°C unless otherwise specified. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, V_{OUT} = 12 V, R_{ON} = 249 kΩ

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
SYSTEM PARAMETERS							
ENABLE CONTROL							
V_{EN}	EN threshold trip point	V_{EN} rising			1.18		V
			over the junction temperature (T_J) range of –40°C to +125°C	1.1		1.25	
V_{EN-HYS}	EN threshold hysteresis				90		mV
SOFT-START							
I_{SS}	SS source current	V_{SS} = 0 V			10		µA
			over the junction temperature (T_J) range of –40°C to +125°C	8		15	
I_{SS-DIS}	SS discharge current				-200		µA
CURRENT LIMIT							
I_{CL}	Current limit threshold	DC average			3.2		A
			over the junction temperature (T_J) range of –40°C to +125°C	2.4		3.95	
VIN UVLO							
VIN_{UVLO}	Input UVLO	EN pin floating V_{IN} rising			3.75		V
$VIN_{UVLO-HYST}$	Hysteresis	EN pin floating V_{IN} falling			130		mV
ON/OFF TIMER							
t_{ON-MIN}	ON timer minimum pulse width				150		ns
t_{OFF}	OFF timer pulse width				260		ns

(1) Minimum and Maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

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Electrical Characteristics (continued)

Limits are for T_J = 25°C unless otherwise specified. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, V_{OUT} = 12 V, R_{ON} = 249 kΩ

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
REGULATION AND OVERVOLTAGE COMPARATOR							
V_{FB}	In-regulation feedback voltage	V_{IN} = 24 V, V_{OUT} = 12 V V_{SS} >+ 0.8 V T_J = -40°C to 125°C I_{OUT} = 10 mA to 2 A			0.803		V
			over the junction temperature (T_J) range of –40°C to +125°C	0.782		0.822	
		V_{IN} = 24 V, V_{OUT} = 12 V V_{SS} >+ 0.8 V T_J = 25°C I_{OUT} = 10 mA to 2 A		0.786	0.803	0.818	
V_{FB}	In-regulation feedback voltage	V_{IN} = 36 V, V_{OUT} = 24 V V_{SS} >+ 0.8 V T_J = -40°C to 125°C I_{OUT} = 10 mA to 2 A			0.803		V
			over the junction temperature (T_J) range of –40°C to +125°C	0.780		0.824	
		V_{IN} = 36 V, V_{OUT} = 24 V V_{SS} >+ 0.8 V T_J = 25°C I_{OUT} = 10 mA to 2 A		0.787	0.803	0.819	
V_{FB-OVP}	Feedback overvoltage protection threshold				0.92		V
I_{FB}	Feedback input bias current				5		nA
I_Q	Nonswitching Input Current	V_{FB}= 0.86 V			1		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0 V			25		µA
THERMAL CHARACTERISTICS							
T_{SD}	Thermal Shutdown	Rising			165		°C
$T_{SD-HYST}$	Thermal Shutdown Hysteresis				15		°C
PERFORMANCE PARAMETERS							
ΔV_{OUT}	Output Voltage Ripple	V_{OUT} = 5 V, C_O = 100 µF 6.3 V X7R			8		mV_{PP}
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 16 V to 42 V, I_{OUT}= 3 A			.01%		
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 24 V, I_{OUT} = 0 A to 2 A			1.5		mV/A
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 12 V I_{OUT} = 1 A			93%		
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 12 V I_{OUT} = 2 A			92%		

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6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

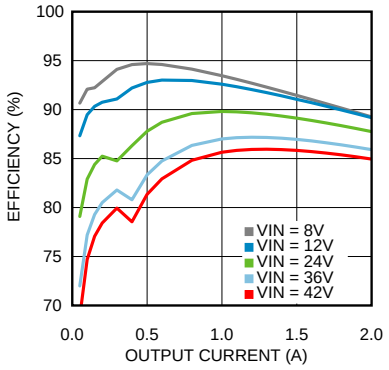


Figure 1. Efficiency V_{OUT} = 5 V T_A = 25°C

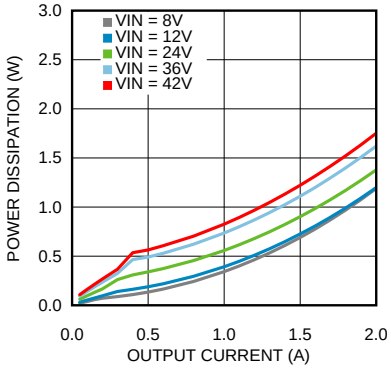


Figure 2. Power Dissipation V_{OUT} = 5 V T_A = 25°C

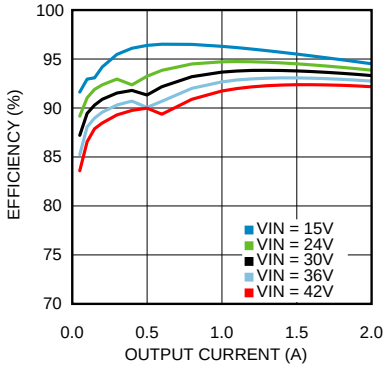


Figure 3. Efficiency V_{OUT} = 12 V T_A = 25°C

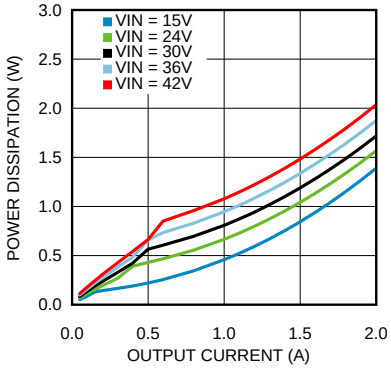


Figure 4. Power Dissipation V_{OUT} = 12 V T_A = 25°C

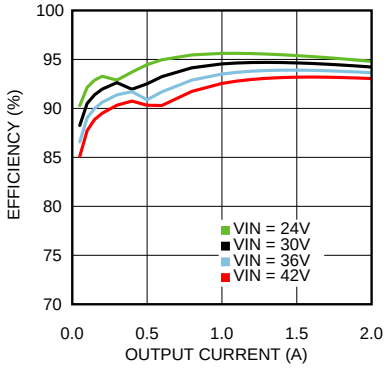


Figure 5. Efficiency V_{OUT} = 15 V T_A = 25°C

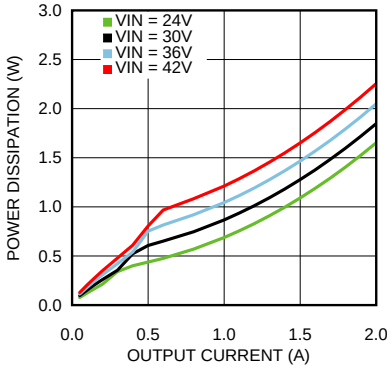


Figure 6. Power Dissipation V_{OUT} = 15 V T_A = 25°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

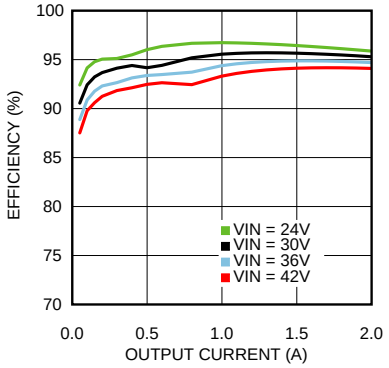


Figure 7. Efficiency V_{OUT} = 18 V T_A = 25°C

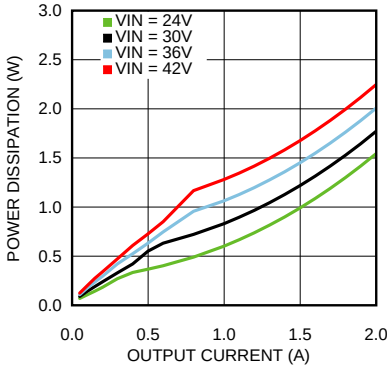


Figure 8. Power Dissipation V_{OUT} = 18 V T_A = 25°C

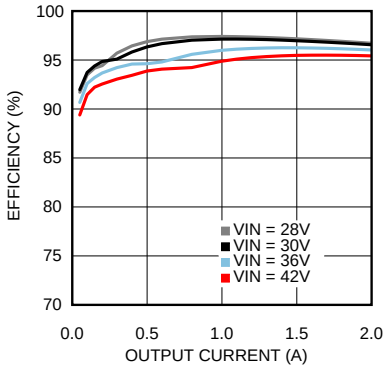


Figure 9. Efficiency V_{OUT} = 24 V T_A = 25°C

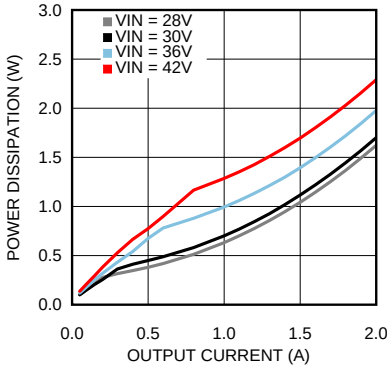


Figure 10. Power Dissipation V_{OUT} = 24 V T_A = 25°C

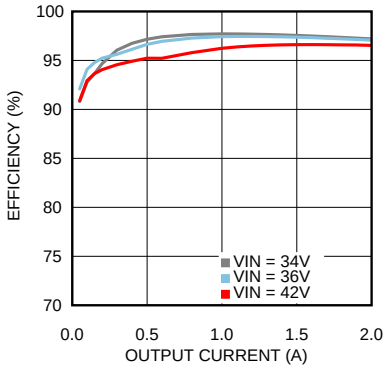


Figure 11. Efficiency V_{OUT} = 30 V T_A = 25°C

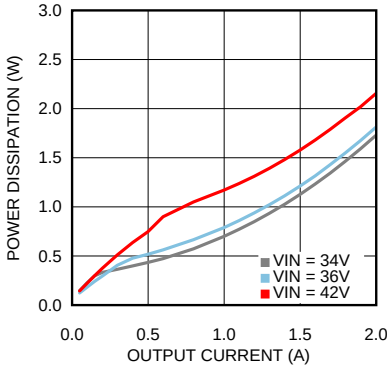


Figure 12. Power Dissipation V_{OUT} = 30 V T_A = 25°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

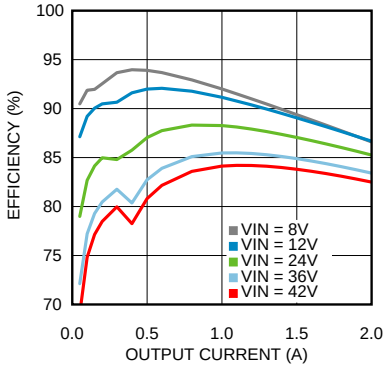


Figure 13. Efficiency V_{OUT} = 5 V T_A = 85°C

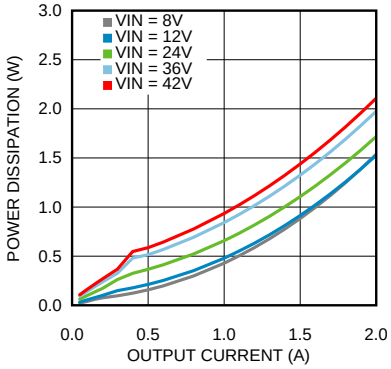


Figure 14. Power Dissipation V_{OUT} = 5 V T_A = 85°C

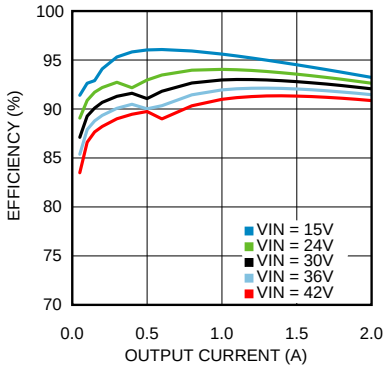


Figure 15. Efficiency V_{OUT} = 12 V T_A = 85°C

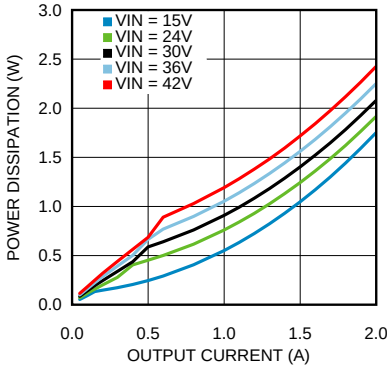


Figure 16. Power Dissipation V_{OUT} = 12 V T = 85°C

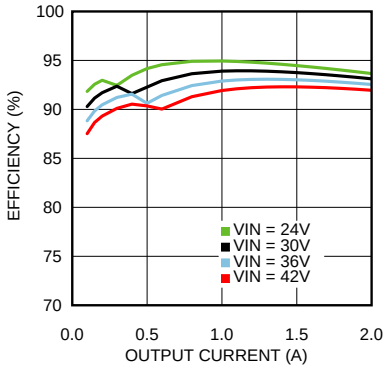


Figure 17. Efficiency V_{OUT} = 15 V T_A = 85°C

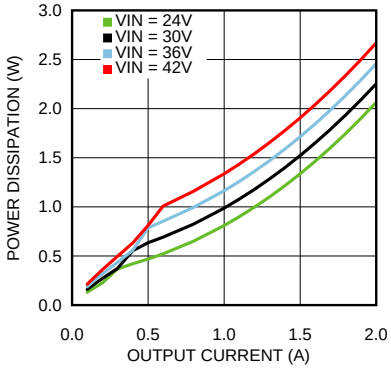


Figure 18. Power Dissipation V_{OUT} = 15 V T_A = 85°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

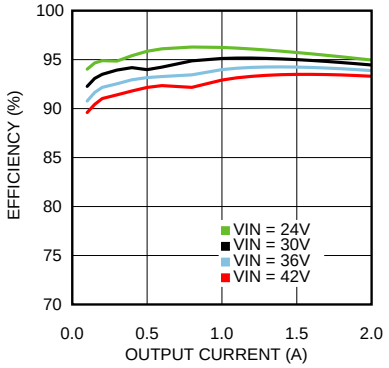


Figure 19. Efficiency V_{OUT} = 18 V T_A = 85°C

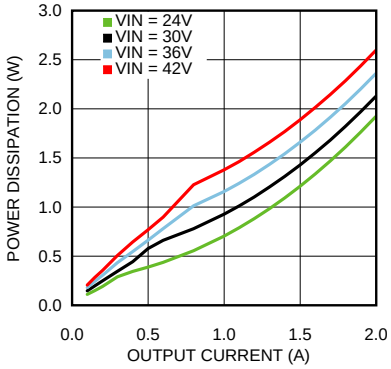


Figure 20. Power Dissipation V_{OUT} = 18 V T_A = 85°C

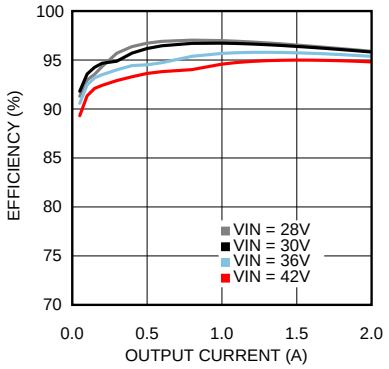


Figure 21. Efficiency V_{OUT} = 24 V T_A = 85°C

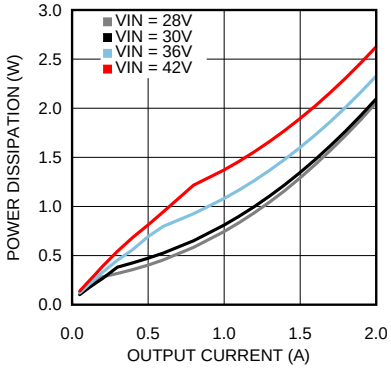


Figure 22. Power Dissipation V_{OUT} = 24 V T_A = 85°C

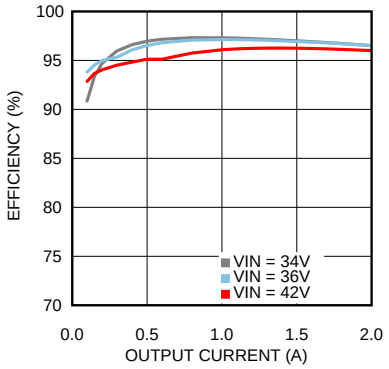


Figure 23. Efficiency V_{OUT} = 30 V T_A = 85°C

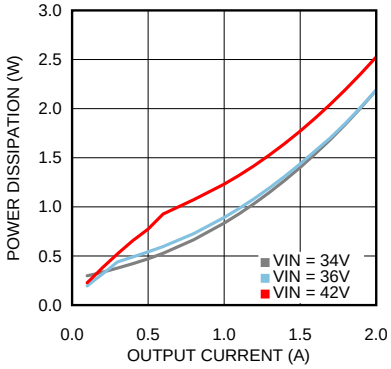


Figure 24. Power Dissipation V_{OUT} = 30 V T_A = 85°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

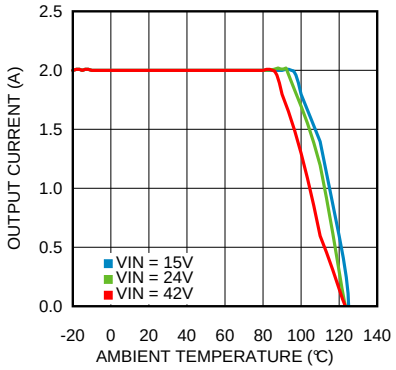


Figure 25. Thermal Derating V_{OUT} = 12 V, $R_{\theta JA}$ = 16°C/W

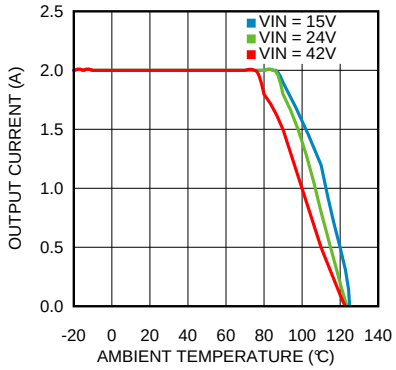


Figure 26. Thermal Derating V_{OUT} = 12 V, $R_{\theta JA}$ = 20°C/W

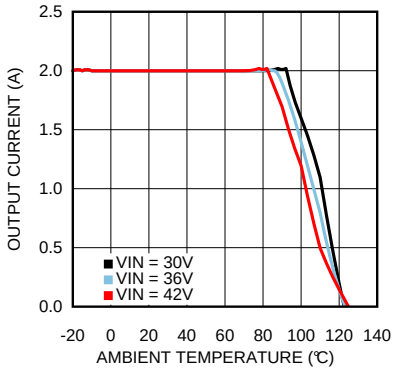


Figure 27. Thermal Derating V_{OUT} = 24 V, $R_{\theta JA}$ = 16°C/W

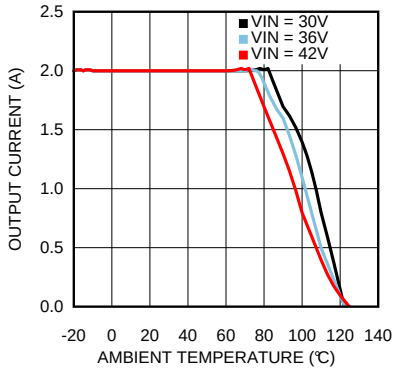


Figure 28. Thermal Derating V_{OUT} = 24 V, $R_{\theta JA}$ = 20°C/W

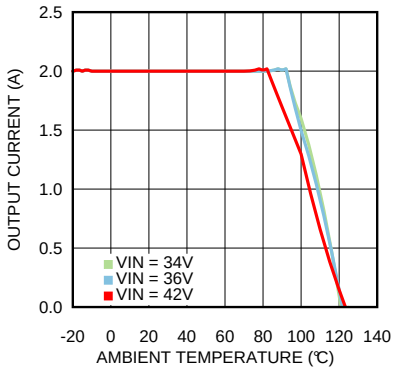


Figure 29. Thermal Derating V_{OUT} = 30 V, $R_{\theta JA}$ = 16°C/W

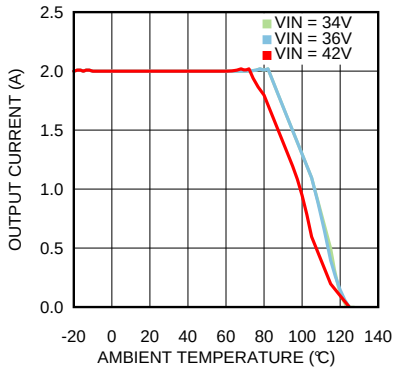


Figure 30. Thermal Derating V_{OUT} = 30 V, $R_{\theta JA}$ = 20°C/W

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

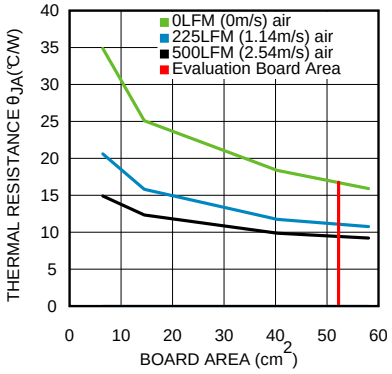


Figure 31. Package Thermal Resistance $R_{\theta JA}$ 4-Layer Printed-Circuit-Board With 1-oz Copper

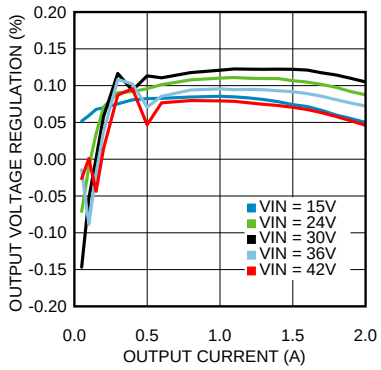


Figure 32. Line and Load Regulation T_A = 25°C

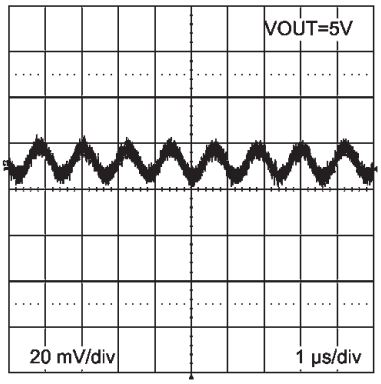


Figure 33. Output Ripple V_{IN} = 12 V, I_{OUT} = 2 A, Ceramic C_{OUT}, BW = 200 MHz

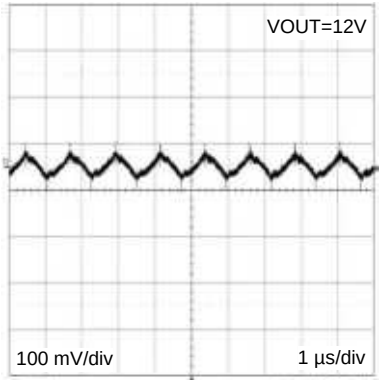


Figure 34. Output Ripple V_{IN} = 24 V, I_{OUT} = 2 A, Polymer Electrolytic C_{OUT}, BW = 200 MHz

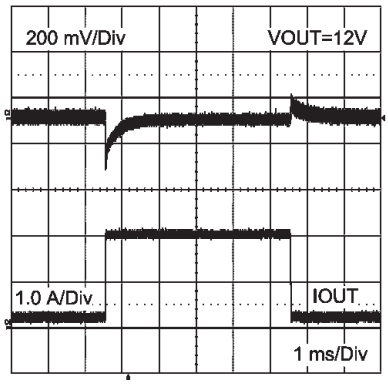


Figure 35. Load Transient Response V_{IN} = 24 V, V_{OUT} = 12 V Load Step from 10% to 100%

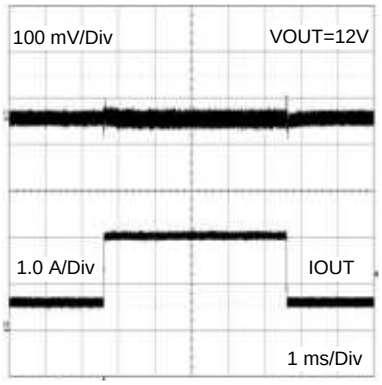


Figure 36. Load Transient Response V_{IN} = 24 V, V_{OUT} = 12 V Load Step from 30% to 100%

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

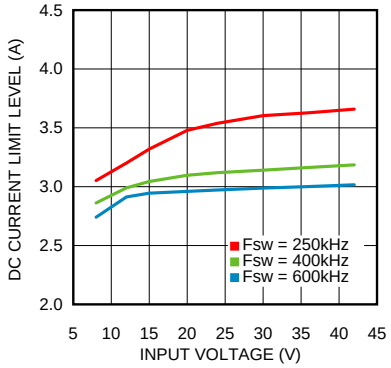


Figure 37. Current Limit vs. Input Voltage
V_{OUT} = 5 V T_A = 25°C

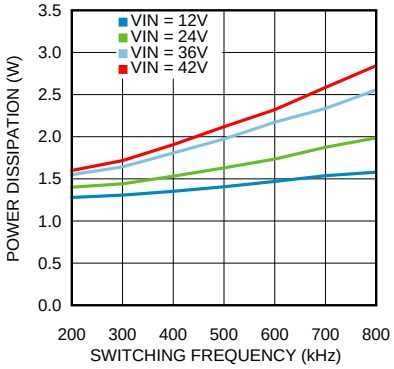


Figure 38. Switching Frequency vs. Power Dissipation
V_{OUT} = 5 V T_A = 25°C

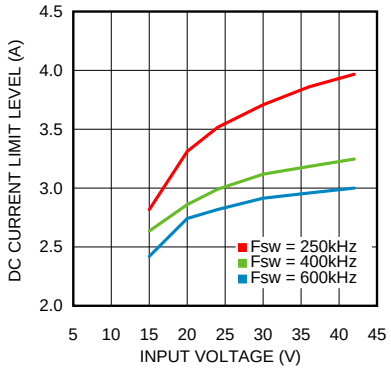


Figure 39. Current Limit vs. Input Voltage
V_{OUT} = 12 V T_A = 25°C

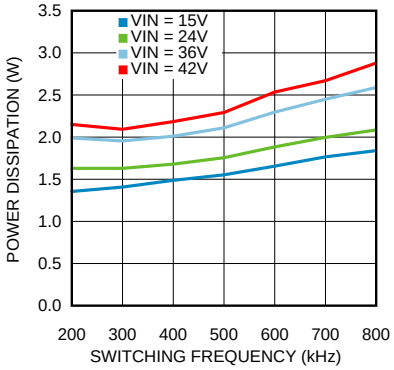


Figure 40. Switching Frequency vs. Power Dissipation
V_{OUT} = 12 V T_A = 25°C

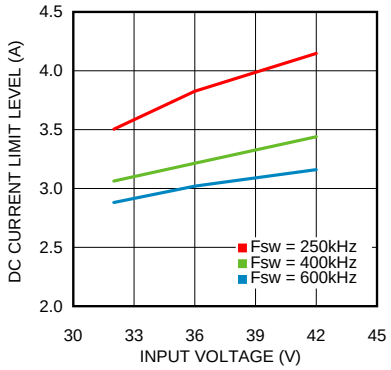


Figure 41. Current Limit vs. Input Voltage
V_{OUT} = 24 V T_A = 25°C

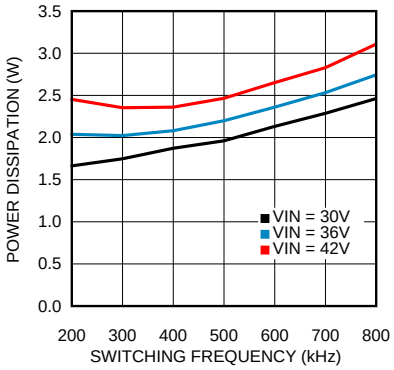


Figure 42. Switching Frequency vs. Power Dissipation
V_{OUT} = 24 V T_A = 25°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

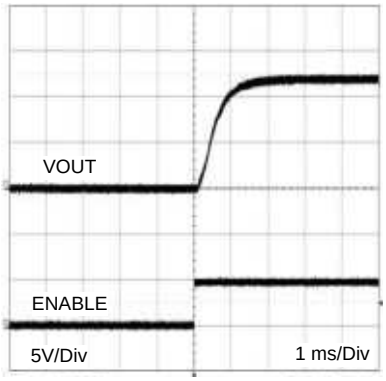


Figure 43. Start-Up
V_{IN} = 24 V I_{OUT} = 2 A

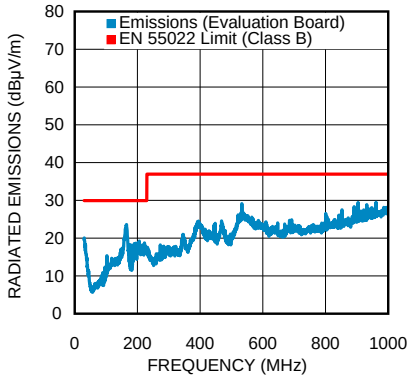


Figure 44. Radiated EMI of Evaluation Board, V_{OUT} = 12 V

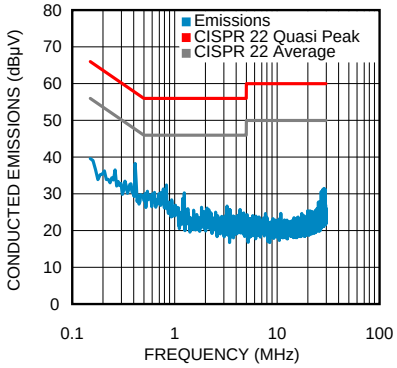


Figure 45. Conducted EMI, V_{OUT} = 12 V
Evaluation Board BOM and 3.3-µH 2×10-µF LC line filter

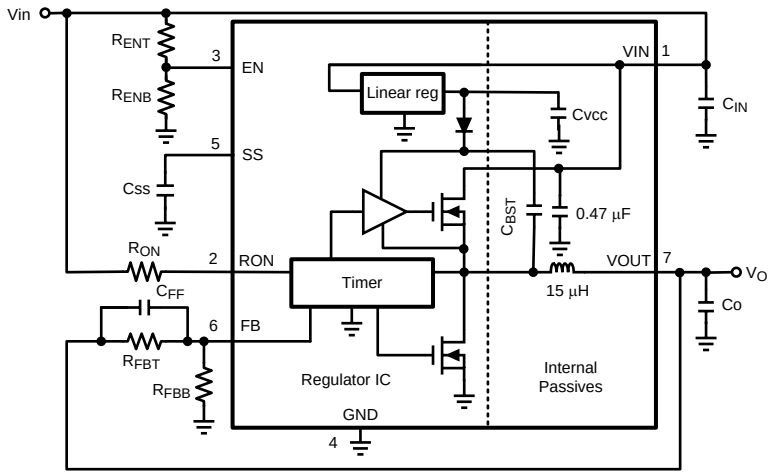
7 Detailed Description

7.1 Overview

7.1.1 COT Control Circuit Overview

Constant On Time control is based on a comparator and an ON-time one-shot, with the output voltage feedback compared to an internal 0.8-V reference. If the feedback voltage is below the reference, the high-side MOSFET is turned on for a fixed ON-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the high-side MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Overvoltage Comparator

The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

7.3.2 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds I_{CL} the current limit comparator disables the start of the next ON-time period. The next switching cycle will occur only if the FB input is less than 0.8 V and the inductor current has decreased below I_{CL}. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds I_{CL}, further ON-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer OFF-time.

NOTE

The DC current limit varies with duty cycle, switching frequency, and temperature.

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Feature Description (continued)

7.3.3 Thermal Protection

The junction temperature of the LMZ14202H should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145 °C (typical Hyst = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

7.3.4 Zero Coil Current Detection

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

7.3.5 Prebiased Start-Up

The LMZ14202H will properly start up into a prebiased output. This is start-up situation is common in multiple rail logic applications where current paths may exist between different power rails during the start-up sequence. The pre-bias level of the output voltage must be less than the input UVLO set point. This will prevent the output prebias from enabling the regulator through the high-side MOSFET body diode.

7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. During the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained because conduction and switching losses are reduced with the smaller load and lower switching frequency.

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8 Application and Implementation

NOTE

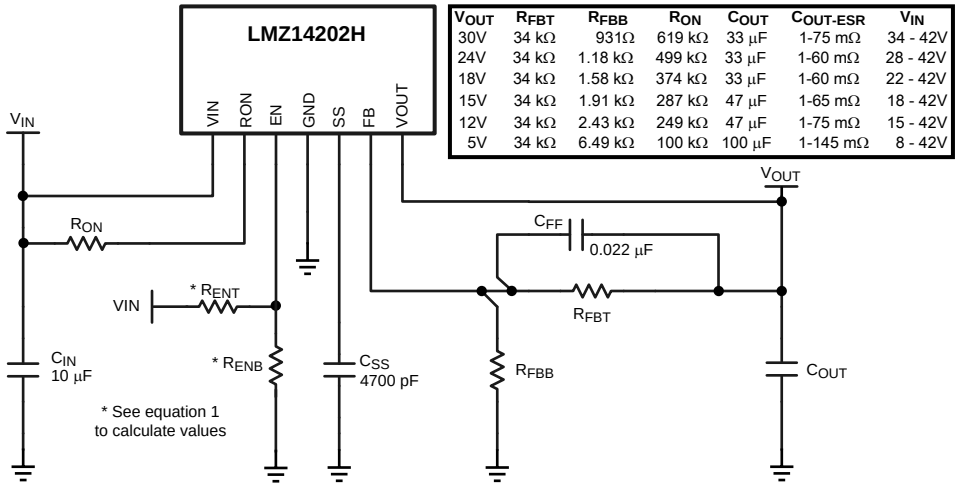
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ14202H is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LMZ14202H. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. For more details, go to www.ti.com.

8.2 Typical Application



VOUT	RFBT	RFBB	RON	COUT	COUT-ESR	VIN
30V	34 kΩ	931Ω	619 kΩ	33 µF	1-75 mΩ	34 - 42V
24V	34 kΩ	1.18 kΩ	499 kΩ	33 µF	1-60 mΩ	28 - 42V
18V	34 kΩ	1.58 kΩ	374 kΩ	33 µF	1-60 mΩ	22 - 42V
15V	34 kΩ	1.91 kΩ	287 kΩ	47 µF	1-65 mΩ	18 - 42V
12V	34 kΩ	2.43 kΩ	249 kΩ	47 µF	1-75 mΩ	15 - 42V
5V	34 kΩ	6.49 kΩ	100 kΩ	100 µF	1-145 mΩ	8 - 42V

Figure 46. Typical Application Schematic

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = Up to 42 V
- V_{OUT} = 5 V to 30 V
- I_{OUT} = 2 A

Refer to the table in Figure 46 for more information.

8.2.2 Detailed Design Procedure

8.2.2.1 Design Steps for the LMZ14202H Application

The LMZ14202H is fully supported by WEBENCH which offers the following:

- Component selection
- Electrical simulation
- Thermal simulation
- Build-it prototype board for a reduction in design time

The following list of steps can be used to manually design the LMZ14202H application.

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Typical Application (continued)

1. Select minimum operating V_{IN} with enable divider resistors.
2. Program V_O with divider resistor selection.
3. Program turnon time with soft-start capacitor selection.
4. Select C_O.
5. Select C_{IN}.
6. Set operating frequency with R_{ON}.
7. Determine module dissipation.
8. Lay out PCB for required thermal performance.

8.2.2.1.1 Enable Divider, R_{ENT} and R_{ENB} Selection

The enable input provides a precise 1.18-V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider shown in the *Functional Block Diagram* is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery-powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14202H output rail. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\text{-}ENABLE} / 1.18\ V) - 1 \quad (1)$$

The EN pin is internally pulled up to VIN and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will ensure smooth start-up and will prevent overloading the input supply.

8.2.2.1.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The high-side MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8\ V \times (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8\ V) - 1 \quad (3)$$

These resistors should be chosen from values in the range of 1 kΩ to 50 kΩ.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , and R_{ON} is included in the simplified applications schematic.

8.2.2.1.3 Soft-Start Capacitor, C_{SS}, Selection

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

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Typical Application (continued)

Upon turnon, after all UVLO conditions have been passed, an internal 8-uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.8\ V \times C_{SS} / 8uA \quad (4)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8\ \mu A / 0.8\ V \quad (5)$$

Use of a 4700-pF capacitor results in 0.5ms soft-start duration. This is a recommended value. Note that high values of C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use Equation 22 below to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the soft-start capacitor value should be less than 0.018µF.

As the soft-start input exceeds 0.8 V the output of the power stage will be in regulation. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200 µA current sink:

- The enable input being “pulled low”
- Thermal shutdown condition
- Overcurrent fault
- Internal V_{IN}UVLO

8.2.2.1.4 Output Capacitor, C_O, Selection

None of the required output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst-case RMS current rating of 0.5 x $I_{LR\ P-P}$, as calculated in Equation 23. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Low ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

8.2.2.1.4.1 Capacitance

Equation 6 provides a good first pass approximation of C_O for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} — V_O) \times V_{OUT\text{-}TRAN}) \quad (6)$$

As an example, for 2-A load step, V_{IN} = 24 V, V_{OUT} = 12 V, $V_{OUT\text{-}TRAN}$ = 50 mV:

$$C_O \geq 2\ A \times 0.8\ V \times 15\ \mu H \times 24\ V / (4 \times 12\ V \times (24\ V — 12\ V) \times 50\ mV) \quad (7)$$

$$C_O \geq 20\ \mu F \quad (8)$$

8.2.2.1.4.2 ESR

The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the overvoltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid overvoltage protection during normal operation. The following equations can be used:

$$ESR_{MAX\text{-}RIPPLE} \leq V_{OUT\text{-}RIPPLE} / I_{LR\ P-P}$$

where

- $I_{LR\ P-P}$ is calculated using Equation 23 below (9)

$$ESR_{MAX\text{-}OVP} < (V_{FB\text{-}OVP} - V_{FB}) / (I_{LR\ P-P} \times A_{FB})$$

where

- A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency. (10)

As worst-case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.

The selected capacitor should have sufficient voltage and RMS current rating. The RMS current through the output capacitor is:

$$I(C_{OUT(RMS)}) = I_{LR\ P-P} / \sqrt{12} \quad (11)$$

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Typical Application (continued)

8.2.2.1.5 Input Capacitor, C_{IN}, Selection

The LMZ14202H module contains an internal 0.47 µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be as close as possible to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst-case input ripple current rating is dictated by Equation 12:

$$I(C_{IN(RMS)}) \cong 1 / 2 \times I_O \times \sqrt{(D / 1-D)}$$

where

- $D \cong V_O / V_{IN}$ (12)

(As a point of reference, the worst-case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10-uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then Equation 13 may be used.

$$C_{IN} \geq I_O \times D \times (1-D) / f_{SW-CCM} \times \Delta V_{IN} \quad (13)$$

If ΔV_{IN} is 1% of V_{IN} for a 24V input to 12V output application this equals 240 mV and f_{SW} = 400 kHz.

$$C_{IN} \geq 2\ A \times 12\ V/24\ V \times (1 - 12\ V/24\ V) / (400000 \times 0.240\ V) \quad (14)$$

$$C_{IN} \geq 5.2\ \mu F \quad (15)$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

8.2.2.1.6 ON-Time, R_{ON}, Resistor Selection

Many designs will begin with a desired switching frequency in mind. As seen in the *Typical Characteristics* section, the best efficiency is achieved in the 300kHz-400kHz switching frequency range. Equation 16 can be used to calculate the R_{ON} value.

$$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \times R_{ON}) \quad (16)$$

This can be rearranged as

$$R_{ON} \cong V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}) \quad (17)$$

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the ON-time and OFF-time for the *COT Control Circuit Overview* section.

The ON-time of the LMZ14202H timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN} \quad (18)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the ON-time at maximum V_{IN} is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by Equation 19:

$$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150\ nsec) \quad (19)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum ON-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq V_{IN(MAX)} \times 150\ nsec / (1.3 \times 10^{-10}) \quad (20)$$

If R_{ON} calculated in Equation 17 is less than the minimum value determined in Equation 20 a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

Additionally, the minimum OFF-time of 260 ns (typical) limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

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Typical Application (continued)

8.2.2.1.6.1 Discontinuous Conduction and Continuous Conduction Modes Selection

Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong V_O \times (V_{IN}\text{-}1) \times 15\ \mu H \times 1.18 \times 10^{20} \times I_O / (V_{IN} - V_O) \times R_{ON}^2 \quad (21)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using Equation 16 above.

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN} - V_O) / (2 \times 15\mu H \times f_{SW(CCM)} \times V_{IN}) \quad (22)$$

The inductor internal to the module is 15 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN} - V_O) / (15\ \mu H \times f_{SW} \times V_{IN})$$

where

- V_{IN} is the maximum input voltage and f_{SW} is determined from Equation 16. (23)

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

8.2.3 Application Curves

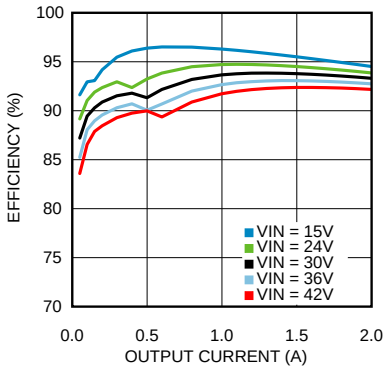


Figure 47. Efficiency V_{OUT} = 12 V

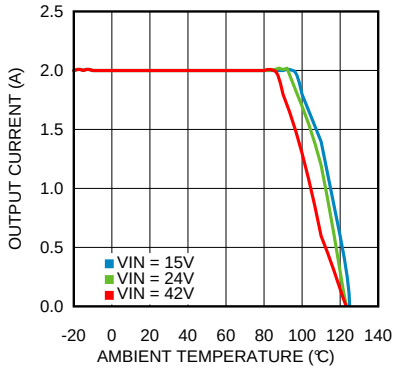


Figure 48. Thermal Derating V_{OUT} = 12 V, $R_{\theta JA}$ = 16°C/W

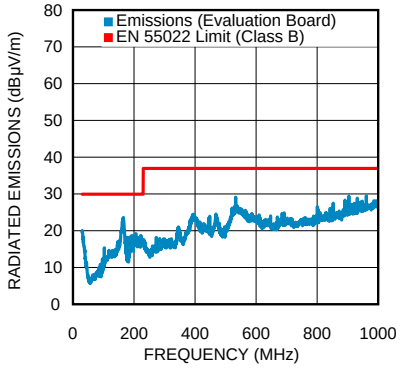


Figure 49. Radiated Emissions (EN 55022 Class B)

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9 Power Supply Recommendations

The LMZ14202H device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ14202H supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ14202H, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14202H. Therefore place C_{IN1} as close as possible to the LMZ14202H VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be close to the FB pin. Because the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14202H to minimize noise pickup.

4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

10.1.1 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher

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Layout Guidelines (continued)

- Stencil Thickness – 0.125 mm to 0.15 mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to application note SNAA214 for Reflow information
- Maximum number of reflows allowed is one

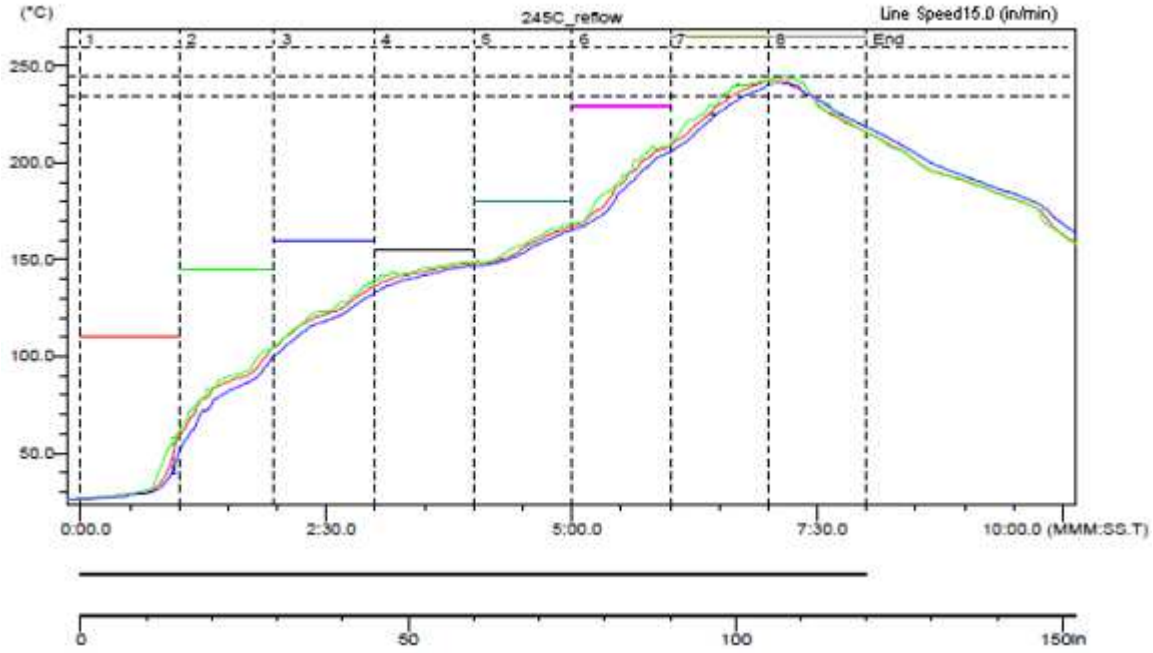


Figure 50. Sample Reflow Profile

Table 1. Sample Reflow Profile Table

PROBE	MAX TEMP (°C)	REACHED MAX TEMP	TIME ABOVE 235°C	REACHED 235°C	TIME ABOVE 245°C	REACHED 245°C	TIME ABOVE 260°C	REACHED 260°C
1	242.5	6.58	0.49	6.39	0.00	–	0.00	–
2	242.5	7.10	0.55	6.31	0.00	7.10	0.00	–
3	241.0	7.09	0.42	6.44	0.00	–	0.00	–

10.2 Layout Example

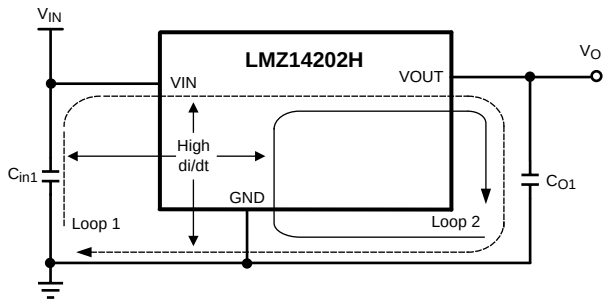


Figure 51. Critical Current Loops to Minimize

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Layout Example (continued)

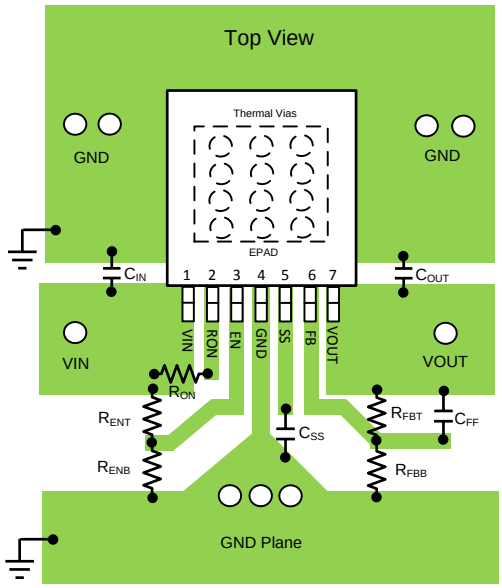


Figure 52. PCB Layout

10.3 Power Dissipation and Board Thermal Requirements

For a design case of V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 2 A, T_A (MAX) = 85°C , and $T_{JUNCTION}$ = 125°C, the device must see a maximum junction-to-ambient thermal resistance of:

$R_{\theta JA\text{-}MAX} < (T_{J\text{-}MAX} - T_{A(MAX)}) / P_D$

This $R_{\theta JA\text{-}MAX}$ will ensure that the junction temperature of the regulator does not exceed $T_{J\text{-}MAX}$ in the particular application ambient temperature.

To calculate the required $R_{\theta JA\text{-}MAX}$ we need to get an estimate for the power losses in the IC. Figure 53 is taken from the *Typical Characteristics* section and shows the power dissipation of the LMZ14202H for V_{OUT} = 12 V at 85°C T_A.

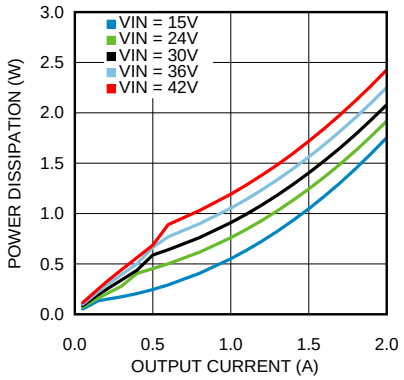


Figure 53. Power Dissipation V_{OUT} = 12 V, T_A = 85°C

Using the 85°C T_A power dissipation data P_D for V_{IN} = 24 V and V_{OUT} = 12 V is estimated to be 1.8 W. The necessary $R_{\theta JA\text{-}MAX}$ can now be calculated.

$R_{\theta JA\text{-}MAX} < (125°C - 85°C) / 1.8W$ (24)

$R_{\theta JA\text{-}MAX} < 22.2°C/W$ (25)

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Power Dissipation and Board Thermal Requirements (continued)

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to the following Figure 54. Figure 54 is taken from the *Typical Characteristics* section and shows how the $R_{\theta JA}$ varies with the PCB area.

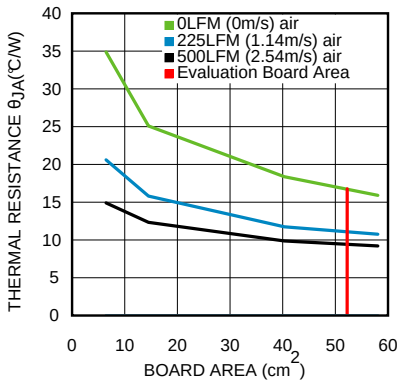


Figure 54. Package Thermal Resistance $R_{\theta JA}$ 4-Layer Printed-Circuit-Board With 1-oz Copper

For $R_{\theta JA\text{-}MAX}$< 22.2°C/W and only natural convection (that is, no air flow), the PCB area will have to be at least 30 cm^2. This corresponds to a square board with approximately 5.5cm × 5.5cm (2.17in × 2.17in) copper area, 4 layers, and 1-oz copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

For more guidelines and insight on PCB copper area, thermal vias placement, and general thermal design practices refer to Application Note AN-2020 (SNVA419).

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documents, please see the following:

- *AN-2027 Inverting Application for the LMZ14203 SIMPLE SWITCHER Power Module*, SNVA425
- *Evaluation Board Application Note AN-2024*, SNVA422
- *AN-2026 Effect of PCB Design on Thermal Performance of SIMPLE SWITCHER Power Modules*, SNVA424
- *AN-2020 Thermal Design By Insight, Not Hindsight*, SNVA419
- *Evaluation Board Application Note AN-2024*, SNVA422
- *Design Summary LMZ1 and LMZ2 Power Modules*, SNAA214

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZ14202HTZ/NOPB	Active	Production	TO-PMOD (NDW) | 7	250 | SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ
LMZ14202HTZ/NOPB.A	Active	Production	TO-PMOD (NDW) | 7	250 | SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ
LMZ14202HTZE/NOPB	Active	Production	TO-PMOD (NDW) | 7	45 | TUBE	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ
LMZ14202HTZE/NOPB.A	Active	Production	TO-PMOD (NDW) | 7	45 | TUBE	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ
LMZ14202HTZX/NOPB	Active	Production	TO-PMOD (NDW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ
LMZ14202HTZX/NOPB.A	Active	Production	TO-PMOD (NDW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14202 HTZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

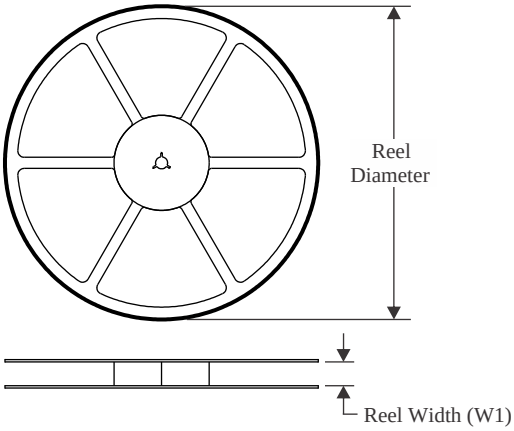
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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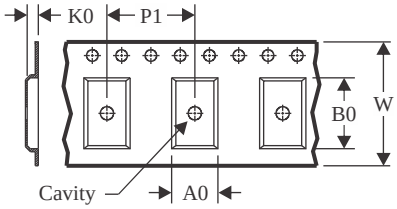
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

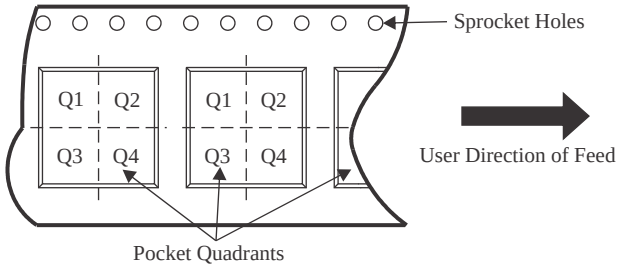


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

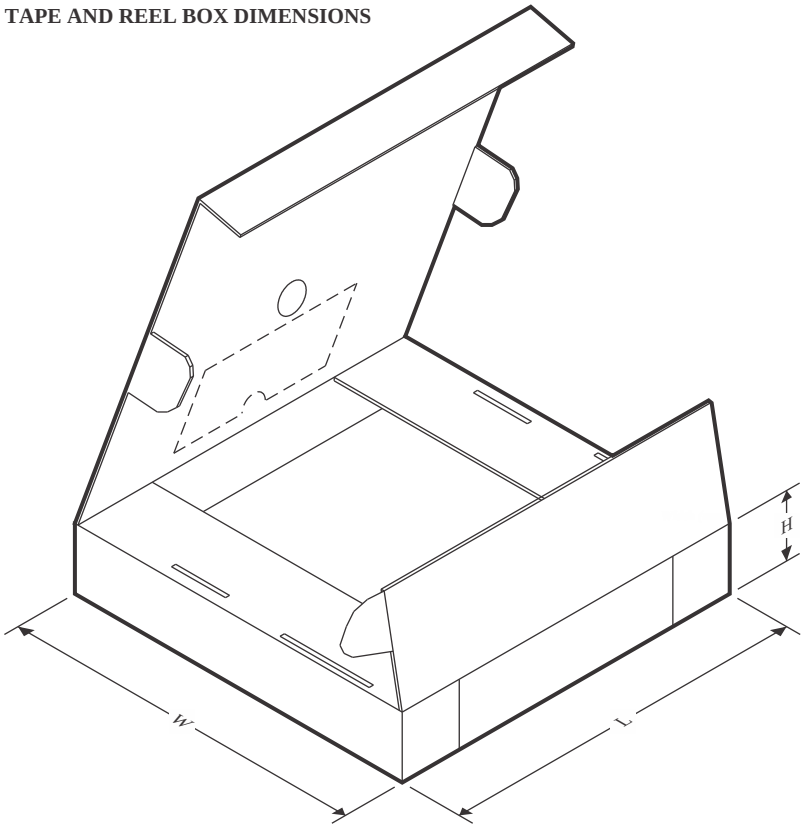
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ14202HTZ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ14202HTZX/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

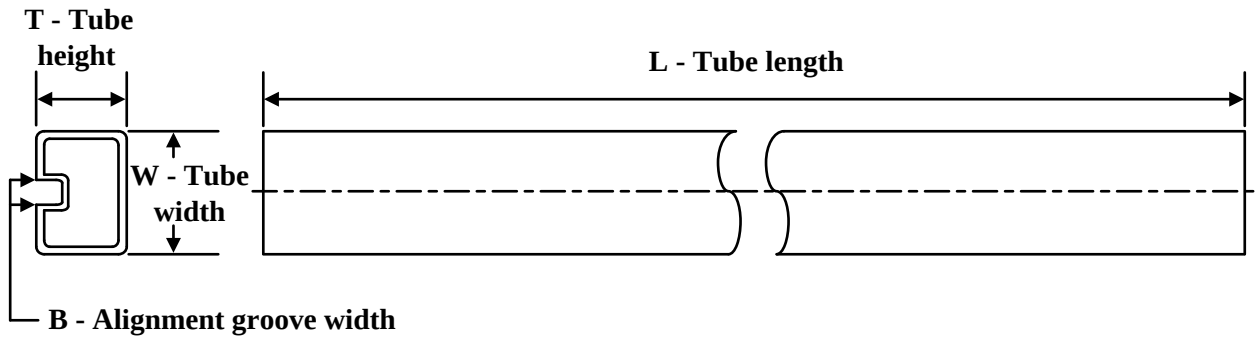
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ14202HTZ/NOPB	TO-PMOD	NDW	7	250	356.0	356.0	45.0
LMZ14202HTZX/NOPB	TO-PMOD	NDW	7	500	356.0	356.0	45.0

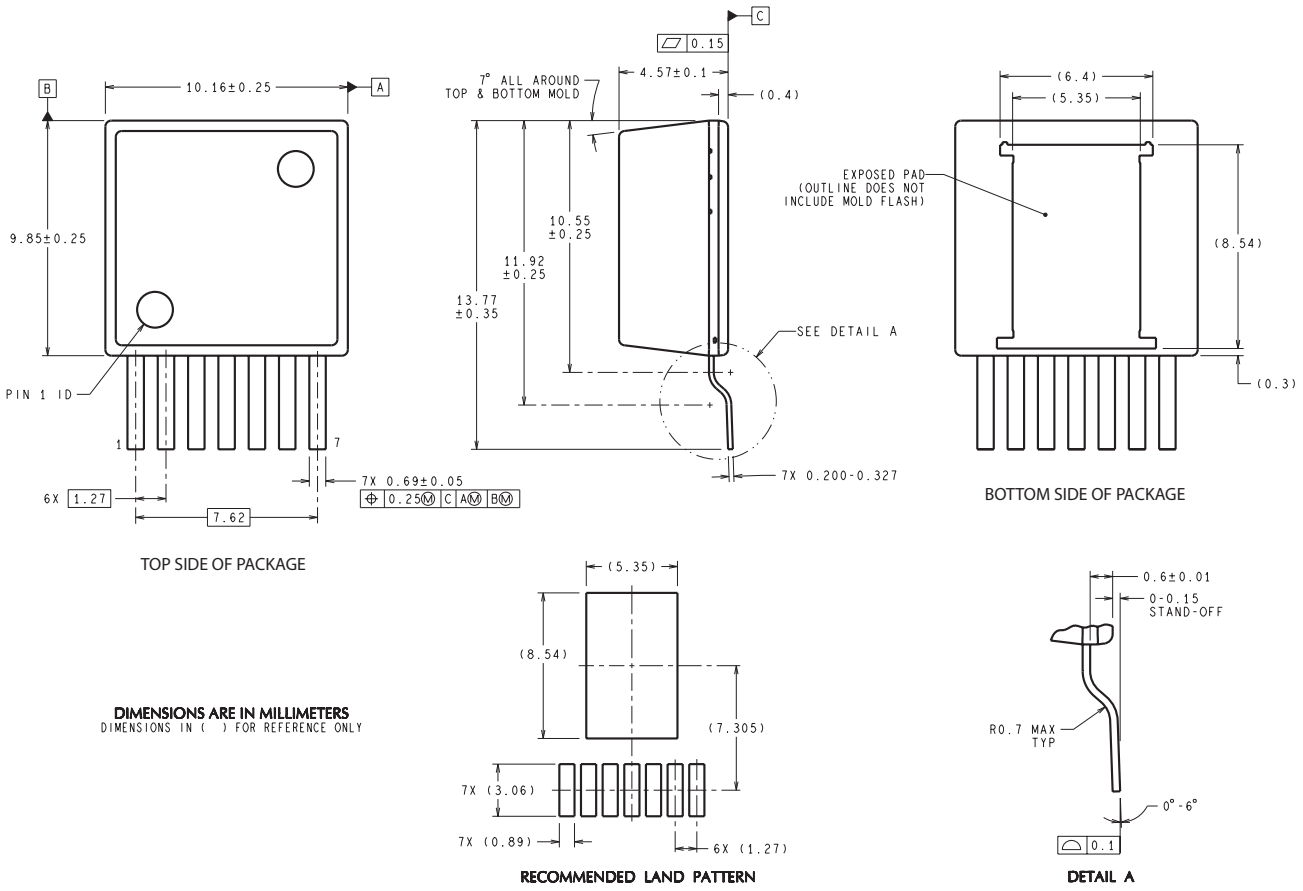
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMZ14202HTZE/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4
LMZ14202HTZE/NOPB.A	NDW	TO-PMOD	7	45	502	17	6700	8.4

NDW0007A



TZA07A (Rev D)

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