LP5912-Q1 Automotive 500-mA Low-Noise, Low-I_Q LDO

1 Features

- Qualified for Automotive Applications
- AEC Q100-Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 2
  - Device CDM Classification Level C6
- Input Voltage Range: 1.6 V to 6.5 V
- Output Voltage Range: 0.8 V to 5.5 V
- Output Current up to 500 mA
- Low Output-Voltage Noise: 12 μV_{RMS} Typical
- PSRR at 1 kHz: 75 dB Typical
- Output Voltage Tolerance ($V_{OUT} \geq 3.3$ V): ±2%
- Low I_Q (Enabled, No Load): 30 µA Typical
- Low Dropout ($V_{OUT} \geq 3.3$ V): 95 mV Typical at 500-mA Load
- Stable With 1-µF Ceramic Input and Output Capacitors
- Thermal-Overload and Short-Circuit Protection
- Reverse Current Protection
- No Noise Bypass Capacitor Required
- Output Automatic Discharge for Fast Turnoff
- Power-Good Output With 140-µs Typical Delay
- Internal Soft-Start to Limit the In-rush Current
- –40°C to +125°C Operating Junction Temperature Range

2 Applications

- Automotive Infotainment
- Telematics Systems
- ADAS Cameras and Radar
- Navigation Systems

3 Description

The LP5912-Q1 is low-noise LDO that can supply up to 500 mA of output current. Designed to meet the requirements of RF and analog circuits, the LP5912-Q1 device provides low noise, high PSRR, low quiescent current, and low line and load transient response. The LP5912-Q1 offers class-leading noise performance without a noise bypass capacitor and with the ability for remote output capacitance placement.

The device is designed to work with a 1-µF input and a 1-µF output ceramic capacitor (no separate noise bypass capacitor required).

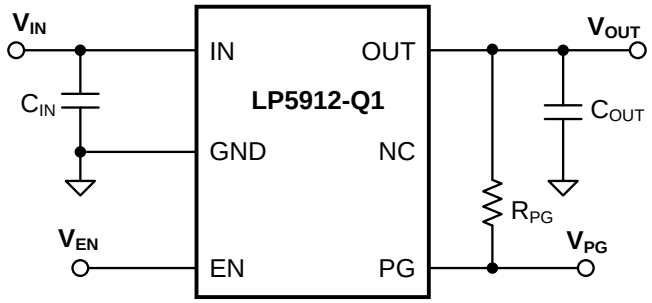
This device is available with fixed output voltages from 0.8 V to 5.5 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option needs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP5912-Q1	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the Package Option Addendum (POA) at the end of this data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2016) to Revision C — **Page**

- Changed wording of data sheet title and list of *Applications* ... 1
- Changed wording of first sentence of *Description* ... 1

Changes from Revision A (April 2016) to Revision B — **Page**

- Changed "linear regulator" to "LDO" on page 1 ... 1

Changes from Original (December 2015) to Revision A — **Page**

- Changed device from preview to production data ... 1
- Changed Block Diagram ... 17

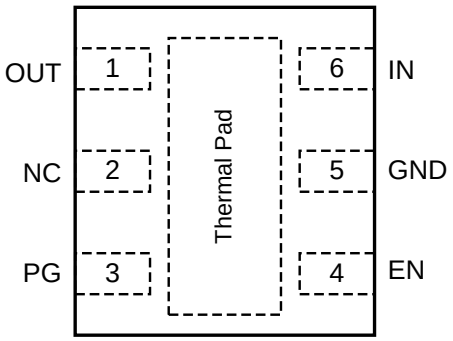
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5 Voltage Options

This device is capable of providing fixed output voltages from 0.8 V to 5.5 V in 25-mV steps. For all available package and voltage options, see the POA at the end of this datasheet. Contact Texas Instruments Sales for specific voltage option needs.

6 Pin Configuration and Functions

DRV Package
6-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT	O	Regulated output voltage
2	NC	—	No internal connection. Leave open, or connect to ground.
3	PG	O	Power-good indicator. Requires external pullup.
4	EN	I	Enable input. Logic high = device is ON, logic low = device is OFF, with internal 3-MΩ pulldown.
5	GND	G	Ground
6	IN	I	Unregulated input voltage
—	Exposed thermal pad	—	Connect to copper area under the package to improve thermal performance. The use of thermal vias to transfer heat to inner layers of the PCB is recommended. Connect the thermal pad to ground, or leave floating. Do not connect the thermal pad to any potential other than ground.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	7	V
V_{OUT}	Output voltage	–0.3	7	V
V_{EN}	Enable input voltage	–0.3	7	V
V_{PG}	Power Good (PG) pin OFF voltage	–0.3	7	V
T_J	Junction temperature		150	°C
P_D	Continuous power dissipation(3)	Internally Limited		W
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage	1.6	6.5	V
V_{OUT}	Output voltage	0.8	5.5	V
V_{EN}	Enable input voltage	0	V_{IN}	V
V_{PG}	PG pin OFF voltage	0	6.5	V
I_{OUT}	Output current	0	500	mA
$T_{J\text{-}MAX\text{-}OP}$	Operating junction temperature(2)	–40	125	°C

(1) All voltages are with respect to the GND pin.
(2) $T_{J\text{-}MAX\text{-}OP} = (T_{A(MAX)} + (P_{D(MAX)} \times R_{\theta JA}))$.

7.4 Thermal Information

THERMAL METRIC(1)		LP5912-Q1 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High-K(2)	71.2(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.1	°C/W
$\psi_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(3) The PCB for the WSON (DRV) package $R_{\theta JA}$ includes two (2) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

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7.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.6 V, whichever is greater; V_{EN} = 1.3 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{OUT} = 1 mA (unless otherwise stated). (1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE						
ΔV_{OUT}	Output voltage tolerance	For $V_{OUT(NOM)} \geq 3.3$ V: $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 1 mA to 500 mA	–2%		2%	
		For 1.1 V ≤ $V_{OUT(NOM)}$ < 3.3 V: $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 1 mA to 500 mA	–3%		3%	
		For $V_{OUT(NOM)}$ < 1.1 V: 1.6 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 1 mA to 500 mA				
	Line regulation	For $V_{OUT(NOM)} \geq 1.1$ V: $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V		0.8		%/V
		For $V_{OUT(NOM)}$ < 1.1 V: 1.6 V ≤ V_{IN} ≤ 6.5 V				
	Load regulation	I_{OUT} = 1 mA to 500 mA		0.0022		%/mA
CURRENT LEVELS						
I_{SC}	Short-circuit current limit	T_J = 25°C, see (4)	700	900	1100	mA
I_{RO}	Reverse leakage current (5)	V_{IN} < V_{OUT}		10	150	µA
I_Q	Quiescent current (6)	V_{EN} = 1.3 V, I_{OUT} = 0 mA		30	55	µA
		V_{EN} = 1.3 V, I_{OUT} = 500 mA		400	600	
$I_{Q(SD)}$	Quiescent current, shutdown mode (6)	V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C		0.2	1.5	µA
		V_{EN} = 0 V		0.2	5	
I_G	Ground current (7)	V_{EN} = 1.3 V, I_{OUT} = 0 mA		35		µA
V_{DO} DROPOUT VOLTAGE						
V_{DO}	Dropout voltage (8)	I_{OUT} = 500 mA, 1.6 V ≤ $V_{OUT(NOM)}$ < 3.3 V		170	250	mV
		I_{OUT} = 500 mA, 3.3 V ≤ $V_{OUT(NOM)}$ ≤ 5.5 V		95	180	mV

(1) All voltages are with respect to the device GND pin, unless otherwise stated.
(2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.
(4) Short-circuit current (I_{SC}) is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
(5) Reverse current (IRO) is measured at the IN pin.
(6) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(7) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device (I_Q + I_{EN}).
(8) Dropout voltage (V_{DO}) is the voltage difference between the input and the output at which the output voltage drops to 150 mV below its nominal value when V_{IN} = V_{OUT} + 0.5 V. Dropout voltage is not a valid condition for output voltages less than 1.6 V as compliance with the minimum operating voltage requirement cannot be assured.

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Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.6 V, whichever is greater; V_{EN} = 1.3 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{OUT} = 1 mA (unless otherwise stated).[1][2][3]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} to V_{OUT} RIPPLE REJECTION						
PSRR	Power Supply Rejection Ratio[9]	f = 100 Hz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		80		dB
		f = 1 kHz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		75		
		f = 10 kHz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		65		
		f = 100 kHz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		40		
		f = 100 Hz, 0.8 V < V_{OUT} < 1.1 V, I_{OUT} = 20 mA		65		
		f = 1 kHz, 0.8 V < V_{OUT} < 1.1 V, I_{OUT} = 20 mA		65		
		f = 10 kHz, 0.8 V < V_{OUT} < 1.1 V, I_{OUT} = 20 mA		65		
		f = 100 kHz, 0.8 V < V_{OUT} < 1.1 V, I_{OUT} = 20 mA		40		
OUTPUT NOISE VOLTAGE						
e_N	Noise voltage	I_{OUT} = 1 mA, BW = 10 Hz to 100 kHz		12		μV_{RMS}
		I_{OUT} = 500 mA, BW = 10 Hz to 100 kHz		12		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			160		°C
T_{HYS}	Thermal shutdown hysteresis			15		°C
LOGIC INPUT THRESHOLDS						
$V_{EN(OFF)}$	OFF threshold	V_{IN} = 1.6 V to 6.5 V V_{EN} falling until device is disabled			0.3	V
$V_{EN(ON)}$	ON threshold	1.6 V ≤ V_{IN} ≤ 6.5 V V_{EN} rising until device is enabled	1.3			
I_{EN}	Input current at EN pin[10]	V_{EN} = 6.5 V, V_{IN} = 6.5 V		2.5		µA
		V_{EN} = 0 V, V_{IN} = 3.3 V		0.001		
PG_{HTH}	PG high threshold (% of nominal V_{OUT})			94%		
PG_{LTH}	PG low threshold (% of nominal V_{OUT})			90%		
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < PG_{LTH}, sink current = 1 mA			100	mV
$I_{IKG(PG)}$	PG pin leakage current	V_{OUT} < PG_{HTH}, V_{PG} = 6.5 V			1	µA
t_{PGD}	PG delay time	Time from V_{OUT} > PG threshold to PG toggling		140		µs

(9) This specification is ensured by design.
(10) There is a 3-MΩ pulldown resistor between the EN pin and GND pin on the device.

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Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.6 V, whichever is greater; V_{EN} = 1.3 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{OUT} = 1 mA (unless otherwise stated).(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSITION CHARACTERISTICS						
ΔV_{OUT}	Line transients(9)	For V_{IN} ↑ and $V_{OUT(NOM)}$ ≥ 1.1 V: V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to ($V_{OUT(NOM)}$ + 1.1 V), V_{IN} t_{rise} = 30 µs			1	mV
		For V_{IN} ↑ and $V_{OUT(NOM)}$ < 1.1 V: V_{IN} = 1.6 V to 2.2 V, V_{IN} t_{rise} = 30 µs				
		For V_{IN} ↓ and $V_{OUT(NOM)}$ ≥ 1.1 V: V_{IN} = ($V_{OUT(NOM)}$ + 1.1 V) to ($V_{OUT(NOM)}$ + 0.5 V) V_{IN} t_{fall} = 30 µs	–1			
		For V_{IN} ↓ and $V_{OUT(NOM)}$ < 1.1 V: V_{IN} = 2.2 V to 1.6 V V_{IN} t_{fall} = 30 µs				
	Load transients(9)	I_{OUT} = 5 mA to 500 mA I_{OUT} t_{rise} = 10 µs	–45			mV
		I_{OUT} = 500 mA to 5 mA I_{OUT} t_{fall} = 10 µs			45	
	Overshoot on start-up(9)	Stated as a percentage of $V_{OUT(NOM)}$			5%	
t_{ON}	Turnon time	From V_{EN} > $V_{EN(ON)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$		200		µs
OUTPUT AUTO DISCHARGE RATE						
R_{AD}	Output discharge pulldown resistance	V_{EN} = 0 V, V_{IN} = 3.6 V		100		Ω

7.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX	UNIT
C_{IN}	Input capacitance(2)	Capacitance for stability	0.7	1		µF
C_{OUT}	Output capacitance(2)		0.7	1	10	µF
ESR	Output voltage(2)		5		500	mΩ

(1) The minimum capacitance must be greater than 0.5 µF over full range of operating conditions. The capacitor tolerance must be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application must be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V, and Z5U may be used with consideration of the application conditions.
(2) This specification is verified by design.

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7.7 Typical Characteristics

Unless otherwise stated: $V_{IN} = V_{OUT} + 0.5$ V, $V_{EN} = V_{IN}$, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, $T_J = 25°C$, unless otherwise stated.

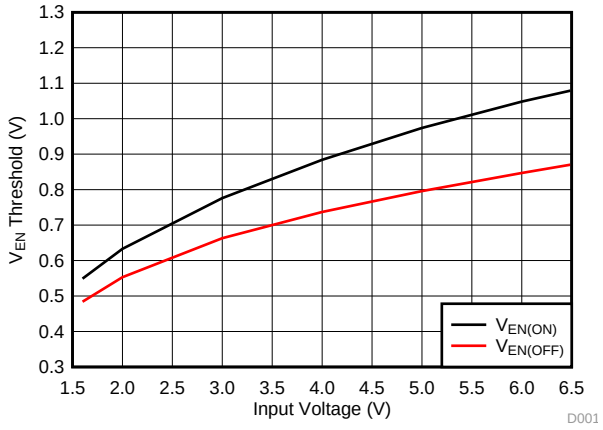


Figure 1. V_{EN} Thresholds vs Input Voltage

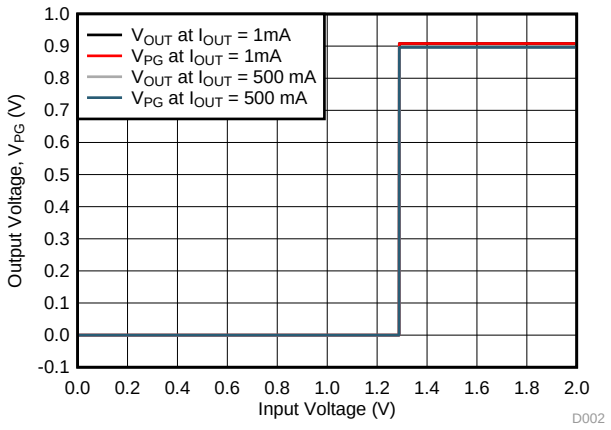


Figure 2. LP5912-0.9 Output Voltage, V_{PG} vs Input Voltage

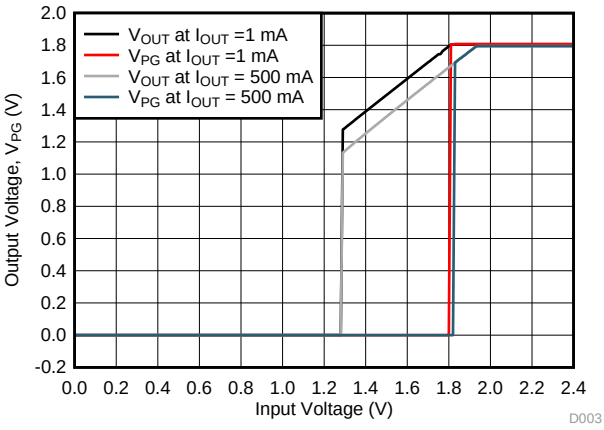


Figure 3. LP5912-1.8 Output Voltage, V_{PG} vs Input Voltage

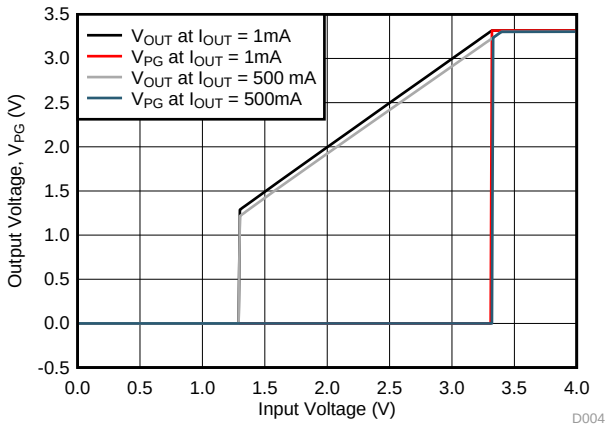


Figure 4. LP5912-3.3 Output Voltage, V_{PG} vs Input Voltage

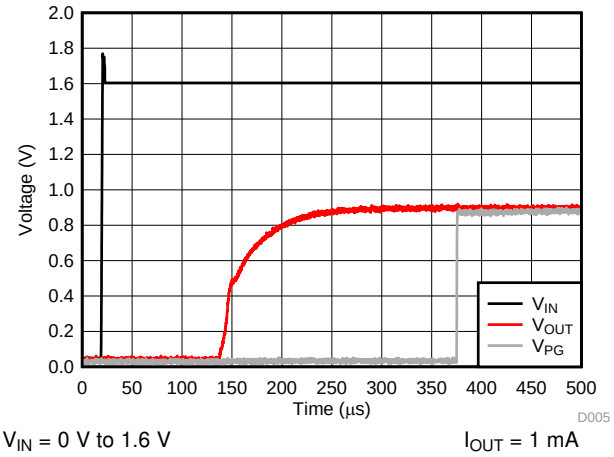


Figure 5. LP5912-0.9 Power Up

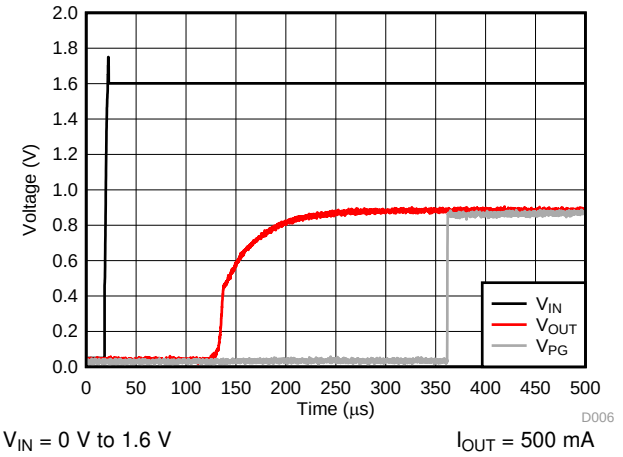


Figure 6. LP5912-0.9 Power Up

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Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C, unless otherwise stated.

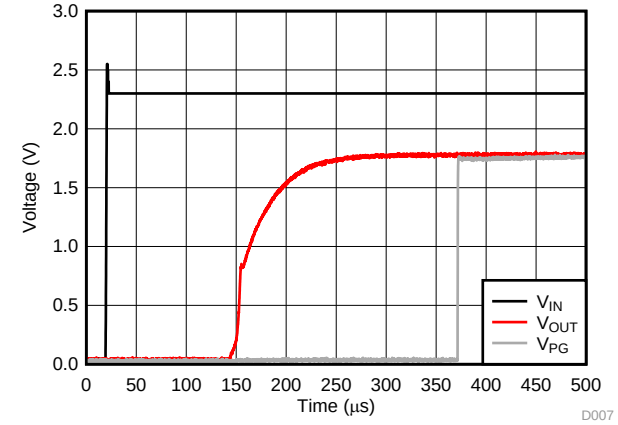


Figure 7. LP5912-1.8 Power Up

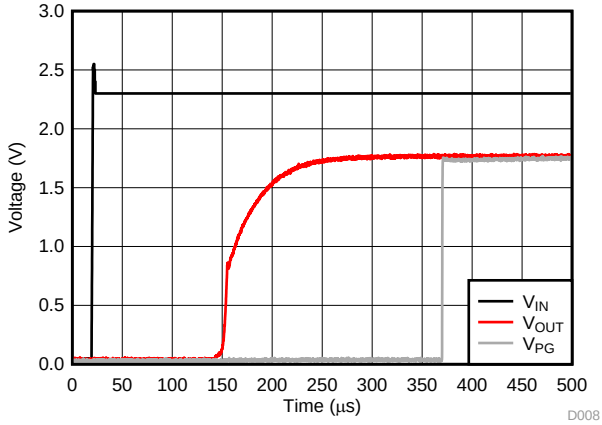


Figure 8. LP5912-1.8 Power Up

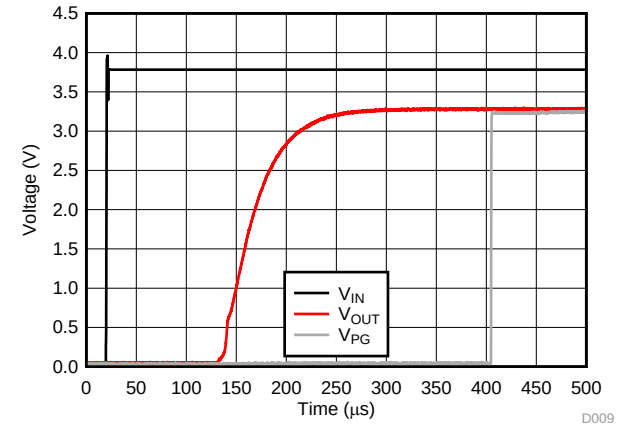


Figure 9. LP5912-3.3 Power Up

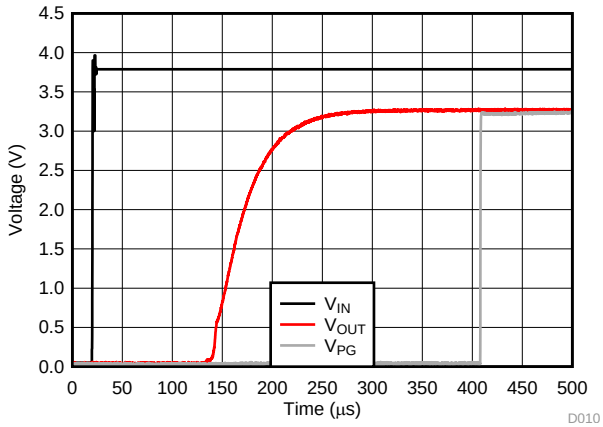


Figure 10. LP5912-3.3 Power Up

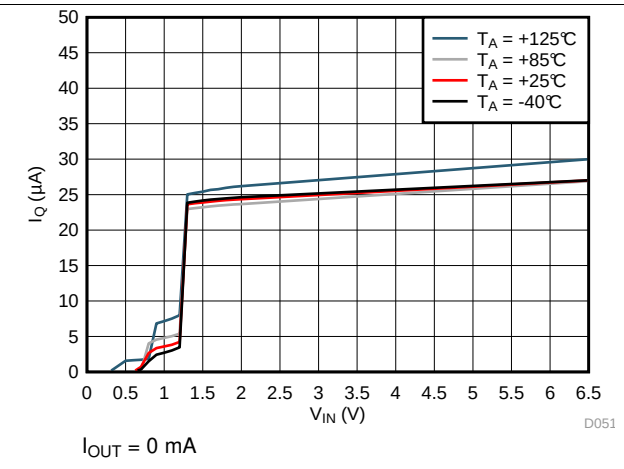


Figure 11. LP5912-0.9 I_Q (No Load) vs V_{IN}

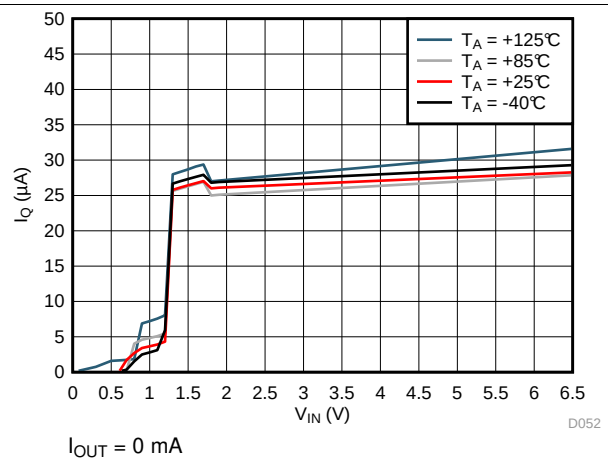
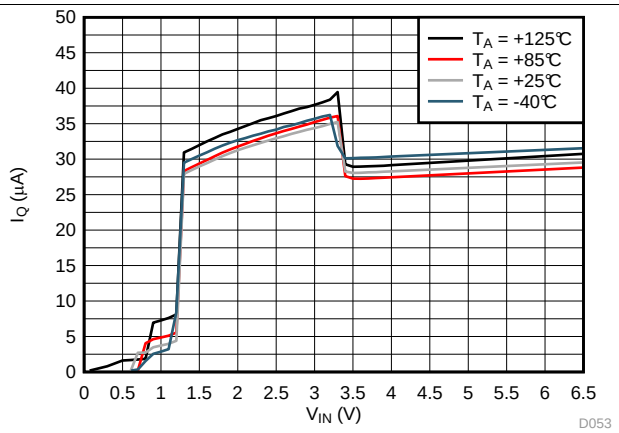


Figure 12. LP5912-1.8 I_Q (No Load) vs V_{IN}

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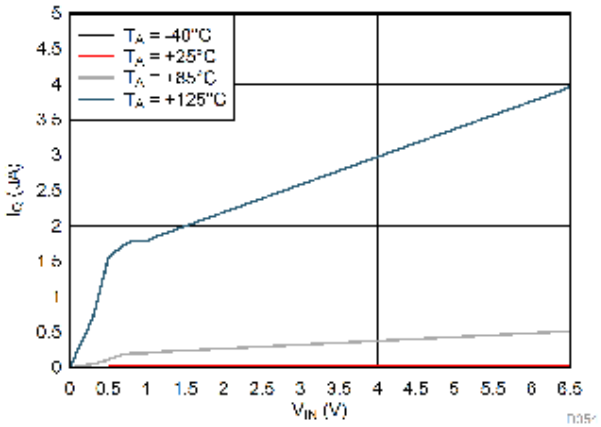
Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C, unless otherwise stated.



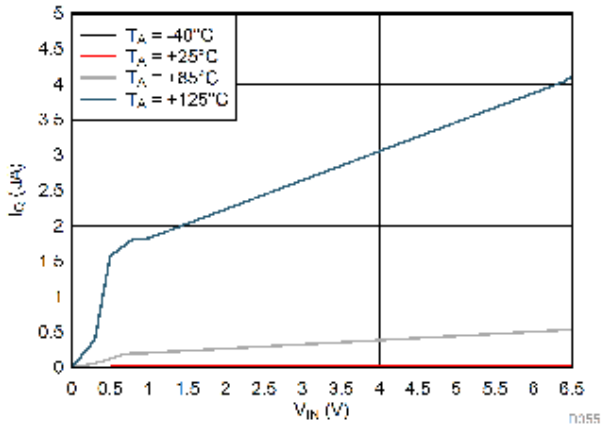
I_{OUT} = 0 mA

Figure 13. LP5912-3.3 I_Q (No Load) vs V_{IN}



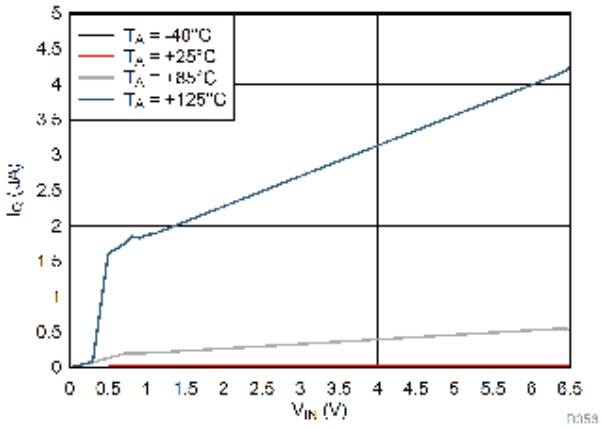
V_{EN} = 0 V

Figure 14. LP5912-0.9 $I_{Q(SD)}$ vs V_{IN}



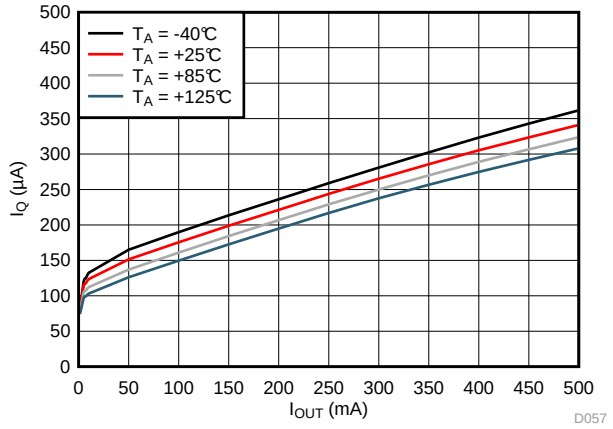
V_{EN} = 0 V

Figure 15. LP5912-1.8 $I_{Q(SD)}$ vs V_{IN}



V_{EN} = 0 V

Figure 16. LP5912-3.3 $I_{Q(SD)}$ vs V_{IN}



V_{IN} = 1.6 V

Figure 17. LP5912-0.9 I_{GND} vs I_{OUT}

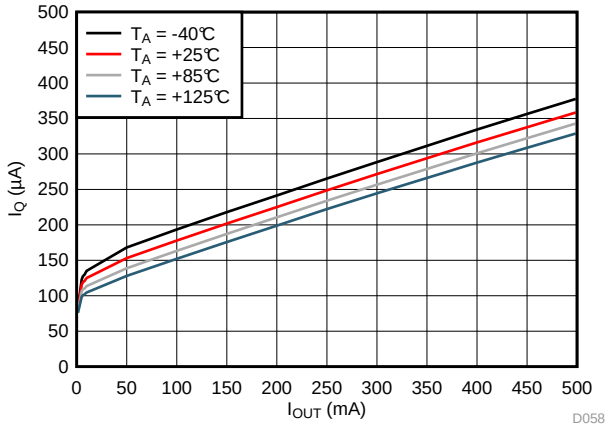


Figure 18. LP5912-1.8 I_{GND} vs I_{OUT}

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Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C, unless otherwise stated.

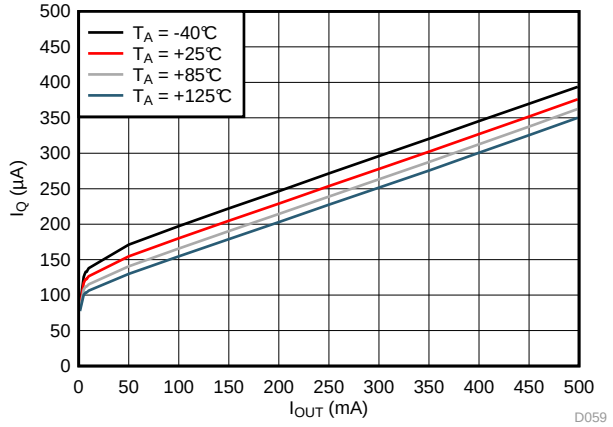


Figure 19. LP5912-3.3 I_{GND} vs I_{OUT}

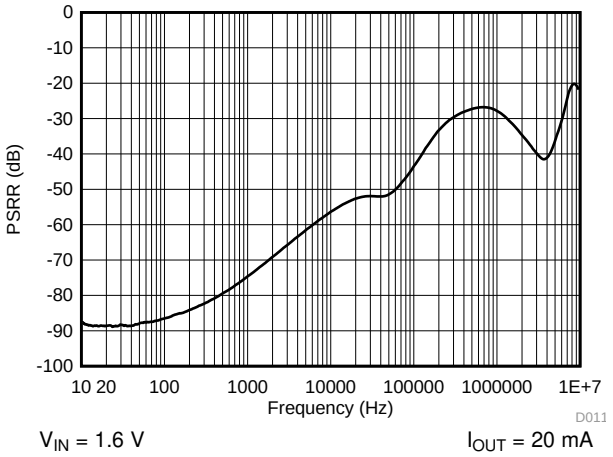


Figure 20. LP5912-0.9 PSRR vs Frequency

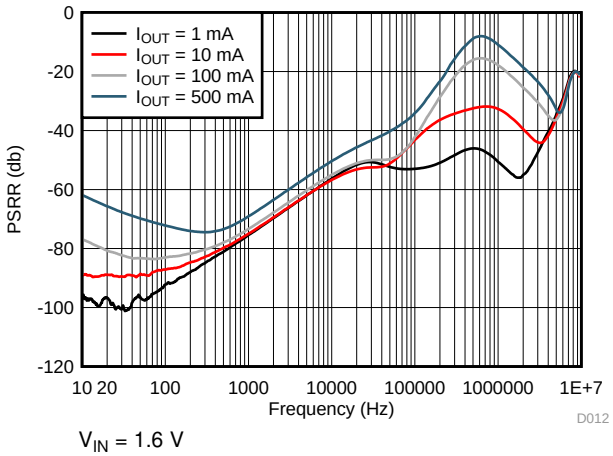


Figure 21. LP5912-0.9 PSRR vs Frequency

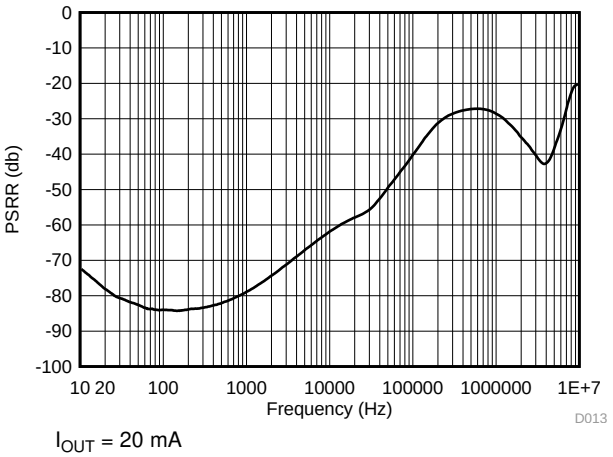


Figure 22. LP5912-1.8 PSRR vs Frequency

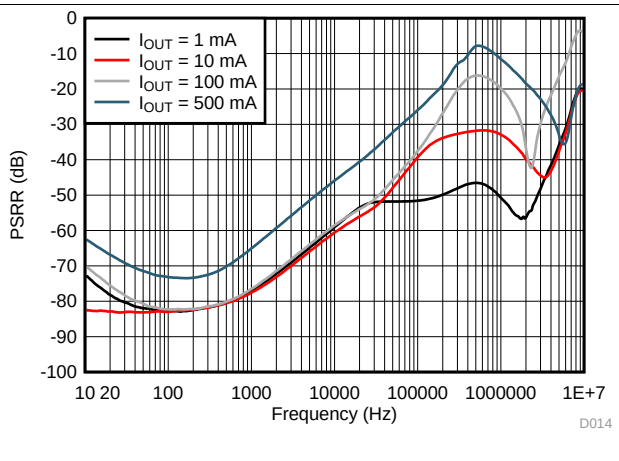


Figure 23. LP5912-1.8 PSRR vs Frequency

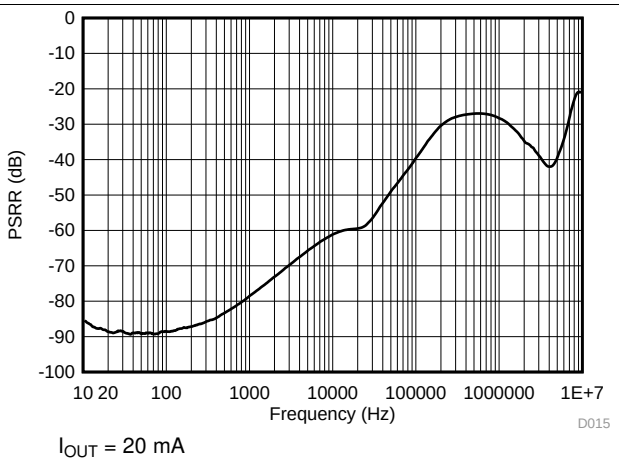


Figure 24. LP5912-3.3 PSRR vs Frequency

Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C, unless otherwise stated.

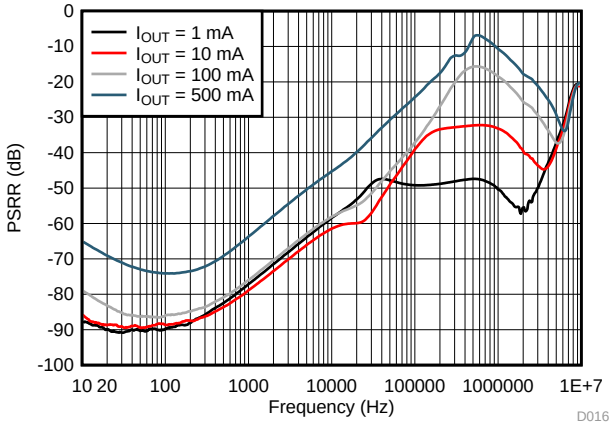


Figure 25. LP5912-3.3 PSRR vs Frequency

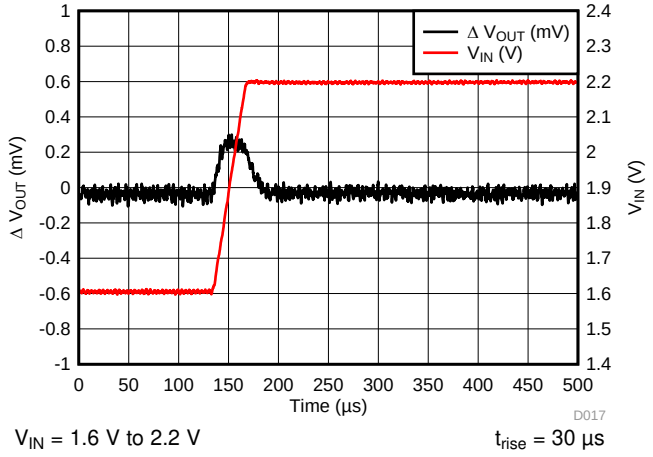


Figure 26. LP5912-0.9 Line Transient

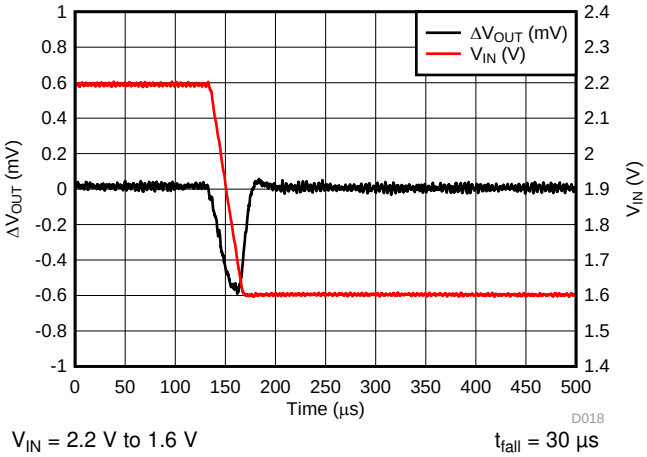


Figure 27. LP5912-0.9 Line Transient

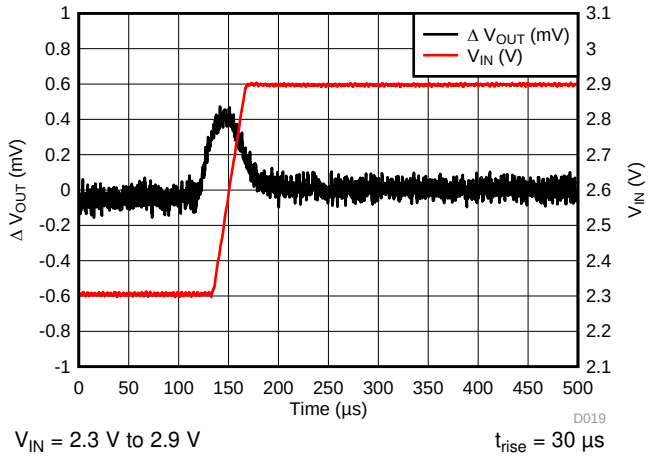


Figure 28. LP5912-1.8 Line Transient

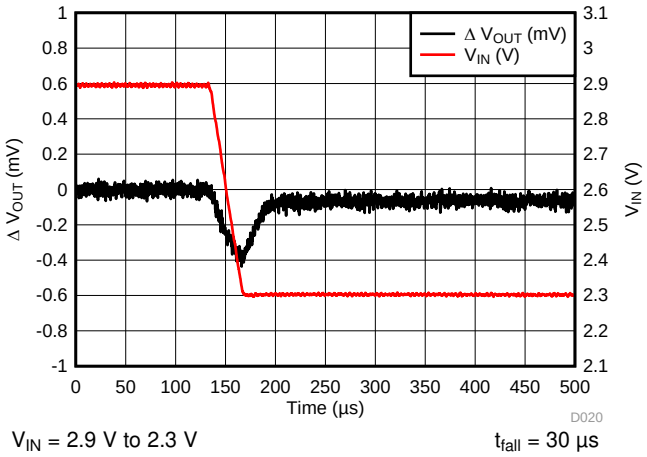


Figure 29. LP5912-1.8 Line Transient

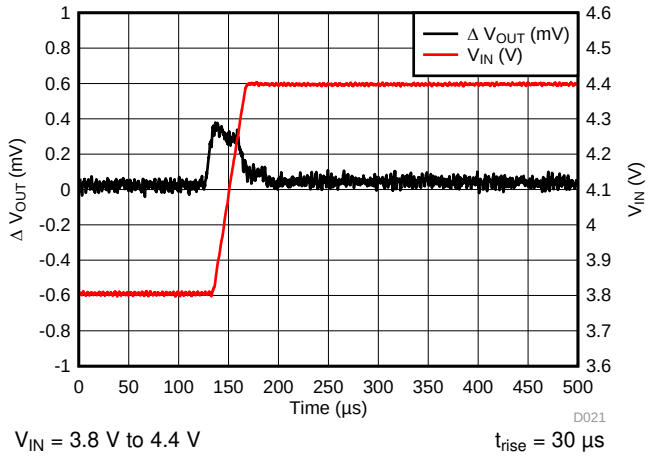
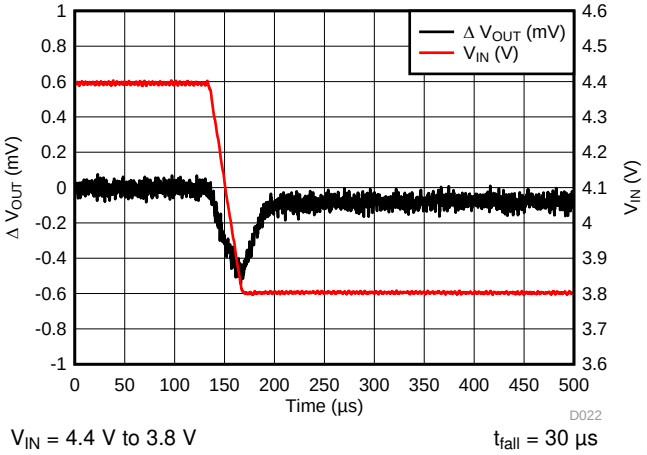


Figure 30. LP5912-3.3 Line Transient

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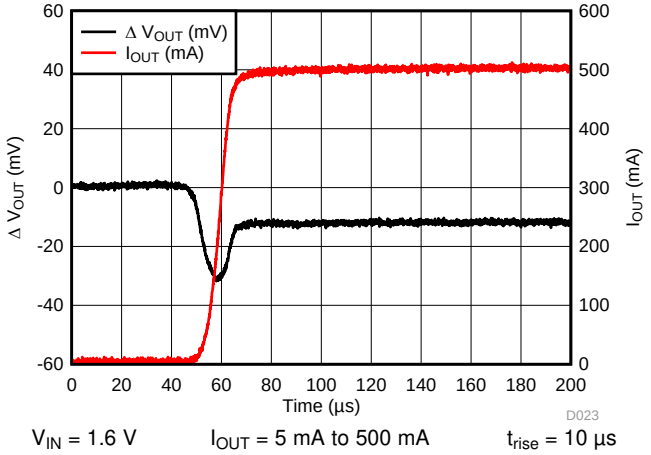
Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = V_{OUT} + 0.5$ V, $V_{EN} = V_{IN}$, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, $T_J = 25°C$, unless otherwise stated.



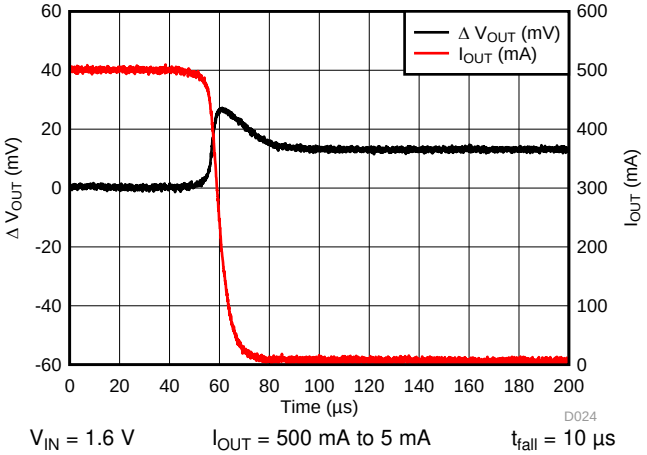
V_{IN} = 4.4 V to 3.8 V t_{fall} = 30 µs

Figure 31. LP5912-3.3 Line Transient



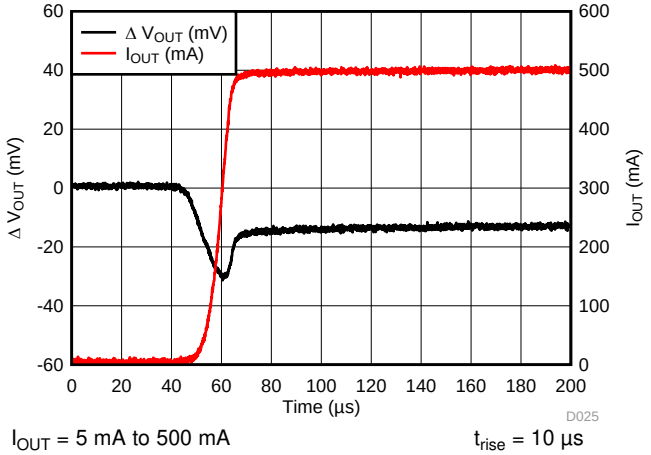
V_{IN} = 1.6 V I_{OUT} = 5 mA to 500 mA t_{rise} = 10 µs

Figure 32. LP5912-0.9 Load Transient Response



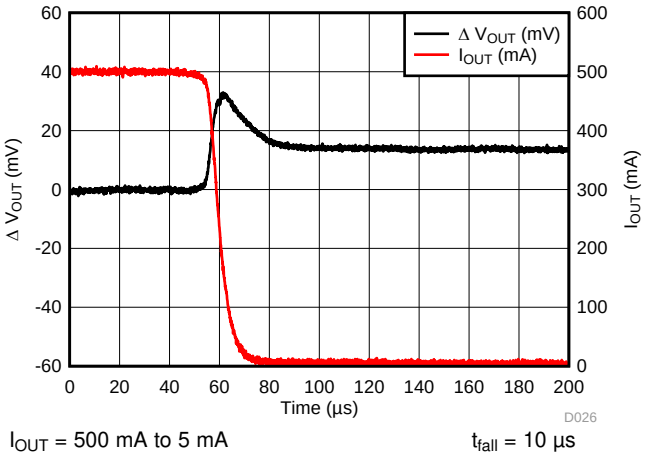
V_{IN} = 1.6 V I_{OUT} = 500 mA to 5 mA t_{fall} = 10 µs

Figure 33. LP5912-0.9 Load Transient Response



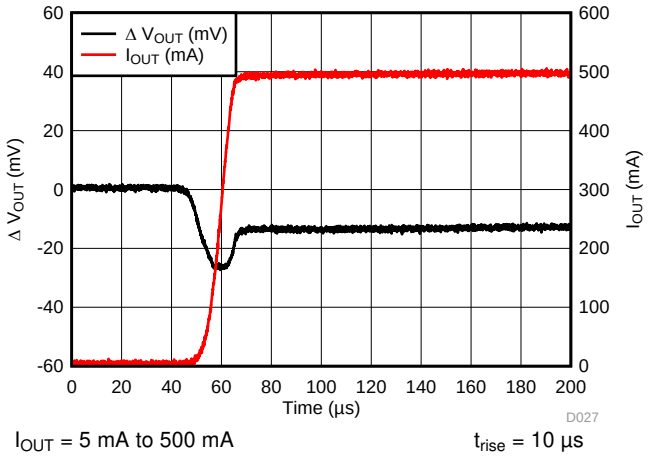
I_{OUT} = 5 mA to 500 mA t_{rise} = 10 µs

Figure 34. LP5912-1.8 Load Transient Response



I_{OUT} = 500 mA to 5 mA t_{fall} = 10 µs

Figure 35. LP5912-1.8 Load Transient Response



I_{OUT} = 5 mA to 500 mA t_{rise} = 10 µs

Figure 36. LP5912-3.3 Load Transient Response

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Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = V_{OUT} + 0.5$ V, $V_{EN} = V_{IN}$, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, $T_J = 25°C$, unless otherwise stated.

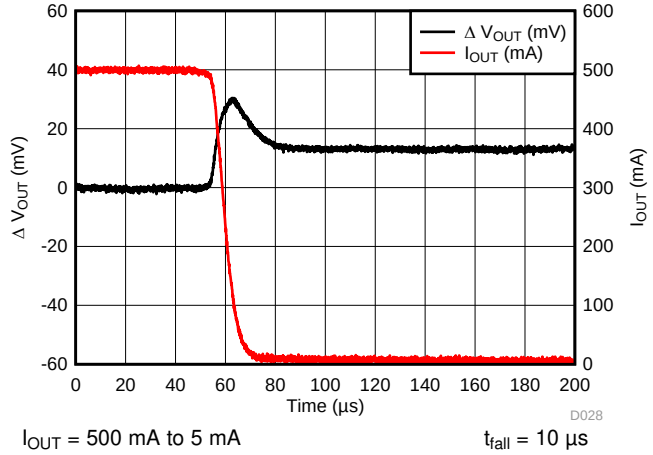


Figure 37. LP5912-3.3 Load Transient Response

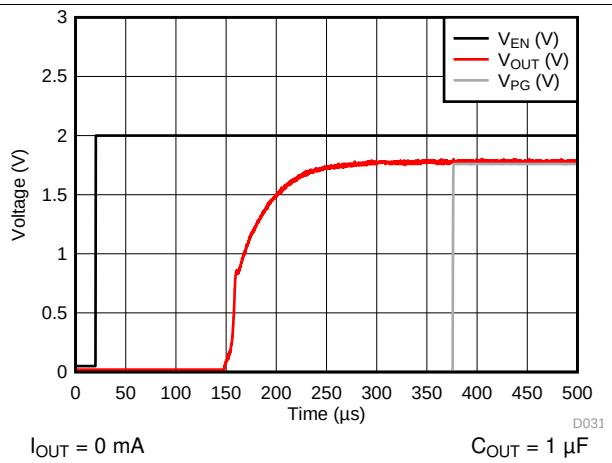


Figure 38. LP5912-1.8 V_{OUT} vs $V_{EN(ON)}$

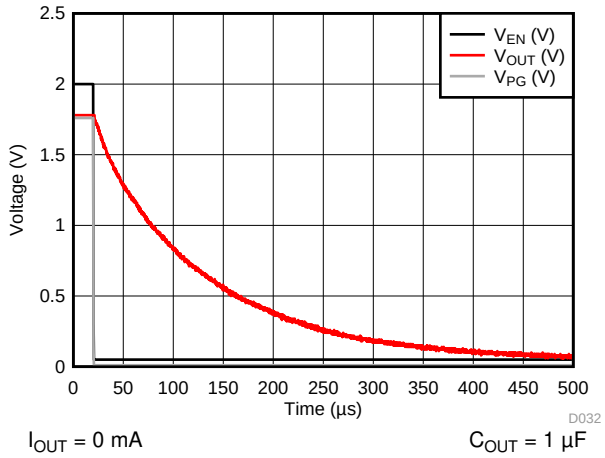


Figure 39. LP5912-1.8 V_{OUT} vs $V_{EN(OFF)}$

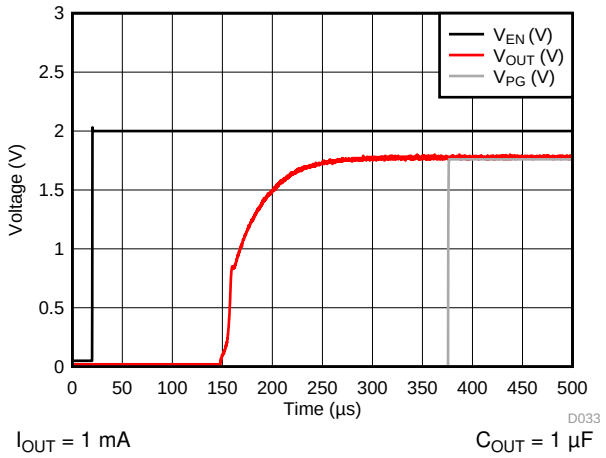


Figure 40. LP5912-1.8 V_{OUT} vs $V_{EN(ON)}$

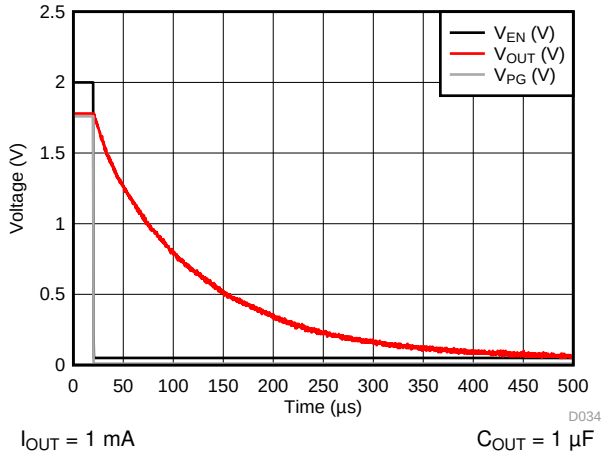


Figure 41. LP5912-1.8 V_{OUT} vs $V_{EN(OFF)}$

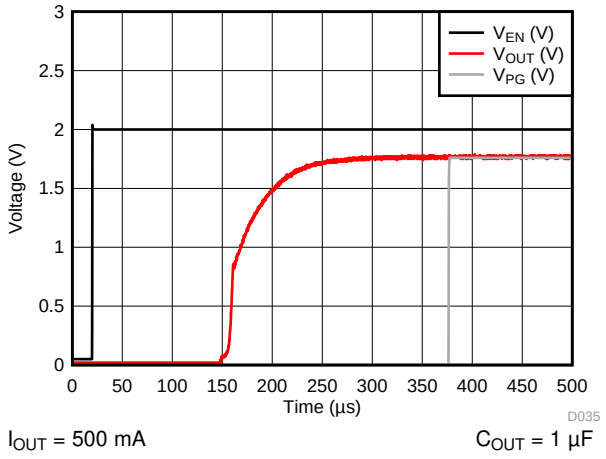


Figure 42. LP5912-1.8 V_{OUT} vs $V_{EN(ON)}$

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Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C, unless otherwise stated.

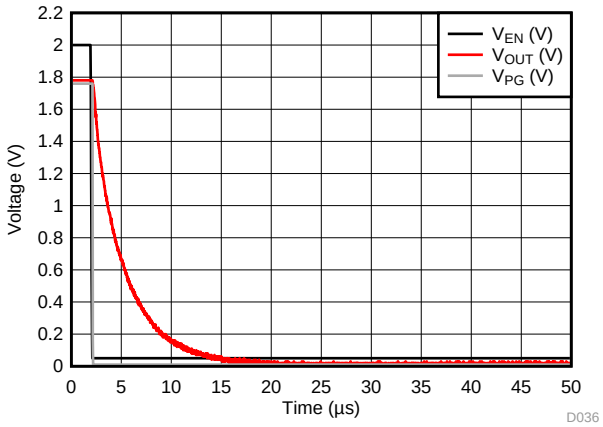


Figure 43. LP5912-1.8 V_{OUT} vs $V_{EN(OFF)}$

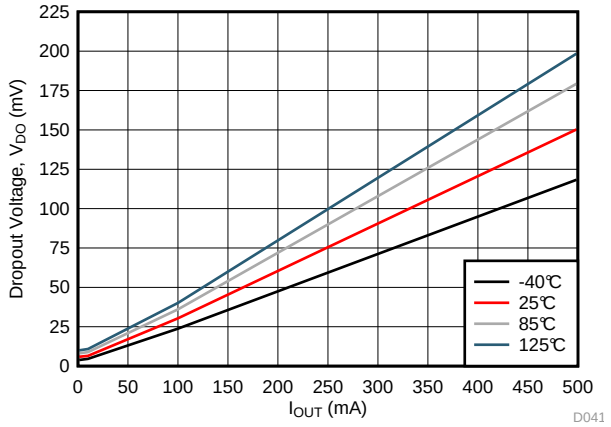


Figure 44. LP5912-1.8 Dropout Voltage (V_{DO}) vs I_{OUT}

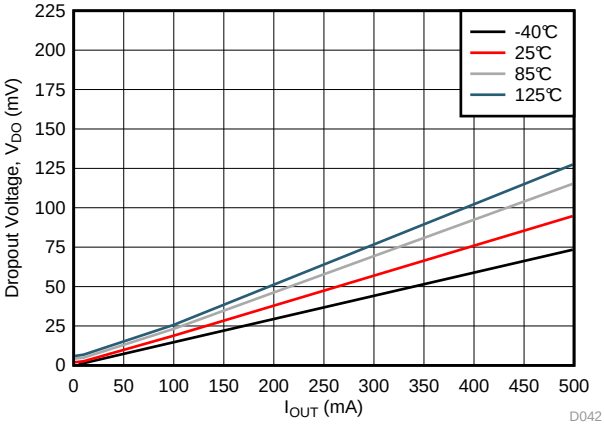


Figure 45. LP5912-3.3 Dropout Voltage (V_{DO}) vs I_{OUT}

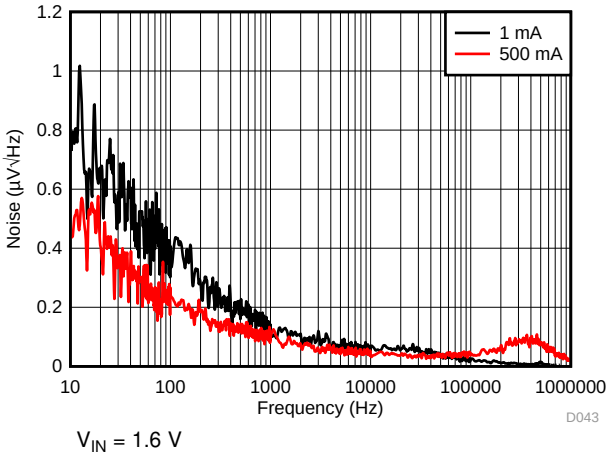


Figure 46. LP5912-0.9 Noise vs Frequency

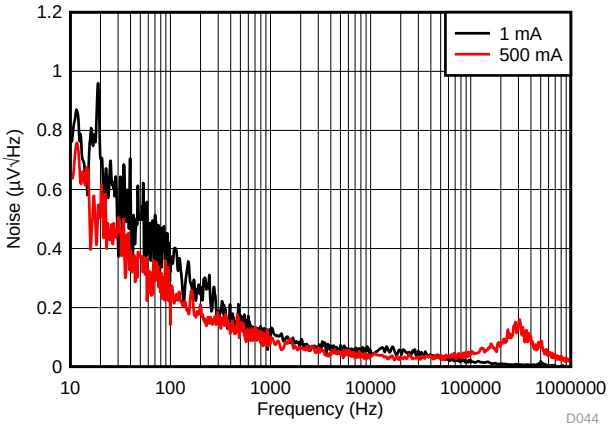


Figure 47. LP5912-1.8 Noise vs Frequency

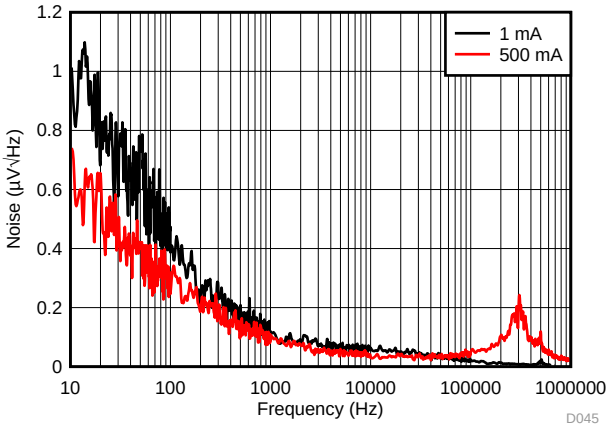


Figure 48. LP5912-3.3 Noise vs Frequency

Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = V_{OUT} + 0.5$ V, $V_{EN} = V_{IN}$, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, $T_J = 25°C$, unless otherwise stated.

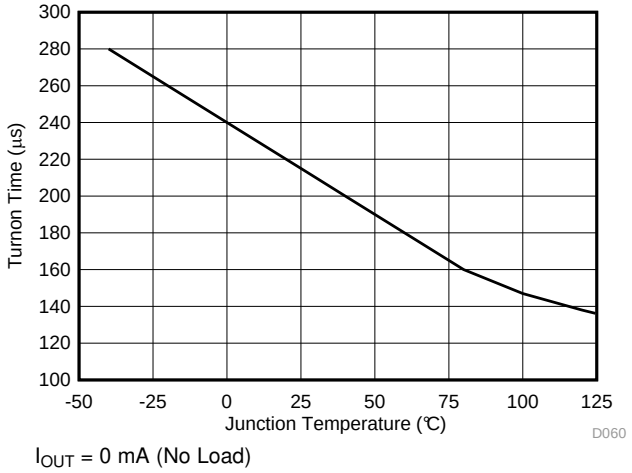


Figure 49. LP5912-3.3 Turnon Time vs Junction Temperature

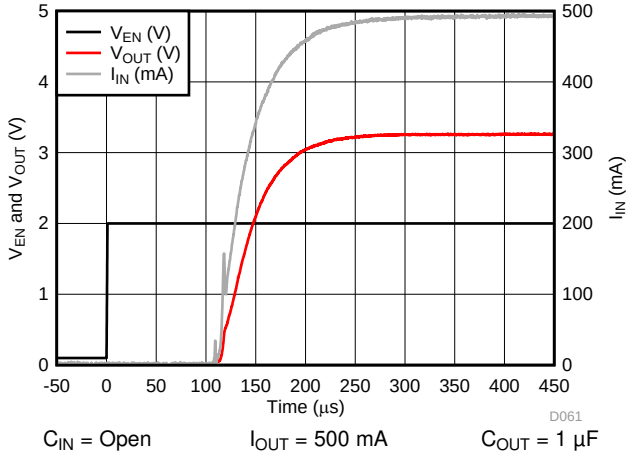


Figure 50. LP5912-3.3 In-Rush Current

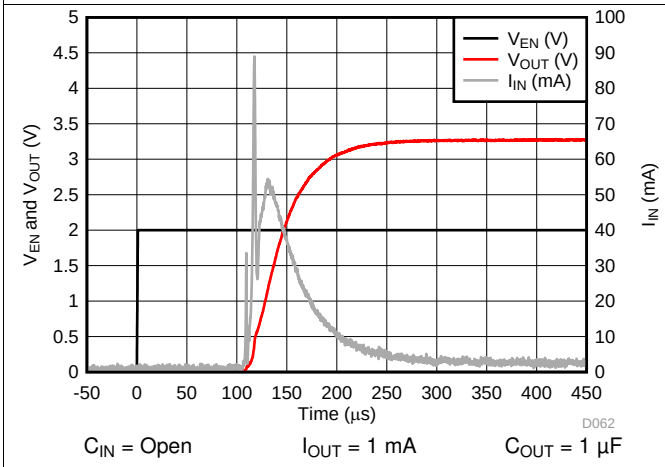


Figure 51. LP5912-3.3 In-Rush Current

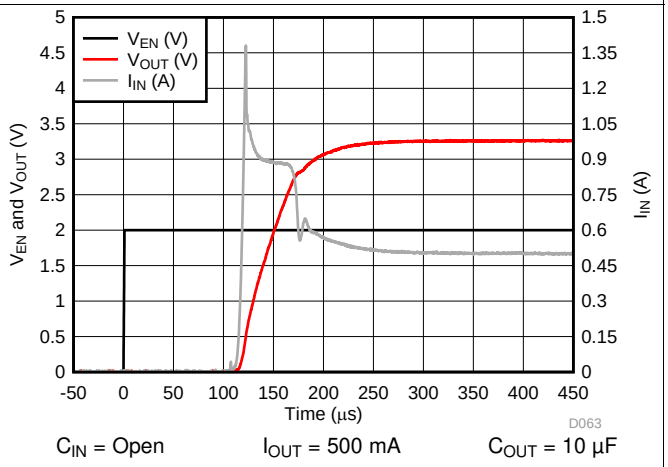


Figure 52. LP5912-3.3 In-Rush Current

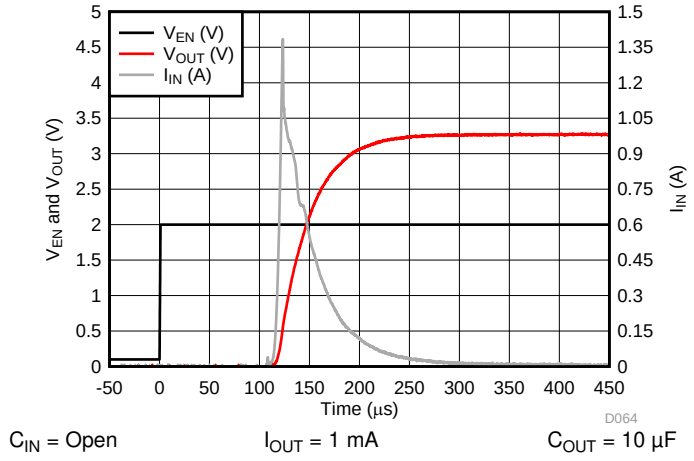


Figure 53. LP5912-3.3 In-Rush Current

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8 Detailed Description

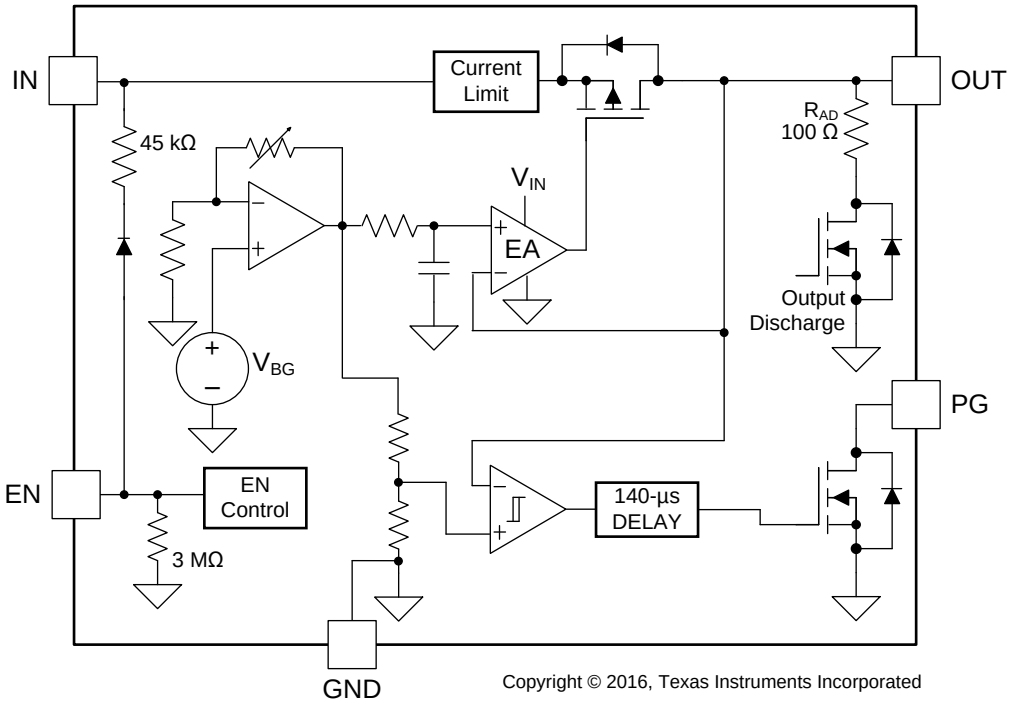
8.1 Overview

The LP5912-Q1 is a low-noise, high PSRR, LDO capable of sourcing a 500-mA load. The LP5912-Q1 can operate down to 1.6-V input voltage and 0.8-V output voltage. This combination of low noise, high PSRR, and low output voltage makes the device an ideal low dropout (LDO) regulator to power a multitude of loads from noise-sensitive communication components to battery-powered system.

The LP5912-Q1 *Functional Block Diagram* contains several features, including:

- Internal output resistor divider feedback;
- Small size and low-noise internal protection circuit current limit;
- Reverse current protection;
- Current limit and in-rush current protection;
- Thermal shutdown;
- Output auto discharge for fast turnoff; and
- Power-good output, with fixed 140-µs typical delay.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Enable (EN)

The LP5912-Q1 EN pin is internally held low by a 3-MΩ resistor to GND. The EN pin voltage must be higher than the $V_{EN(ON)}$ threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the $V_{EN(OFF)}$ threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

When the device is disabled the output stage is disabled, the PG output pin is low, and the output automatic discharge is ON.

Feature Description (continued)

8.3.2 Output Automatic Discharge (R_{AD})

The LP5912-Q1 output employs an internal 100-Ω (typical) pulldown resistance to discharge the output when the EN pin is low. Note that if the LP5912-Q1 EN pin is low (the device is OFF) and the OUT pin is held high by a secondary supply, current flows from the secondary supply through the automatic discharge pulldown resistor to ground.

8.3.3 Reverse Current Protection (I_{RO})

The LP5912-Q1 input is protected against reverse current when output voltage is higher than the input. In the event that extra output capacitance is used at the output, a power-down transient at the input would normally cause a large reverse current through a conventional regulator. The LP5912-Q1 includes a reverse voltage detector that trips when V_{IN} drops below V_{OUT}, shutting off the regulator and opening the PMOS body diode connection, preventing any reverse current from the OUT pin from flowing to the IN pin.

If the LP5912 EN pin is low (the LP5912 is OFF) and the OUT pin is held high by a secondary supply, current flows from the secondary supply through the automatic discharge pulldown resistor to ground. This is not reverse current, this is automatic discharge pulldown current.

Note that reverse current (I_{RO}) is measured at the IN pin.

8.3.4 Internal Current Limit (I_{SC})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate continuously at the I_{SC} current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

8.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

8.3.6 Power-Good Output (PG)

The LP5912-Q1 device has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages (low impedance to GND). When the output voltage rises above the PG threshold voltage (PGV_{HTH}), the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Use a pullup resistor from 10 kΩ to 100 kΩ for best results.

The input supply, V_{IN}, must be no less than the minimum operating voltage of 1.6 V to ensure that the PG pin output status is valid. The PG pin output status is undefined when V_{IN} is less than 1.6 V.

In power-good function, the PG output pin being pulled high is typically delayed 140 µs after the output voltage rises above the PG_{HTH} threshold voltage. If the output voltage rises above the PG_{HTH} threshold and then falls below the PG_{LTH} threshold voltage the PG pin falls immediately with no delay time.

If the PG function is not needed, the pullup resistor can be eliminated, and the PG pin can be either connected to ground or left floating.

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8.4 Device Functional Modes

8.4.1 Enable (EN)

The LP5912-Q1 EN pin is internally held low by a 3-MΩ resistor to GND. The EN pin voltage must be higher than the $V_{EN(ON)}$ threshold to ensure that the device is fully enabled under all operating conditions. When the EN pin voltage is lower than the $V_{EN(OFF)}$ threshold, the output stage is disabled, the PG pin goes low, and the output automatic discharge circuit is activated. Any charge on the OUT pin is discharged to ground through the internal 100-Ω (typical) output auto discharge pulldown resistance.

8.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5912-Q1 device does not include any dedicated UVLO circuit. The device internal circuit is not fully functional until V_{IN} is at least 1.6 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 1.6 V or (V_{OUT} + V_{DO}).

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9 Applications and Implementation

NOTE

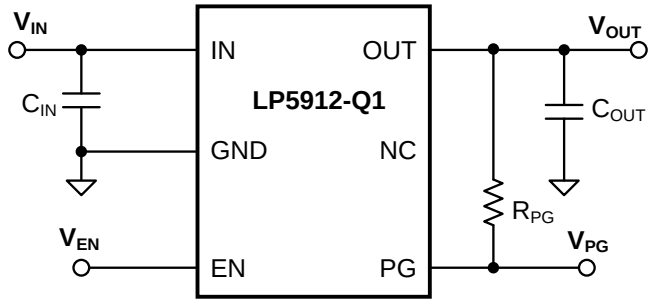
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP5912-Q1 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The device delivers this performance in an industry standard WSON package, which for this device is specified with an operating junction temperature (T_J) of –40°C to +125°C.

9.2 Typical Application

Figure 54 shows the typical application circuit for the LP5912-Q1. Input and output capacitances may need to be increased above the 1-µF minimum for some applications.



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Figure 54. LP5912-Q1 Typical Application

9.2.1 Design Requirements

For typical RF linear regulator applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	1.6 to 6.5 V
Output voltage	0.8 to 5.5 V
Output current	500 mA
Output capacitor	1 to 10 µF
Input/output capacitor ESR range	5 mΩ to 500 mΩ

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9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitors

Like most low-dropout regulators, the LP5912-Q1 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.2 Input Capacitor

An input capacitor is required for stability. The input capacitor must be at least equal to, or greater than, the output capacitor for good load-transient performance. A capacitor of at least 1 µF must be connected between the LP5912-Q1 IN pin and ground for stable operation over full load-current range. It is acceptable to have more output capacitance than input, as long as the input is at least 1 µF.

The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5912-Q1, increasing the value of the input capacitor to at least 10 µF is recommended. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (such as a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains 1 µF ±30% over the entire operating temperature range.

9.2.2.3 Output Capacitor

The LP5912-Q1 is designed specifically to work with a very small ceramic output capacitor, typically 1 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 1-µF to 10-µF range, and with an ESR from 5 mΩ to 500 mΩ, is suitable in the LP5912-Q1 application circuit. For this device the output capacitor must be connected between the OUT pin with a good connection back to the GND pin.

Tantalum or film capacitors may also be used at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

9.2.2.4 Capacitor Characteristics

The LP5912-Q1 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5912-Q1.

The preferred choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 10-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. While it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. Also, the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

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9.2.2.5 Remote Capacitor Operation

To ensure stability the LP5912-Q1 requires at least a 1-μF capacitor at the OUT pin. There is no strict requirement about the location of the output capacitor in regards to the LDO OUT pin; the output capacitor may be located 5 to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the OUT pin if there are already respective capacitors in the system. This placement flexibility requires that the output capacitor be connected directly between the LP5912-Q1 OUT pin and GND pin with no vias. This remote capacitor feature can help users to minimize the number of capacitors in the system.

As a good design practice, keep the wiring parasitic inductance at a minimum, which means using as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close to ground layer as possible, avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. Keeping parasitic wiring inductance less than 35 nH is recommended. For applications with fast load transients use an input capacitor equal to, or larger than, the sum of the capacitance at the output node for the best load-transient performance.

9.2.2.6 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that is greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (DRV) package, the primary conduction path for heat is through the exposed power pad into the PCB. To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 2:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_D = T_{J(MAX)} - T_{A(MAX)} / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

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9.2.2.7 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)}) \quad (4)$$

where

- $P_{D(MAX)}$ is explained in Equation 3
- T_{TOP} is the temperature measured at the center-top of the device package.

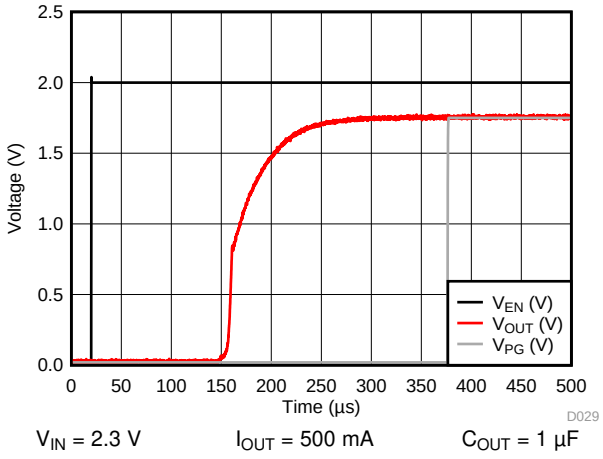
$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)}) \quad (5)$$

where

- $P_{D(MAX)}$ is explained in Equation 3.
- T_{BOARD} is the PCB surface temperature measured 1 mm from the device package and centered on the package edge.

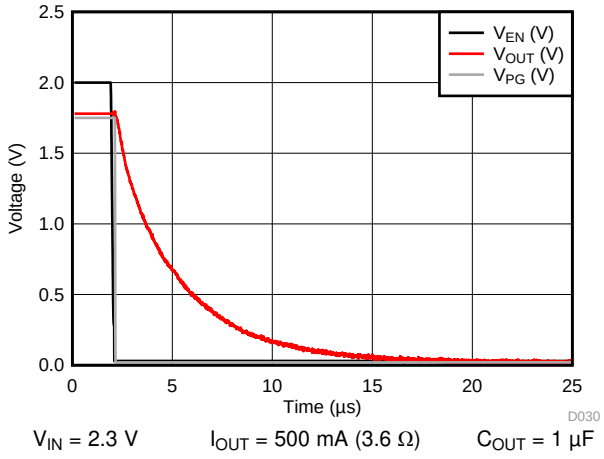
For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics* ; for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics* ; and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*. These application notes are available at www.ti.com.

9.2.3 Application Curves



V_{IN} = 2.3 V I_{OUT} = 500 mA C_{OUT} = 1 µF

Figure 55. LP5912-1.8 V_{OUT} vs V_{EN} (ON)



V_{IN} = 2.3 V I_{OUT} = 500 mA (3.6 Ω) C_{OUT} = 1 µF

Figure 56. LP5912-1.8 V_{OUT} vs V_{EN} (OFF)

10 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5912-Q1 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 0.5 V. A minimum capacitor value of 1 µF is required to be within 1 cm of the IN pin.

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11 Layout

11.1 Layout Guidelines

The dynamic performance of the LP5912-Q1 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5912-Q1.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5912-Q1, and as close to the package as is practical. The ground connections for C_{IN} and C_{OUT} must be back to the LP5912-Q1 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. Such connections add parasitic inductances and resistance that result in inferior performance especially during transient conditions.

11.2 Layout Example

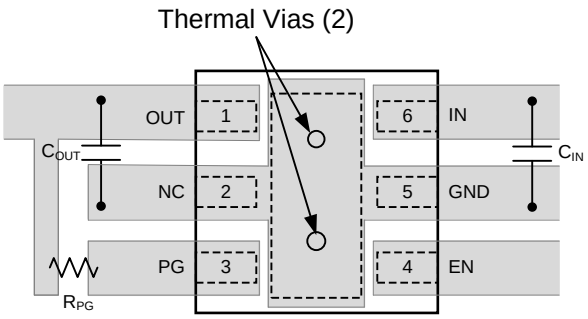


Figure 57. LP5912-Q1 Typical Layout

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12 Device and Documentation Support

12.1 Related Documentation

For additional information, see the following:

- *AN1187 Leadless Leadframe Package (LLP)*
- *Semiconductor and IC Package Thermal Metrics*
- *Using New Thermal Metrics*
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5912Q0.9DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QA
LP5912Q0.9DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QA
LP5912Q0.9DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QA
LP5912Q0.9DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QA
LP5912Q1.1DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QH
LP5912Q1.1DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QH
LP5912Q1.1DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QH
LP5912Q1.1DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QH
LP5912Q1.2DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QB
LP5912Q1.2DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QB
LP5912Q1.2DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QB
LP5912Q1.2DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QB
LP5912Q1.5DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QC
LP5912Q1.5DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QC
LP5912Q1.5DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QC
LP5912Q1.5DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QC
LP5912Q1.8DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QD
LP5912Q1.8DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QD
LP5912Q1.8DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QD
LP5912Q1.8DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QD
LP5912Q2.8DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QE
LP5912Q2.8DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QE
LP5912Q2.8DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QE
LP5912Q2.8DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QE
LP5912Q3.0DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QG
LP5912Q3.0DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QG
LP5912Q3.0DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QG
LP5912Q3.0DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QG
LP5912Q3.3DRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QF

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5912Q3.3DRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QF
LP5912Q3.3DRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12QF
LP5912Q3.3DRVTQ1	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	12QF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP5912-Q1 :

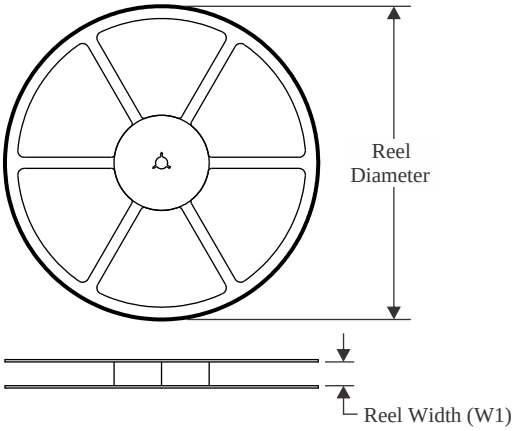
- Catalog : LP5912
- Enhanced Product : LP5912-EP

NOTE: Qualified Version Definitions:

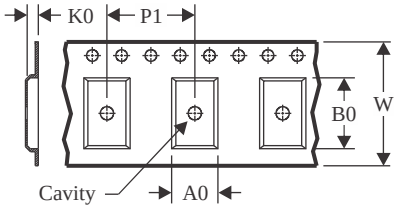
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

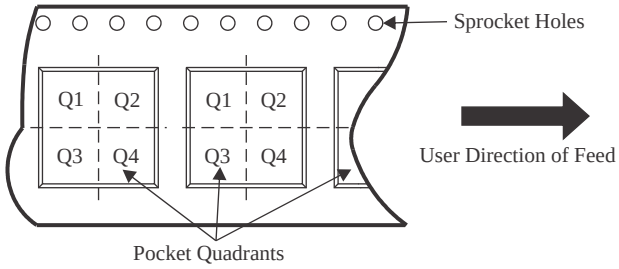


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

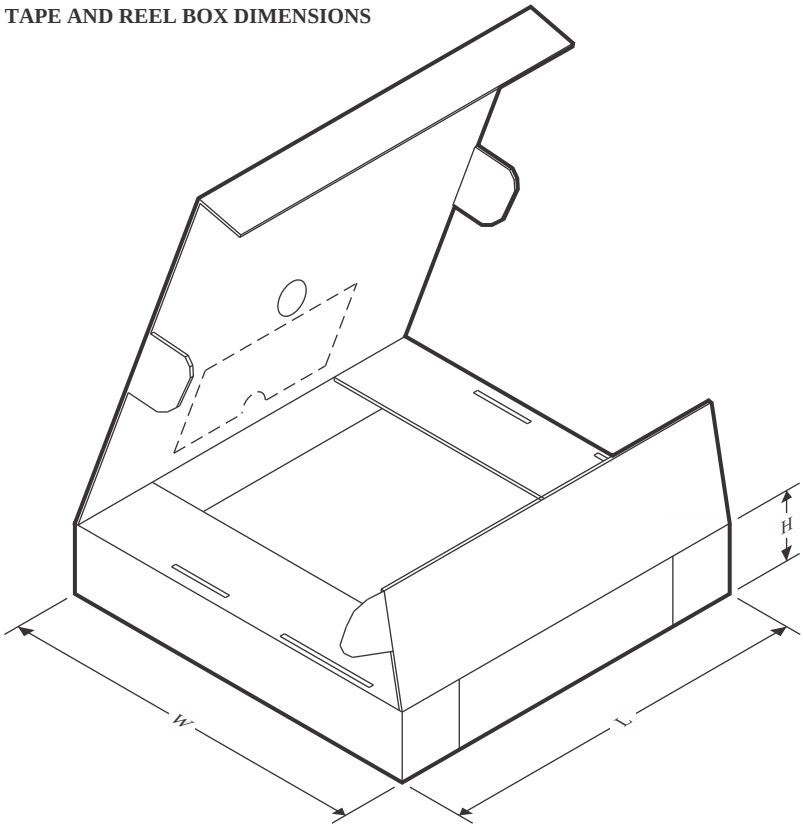
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5912Q0.9DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q0.9DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.1DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.1DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.2DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.2DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.5DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.5DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.8DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q1.8DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q2.8DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q2.8DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.0DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.0DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.3DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5912Q3.3DRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



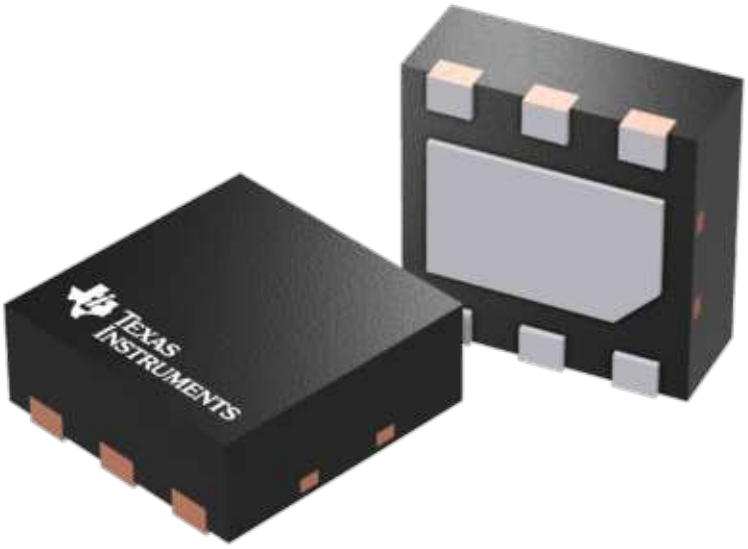
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5912Q0.9DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q0.9DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.1DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.1DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q1.2DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.2DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q1.5DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.5DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q1.8DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q1.8DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q2.8DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q2.8DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q3.0DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q3.0DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
LP5912Q3.3DRVRQ1	WSON	DRV	6	3000	182.0	182.0	20.0
LP5912Q3.3DRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

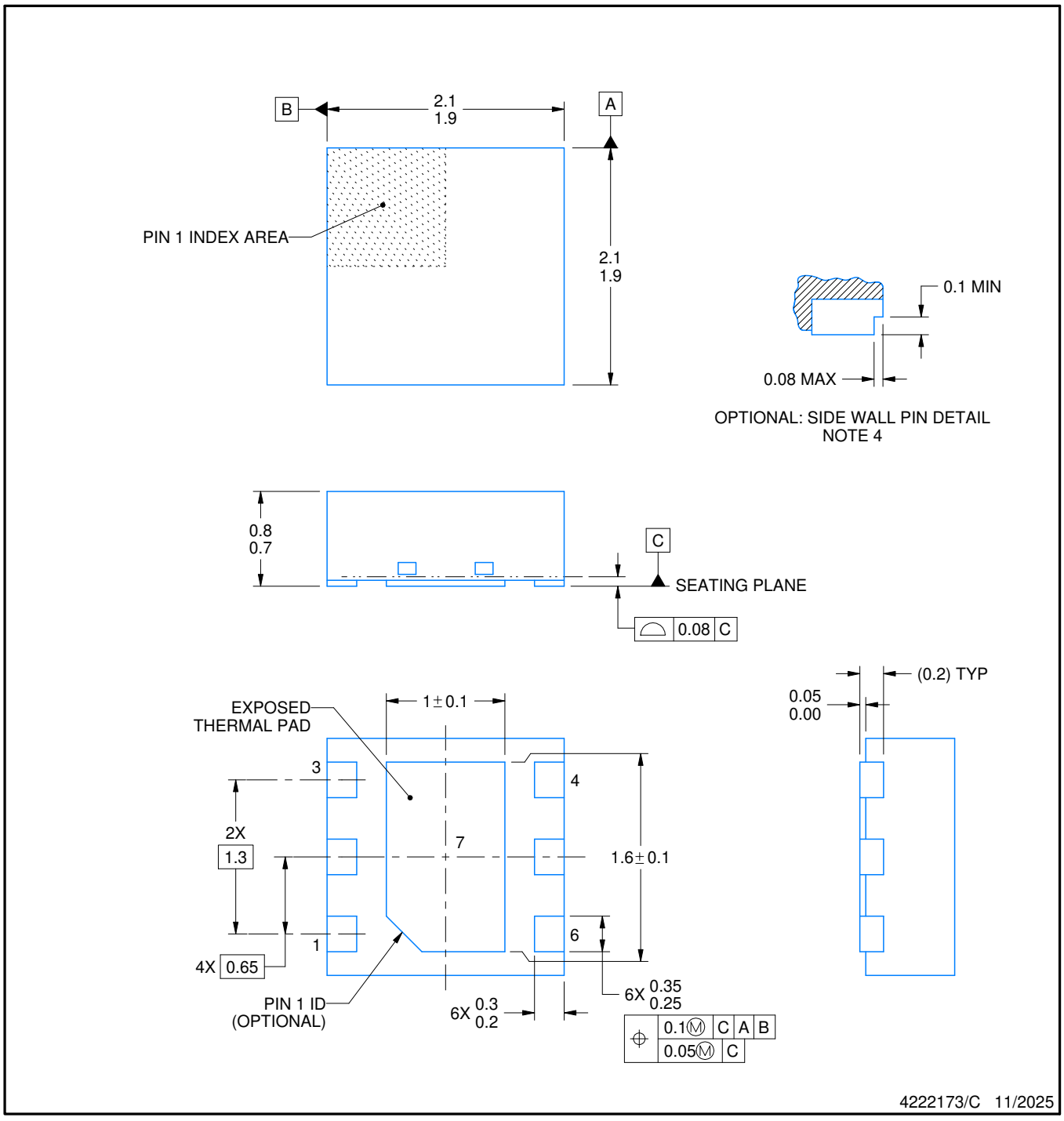
DRV0006A



PACKAGE OUTLINE

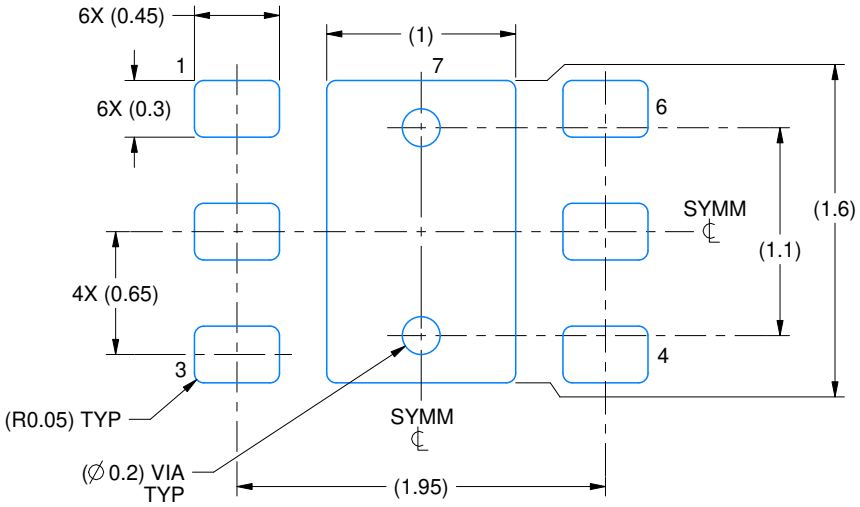
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

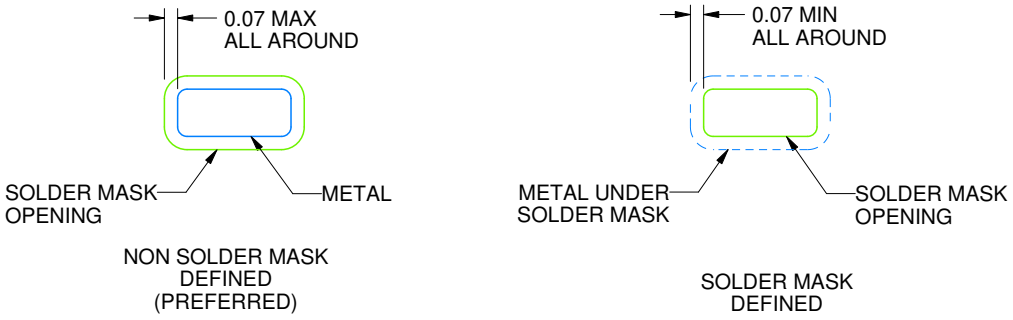


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

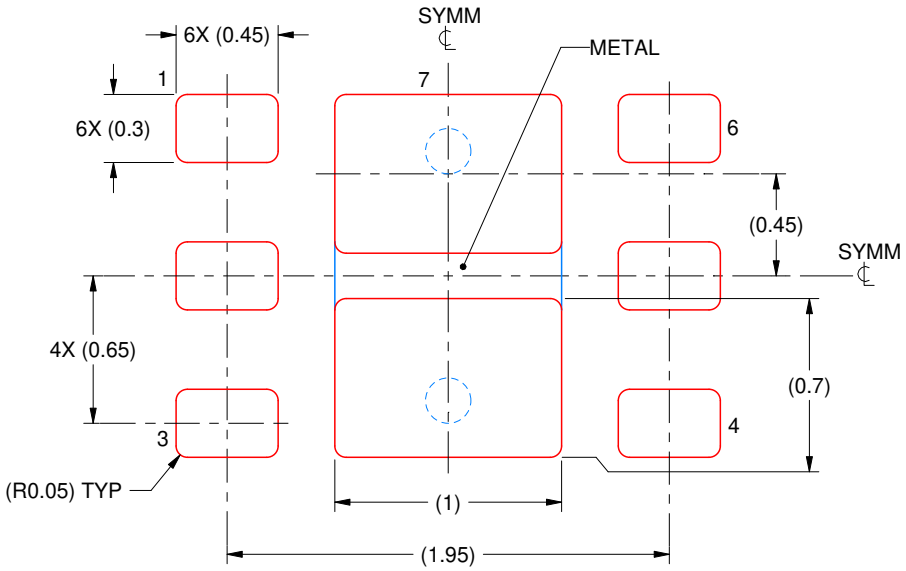


SOLDER MASK DETAILS

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NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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