LSF0204x 4-Bits Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Application

1 Features

- Provides bidirectional voltage translation with no direction terminal
- Supports up to 100-MHz up translation and greater than 100-MHz down translation at ≤ 30-pF capacitor load and up to 40-MHz up/down translation at 50-pF capacitor load
- Supports I_{off}, partial power-down mode (refer to *Feature Description*)
- Allows bidirectional voltage level translation between
  - 0.8 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.2 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.8 V ↔ 2.5, 3.3, 5 V
  - 2.5 V ↔ 3.3, 5 V
  - 3.3 V ↔ 5 V
- Low standby current
- 5 V Tolerance I/O port to support TTL
- Low R_{on} provides less signal distortion
- High-impedance I/O terminals for EN = Low
- Flow-through pinout for easy PCB trace routing
- Latch-up performance exceeds 100 mA per JESD17
- –40°C to 125°C operating temperature range
- ESD performance tested per JESD 22
  - 2000-V human-body model (A114-B, Class II)
  - 200-V machine model (A115-A)
  - 1000-V charged-device model (C101)

2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C, and other interfaces in telecom infrastructure
- Industrial
- Automotive
- Personal computing

3 Description

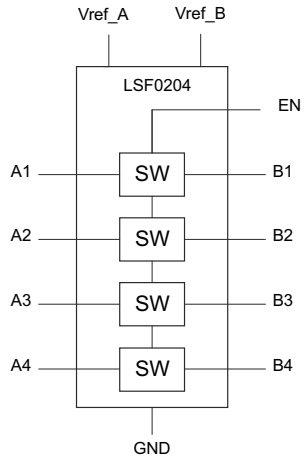
The LSF family consists of bidirectional voltage level translators that operate from 0.8 V to 4.5 V (Vref_A) and 1.8 V to 5.5 V (Vref_B). This range allows for bidirectional voltage translations between 0.8 V and 5.0 V without the need for a direction terminal in open-drain or push-pull applications. The LSF family supports level translation applications with transmission speeds greater than 100 MHz for open-drain systems that utilize a 15-pF capacitance and 165-Ω pull-up resistor.

When the An or Bn port is LOW, the switch is in the ON-state and a low resistance connection exists between the An and Bn ports. The low R_{on} of the switch allows connections to be made with minimal propagation delay and signal distortion. The voltage on the A or B side will be limited to Vref_A and can be pulled up to any level between Vref_A and 5 V. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LSF0204x	TSSOP (14)	5.00 mm × 4.40 mm
	UQFN (12)	2.00 mm × 1.70 mm
	VQFN (14)	3.50 mm × 3.50 mm
	DSBGA (12)	1.90 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (November 2019) to Revision H (April 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Bidirectional Translation* section to include inclusive terminology	14

Changes from Revision F (January 2019) to Revision G (November 2019)	Page
• Changed $V_{ref_A/B/EN}$ max voltage to 5.5 V in the Recommended Operating Conditions table	6

Changes from Revision E (December 2018) to Revision F (January 2019)	Page
• Changed location of YZP-package indicator dot to A3 position.	4
• Added YZP package to *Thermal Information* table	6

Changes from Revision D (December 2015) to Revision E (December 2018)	Page
• Changed location of YZP-package A1-pin indicator dot. View is looking through the device, as in an X-ray.	4

Changes from Revision C (August 2015) to Revision D (December 2015)	Page
• Added Type Column to *Pin Functions* table	4
• Added Junction Temperatures to *Thermal Information* table	6

Changes from Revision B (April 2015) to Revision C (August 2015)	Page
• Removed bullet "Less than 1.5 ns max propagation delay" from Features	1
• Updated "Supports High Speed Translation, Greater Than 100 MHz" bullet in Features	1

Changes from Revision A (December 2014) to Revision B (April 2015)	Page
• Added YZP package to device.	1

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Changes from Revision * (November 2014) to Revision A (December 2014)	Page
• Changed From a first page Product Preview To a full datasheet	1
• Changed text in the *Section 3* From: "transmission speeds greater than 100 Mbps" To: "transmission speeds greater than 100 MHz"	1

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5 Description (continued)

The supply voltage ($V_{pu\#}$) for each channel may be individually set up with a pull up resistor. For example, CH1 may be used in up-translation mode (1.2 V ↔ 3.3 V) and CH2 in down-translation mode (2.5 V ↔ 1.8 V).

When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_A. EN must be LOW to ensure the high-impedance state during power-up or power-down.

Device Comparison Table

PART NUMBER	EN	An	Bn	DESCRIPTION
LSF0204D	H	Place all data pins in 3 state mode (Hi-Z)	Place all data pins in 3 state mode (Hi-Z)	3-state output mode enable (active Low; referenced to Vref_A)
LSF0204D	L	Input or output	Input or output	
LSF0204	H	Input or output	Input or output	3-state output mode enable (active High, referenced to Vref_A)
LSF0204	L	Place all data pins in 3 state mode (Hi-Z)	Place all data pins in 3 state mode (Hi-Z)	

6 Pin Configuration and Functions

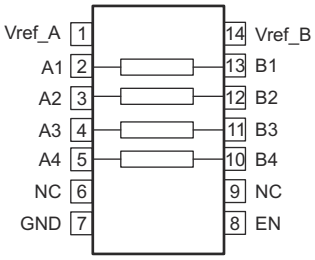


Figure 6-1. PW Package, 14-Pin TSSOP (Top View)

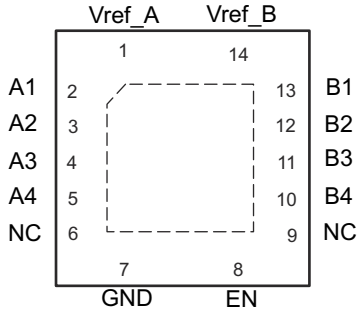


Figure 6-2. RGY Package, 14-Pin VQFN (Transparent Top View)

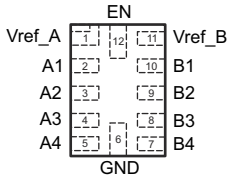


Figure 6-3. RUT Package, 12-Pin UQFN (Transparent Top View)

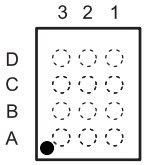


Figure 6-4. YZP Package, 12-Pin DSBGA (Transparent Top View)

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Table 6-1. Pin Functions

PIN				TYPE(1)	DESCRIPTION
NAME	NO.				
	PW, RGY	RUT	YZP		
V_{ref_A}	1	1	B2	—	Reference supply voltage; see Application and Implementation section
A1	2	2	A3	I/O	Input/output 1.
A2	3	3	B3	I/O	Input/output 2.
A3	4	4	C3	I/O	Input/output 3.
A4	5	5	D3	I/O	Input/output 4.
NC	6	–	—	—	No connection. Not internally connected.
GND	7	6	D2	—	Ground
EN	8	12	C2	I	Switch enable input; LSF0204: EN is high-active; LSF0204D: EN is low-active
NC	9	–	—	—	No connection. Not internally connected.
B4	10	7	D1	I/O	Input/output 4.
B3	11	8	C1	I/O	Input/output 3.
B2	12	9	B1	I/O	Input/output 2.
B1	13	10	A1	I/O	Input/output 1.
V_{ref_B}	14	11	A2	—	Reference supply voltage; see Application and Implementation section

(1) I = input, O = output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_I	Input voltage (2)		–0.5	7	V
$V_{I/O}$	Input/output voltage (2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	VI < 0		–50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5.5	V
$V_{ref_A/B/EN}$	Reference voltage	0	5.5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		LSF0204				UNIT
		RGY (VQFN)	RUT (UQFN)	PW (TSSOP)	YZP (DSBGA)	
		14 PINS	12 PINS	14 PINS	12 BALLS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.2	195.8	157.9	83.7	°C
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.2	98.7	82.3	0.6	°C
$R_{\theta JB}$	Junction-to-board thermal resistance	59.2	122.6	100.0	23.7	°C
ψ_{JT}	Junction-to-top characterization parameter	17.4	6.2	22.9	0.4	°C
ψ_{JB}	Junction-to-board characterization parameter	59.4	122.6	99.0	23.7	°C
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	38.7	N/A	N/A	N/A	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		I_I = -18 mA, V_{EN} = 0				–1.2	V
I_{IH}		V_I = 5 V, V_{EN} = 0				5.0	µA
I_{CCBA}	Leakage from Vref_B to Vref_A	V_{ref_B} = 3.3 V, V_{ref_A} = 1.8 V, V_{EN} = V_{ref_A} I_O = 0, V_I = 3.3 V or GND				3.5	µA
I_{CCA} + I_{CCB} (4)	Total Current through GND	V_{ref_B} = 3.3 V, V_{ref_A} = 1.8 V, V_{EN} = V_{ref_A} I_O = 0, V_I = 3.3 V or GND			0.2		µA
I_{IN}	Control pin current	V_{ref_B} = 5.5 V, V_{ref_A} = 4.5 V, V_{EN} = 0 to V_{ref_A} I_O = 0				±1	µA
I_{off}	Power Off Leakage Current	V_{ref_B} = V_{ref_A} = 0 V, V_{EN} = GND I_O = 0, V_I = 5 V or GND				±1	µA
$C_{I(ref_A/B/EN)}$		V_I = 3 V or 0			7		pF
$C_{io(off)}$		V_O = 3 V or 0, VEN = 0			5.0	6.0	pF
$C_{io(on)}$		V_O = 3 V or 0, VEN = Vref_A			10.5	13	pF
(3)V_{IH} (EN pin)	High-level input voltage	V_{ref_A} = 1.5 V to 4.5 V		0.7×Vref_A			V
V_{IL} (EN pin)	Low-level input voltage	V_{ref_A} = 1.5 V to 4.5 V				0.3×Vref_A	V
V_{IH} (EN pin)	High-level input voltage	V_{ref_A}= 1.0 V to 1.5 V		0.8×Vref_A			V
V_{IL} (EN pin)	Low-level input voltage	V_{ref_A} = 1.0 V to 1.5 V				0.3×Vref_A	V
Δt/Δv (EN pin)	Input transition rise or fall rate for EN pin				10		ns/V
r_{on} (2)		V_I = 0, I_O = 64 mA	V_{ref_A} = V_{EN} = 3.3 V; V_{ref_B} = 5 V		3		Ω
			V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 5 V		4		
		V_I = 0, I_O = 32 mA	V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 5 V		9		Ω
			V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 5 V		4		
		V_I = 0, I_O = 32 mA , V_{ref_A} = V_{EN} = 2.5 V; V_{ref_B} = 5 V			10		Ω
		V_I = 1.8 V, I_O = 15 mA, V_{ref_A} = V_{EN} = 3.3 V; V_{ref_B} = 5 V			5		Ω
		V_I = 1.0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 3.3 V			8		Ω
		V_I = 0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 3.3 V			6		Ω
		V_I = 0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 1.8 V			6		Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.
(3) Enable pin test conditions are for the LSF0204. The enable pin test conditions for LSF0204D are oppositely set.
(4) The actual supply current for LSF0204 is I_{CCA} + I_{CCB}; the leakage from Vref_B to Vref_A can be measured on Vref_A and Vref_B pin

7.6 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.8 V)

over recommended operating free-air temperature range, $V_{rev\text{-}A}$ = 1.8 V, $V_{rev\text{-}B}$ = 3.3 V, V_{EN} = 1.8 V, Vpu_1 = 3.3 V, Vpu_2 = 1.8 V, R_L = NA, V_{IH} = 3.3 V, V_{IL} = 0 V_M = 1.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.7	5.49	0.5	5.29	0.3	5.19	ns
t_{PHL}			0.9	4.9	0.7	4.7	0.5	4.5	ns
t_{PLZ}			13	18	12	16.5	11	15	ns
t_{PZL}			33	45	30	40	23	37	ns
f_{MAX}			50		100		100		MHz

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7.7 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.2 V)

over recommended operating free-air temperature range V_{rev-A} = 1.2 V, V_{rev-B} = 3.3 V, V_{EN} = 1.2 V, Vpu_1 = 3.3 V, Vpu_2 = 1.2 V, R_L = NA, V_{IH} = 3.3 V, V_{IL} = 0 V_M = 0.85 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.8	4.1	0.5	3.9	0.3	3.8	ns
t_{PHL}			0.9	4.7	0.7	4.5	0.6	4.3	ns
f_{MAX}			50		100		100		MHz

7.8 Switching Characteristics: AC Performance (Translating Up, 1.8 V to 3.3 V)

over recommended operating free-air temperature range V_{rev-A} = 1.8 V, V_{rev-B} = 3.3 V, V_{EN} = 1.8 V, Vpu_1 = 3.3 V, Vpu_2 = 1.8 V, R_L = 500 Ω, V_{IH} = 1.8 V,V_{IL} = 0 V_M = 0.9 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.6	5.7	0.4	5.3	0.2	5.13	ns
t_{PHL}			1.3	6.7	1	6.4	0.7	5.3	ns
t_{PLZ}			13	18	12	16.5	11	15	ns
t_{PZL}			33	45	30	40	23	37	ns
f_{MAX}			50		100		100		MHz

7.9 Switching Characteristics: AC Performance (Translating Up, 1.2 V to 1.8 V)

over recommended operating free-air temperature range, V_{rev-A} = 1.2 V, V_{rev-B} = 1.8 V, V_{EN} = 1.2 V, Vpu_1 = 1.8 V, Vpu_2 = 1.2 V, R_L = 500 Ω, V_{IH} = 1.2 V, V_{IL} = 0 V_M = 0.6 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	0.65	7.25	0.4	7.05	0.2	6.85	ns
t_{PHL}			1.6	7.03	1.3	6.5	1	5.4	ns
f_{MAX}			50		100		100		MHz

7.10 Typical Characteristics

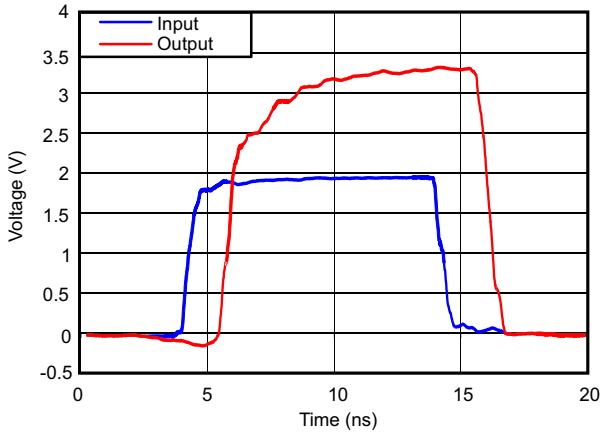
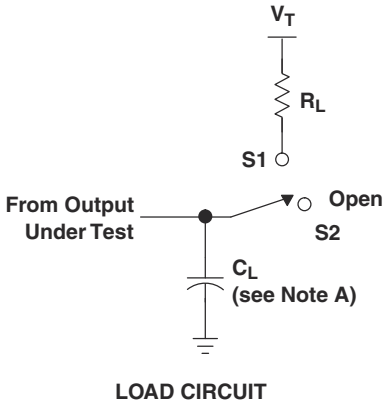


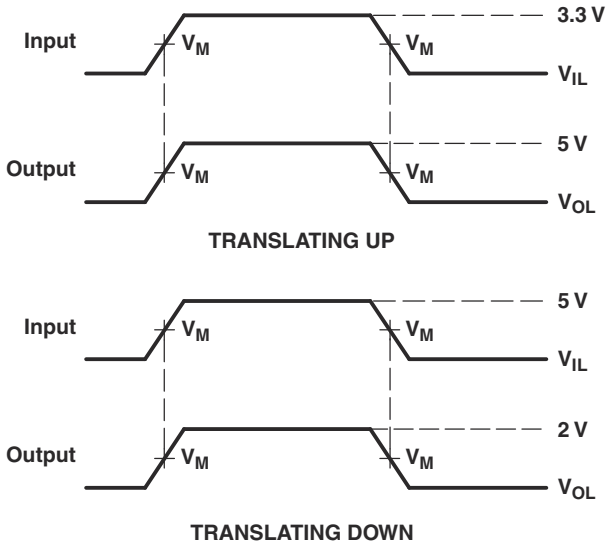
Figure 7-1. Signal Integrity (1.8 V to 3.3 V Translation Up at 50 MHz)

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8 Parameter Measurement Information

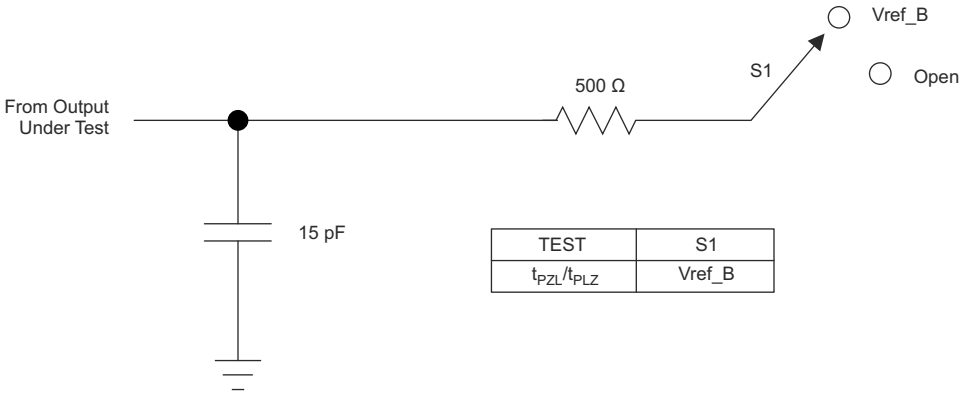


USAGE	SWITCH
Translating up	S1
Translating down	S2



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 8-1. Load Circuit for Outputs



TEST	S1
t_{PZL}/t_{PLZ}	Vref_B

Figure 8-2. Load Circuit for Enable/Disable Time Measurement

8.1 Load Circuit AC Waveform for Outputs

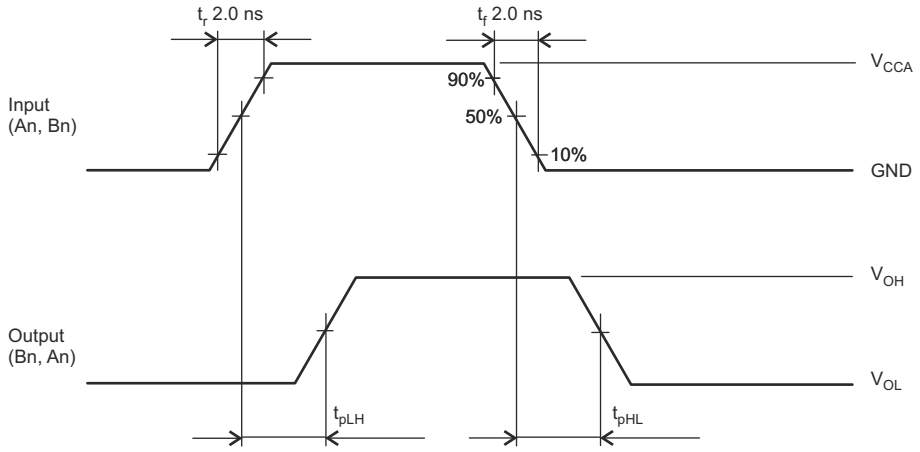


Figure 8-3. t_{PLH}, t_{PHL}

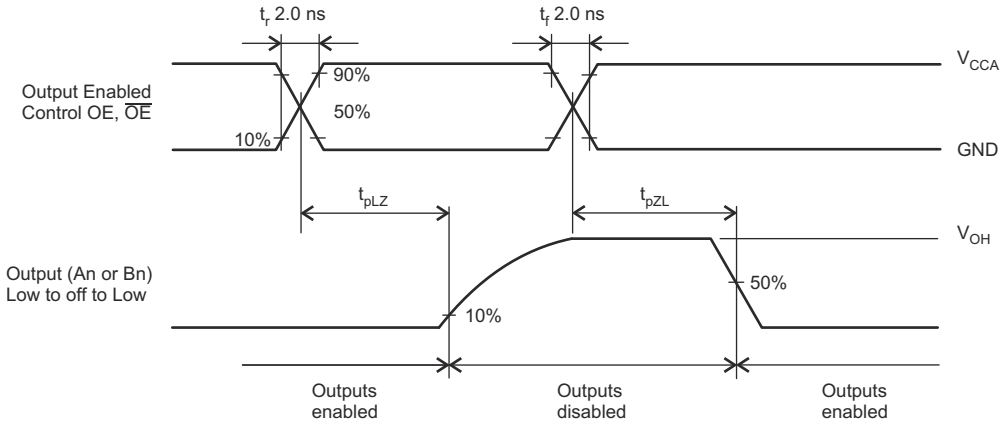


Figure 8-4. t_{PLZ}, t_{PZL}

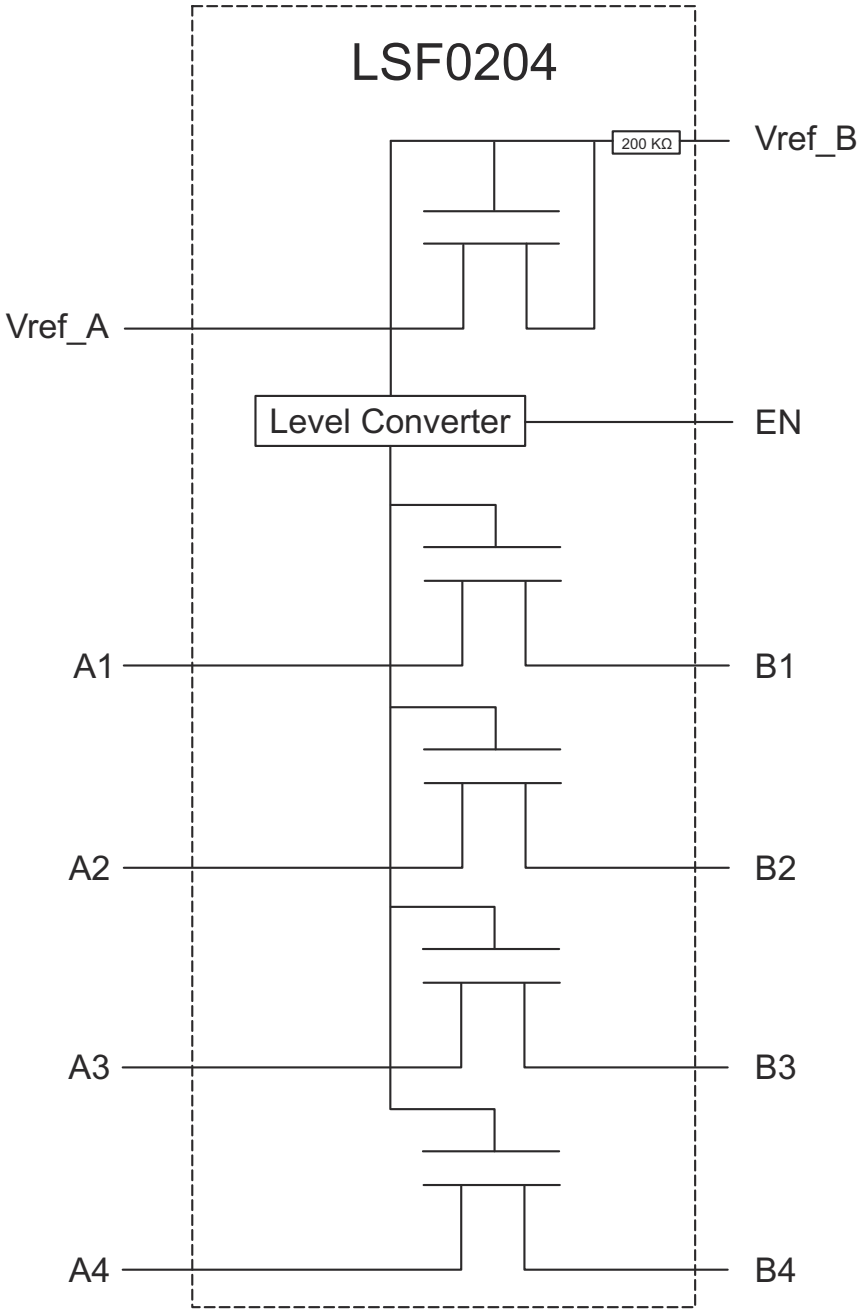
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9 Detailed Description

9.1 Overview

The LSF Family may be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The LSF Family is ideal for use in applications where an open-drain driver is connected to the data I/Os. LSF can achieve 100 MHz with the appropriate pull-up resistors and layout. The LSF Family may also be used in applications where a push-pull driver is connected to the data I/Os.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Support High Speed Translation, Greater than 100 MHz

Allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).

9.3.2 Bidirectional Voltage Translation Without DIR Terminal

Minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I2C, or SMbus).

9.3.3 5-V Tolerance on IO Port and 125°C Support

The LSF family, with 5-V tolerance and 125°C support, is flexible and compliant with TTL levels in industrial and telecom applications.

9.3.4 Channel Specific Translation

The LSF family is able to set up different voltage translation levels on each channel.

9.3.5 Ioff, Partial Power Down Mode

When V_{ref_A}, V_{ref_B} = 0, all of data pins and EN pin are Hi-Z.

EN logic circuit is supplied by V_{ref_A}, once V_{ref_A} power up first and all of data pins are unknown state until V_{ref_B} and EN ready. No power sequence is required to enable LSF0204 and operate function normally.

9.4 Device Functional Modes

Table 9-1 lists the device functional modes of the LSF0204x family of devices.

Table 9-1. Function Table

INPUT EN(1) TERMINAL	FUNCTION
H	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_A} logic levels.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

LSF performs voltage translation for open-drain or push-pull interface. Table 10-1 provides some consumer/telecom interfaces as reference in regards to the different channel numbers that are supported by the LSF family.

Table 10-1. Voltage Translator for Consumer/Telecom Interface

PART NAME	CH#	INTERFACE
LSF0101	1	GPIO
LSF0102	2	GPIO, MDIO, SMBus, PMBus, I2C
LSF0204	4	GPIO, SPI. MDIO, SMBus, PMBus, I2C, UART, SVID
LSF0108	8	GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I2C, SPI

10.2 Typical Applications

10.2.1 I²C PMBus, SMBus, GPIO, Application

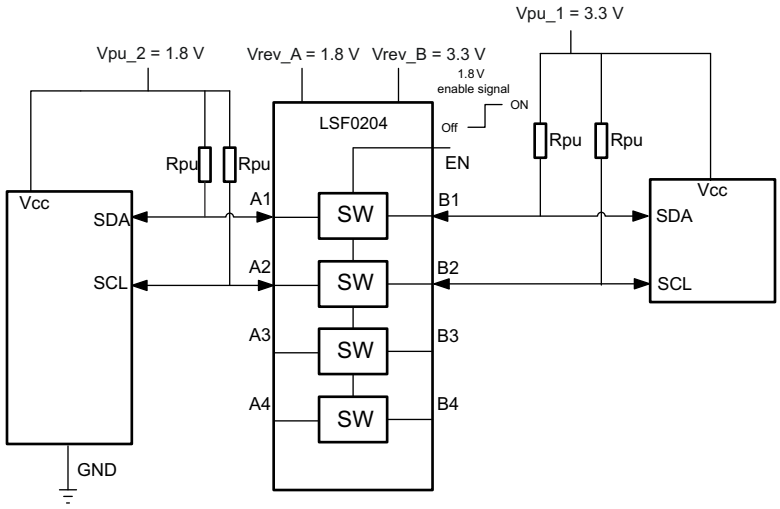


Figure 10-1. Bidirectional Translation to Multiple Voltage Levels

10.2.1.1 Design Requirements

10.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF family has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF family is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF family for bidirectional application (I2C, SMBus, PMBus, or MDIO).

Table 10-2. Application Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Vref_A	Reference voltage (A)	0.8		4.5	V
Vref_B	Reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$ (1)	Input voltage on EN terminal	0		Vref_A	V
Vpu	Pull-up supply voltage	0		Vref_B	V

(1) Refer V_{IH} and V_{IL} for $V_{I(EN)}$

Also Vref_B is recommended to be at 1.0 V higher than Vref_A for best signal integrity.

The LSF Family is able to set different voltage translation level on each channel.

Note

Vref_A must be set as lowest voltage level.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Bidirectional Translation

The controller output driver may be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

Note

However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

In Figure 10-1, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through to a 3.3 V Vpu power supply, and Vref_A is set 1.0V. The output of A3 and B4 has a maximum output voltage equal to Vref_A, and the bidirectional interface (Ch1/2, MDIO) has a maximum output voltage equal to Vpu.

10.2.1.2.1.1 Pull-Up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, to calculate the pull-up resistor value use Equation 1.

$$Rpu = (Vpu – 0.35\ V) / 0.015\ A \quad (1)$$

Table 10-3 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175 V, although the 15 mA applies only to current flowing through the LSF family device.

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Table 10-3. Pullup Resistor Values

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15 mA	10 mA	3 mA			
	NOMINAL	+10%(1)	NOMINAL	+10%(1)	NOMINAL	+10%(1)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) +10% to compensate for V_{DD} range and resistor tolerance

10.2.1.2.2 LS Family Bandwidth

The maximum frequency of the LSF family is dependent on the application. The device may operate at speeds of >100 MHz gave the correct conditions. The maximum frequency is dependent upon the loading of the application. The LSF family behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 10-2 shows a bandwidth measurement of the LSF family using a two-port network analyzer.

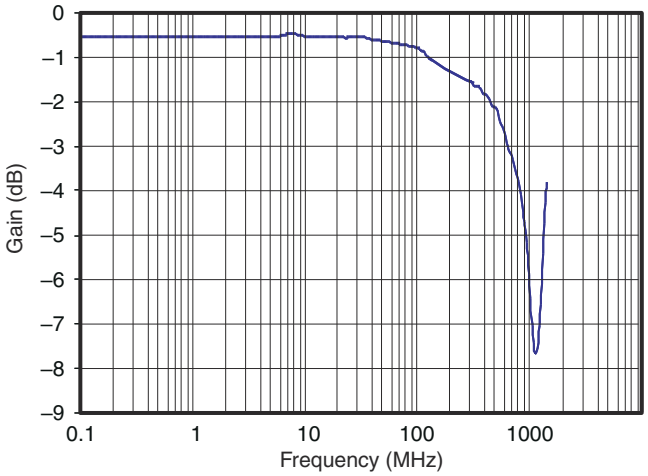


Figure 10-2. 3-dB Bandwidth

The 3-dB point of the LSF family is ≈600 MHz; however, this measurement is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is important in determining the overall shape of the digital signal. In the case of the LSF family, a digital clock frequency of greater than 100 MHz may be achieved.

The LSF family does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the LSF family is being driven by standard CMOS totem pole output driver. Best practice is to minimize the trace length from the LSF family on the sink side (1.8 V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

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To calculate the maximum *practical* frequency component, or the *knee* frequency (f_{knee}), use the following equations:

$$f_{knee} = 0.5/RT \ (10–80\%) \quad (2)$$

$$f_{knee} = 0.4/RT \ (20–80\%) \quad (3)$$

For signals with rise time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which is very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the LSF family close to the I^2C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

10.2.1.3 Application Curve

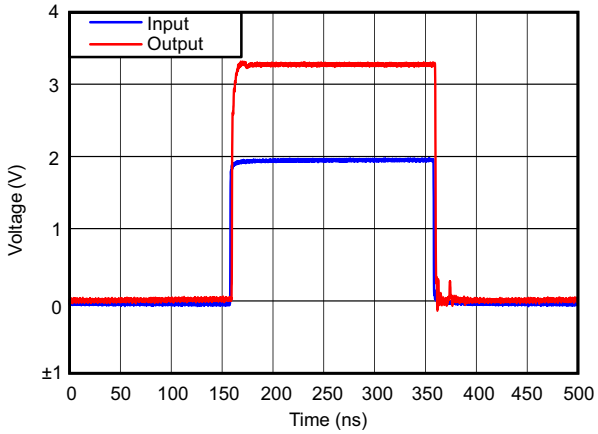


Figure 10-3. Captured Waveform From Above I^2C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

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10.2.2 MDIO Application

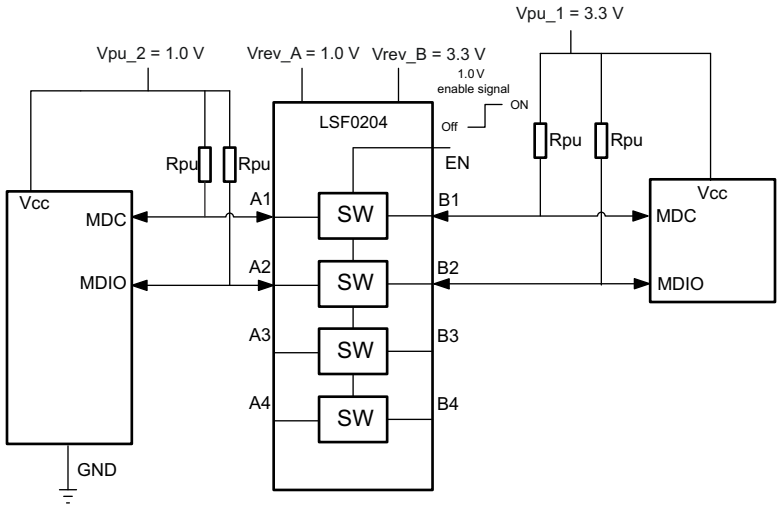


Figure 10-4. Typical Application Circuit (MDIO/Bidirectional Interface)

10.2.2.1 Design Requirements

Refer to *Design Requirements*.

10.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*

10.2.2.3 Application Curve

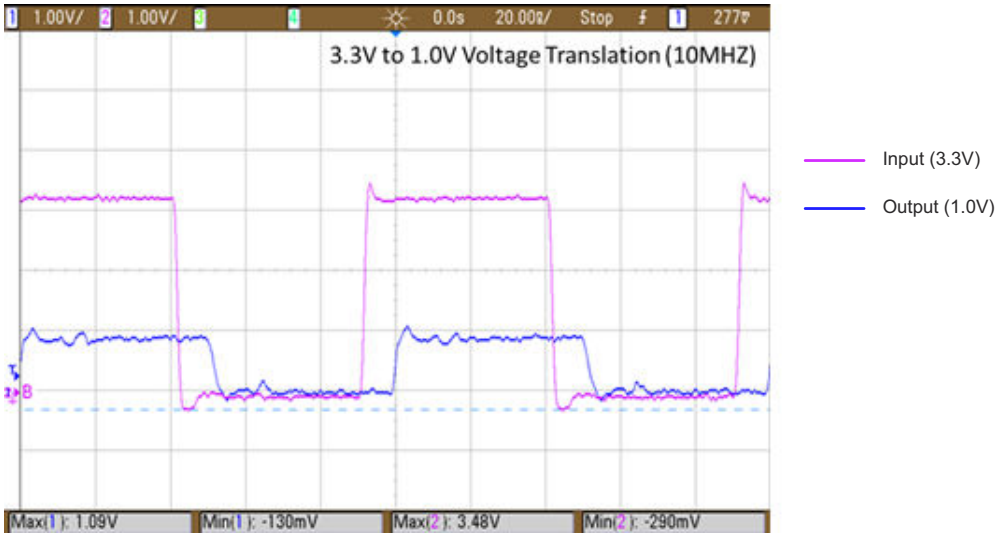
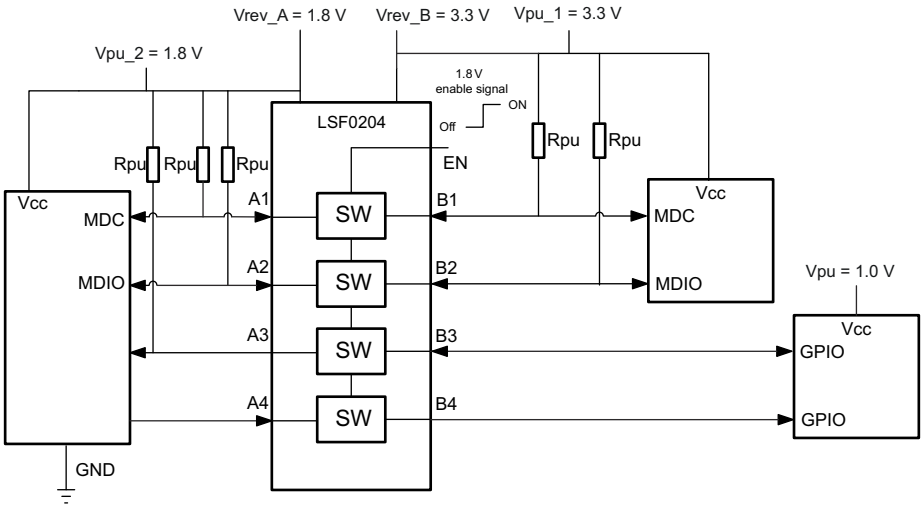


Figure 10-5. Captured Waveform From Above MDIO Setup

10.2.3 Multiple Voltage Translation in Single Device, Application



10.2.3.1 Design Requirements

Refer to *Design Requirements*.

10.2.3.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*

10.2.3.3 Application Curve

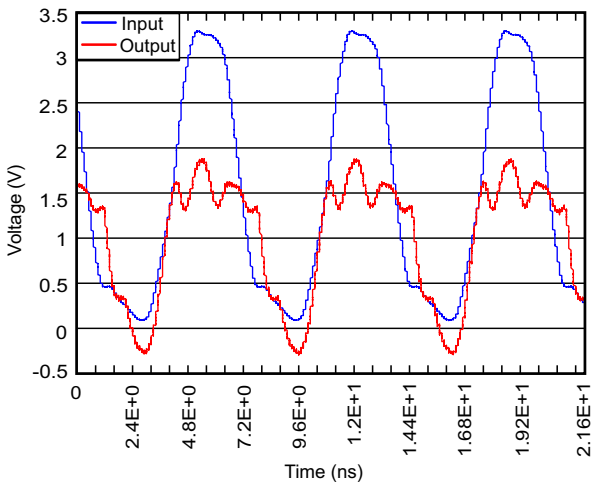


Figure 10-6. Translation Down (3.3 V to 1.8 V) at 150 MHz

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11 Power Supply Recommendations

There are no power sequence requirements for the LSF Family. Refer to *Section 10.2.1.1.1* for enabling and reference voltage guidelines.

12 Layout

12.1 Layout Guidelines

The signal integrity is highly related with pull-up resistor and PCB capacitance condition because LSF Family is switch-type level translator

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF close to high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

12.2 Layout Example

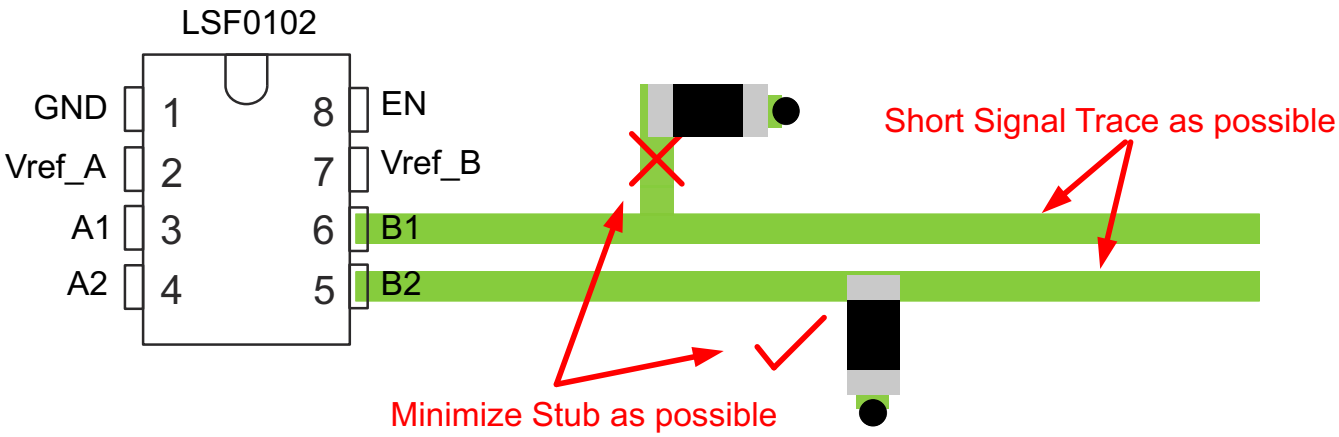


Figure 12-1. Short Trace Layout

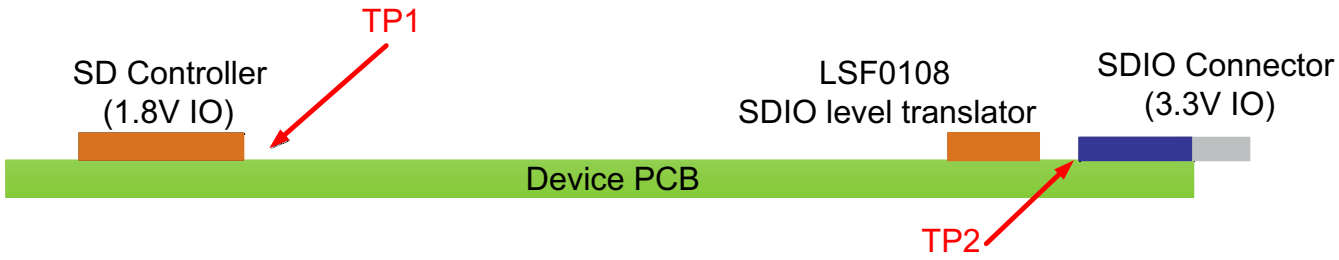


Figure 12-2. Device Placement

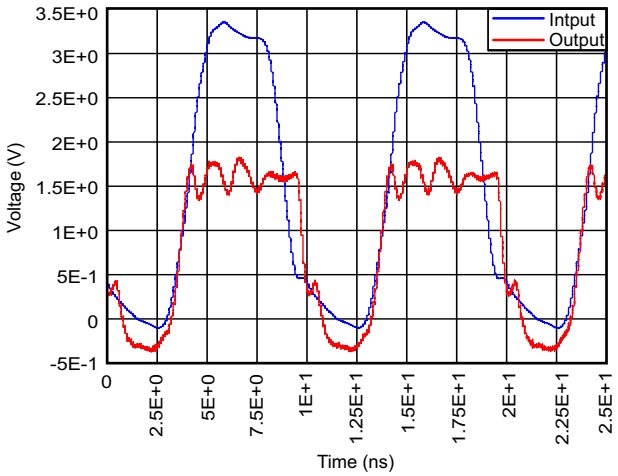


Figure 12-3. Waveform From TP1 (Pullup Resistor: 160-Ω and 50-pF Capacitance 3.3 to 1.8 V at 100 MHz)

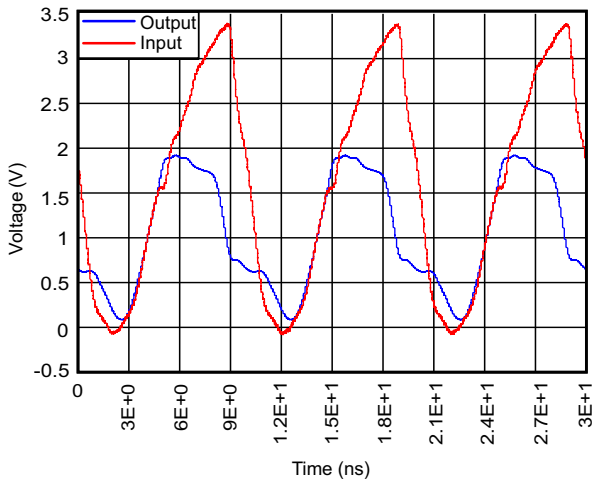


Figure 12-4. Waveform From TP2 (Pullup Resistor: 160-Ω and 50-pF Capacitance 1.8 to 3.3 V at 100 MHz)

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13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

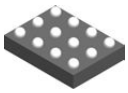
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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LSF0204/LSF0204D

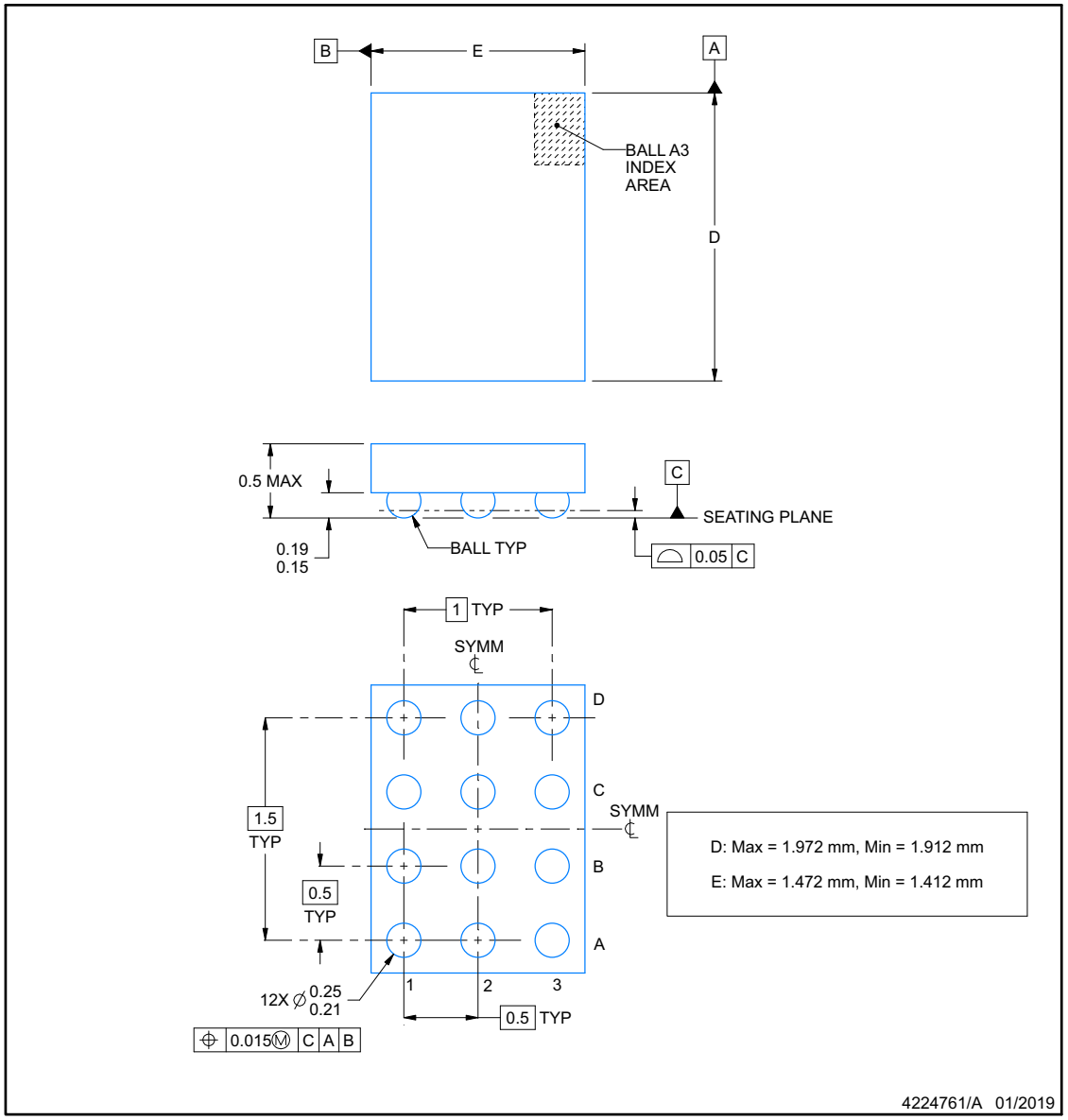
YZP0012-C01



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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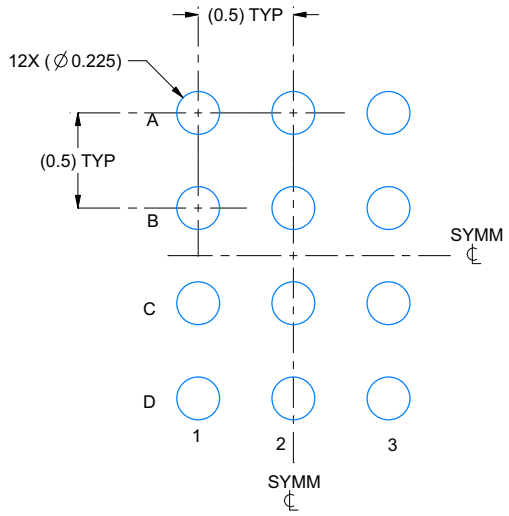
LSF0204/LSF0204D

YZP0012-C01

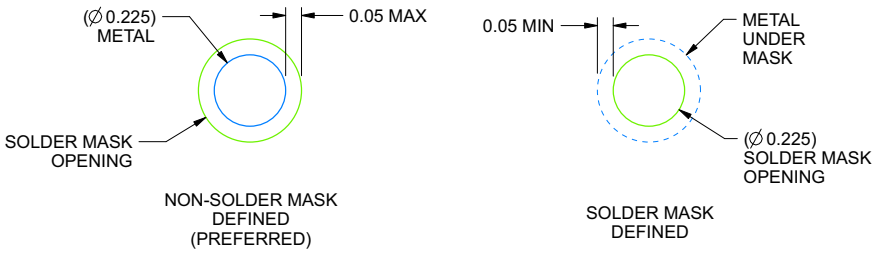
EXAMPLE BOARD LAYOUT

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4224761/A 01/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

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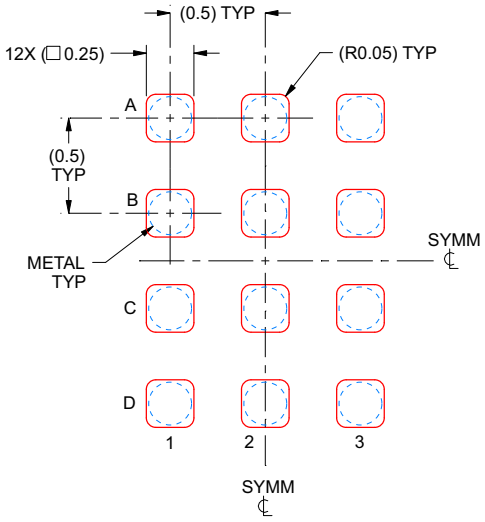
LSF0204/LSF0204D

YZP0012-C01

EXAMPLE STENCIL DESIGN

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224761/A 01/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LSF0204DPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LSF204D
LSF0204DPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LSF204D
LSF0204DRGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LSF24D
LSF0204DRGYR.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LSF24D
LSF0204DRGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LSF24D
LSF0204DRGYRG4.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LSF24D
LSF0204DRUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIO
LSF0204DRUTR.B	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIO
LSF0204DRUTRG4	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIO
LSF0204DRUTRG4.B	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIO
LSF0204DYZPR	Active	Production	DSBGA (YZP) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G6
LSF0204DYZPR.B	Active	Production	DSBGA (YZP) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G6
LSF0204PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LSF204
LSF0204PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LSF204
LSF0204RGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF24
LSF0204RGYR.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF24
LSF0204RGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF24
LSF0204RGYRG4.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF24
LSF0204RUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIN
LSF0204RUTR.B	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIN
LSF0204RUTRG4	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIN
LSF0204RUTRG4.B	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIN
LSF0204YZPR	Active	Production	DSBGA (YZP) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G5
LSF0204YZPR.B	Active	Production	DSBGA (YZP) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LSF0204 :

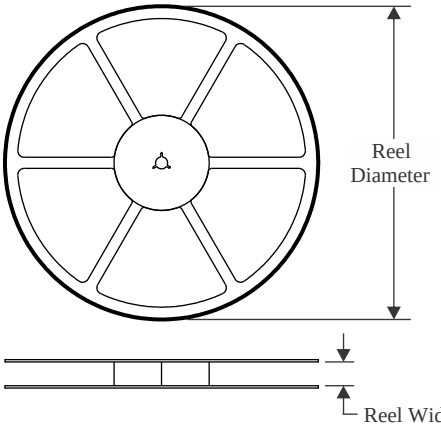
- Automotive : LSF0204-Q1

NOTE: Qualified Version Definitions:

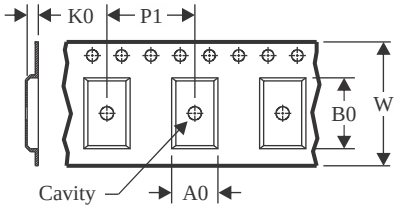
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

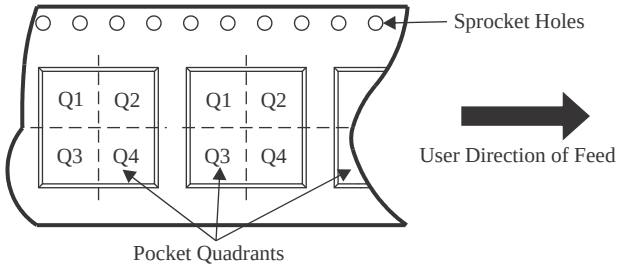


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

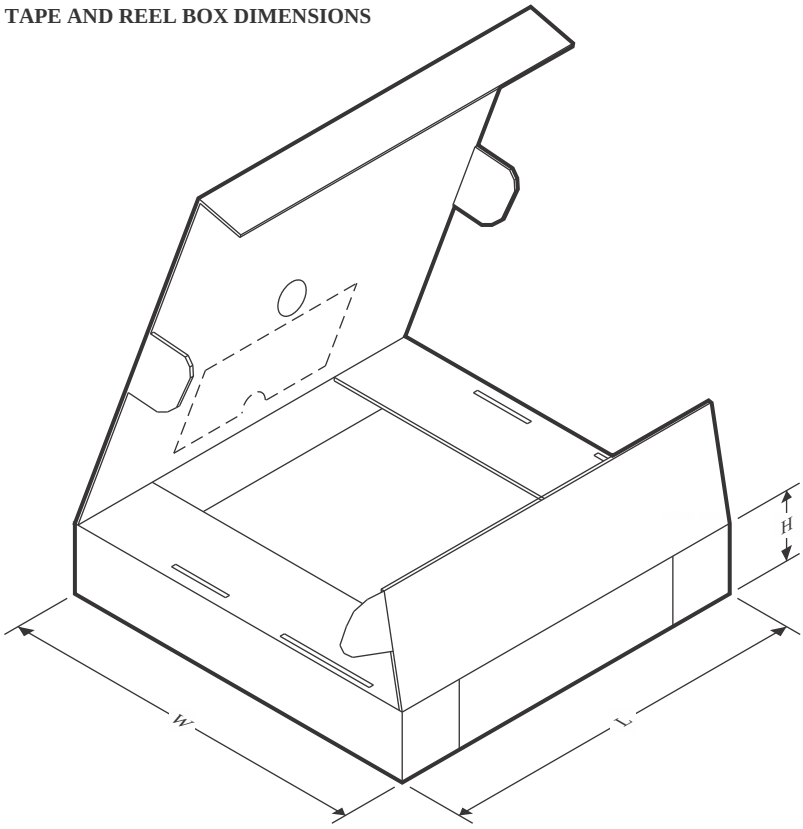
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0204DPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LSF0204DRGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
LSF0204DRGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
LSF0204DRUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
LSF0204DRUTRG4	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
LSF0204DYZPR	DSBGA	YZP	12	3000	180.0	8.4	1.63	2.08	0.69	4.0	8.0	Q2
LSF0204PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LSF0204RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
LSF0204RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
LSF0204RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
LSF0204RUTRG4	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
LSF0204YZPR	DSBGA	YZP	12	3000	180.0	8.4	1.63	2.08	0.69	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0204DPWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LSF0204DRGYR	VQFN	RGY	14	3000	346.0	346.0	33.0
LSF0204DRGYRG4	VQFN	RGY	14	3000	346.0	346.0	33.0
LSF0204DRUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
LSF0204DRUTRG4	UQFN	RUT	12	3000	184.0	184.0	19.0
LSF0204DYZPR	DSBGA	YZP	12	3000	182.0	182.0	20.0
LSF0204PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LSF0204RGYR	VQFN	RGY	14	3000	346.0	346.0	33.0
LSF0204RGYRG4	VQFN	RGY	14	3000	346.0	346.0	33.0
LSF0204RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
LSF0204RUTRG4	UQFN	RUT	12	3000	184.0	184.0	19.0
LSF0204YZPR	DSBGA	YZP	12	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

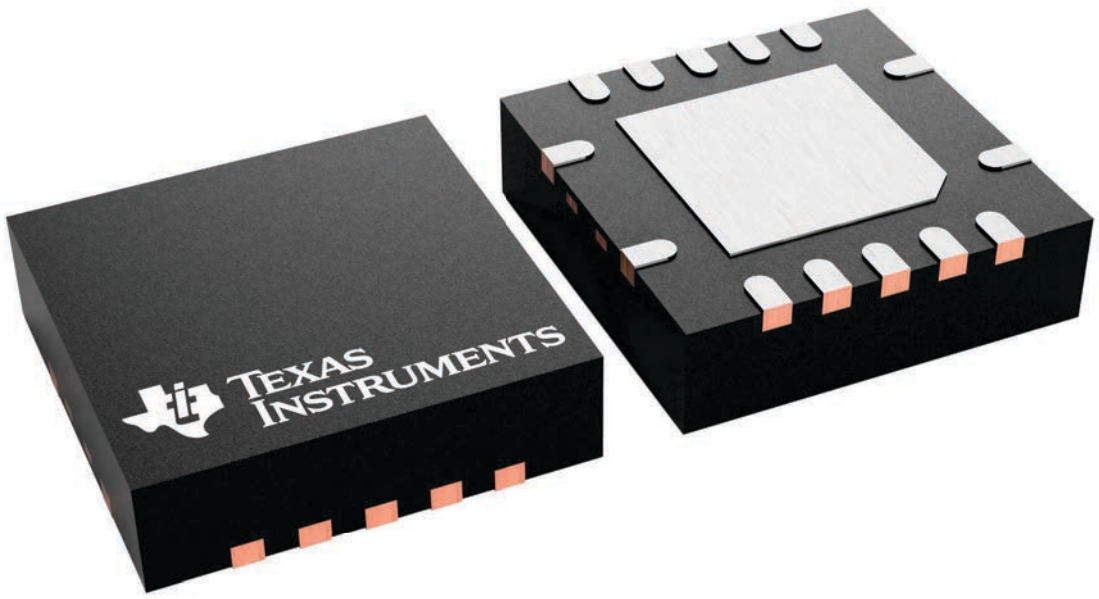
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



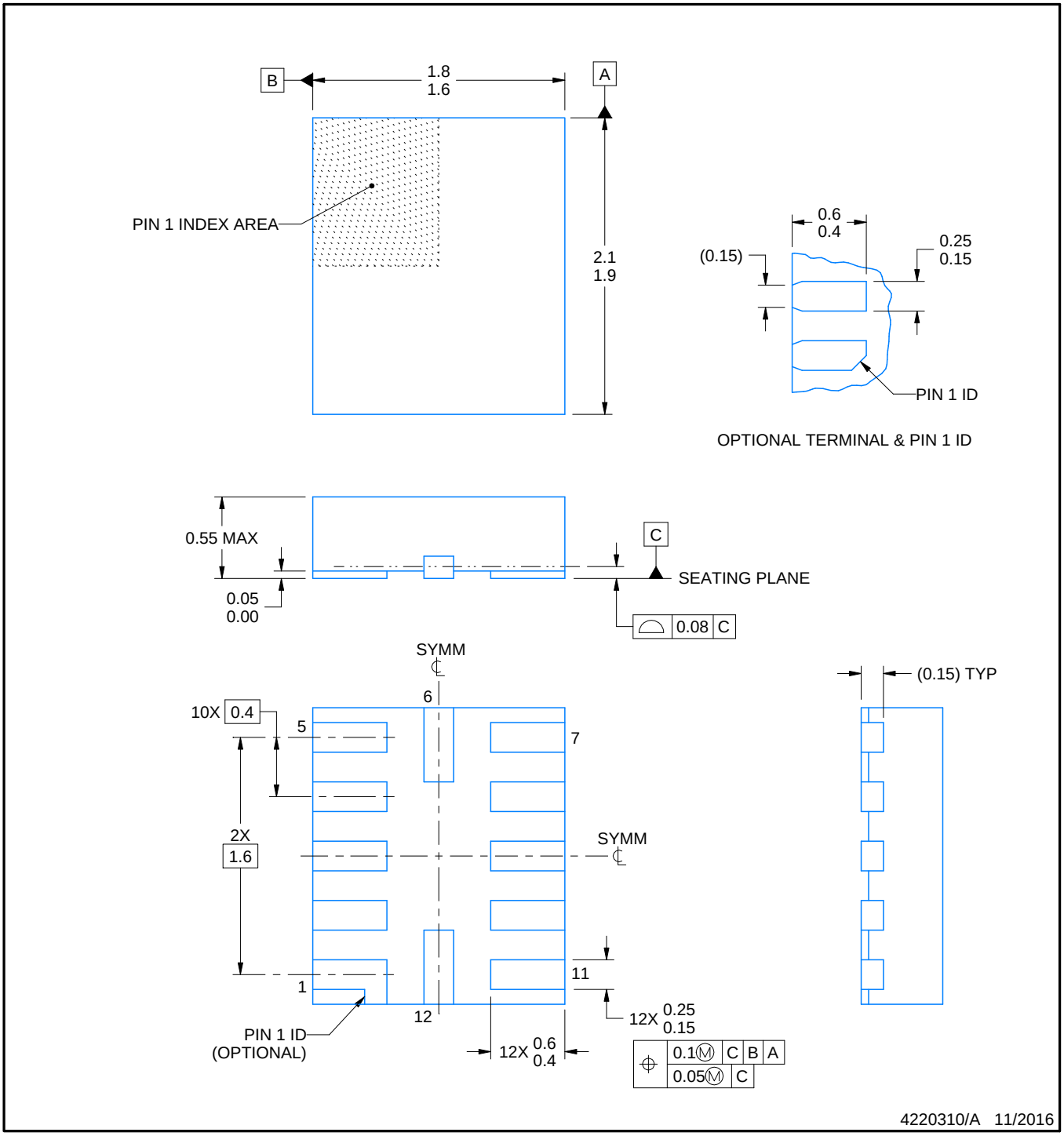
4231541/A

RUT0012A

PACKAGE OUTLINE

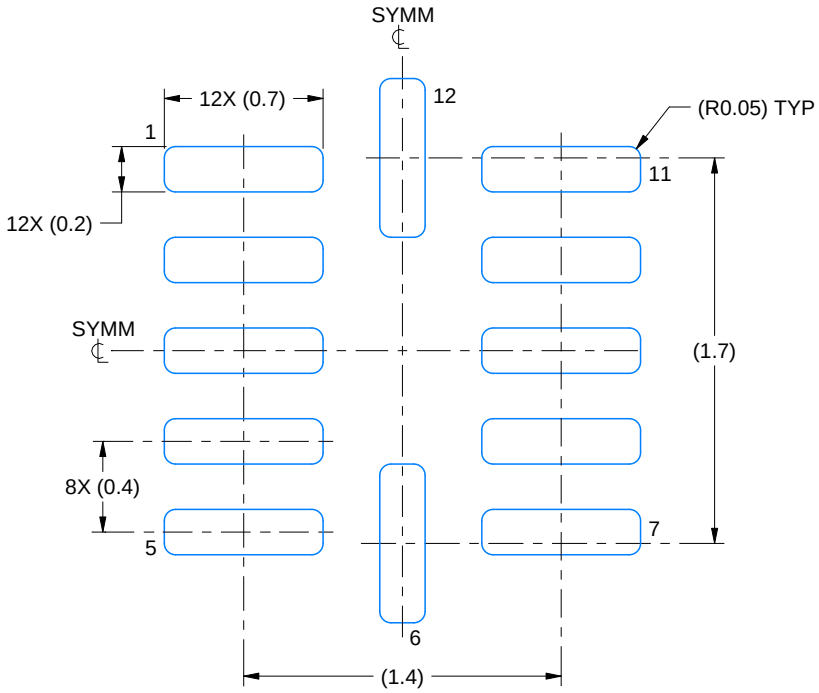
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

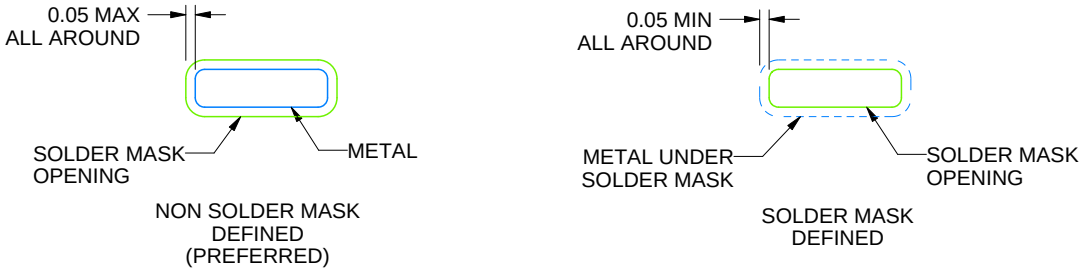


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

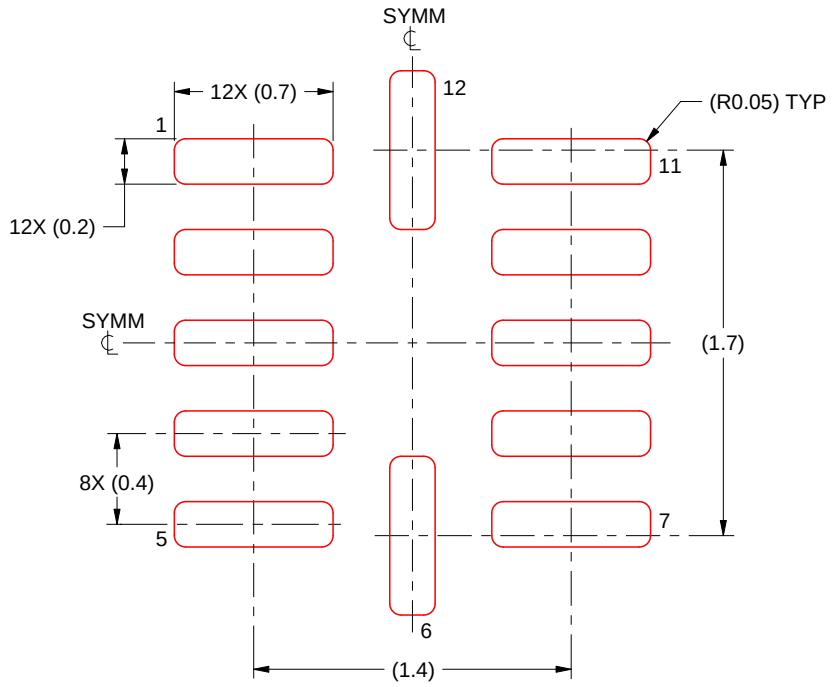


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

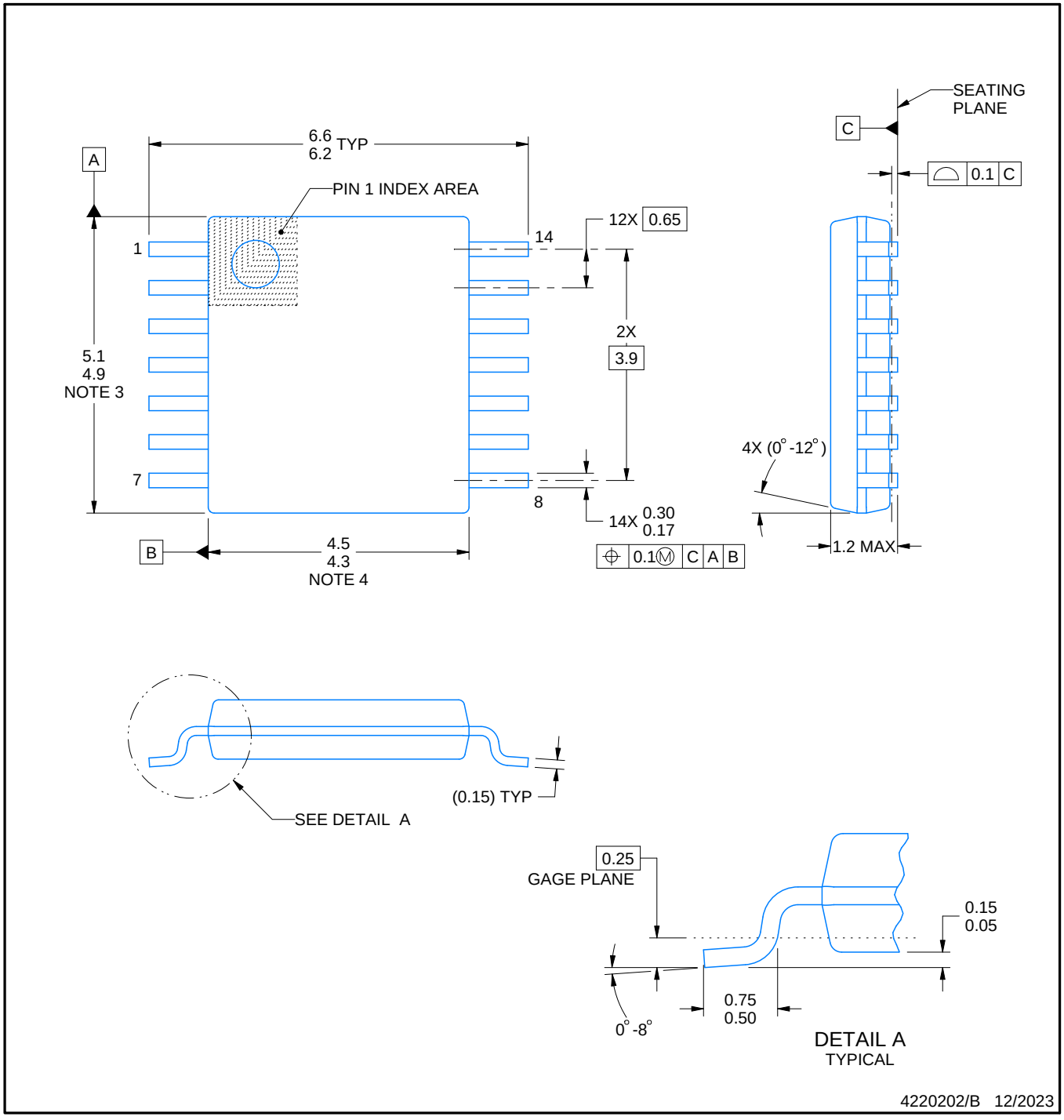
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

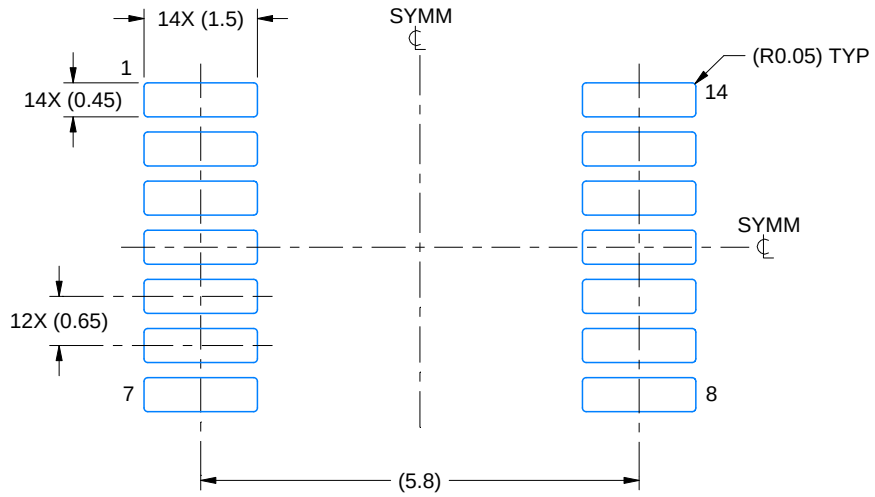
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

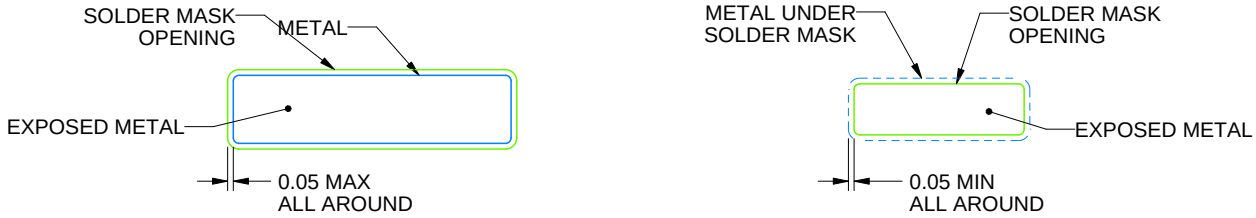


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

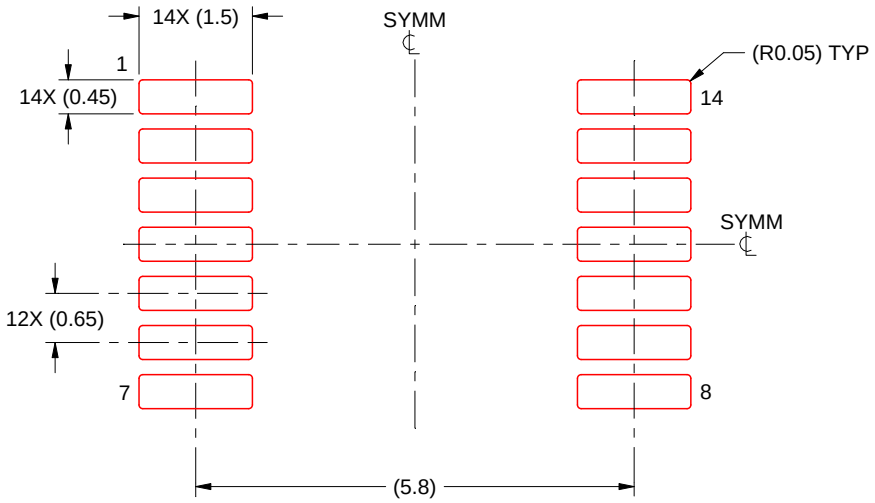


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025