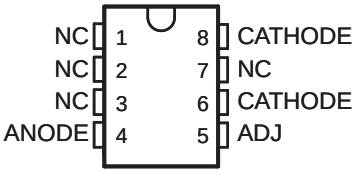
2.5-V INTEGRATED REFERENCE CIRCUIT

FEATURES

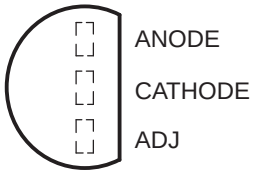
- **Excellent Temperature Stability**
- **Initial Tolerance: 0.2% Max**
- **Dynamic Impedance: 0.6 Ω Max**
- **Wide Operating Current Range**
- **Directly Interchangeable With LM136**
- **Needs No Adjustment for Minimum Temperature Coefficient**

D OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

LP PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

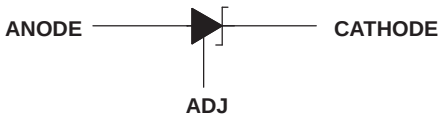
The LT1009 reference circuit is a precision-trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. The maximum initial tolerance is ±5 mV in the LP package and ±10 mV in the D and PW packages. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient, α_{VZ}.

Although the LT1009 needs no adjustments, a third terminal (ADJ) allows the reference voltage to be adjusted ±5% to eliminate system errors. In many applications, the LT1009 can be used as a terminal-for-terminal replacement for the LM136-2.5, which eliminates the external trim network.

The LT1009 uses include 5-V system references, 8-bit analog-to-digital converter (ADC) and digital-to-analog converter (DAC) references, and power-supply monitors. The device also can be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from –40°C to 85°C.

SYMBOL



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

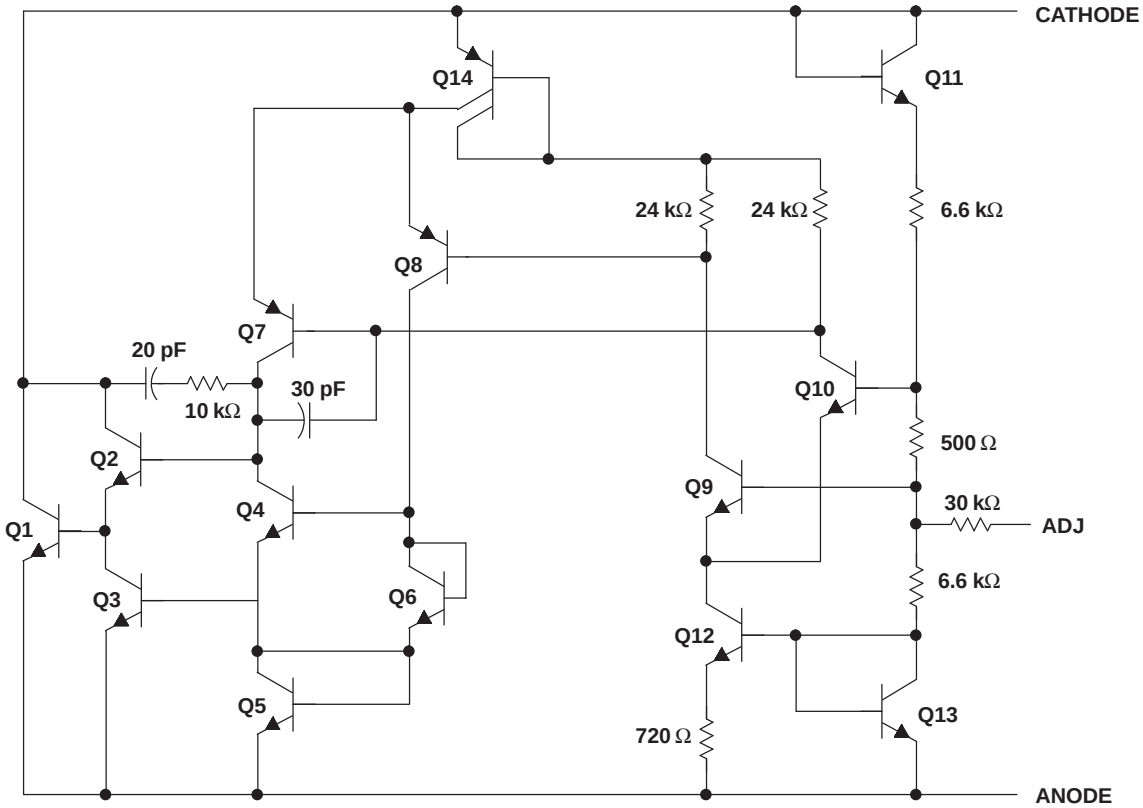
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ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube of 75	LT1009CD	1009C
		Reel of 2500	LT1009CDR	
	TO-226/TO-92 – LP	Bulk of 1000	LT1009CLP	LT1009C
		Ammo of 2000	LT1009CLPM	
		Reel of 2000	LT1009CLPR	
	TSSOP – PW	Tube of 150	LT1009CPW	1009C
		Reel of 2000	LT1009CPWR	
–40°C to 85°C	SOIC – D	Tube of 75	LT1009ID	1009I
		Reel of 2500	LT1009IDR	
	TO-226/TO-92 – LP	Bulk of 1000	LT1009ILP	LT1009I
		Ammo of 2000	LT1009ILPM	
		Reel of 2000	LT1009ILPR	
	TSSOP – PW	Tube of 150	LT1009IPW	1009I
		Reel of 2000	LT1009IPWR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SCHEMATIC



NOTE: All component values shown are nominal.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I_R	Reverse current			20	mA
I_F	Forward current			10	mA
θ_{JA}	Package thermal impedance(2) (3)	D package		97	°C/W
		LP package		140	
		PW package		149	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
T_A	Operating free-air temperature range	LT1009C	0	70	°C
		LT1009I	–40	85	

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ELECTRICAL CHARACTERISTICS

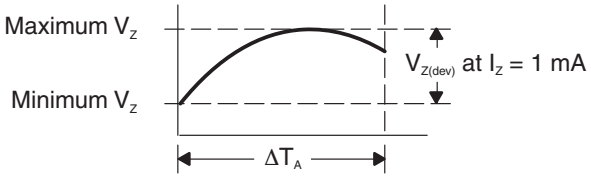
at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A (1)	LT1009C			LT1009I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 1 mA	D/PW package	25°C	2.49	2.5	2.51	2.49	2.5	2.51	V
			LP package		2.495	2.5	2.505	2.495	2.5	2.505	
			D/PW package	Full range	2.485		2.515	2.475		2.525	
			LP package		2.491		2.509	2.48		2.52	
V_F	Forward voltage	I_F = 2 mA		25°C	0.4		1	0.4		1	V
	Adjustment range	I_Z = 1 mA, V_{ADJ} = GND to V_Z		25°C	125			125			mV
		I_Z = 1 mA, V_{ADJ} = 0.6 V to V_Z – 0.6 V			45			45			
$\Delta V_{Z(temp)}$	Change in reference voltage with temperature	D/PW package		Full range			5			15	mV
		LP package					4			15	
αV_Z	Average temperature coefficient of reference voltage (2)	I_Z = 1 mA, V_{ADJ} = open		0°C to 70°C		15	25		15	25	ppm/°C
				–40°C to 85°C					20	35	
ΔV_Z	Change in reference voltage with current	I_Z = 400 µA to 10 mA		25°C		2.6	10		2.6	6	mV
				Full range			12			10	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 1 mA		25°C		20			20		ppm/khr
Z_Z	Reference impedance	I_Z = 1 mA		25°C		0.3	1		0.3	1	Ω
				Full range			1.4			1.4	

(1) Full range is 0°C to 70°C for the LT1009C and –40°C to 85°C for the LT1009I.

(2) The deviation parameter $V_{Z(dev)}$ is defined as the difference between the maximum and minimum values obtained over the recommended operating temperature range, measured at I_Z = 1 mA. The average full-range temperature coefficient of the reference voltage (αV_Z) is defined as:

$$|\alpha V_z| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{Z(dev)}}{V_Z \text{ at } 25°C}\right) \times 10^6}{\Delta T_A}$$



αV_Z can be positive or negative, depending upon whether the minimum V_Z or maximum V_Z, respectively, occurs at the lower temperature.

For example, at I_Z = 1 mA, maximum V_Z = 2501 mV at 30°C, minimum V_Z = 2497 mV at 0°C, V_Z = 2500 mV at 25°C, ΔT_A = 70°C for LT1009C:

$$|\alpha V_z| = \frac{\left(\frac{4 \text{ mV}}{2500 \text{ mV}}\right) \times 10^6}{70°C} \approx 23 \frac{ppm}{°C}$$

Because minimum V_Z occurs at the lower temperature, the coefficient in this example is positive.

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TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

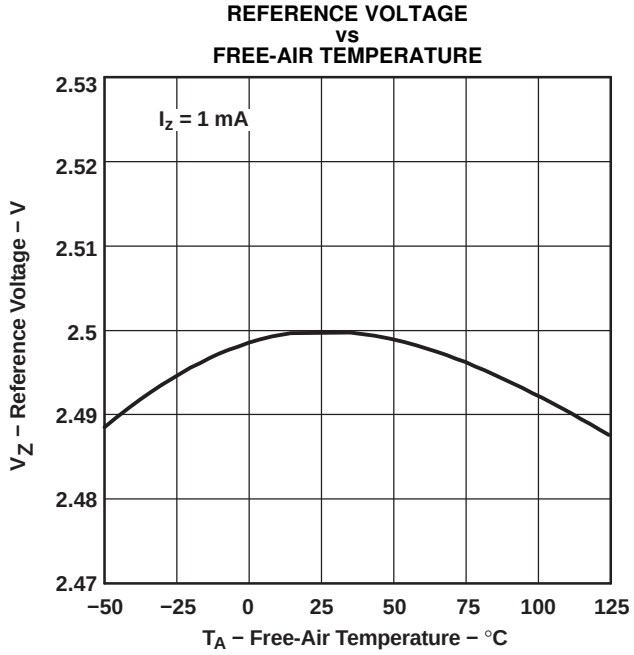


Figure 1.

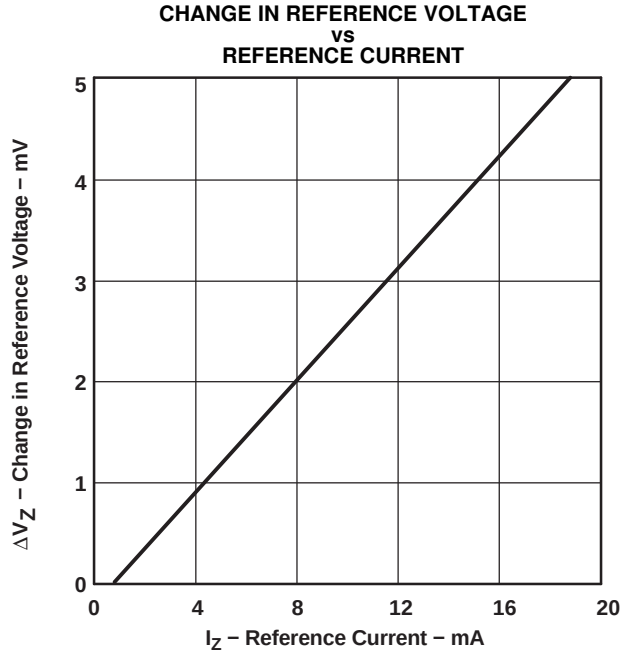


Figure 2.

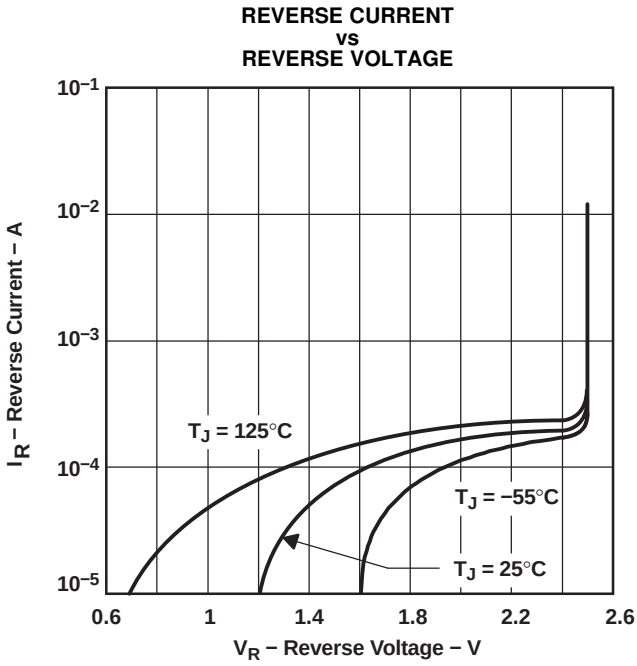


Figure 3.

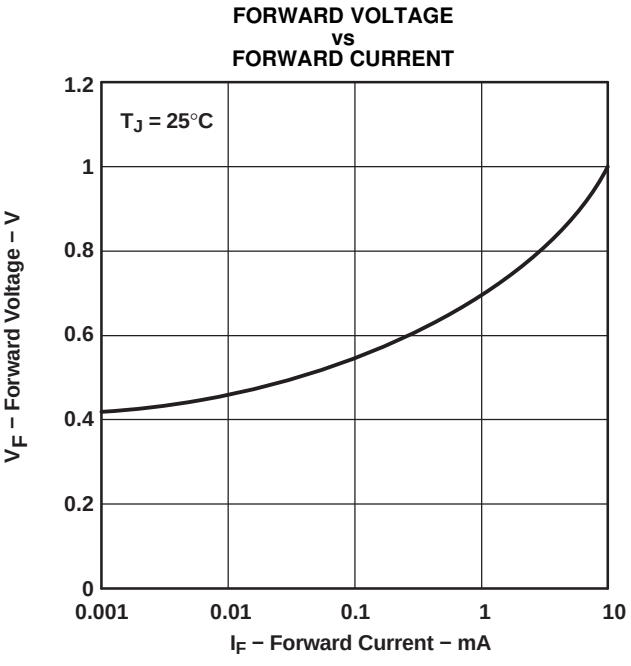


Figure 4.

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TYPICAL CHARACTERISTICS (continued)

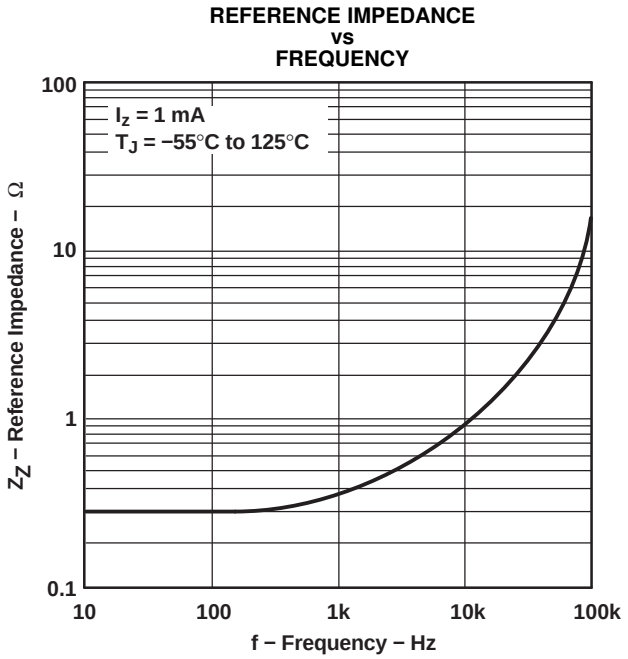


Figure 5.

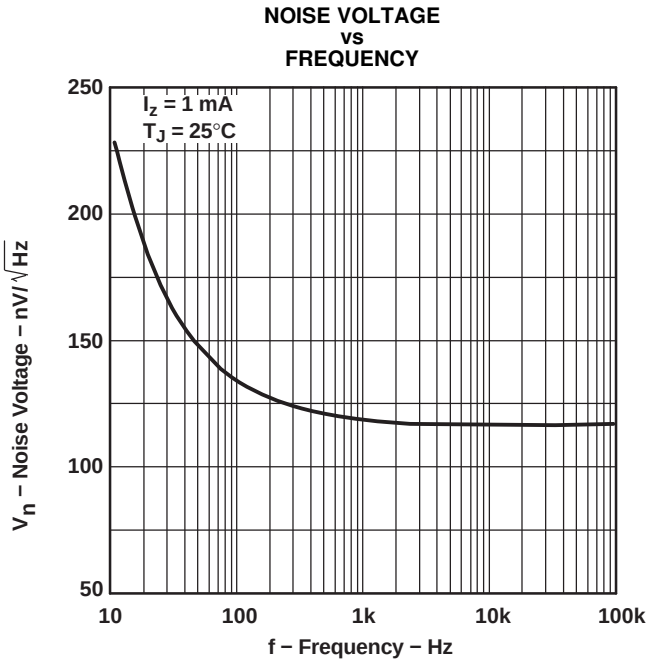


Figure 6.

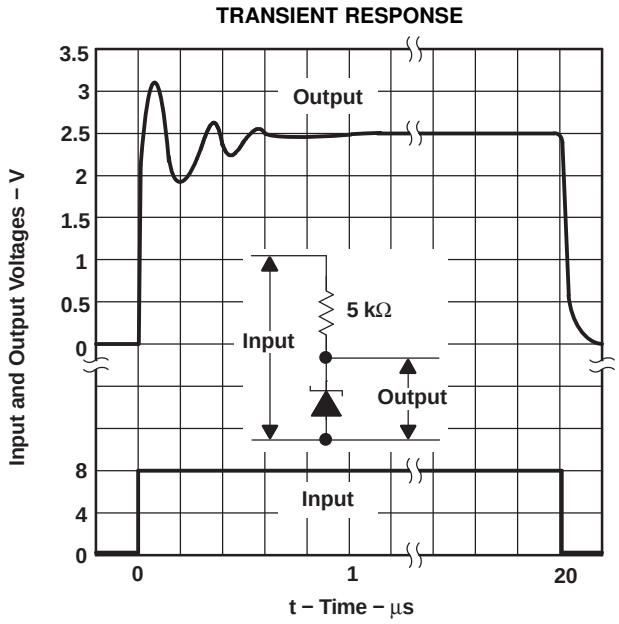
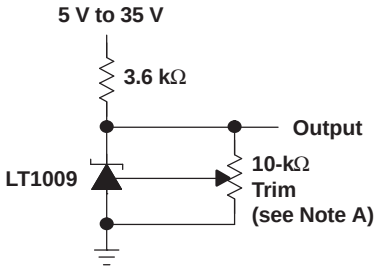


Figure 7.

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APPLICATION INFORMATION



A. This does not affect temperature coefficient. It provides ±5% trim range.

Figure 8. 2.5-V Reference

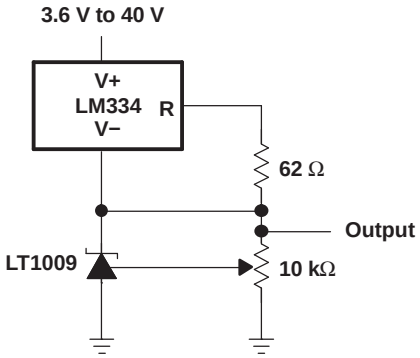


Figure 9. Adjustable Reference With Wide Supply Range

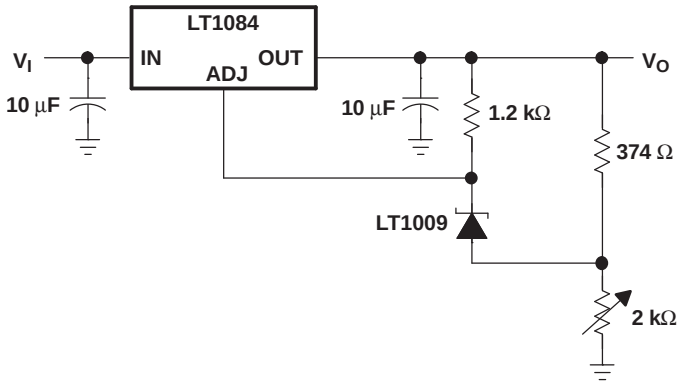


Figure 10. Power Regulator With Low Temperature Coefficient

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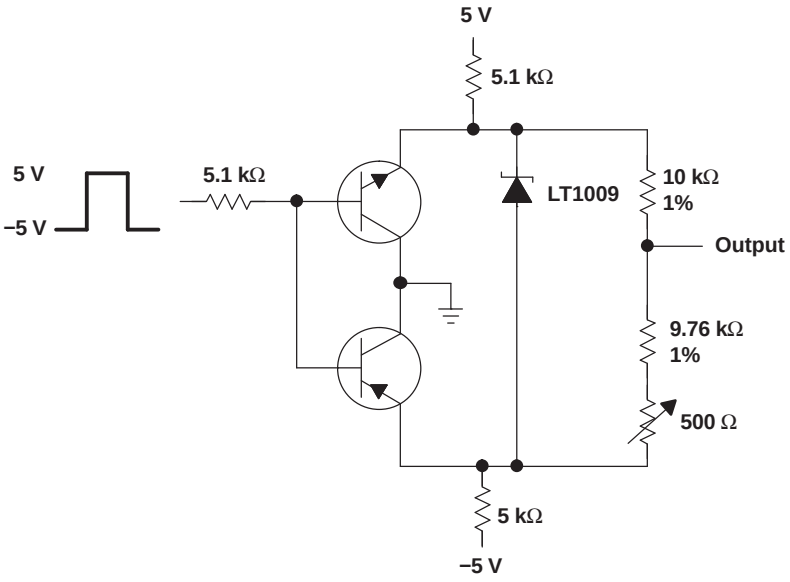


Figure 11. Switchable ±1.25-V Bipolar Reference

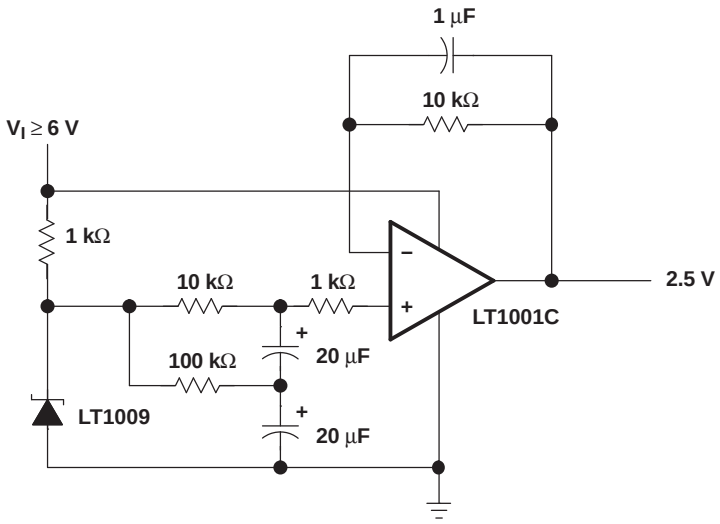


Figure 12. Low-Noise 2.5-V Buffered Reference

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LT1009CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C
LT1009CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C
LT1009CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C
LT1009CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C
LT1009CLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 70	LT1009C
LT1009CLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 70	LT1009C
LT1009CLPM	Active	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	0 to 70	LT1009C
LT1009CLPM.A	Active	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	0 to 70	LT1009C
LT1009CLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	LT1009C
LT1009CLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	LT1009C
LT1009CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C
LT1009CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C
LT1009ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I
LT1009ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I
LT1009IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I
LT1009IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I
LT1009ILP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 85	LT1009I
LT1009ILP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 85	LT1009I
LT1009ILPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	LT1009I
LT1009ILPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	LT1009I
LT1009IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I
LT1009IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LT1009 :

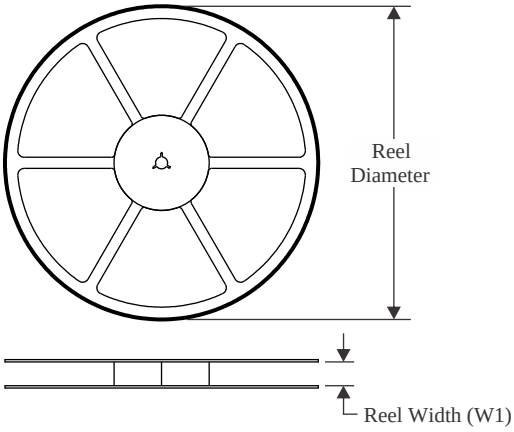
- Military : LT1009M

NOTE: Qualified Version Definitions:

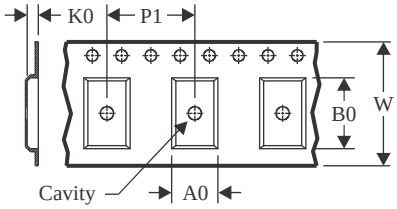
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

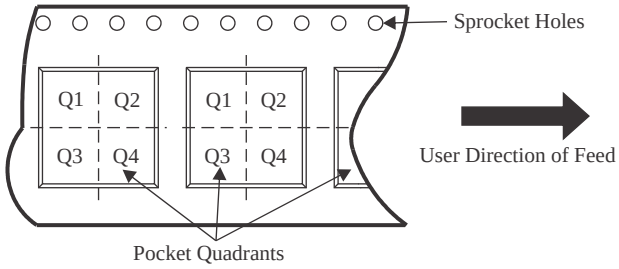


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

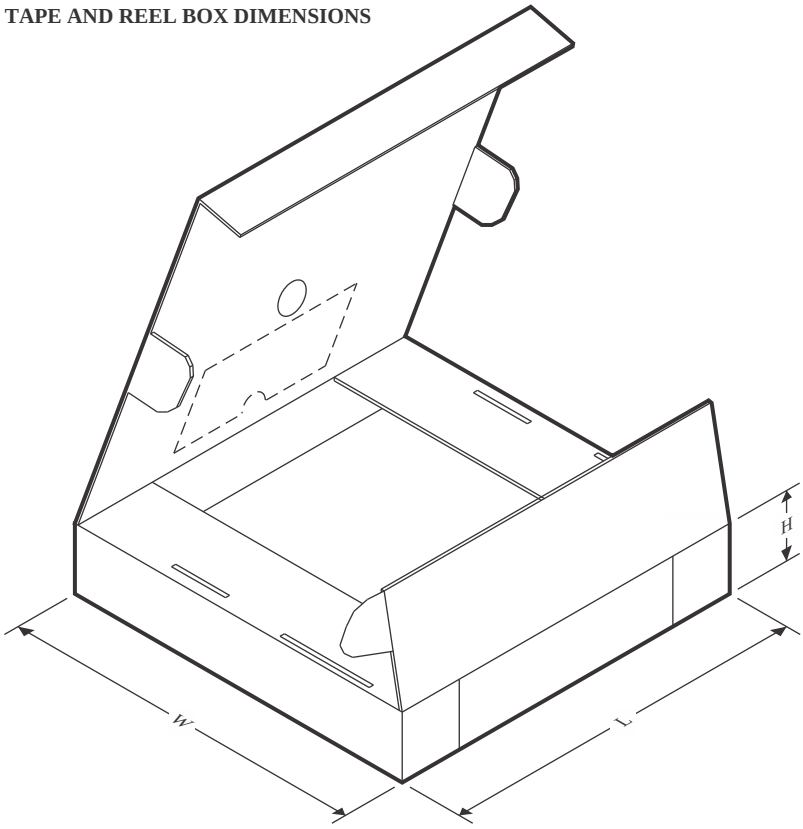
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1009CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1009CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LT1009IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1009IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

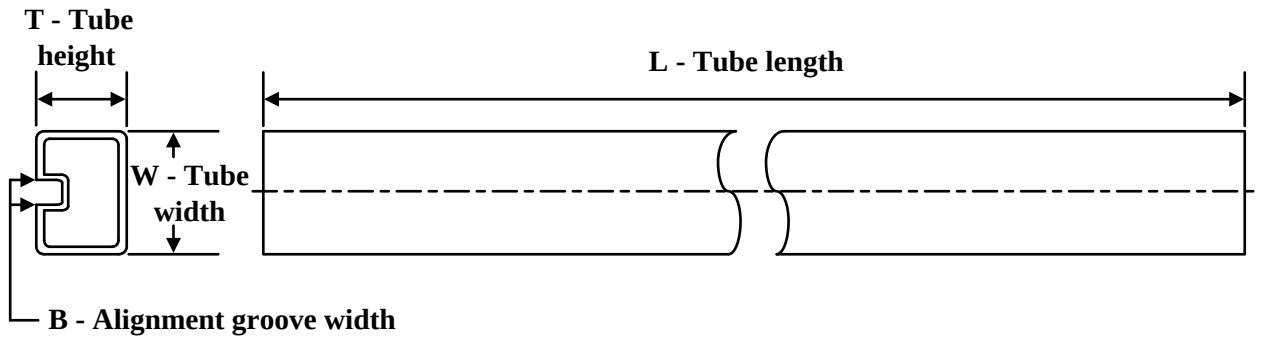
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1009CDR	SOIC	D	8	2500	353.0	353.0	32.0
LT1009CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LT1009IDR	SOIC	D	8	2500	353.0	353.0	32.0
LT1009IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LT1009CD	D	SOIC	8	75	507	8	3940	4.32
LT1009CD.A	D	SOIC	8	75	507	8	3940	4.32
LT1009ID	D	SOIC	8	75	507	8	3940	4.32
LT1009ID.A	D	SOIC	8	75	507	8	3940	4.32

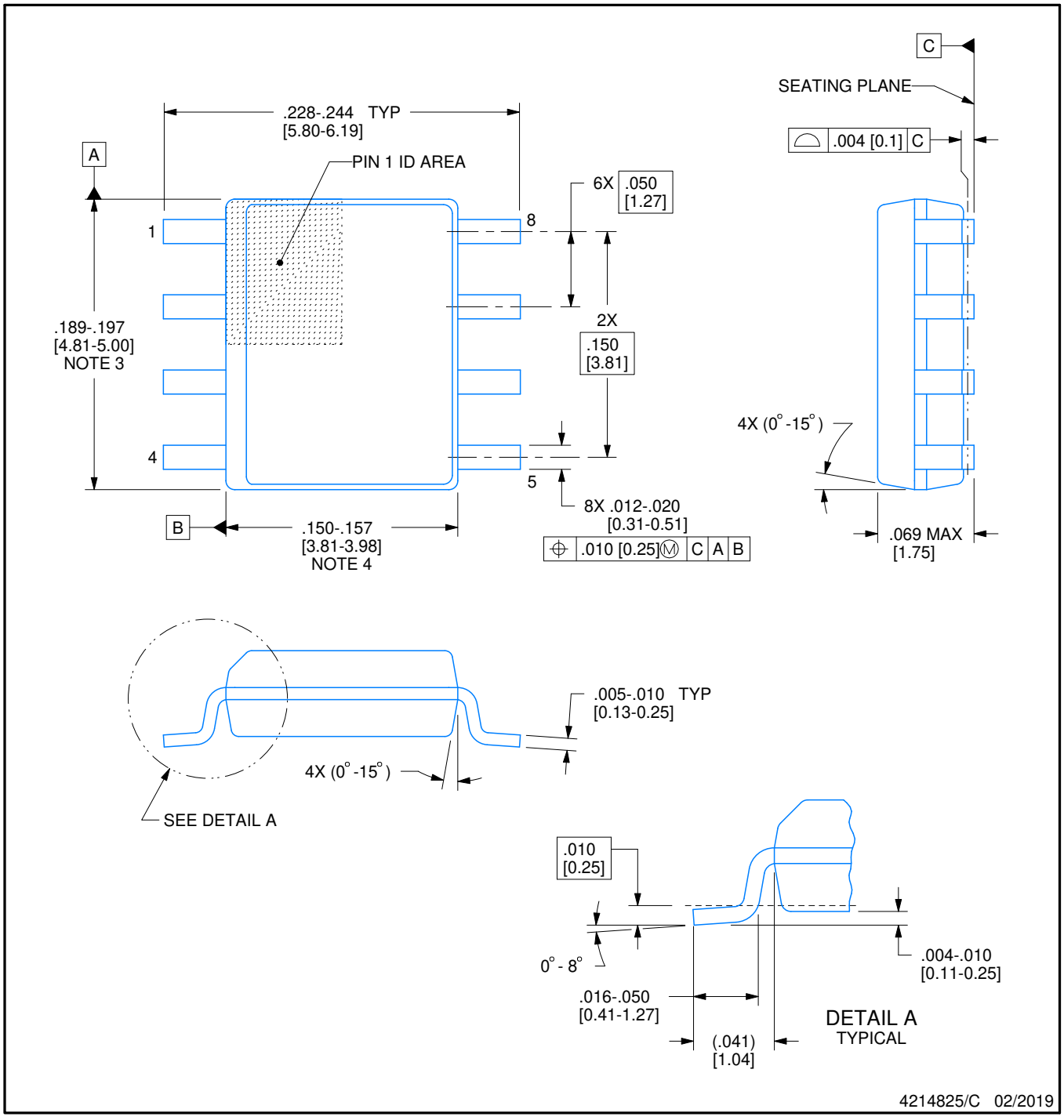


PACKAGE OUTLINE

D0008A

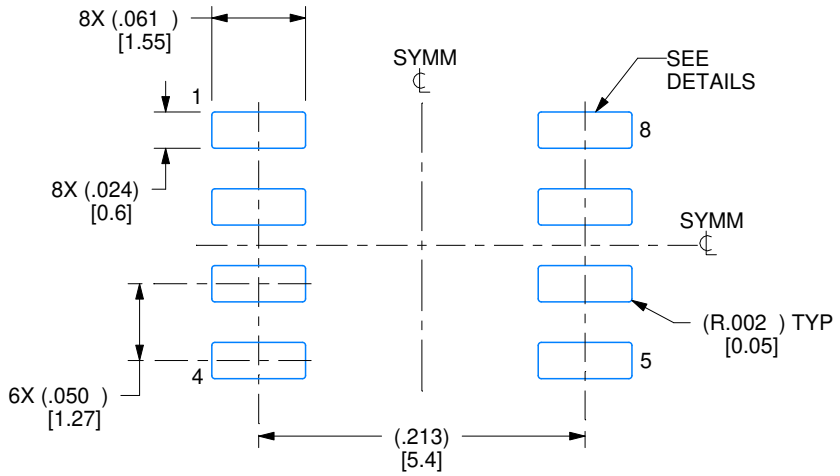
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

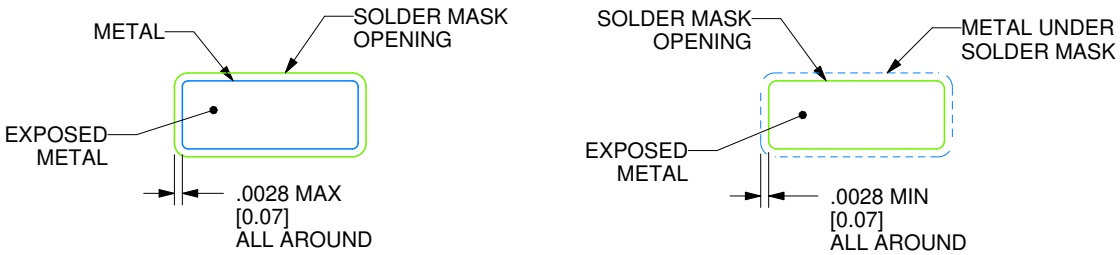


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

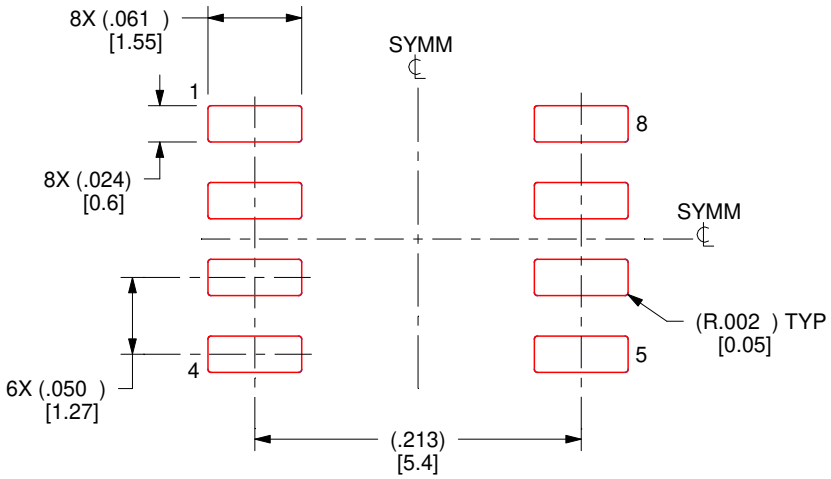
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

LP0003A

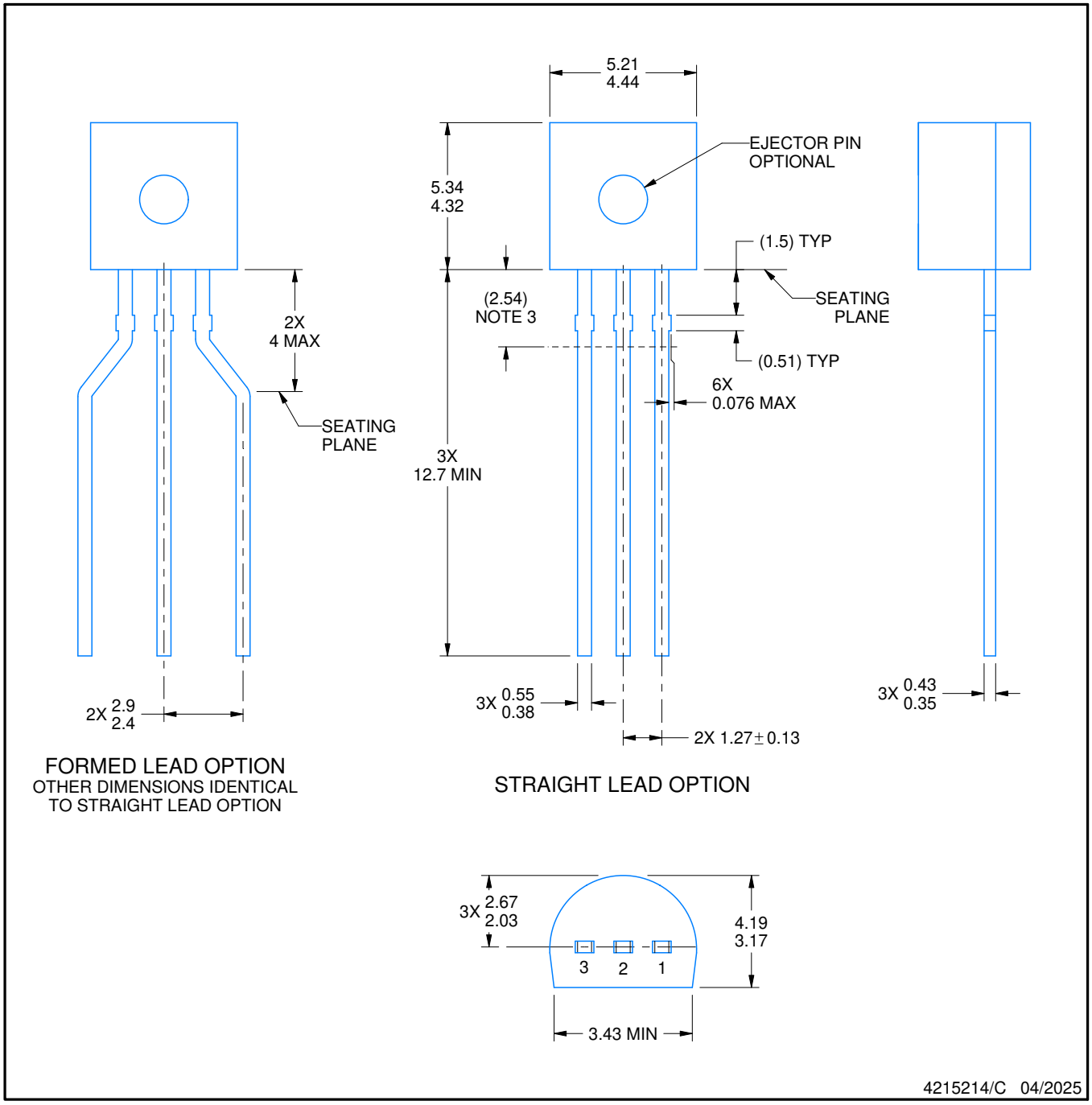




PACKAGE OUTLINE

TO-92 - 5.34 mm max height

TO-92



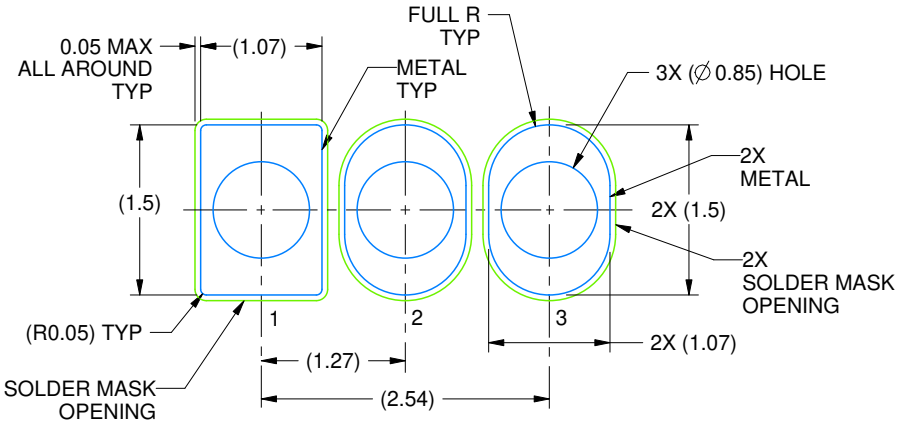
FORMED LEAD OPTION
OTHER DIMENSIONS IDENTICAL
TO STRAIGHT LEAD OPTION

STRAIGHT LEAD OPTION

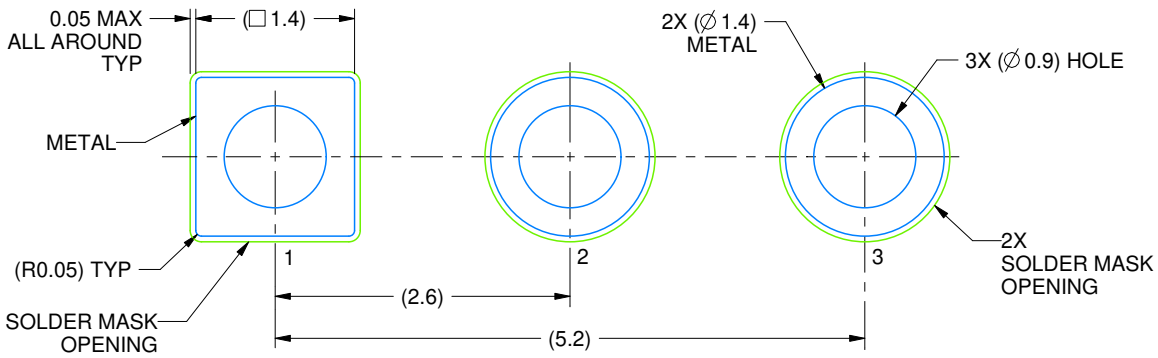
4215214/C 04/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



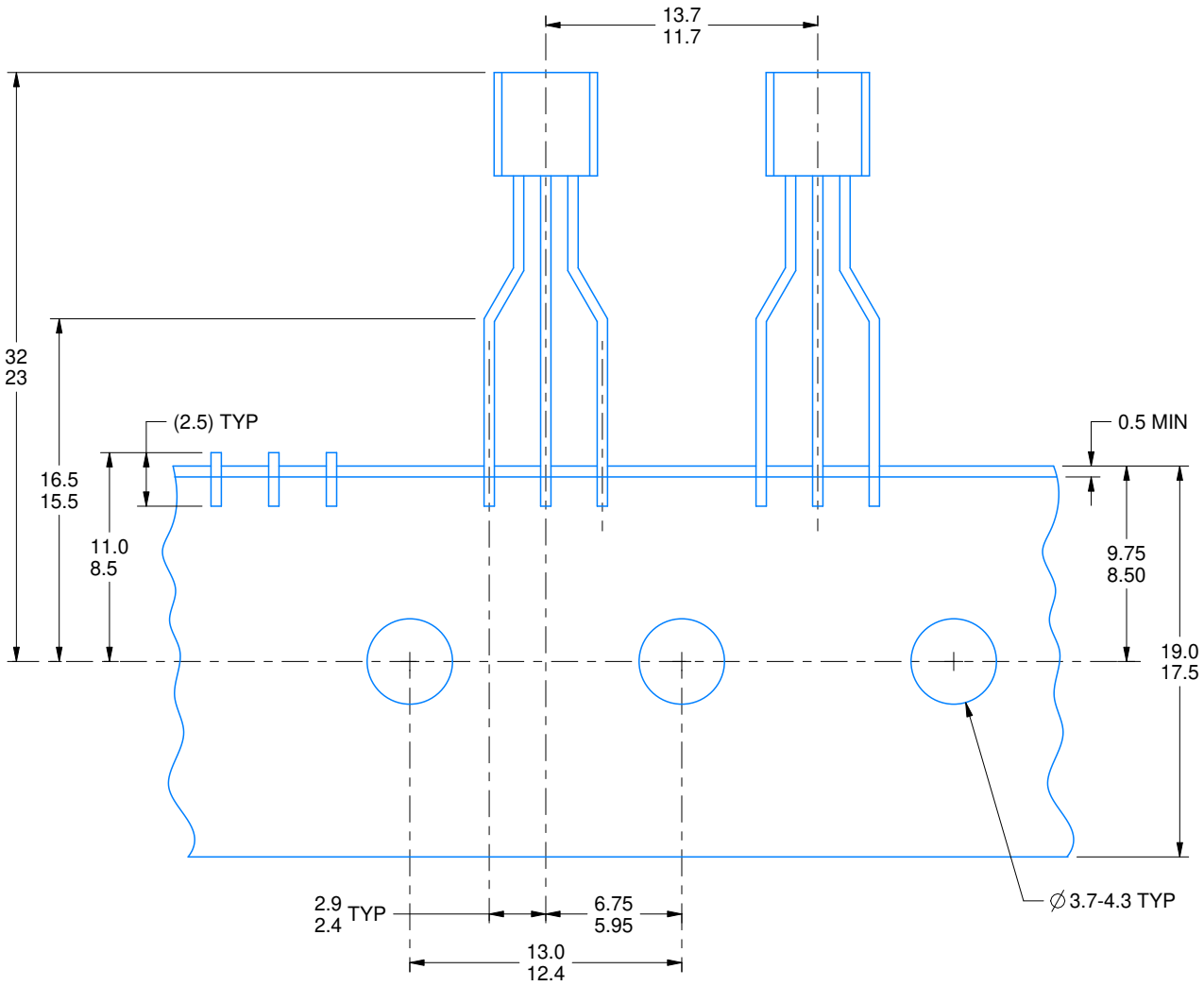
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/C 04/2025

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/C 04/2025

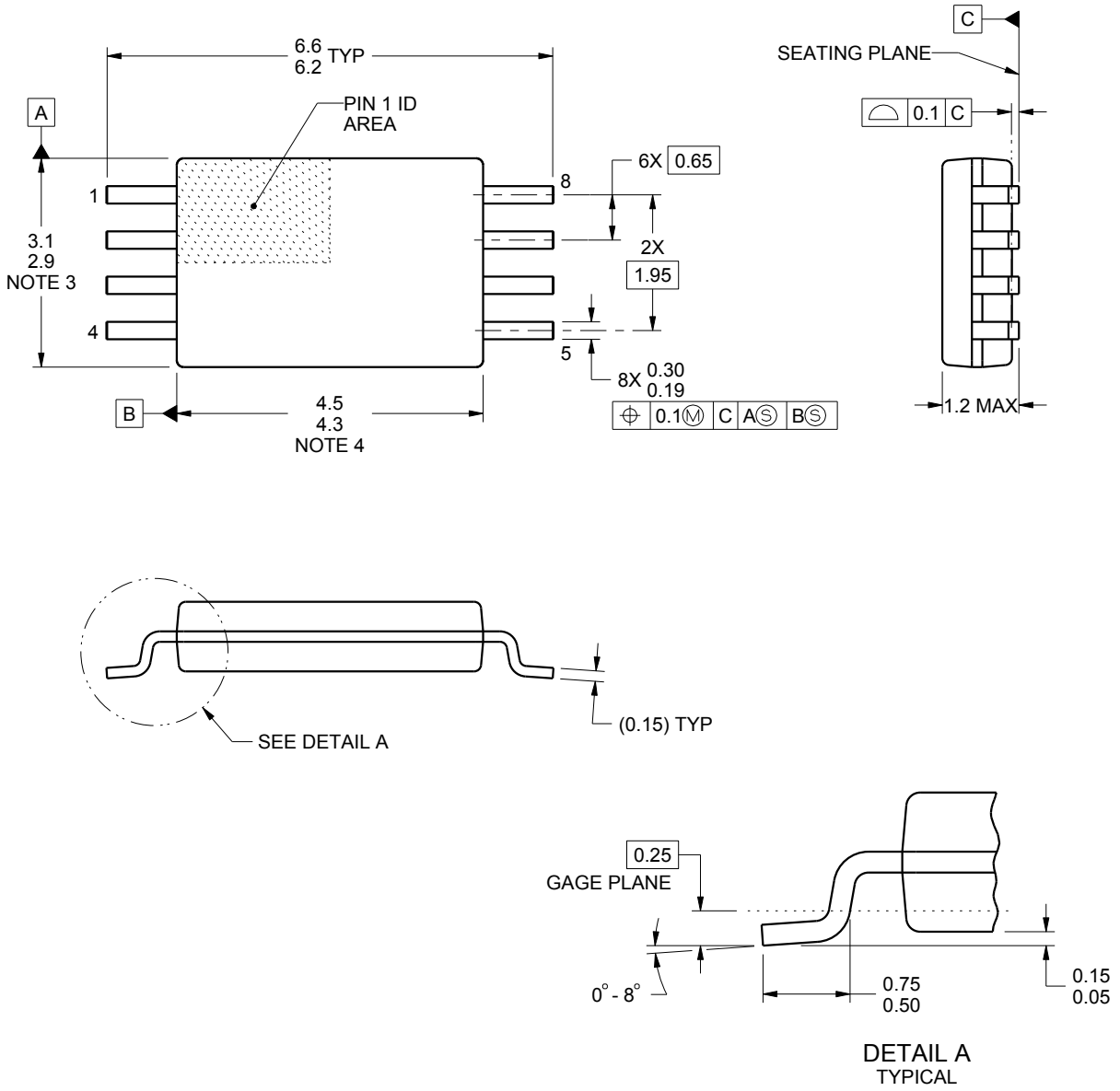


PACKAGE OUTLINE

PW0008A

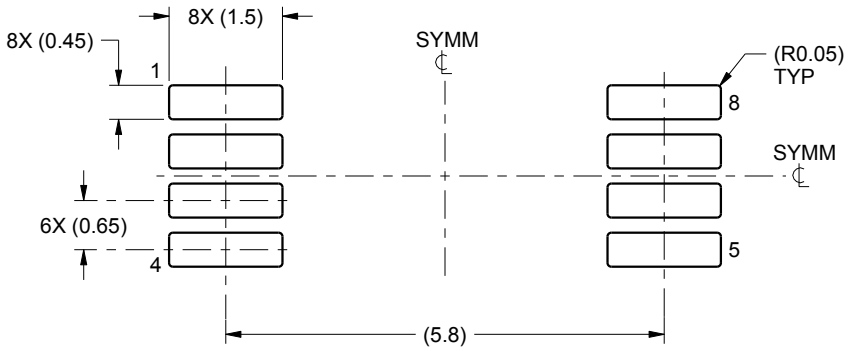
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

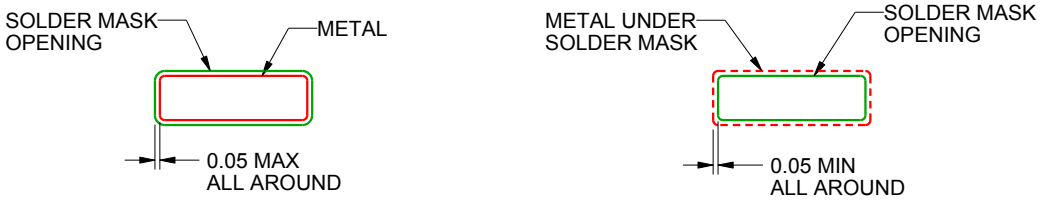


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

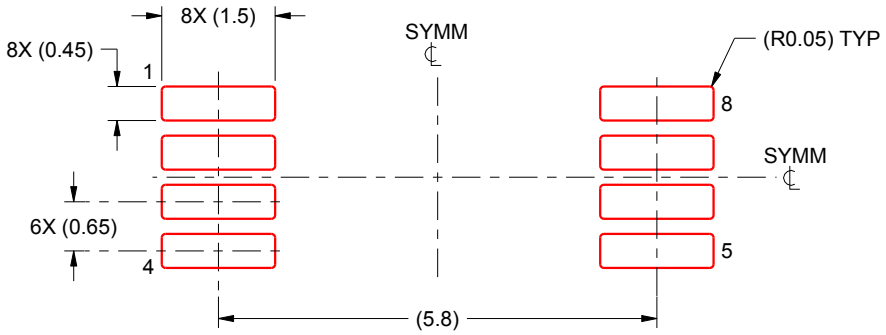


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025