2µA Supply Current, Low I_B, Zero-Drift Operational Amplifiers

FEATURES

- **Low Supply Current: 2µA Maximum (per Amplifier)**
- **Offset Voltage: 5µV Maximum**
- **Offset Voltage Drift: 0.02µV/°C Maximum**
- **Input Bias Current:**
  - **3pA Typical**
  - **30pA Maximum, –40°C to 85°C**
  - **100pA Maximum, –40°C to 125°C**
- **Integrated EMI Filter (114dB Rejection at 1.8GHz)**
- **Shutdown Current: 170nA Maximum (per Amplifier)**
- Rail-to-Rail Input and Output
- 1.7V to 5.25V Operating Supply Range
- A_{VOL}: 140dB Typical
- Low-Charge Power-Up for Duty Cycled Applications
- Specified Temperature Ranges:
  - –40°C to 85°C
  - –40°C to 125°C
- SC70, TSOT23, MS8, DFN10, TSSOP14 and QFN16 Packages

APPLICATIONS

- Signal Conditioning in Wireless Mesh Networks
- Portable Instrumentation Systems
- Low-Power Sensor Conditioning
- Gas Detection
- Temperature Measurement
- Medical Instrumentation
- Energy Harvesting Applications
- Low Power Current Sensing

DESCRIPTION

The LTC®2063/LTC2064/LTC2065 are single, dual, and quad low power, zero-drift, 20kHz amplifiers. The LTC2063/LTC2064/LTC2065 enable high resolution measurement at extremely low power levels.

Typical supply current is 1.4µA per amplifier with a maximum of 2µA. The available shutdown mode has been optimized to minimize power consumption in duty-cycled applications and features low charge loss during power-up, reducing total system power.

The LTC2063/LTC2064/LTC2065's self-calibrating circuitry results in very low input offset (5µV max) and offset drift (0.02µV/°C). The maximum input bias current is only 20pA and does not exceed 100pA over the full specified temperature range. The extremely low input bias current of the LTC2063/LTC2064/LTC2065 allows the use of high value power-saving resistors in the feedback network.

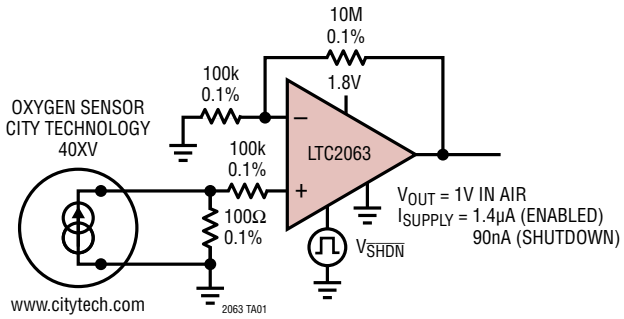
With its ultralow quiescent current and outstanding precision, the LTC2063/LTC2064/LTC2065 can serve as a signal chain building block in portable, energy harvesting and wireless sensor applications.

The LTC2063 is available in 6-lead SC70 and 5-lead TSOT-23 packages. The LTC2064 is available in 8-lead MSOP and 10-lead DFN packages. The LTC2065 is available in 14-lead TSSOP and 16-lead 3mm × 3mm QFN packages. These devices are fully specified over the –40°C to 85°C and –40°C to 125°C temperature ranges.

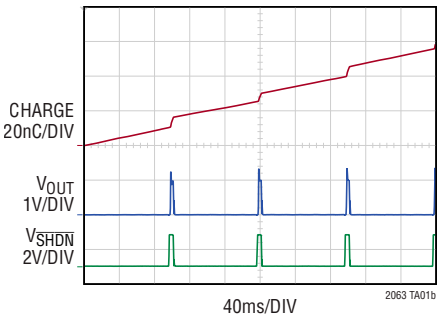
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TYPICAL APPLICATION

Micropower Precision Oxygen Sensor



Duty Cycle Lowers System Power



Rev. C

ABSOLUTE MAXIMUM RATINGS (Note 1)

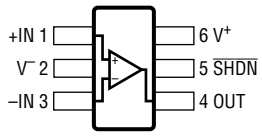
Total Supply Voltage (V^+ to V^-) 5.5V
Differential Input Current (+IN to –IN) (Note 2) .... ±10mA
Differential Input Voltage (+IN to –IN) 5.5V
Input Voltage +IN, –IN, $\overline{SHDN}$. (V^-) – 0.3V to (V^+) + 0.3V
Input Current +IN, –IN, $\overline{SHDN}$ (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Thermally Limited

Operating and Specified Temperature Range (Note 4)
LTC2063I/LTC2064I/LTC2065I ..... –40°C to 85°C
LTC2063H/LTC2064H/LTC2065H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION

LTC2063

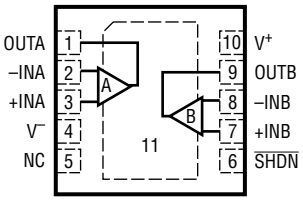
TOP VIEW



SC6 PACKAGE
6-LEAD PLASTIC SC70
θ_{JA} = 265°C/W (Note 5)

LTC2064

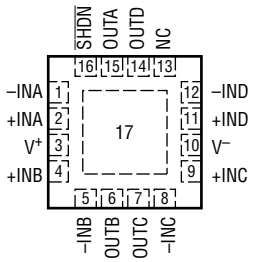
TOP VIEW



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W (Note 5)
EXPOSED PAD (PIN 11) IS CONNECTED TO V^- (PIN 4)
(PCB CONNECTION OPTIONAL)

LTC2065

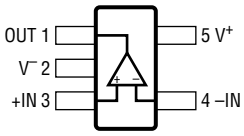
TOP VIEW



QFN16 PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
θ_{JA} = 68°C/W (NOTE 5)
EXPOSED PAD (PIN 17) MUST BE CONNECTED TO V^- (PIN 10)

LTC2063

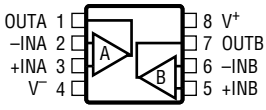
TOP VIEW



S5 PACKAGE
5-LEAD PLASTIC TSOT-23
θ_{JA} = 215°C/W (Note 5)

LTC2064

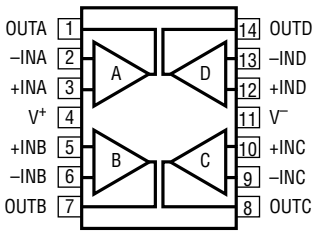
TOP VIEW



MS8 PACKAGE
8-LEAD PLASTIC MSOP
θ_{JA} = 163°C/W, θ_{JC} = 40°C/W (Note 5)

LTC2065

TOP VIEW



TSSOP14 PACKAGE
14-LEAD PLASTIC TSSOP
θ_{JA} = 100°C/W (NOTE 5)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2063ISC6#TRMPBF	LTC2063ISC6#TRPBF	LGTX	6-Lead Plastic SC70	–40°C to 85°C
LTC2063HSC6#TRMPBF	LTC2063HSC6#TRPBF	LGTX	6-Lead Plastic SC70	–40°C to 125°C
LTC2063IS5#TRMPBF	LTC2063IS5#TRPBF	LTGTW	5-Lead Plastic TSOT-23	–40°C to 85°C
LTC2063HS5#TRMPBF	LTC2063HS5#TRPBF	LTGTW	5-Lead Plastic TSOT-23	–40°C to 125°C
LTC2064IMS8#PBF	LTC2064IMS8#TRPBF	LTHCX	8-Lead Plastic MSOP	–40°C to 85°C
LTC2064HMS8#PBF	LTC2064HMS8#TRPBF	LTHCX	8-Lead Plastic MSOP	–40°C to 125°C
LTC2064IDD#PBF	LTC2064IDD#TRPBF	LHCW	10-Lead (3mm × 3mm)Plastic DFN	–40°C to 85°C
LTC2064HDD#PBF	LTC2064HDD#TRPBF	LHCW	10-Lead (3mm × 3mm)Plastic DFN	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2065IUD#PBF	LTC2065IUD#TRPBF	LHKT	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC2065HUD#PBF	LTC2065HUD#TRPBF	LHKT	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC2065IF#PBF	LTC2065IF#TRPBF	LTC2065	14-Lead TSSOP	–40°C to 85°C
LTC2065HF#PBF	LTC2065HF#TRPBF	LTC2065	14-Lead TSSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Parts ending with PBF are RoHS and WEEE compliant.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_S = 1.8V, V_{CM} = V_{OUT} = V_S/2, $V_{\overline{SHDN}}$ = 1.8V, R_L to V_S/2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 6)	V_S = 1.7V	 ●		1	±5 ±10	µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	–40°C to 85°C –40°C to 125°C	● ●			±0.03 ±0.06	µV/°C µV/°C
I_B	Input Bias Current (Note 7)				0.5		pA
I_{OS}	Input Offset Current (Note 7)				1		pA
i_n	Input Noise Current Spectral Density	f ≤ 100Hz			12		fA/√Hz
e_n	Input Noise Voltage Spectral Density	f ≤ 100Hz			230		nV/√Hz
$e_{n\ P-P}$	Input Noise Voltage	DC to 10Hz			4.8		μV_{P-P}
C_{IN}	Input Capacitance	Differential Common Mode			3.3 3.5		pF pF
V_{CMR}	Input Voltage Range	Guaranteed by CMRR	●	(V^-) – 0.1		(V^+) + 0.1	V
CMRR	Common Mode Rejection Ratio (Note 8)	V_{CM} = (V^-) – 0.1V to (V^+) + 0.1V R_L = 499k	 ●	103 100	130		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 1.7V to 5.25V R_L = 499k	 ●	108 106	126		dB dB
A_{VOL}	Open Loop Gain	V_{OUT} = (V^-) + 0.1V to (V^+) – 0.1V, R_L = 499k			135		dB
V_{OL}	Output Voltage Swing Low ($V_{OUT} - V^-$)	R_L = 499k			0.05		mV
		R_L = 10k	 ●		3	10 20	mV mV
V_{OH}	Output Voltage Swing High ($V^+ - V_{OUT}$)	R_L = 499k			0.1		mV
		R_L = 10k	 ●		4.5	10 50	mV mV
I_{SC}	Output Short Circuit Current	Sourcing	 ●	5.8 5.6	7.5		mA mA
		Sinking	 ●	10.4 5	13		mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_S = 1.8V, V_{CM} = V_{OUT} = V_S/2, $V_{\overline{SHDN}}$ = 1.8V, R_L to V_S/2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	A_V = +1			3.5		V/ms
GBW	Gain Bandwidth Product	R_L = 499k			20		kHz
t_{ON}	Power-Up Time				2		ms
f_C	Internal Chopping Frequency				5		kHz
V_S	Supply Voltage Range	Guaranteed by PSRR	●	1.7		5.25	V
I_S	Supply Current per Amplifier	No Load			1.3	2	µA
		–40°C to 85°C	●			2.5	µA
		–40°C to 125°C	●			4	µA
		In Shutdown ($\overline{SHDN}$ = V^-)			90	170	nA
		–40°C to 85°C	●			250	nA
		–40°C to 125°C	●			500	nA
V_H	$\overline{SHDN}$ Pin Threshold, Logic High (Referred to V^-)		●	1.0			V
V_L	$\overline{SHDN}$ Pin Threshold, Logic Low (Referred to V^-)		●			0.65	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0V	●	–150		–20	nA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_S = 5V, V_{CM} = V_{OUT} = V_S/2, $V_{\overline{SHDN}}$ = 5V, R_L to V_S/2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 6)	V_S = 5.25V			1	±5	µV
			●			±10	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	–40°C to 85°C	●			±0.02	µV/°C
		–40°C to 125°C	●			±0.05	µV/°C
I_B	Input Bias Current				–3	±20	pA
		–40°C to 85°C	●			±30	pA
		–40°C to 125°C	●			±100	pA
I_{OS}	Input Offset Current				1.5	±20	pA
		–40°C to 85°C	●			±30	pA
		–40°C to 125°C	●			±100	pA
i_n	Input Noise Current Spectral Density	f ≤ 100Hz			12		fA/√Hz
e_n	Input Noise Voltage Spectral Density	f ≤ 100Hz			220		nV/√Hz
$e_{n\ P-P}$	Input Noise Voltage	DC to 10Hz			4.6		μV_{P-P}
C_{IN}	Input Capacitance	Differential			3.3		pF
		Common Mode			3.5		pF
V_{CMR}	Input Voltage Range	Guaranteed by CMRR	●	(V^-) – 0.1		(V^+) + 0.1	V
CMRR	Common Mode Rejection Ratio	V_{CM} = (V^-) – 0.1V to (V^+) + 0.1V		111	130		dB
		R_L = 499k	●	108			dB
PSRR	Power Supply Rejection Ratio	V_S = 1.7V to 5.25V		108	126		dB
		R_L = 499k	●	106			dB
EMIRR	EMI Rejection Ratio	f = 400MHz			81		dB
	V_{RF} = 100mV_{PK}	f = 900MHz			102		dB
	EMIRR = 20 • log($V_{RF}/\Delta V_{OS}$)	f = 1800MHz			114		dB
		f = 2400MHz			100		dB
A_{VOL}	Open Loop Gain	V_{OUT} = (V^-) + 0.1V to (V^+) – 0.1V, R_L = 499k		112	140		dB
			●	110			dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_S = 5V, V_{CM} = V_{OUT} = V_S/2, $V_{\overline{SHDN}}$ = 5V, R_L to V_S/2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing Low (V_{OUT} – V^-)	R_L = 499k			0.1		mV
		R_L = 10k	 ●		5.5	15 20	mV mV
V_{OH}	Output Voltage Swing High (V^+ – V_{OUT})	R_L = 499k			0.15		mV
		R_L = 10k	 ●		7	15 20	mV mV
I_{SC}	Output Short Circuit Current	Sourcing	 ●	30 16	51		mA mA
		Sinking	 ●	20 5	48		mA mA
SR	Slew Rate	A_V = +1			3.5		V/ms
GBW	Gain Bandwidth Product	R_L = 499k			20		kHz
t_{ON}	Power-Up Time				2		ms
f_C	Internal Chopping Frequency				5		kHz
V_S	Supply Voltage Range	Guaranteed by PSRR	●	1.7		5.25	V
I_S	Supply Current per Amplifier	No Load –40°C to 85°C –40°C to 125°C	 ● ●		1.4	2 2.5 4	µA µA µA
		In Shutdown ($\overline{SHDN}$ = V^-) –40°C to 85°C –40°C to 125°C	 ● ●		90	170 250 500	nA nA nA
V_H	$\overline{SHDN}$ Pin Threshold, Logic High (Referred to V^-)		●	1.8			V
V_L	$\overline{SHDN}$ Pin Threshold, Logic Low (Referred to V^-)		●			0.8	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0V	●	–150		–20	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by two series connected ESD protection diodes to each power supply. The input current should be limited to less than 10mA. The input voltage should not exceed 300mV beyond the power supply.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC2063I/LTC2064I/LTC2065I are guaranteed to meet specified performance from –40°C to 85°C. The LTC2063H/LTC2064H/LTC2065H are guaranteed to meet specified performance from –40°C to 125°C.

Note 5: Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

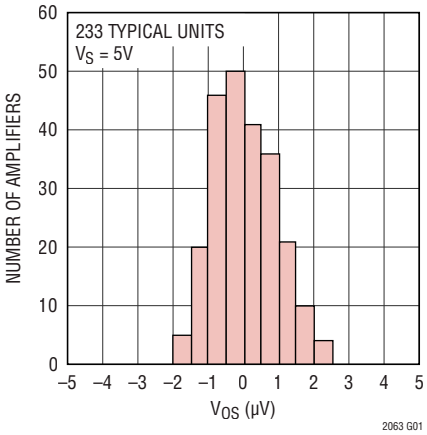
Note 6: These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing. V_{OS} is measured to a limit determined by test equipment capability.

Note 7: Input bias current is only production tested at 5V. Input bias current at 1.8V is expected to meet or exceed 5V specifications.

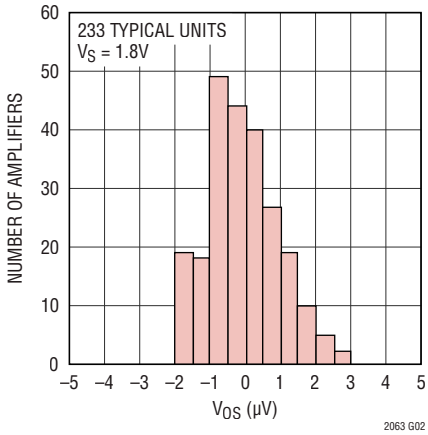
Note 8: Minimum specifications for these parameters are limited by noise and the capabilities of the automated test system.

TYPICAL PERFORMANCE CHARACTERISTICS

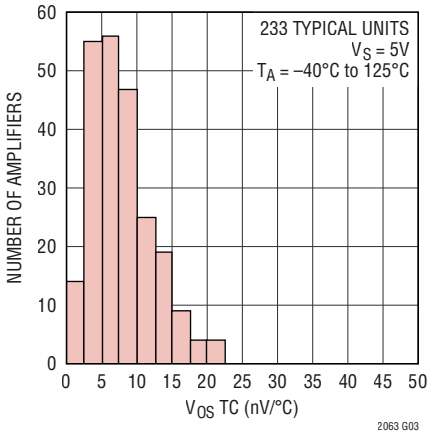
Input Offset Voltage Distribution



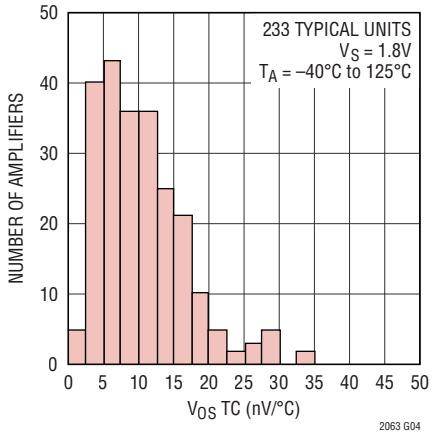
Input Offset Voltage Distribution



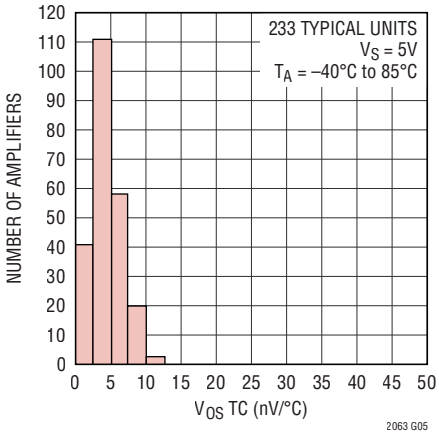
Input Offset Voltage Drift Distribution



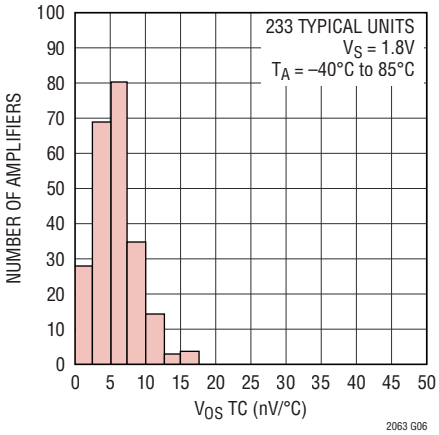
Input Offset Voltage Drift Distribution



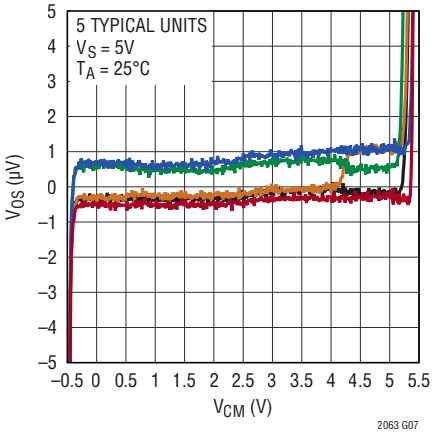
Input Offset Voltage Drift Distribution



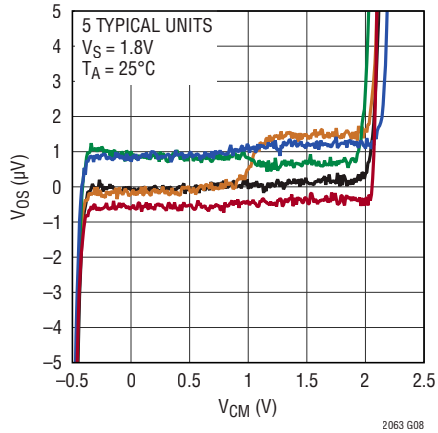
Input Offset Voltage Drift Distribution



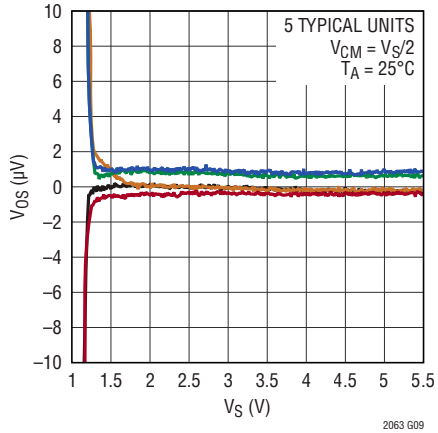
Input Offset Voltage vs Input Common Mode Voltage



Input Offset Voltage vs Input Common Mode Voltage

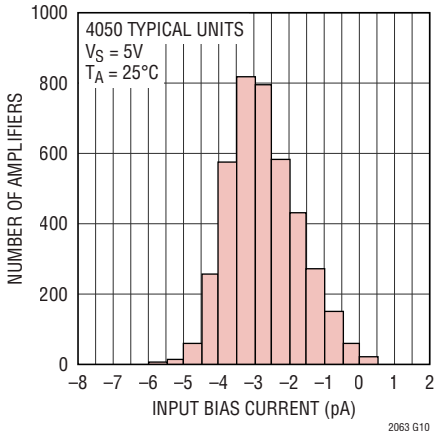


Input Offset Voltage vs Supply Voltage

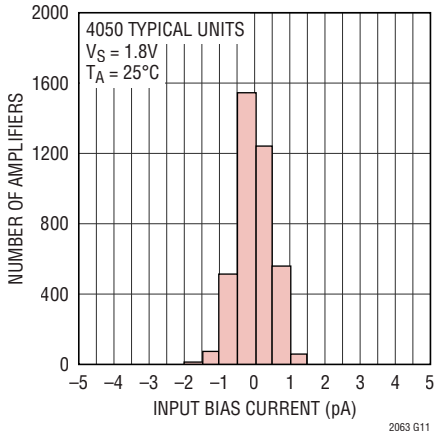


TYPICAL PERFORMANCE CHARACTERISTICS

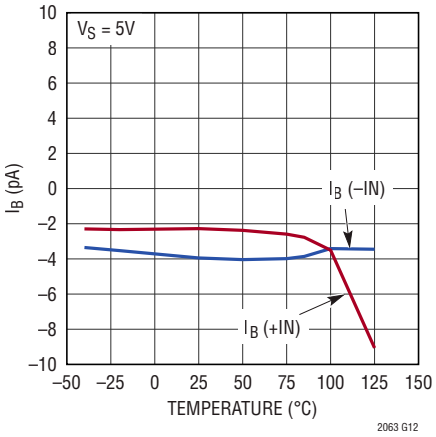
Input Bias Current Distribution



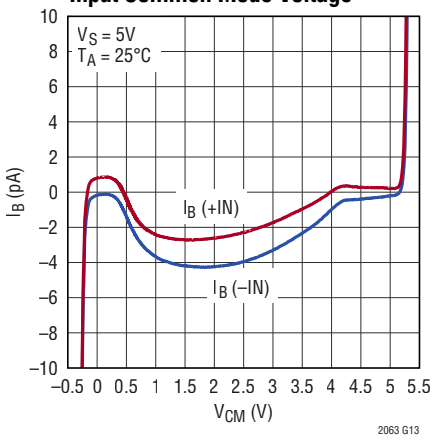
Input Bias Current Distribution



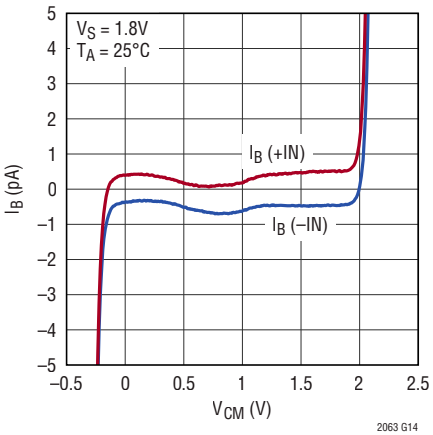
Input Bias Current vs Temperature



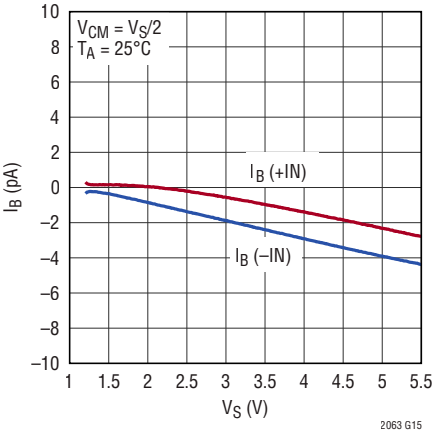
Input Bias Current vs Input Common Mode Voltage



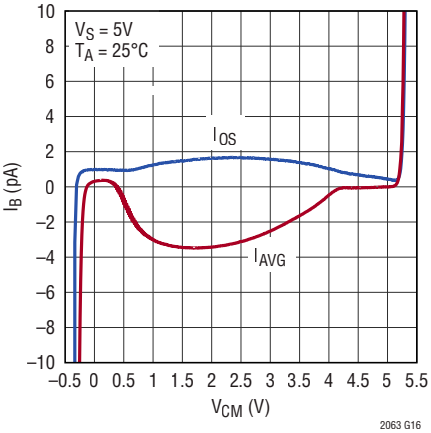
Input Bias Current vs Input Common Mode Voltage



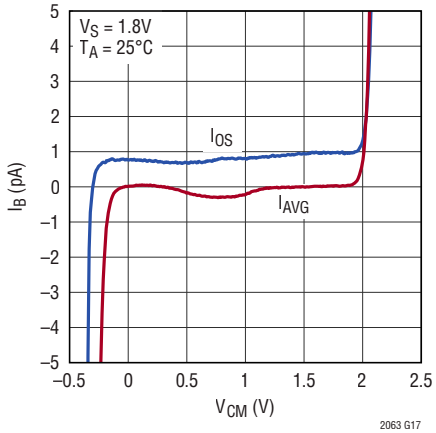
Input Bias Current vs Supply Voltage



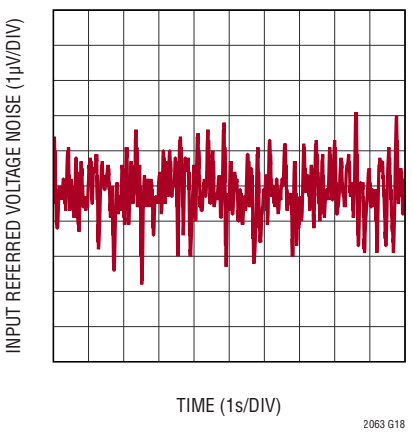
Input Offset and Average Current vs Input Common Mode Voltage



Input Offset and Average Current vs Input Common Mode Voltage

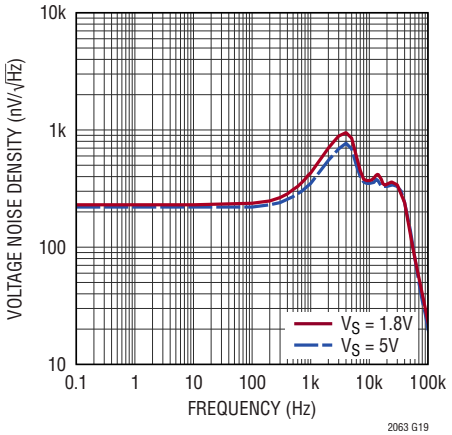


DC to 10Hz Voltage Noise

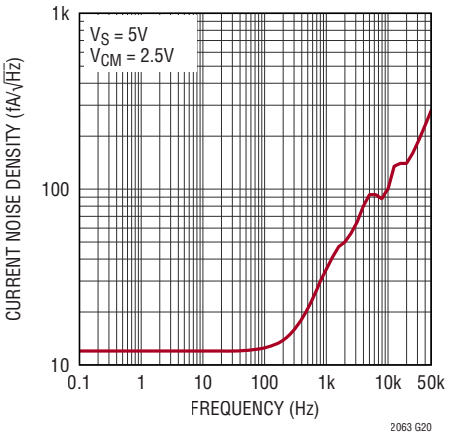


TYPICAL PERFORMANCE CHARACTERISTICS

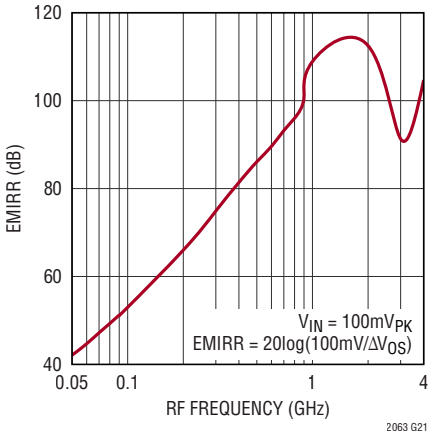
Input Referred Voltage Noise Density



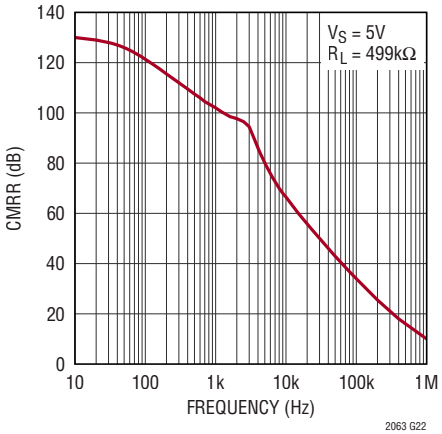
Input Referred Current Noise Density



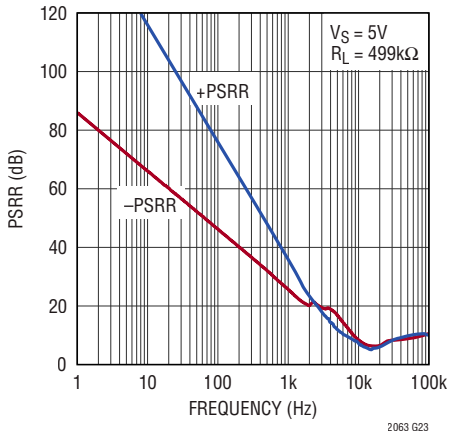
EMI Rejection vs Frequency



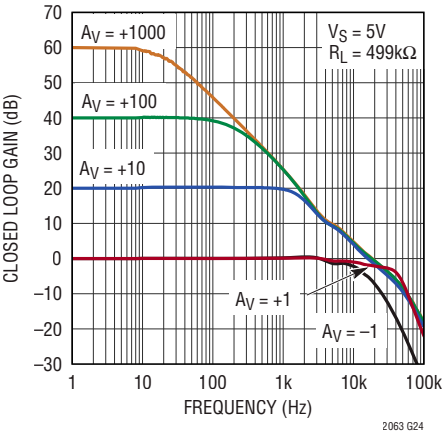
Common Mode Rejection Ratio vs Frequency



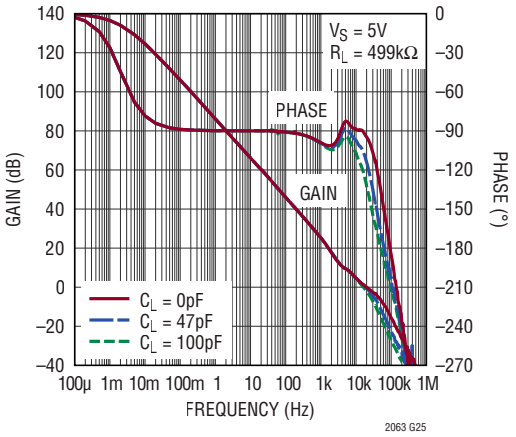
Power Supply Rejection Ratio vs Frequency



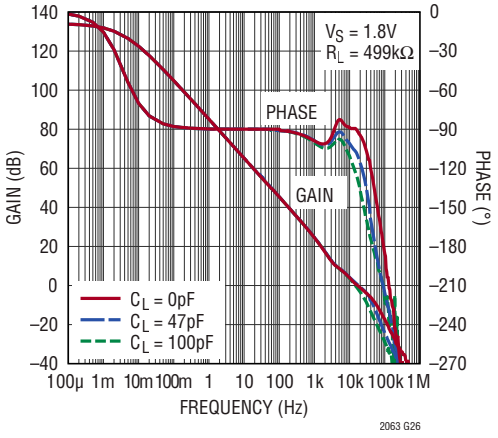
Closed Loop Gain vs Frequency



Open Loop Gain and Phase vs Frequency

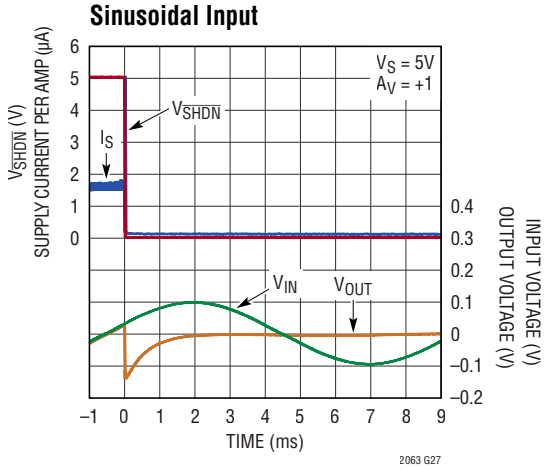


Open Loop Gain and Phase vs Frequency

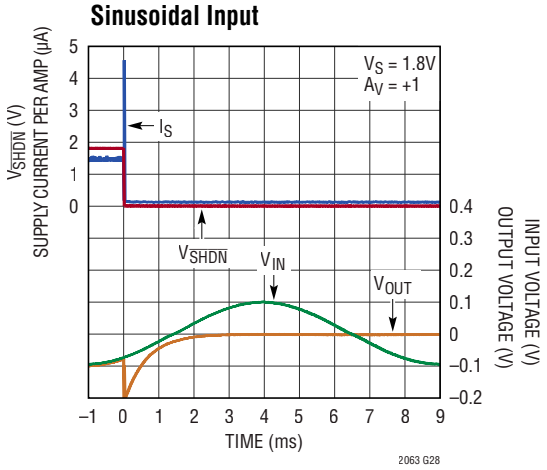


TYPICAL PERFORMANCE CHARACTERISTICS

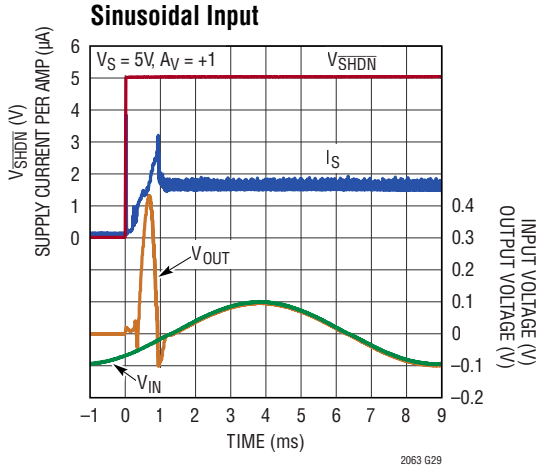
Shutdown Transient with Sinusoidal Input



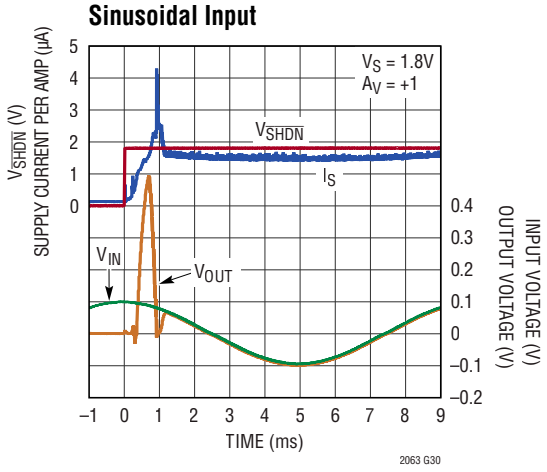
Shutdown Transient with Sinusoidal Input



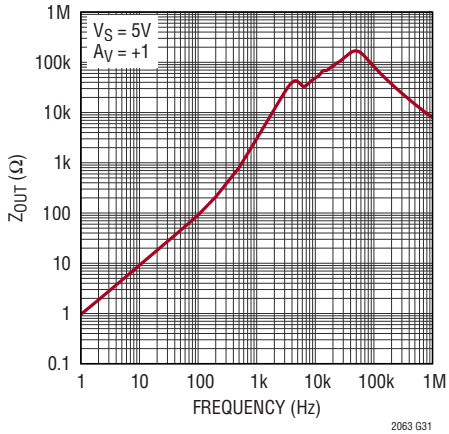
Enable Transient with Sinusoidal Input



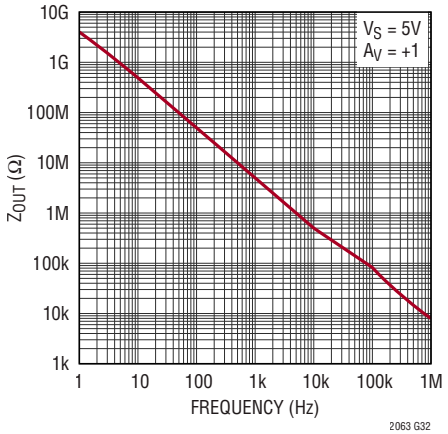
Enable Transient with Sinusoidal Input



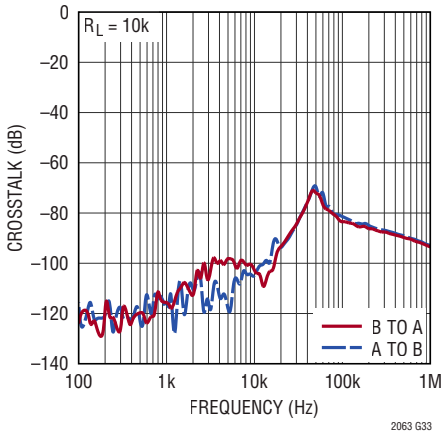
Closed Loop Output Impedance vs Frequency



Output Impedance in Shutdown vs Frequency

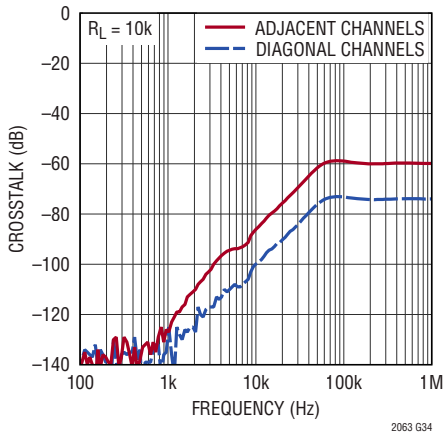


LTC2064 Crosstalk vs Frequency

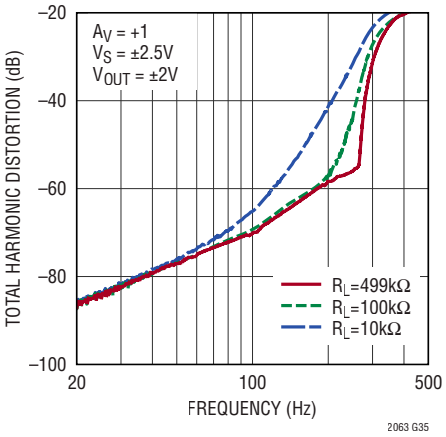


TYPICAL PERFORMANCE CHARACTERISTICS

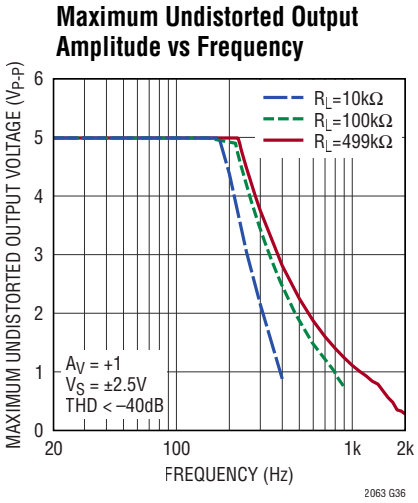
LTC2065 Crosstalk vs Frequency



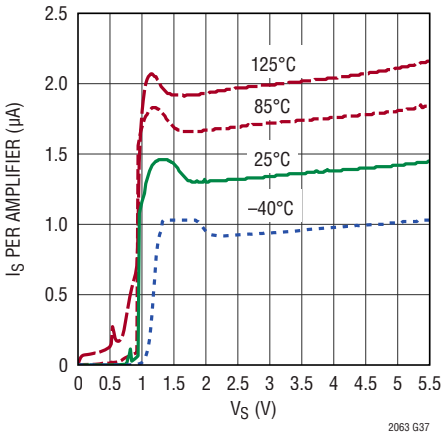
THD vs Frequency



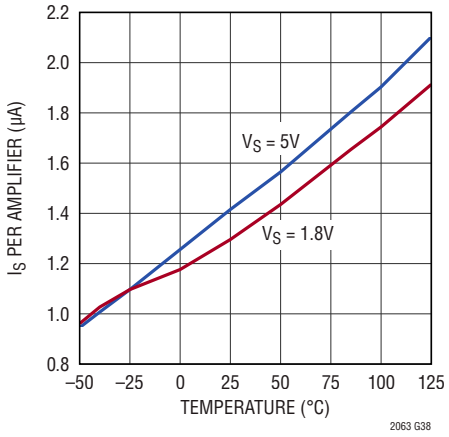
Maximum Undistorted Output Amplitude vs Frequency



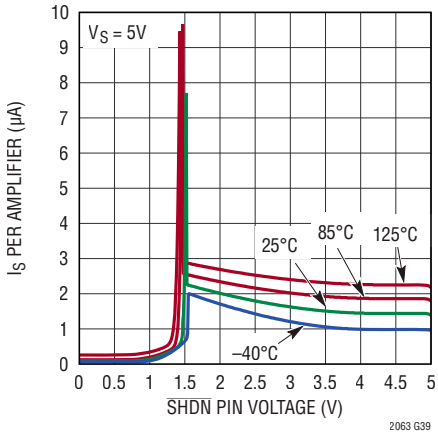
Supply Current vs Supply Voltage



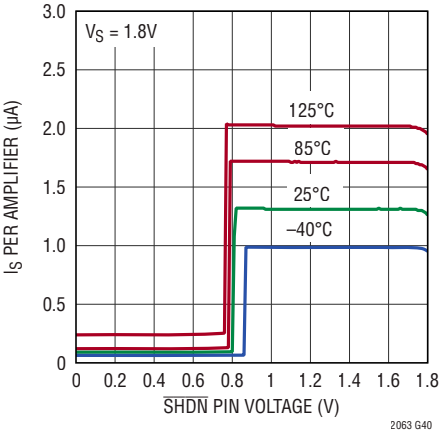
Supply Current vs Temperature



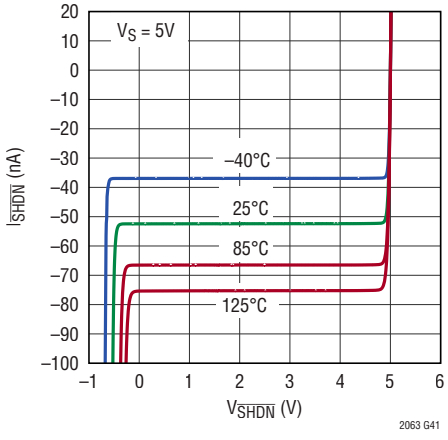
Supply Current vs $\overline{SHDN}$ Pin Voltage



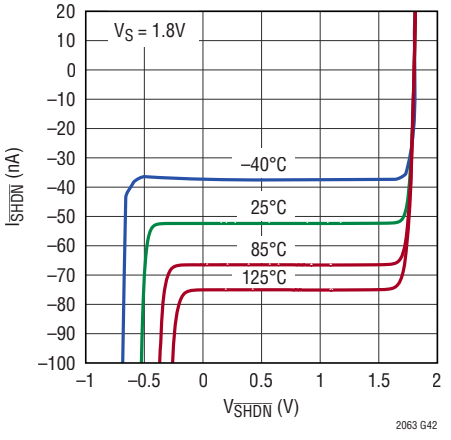
Supply Current vs $\overline{SHDN}$ Pin Voltage



$\overline{SHDN}$ Pin Pull-Up Current vs $\overline{SHDN}$ Pin Voltage

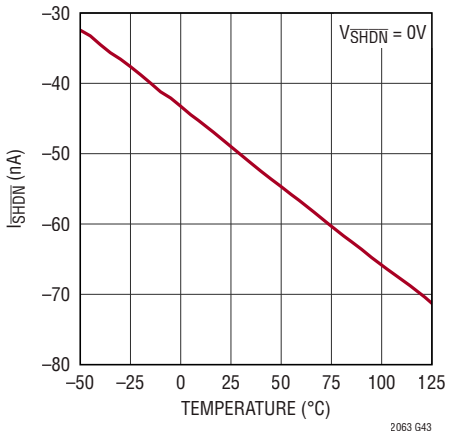


$\overline{SHDN}$ Pin Pull-Up Current vs $\overline{SHDN}$ Pin Voltage

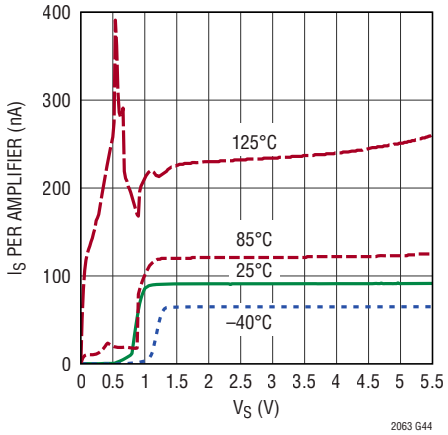


TYPICAL PERFORMANCE CHARACTERISTICS

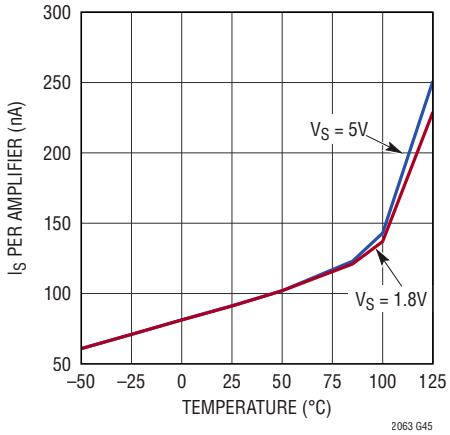
$\overline{SHDN}$ Pin Current vs Temperature



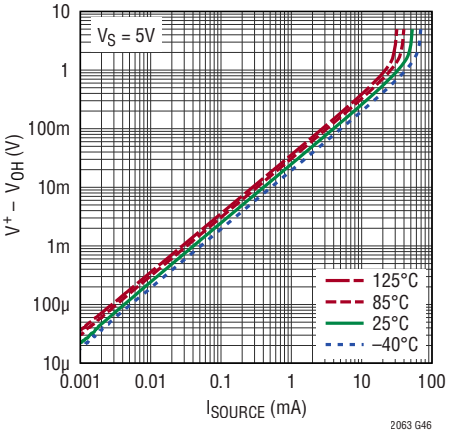
Shutdown Supply Current vs Supply Voltage



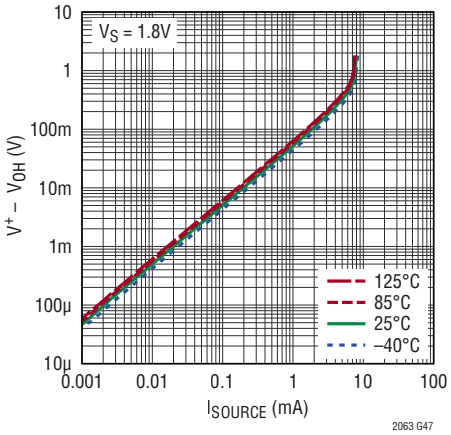
Shutdown Supply Current vs Temperature



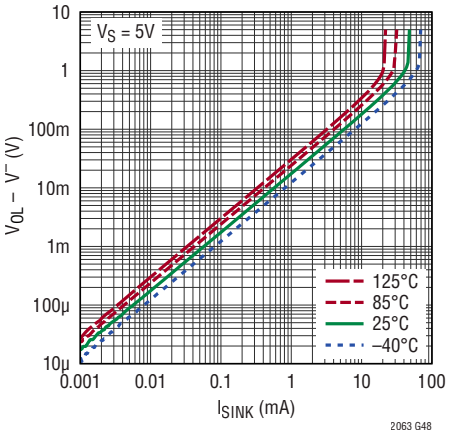
Output Voltage Swing High vs Load Current



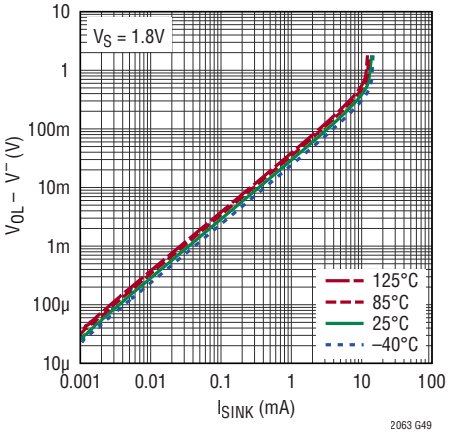
Output Voltage Swing High vs Load Current



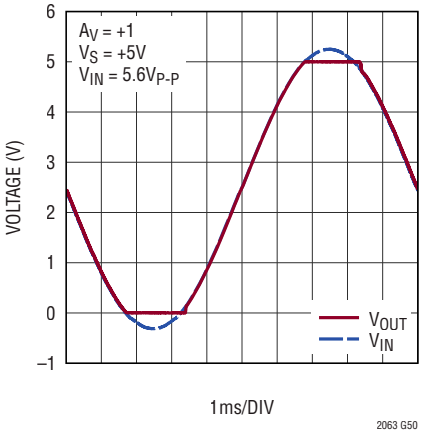
Output Voltage Swing Low vs Load Current



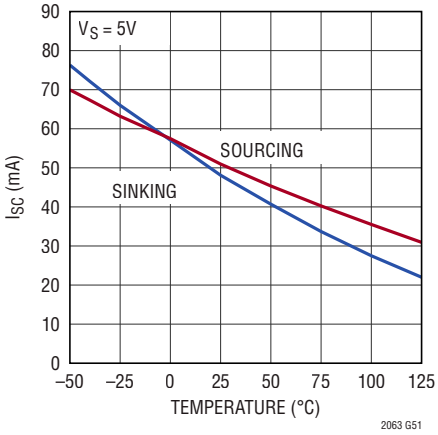
Output Voltage Swing Low vs Load Current



No Phase Reversal

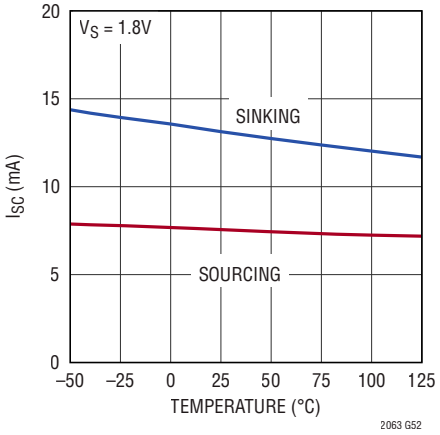


Output Short Circuit Current vs Temperature

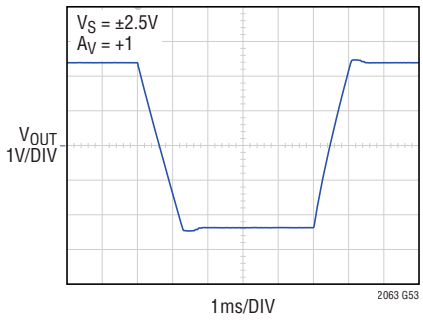


TYPICAL PERFORMANCE CHARACTERISTICS

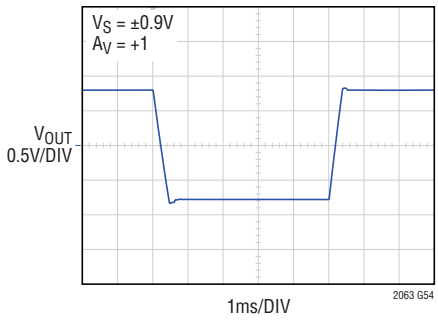
Output Short Circuit Current vs Temperature



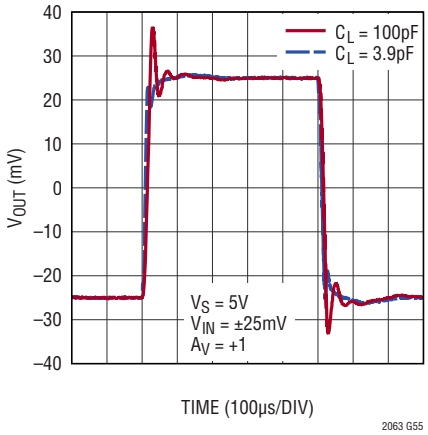
Large Signal Response



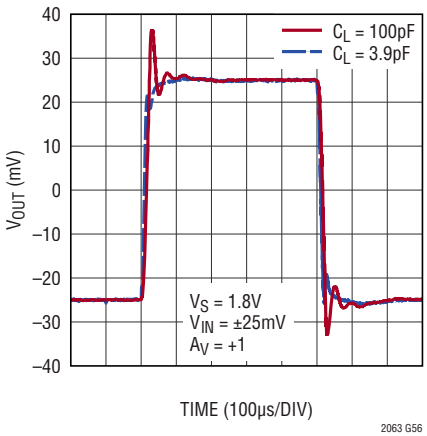
Large Signal Response



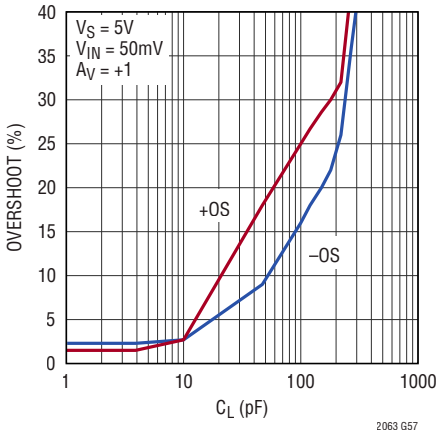
Small Signal Response



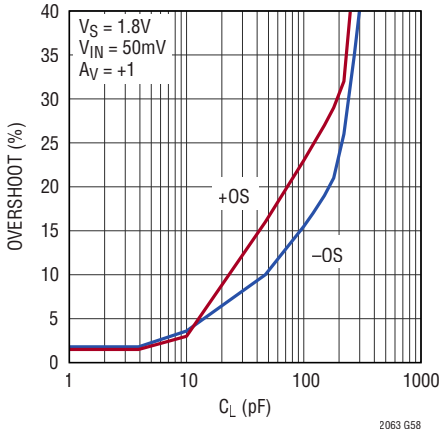
Small Signal Response



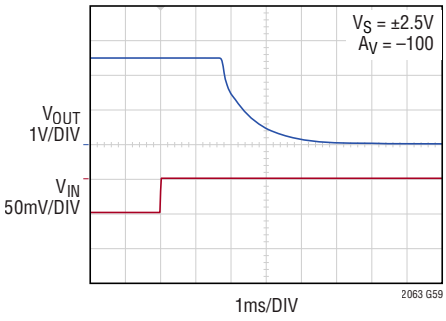
Small Signal Overshoot vs Load Capacitance



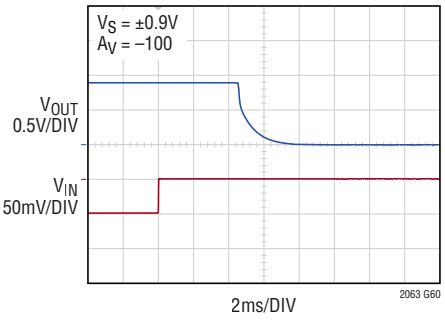
Small Signal Overshoot vs Load Capacitance



Positive Output Overload Recovery

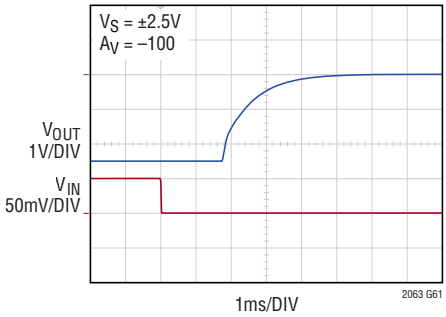


Positive Output Overload Recovery

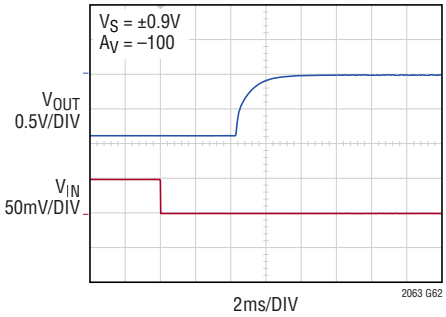


TYPICAL PERFORMANCE CHARACTERISTICS

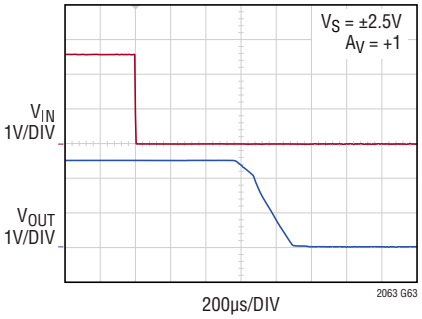
Negative Output Overload Recovery



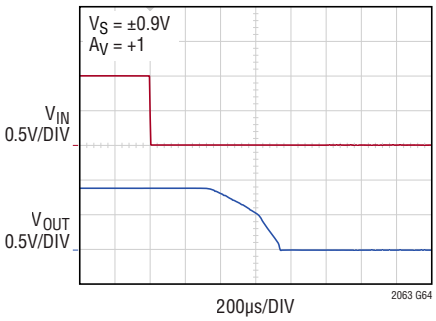
Negative Output Overload Recovery



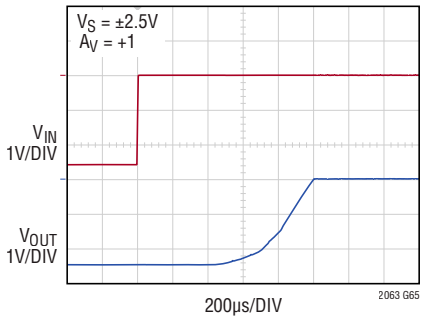
Positive Input Overload Recovery



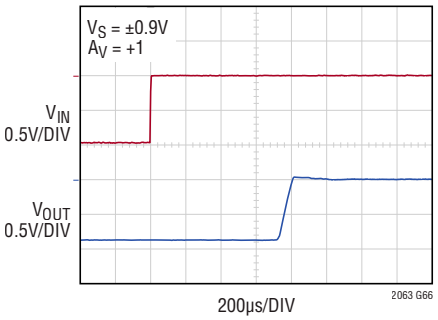
Positive Input Overload Recovery



Negative Input Overload Recovery



Negative Input Overload Recovery



PIN FUNCTIONS

OUT: Amplifier Output

–IN: Inverting Amplifier Input

+IN: Noninverting Amplifier Input

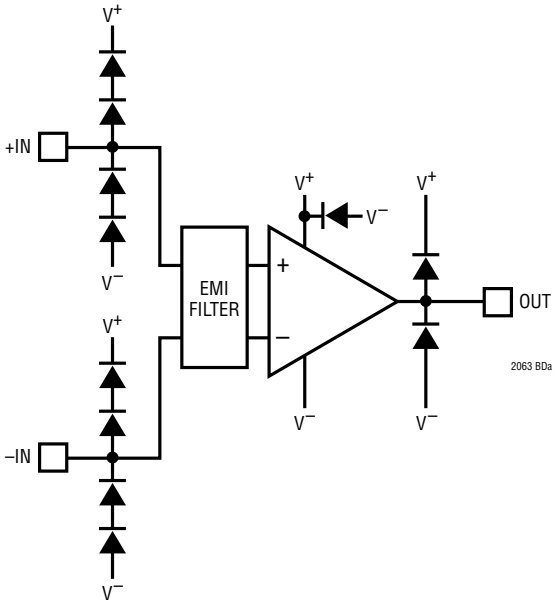
V^+: Positive Power Supply. A bypass capacitor should be used between supply pins and ground.

$V^–$: Negative Power Supply. A bypass capacitor should be used between supply pins and ground.

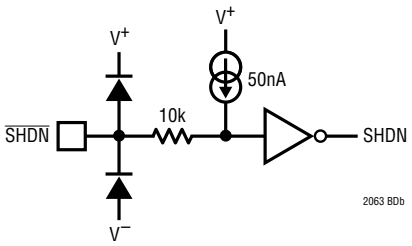
$\overline{SHDN}$: Shutdown Control Pin. The $\overline{SHDN}$ pin threshold is referenced to $V^–$. If tied to V^+, the part is enabled. If tied to $V^–$, the part is disabled and draws less than 170nA of supply current per amplifier. It is recommended to not float this pin.

BLOCK DIAGRAM

Amplifier



Shutdown Circuit



APPLICATIONS INFORMATION

Using the LTC2063/LTC2064/LTC2065

The LTC2063/LTC2064/LTC2065 are single, dual and quad zero-drift operational amplifiers with the open-loop voltage gain and bandwidth characteristics of a conventional operational amplifier. Advanced circuit techniques allow the LTC2063/LTC2064/LTC2065 to operate continuously through its entire bandwidth while self-calibrating unwanted errors.

Input Voltage Noise

Zero-drift amplifiers like the LTC2063/LTC2064/LTC2065 achieve low input offset voltage and 1/f noise by heterodyning DC and flicker noise to higher frequencies. In early zero-drift amplifiers, this process resulted in idle tones at the self-calibration frequency, often referred to as the chopping frequency. These artifacts made early zero-drift amplifiers difficult to use. The advanced circuit techniques used by the LTC2063/LTC2064/LTC2065 suppress these spurious artifacts, allowing for trouble-free use.

Input Current Noise

For applications with high source and feedback impedances, input current noise can be a significant contributor to total output noise. For this reason, it is important to consider noise current interaction with circuit elements placed at the amplifier's inputs.

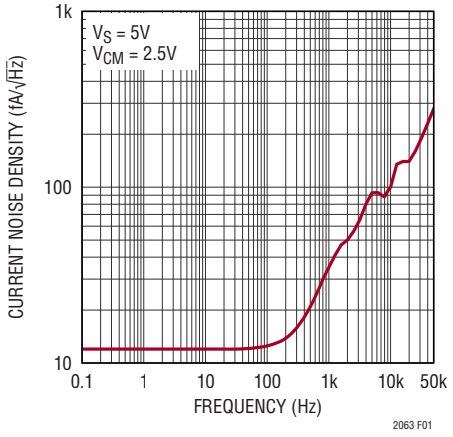


Figure 1. Input Current Noise Spectrum

The current noise spectrum of the LTC2063/LTC2064/LTC2065 is shown in Figure 1. Low input current noise is achieved through the use of MOSFET input devices and self-calibration techniques to eliminate 1/f current noise. As with all zero-drift amplifiers, there is an increase in current noise at the offset-nulling frequency. This phenomenon is discussed in the Input Bias Current and Clock Feedthrough section.

Input current noise also rises with frequency due to capacitive coupling of MOSFET channel thermal noise.

Input Bias Current and Clock Feedthrough

The input bias current of zero-drift amplifiers has different characteristics than that of a traditional operational amplifier. The specified input bias current is the DC average of transient currents which conduct due to the input stage's switching circuitry. In addition to this, junction leakages can contribute additional input bias current at elevated temperatures. Through careful design and the use of an innovative boot-strap circuit, the input bias current of the LTC2063/LTC2064/LTC2065 does not exceed 20pA at room and 100pA over the full temperature range. This minimizes bias current induced errors even in high impedance circuits.

Transient switching currents at the input interact with source and feedback impedances, producing error voltages which are indistinguishable from a valid input signal. The resulting error voltages are amplified by the amplifier's closed-loop gain, which acts as a filter, attenuating frequency components above the circuit bandwidth. This phenomenon is known as clock feedthrough and is present in all zero-drift amplifiers. Understanding the cause and effect of clock feedthrough is important when using zero-drift amplifiers.

For zero-drift amplifiers, clock feedthrough is proportional to source and feedback impedances, as well as the magnitude of the transient currents. These transient currents have been minimized in the LTC2063/LTC2064/LTC2065 to allow use with high source and feedback impedances.

APPLICATIONS INFORMATION

Many circuit designs require high feedback impedances to minimize power consumption and/or require a sensor which is intrinsically high impedance. In these cases, a capacitor can be used, either at the input or across the feedback resistor, to limit the bandwidth of the closed-loop system. Doing so will effectively filter out the clock feedthrough signal.

Thermocouple Effects

In order to achieve accuracy on the microvolt level, thermocouple effects must be considered. Any connection of dissimilar metals forms a thermoelectric junction and generates a small temperature-dependent voltage. Also known as the Seebeck Effect, these thermal EMFs can be the dominant error source in low-drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solder are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C, which significantly exceeds the maximum drift specification of the LTC2063/LTC2064/LTC2065. Figures 2 and 3 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

In order to minimize thermocouple-induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits. Doing so will often reduce thermocouple noise substantially. A summary of techniques can be found in Figure 4.

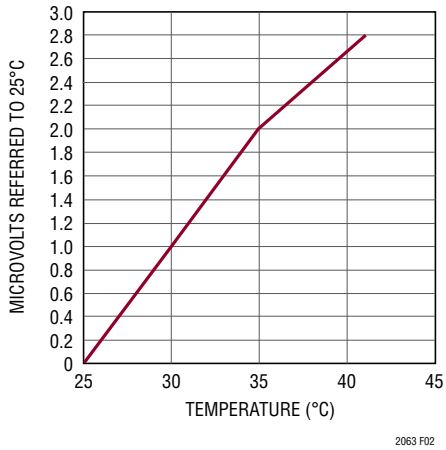


Figure 2. Thermal EMF Generated by Two Copper Wires from Different Manufacturers

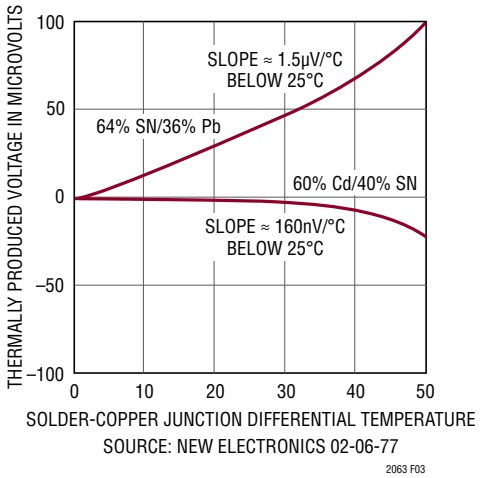
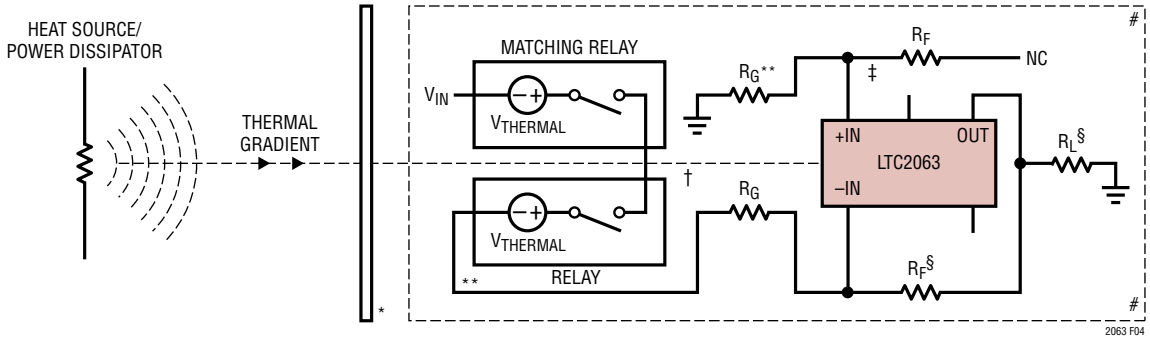


Figure 3. Solder-Copper Thermal EMFs

Leakage Effects

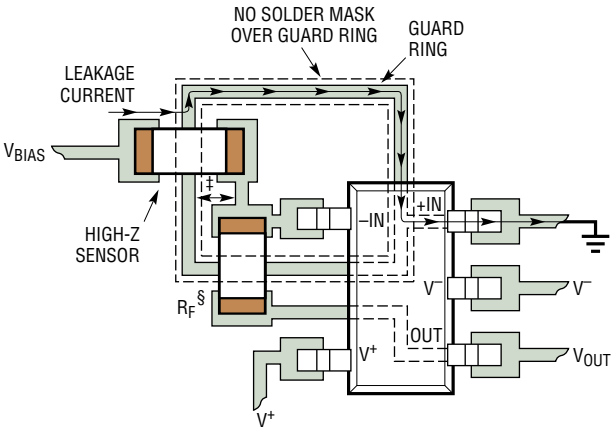
Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of sub-nanoamp signals. High voltage and high temperature applications are especially susceptible to these issues. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

APPLICATIONS INFORMATION

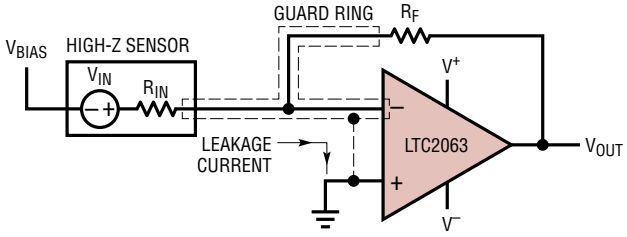


* CUT SLOTS IN PCB FOR THERMAL ISOLATION.
** INTRODUCE DUMMY JUNCTIONS AND COMPONENTS TO OFFSET UNAVOIDABLE JUNCTIONS OR CANCEL THERMAL EMFs.
† ALIGN INPUTS SYMMETRICALLY WITH RESPECT TO THERMAL GRADIENTS.
‡ INTRODUCE DUMMY TRACES AND COMPONENTS FOR SYMMETRICAL THERMAL HEAT SINKING.
§ LOADS AND FEEDBACK CAN DISSIPATE POWER AND GENERATE THERMAL GRADIENTS. BE AWARE OF THEIR THERMAL EFFECTS.
# COVER CIRCUIT TO PREVENT AIR CURRENTS FROM CREATING THERMAL GRADIENTS.

Figure 4. Techniques for Minimizing Thermocouple-Induced Errors



‡ NO LEAKAGE CURRENT, $V_{–IN} = V_{+IN}$
§ AVOID DISSIPATING SIGNIFICANT AMOUNTS OF POWER IN THIS RESISTOR. IT WILL GENERATE THERMAL GRADIENTS WITH RESPECT TO THE INPUT PINS AND LEAD TO THERMOCOUPLE-INDUCED ERROR. THERMALLY ISOLATE OR ALIGN WITH INPUTS IF RESISTOR WILL CAUSE HEATING.



LEAKAGE CURRENT IS ABSORBED BY GROUND INSTEAD OF CAUSING A MEASUREMENT ERROR.

2063 F05

Figure 5. Example Layout of Inverting Amplifier with Leakage Guard Ring

APPLICATIONS INFORMATION

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential very close to that of the inputs. The ring must be tied to a low impedance node. For inverting configurations, the guard ring should be tied to the potential of the positive input (+IN). For noninverting configurations, the guard ring should be tied to the potential of the negative input (–IN). In order for this technique to be effective, the guard ring must not be covered by solder mask. Ringing both sides of the printed circuit board may be required. See Figure 5 for an example of proper layout.

Shutdown Mode

The LTC2063 in the SC70 package, the LTC2064 in the DFN package, and the LTC2065 in the QFN package feature a shutdown mode for low-power applications. In the OFF state, each amplifier draws less than 170nA of supply current and the outputs present a high impedance to external circuitry.

Shutdown operation is accomplished by tying $\overline{SHDN}$ below V_L. If the shutdown feature is not required, it is recommended that $\overline{SHDN}$ be tied to V^+. A current source pulls the $\overline{SHDN}$ pin high to automatically keep the amplifier in the ON state when the pin is floated, however this may not be reliable at elevated temperatures due to board leakage (see $\overline{SHDN}$ Circuit Block Diagram). For operation in noisy environments, a capacitor between $\overline{SHDN}$ and V^+ is recommended to prevent noise from changing the shutdown state. When there is a danger of $\overline{SHDN}$ being pulled beyond the supply rails, resistance in series with the $\overline{SHDN}$ pin is recommended to limit the resulting current.

Start-Up Characteristics

Micropower op amps are often not micropower during start-up, which can cause problems when used on low current supplies. Large transient currents can conduct during power-up until the internal bias nodes settle to their final values. A large amount of current can be drawn from the supplies during this transient, which can sustain for several milliseconds in the case of a micropower part. In the worst case, there may not be enough supply current available to take the system up to nominal voltages. In other cases, this transient power-up current will lead to added power loss in duty-cycled applications.

A way to quantify the transient current loss is to integrate the supply current during power-up to examine the total charge loss. If there were no additional transient current, the integrated supply current would appear as a smooth, straight line with a slope equal to the DC supply current of the part. Any deviation from a straight line indicates additional transient current that is drawn from the supply. The LTC2063/LTC2064/LTC2065 have been designed to minimize this charge loss during power-up so that power can be conserved in duty-cycled applications. Figure 6 shows the integrated supply current (i.e. charge) of the LTC2063 during power-up. Likewise, Figure 7 shows the charge loss due to enabling and disabling the part via the $\overline{SHDN}$ pin.

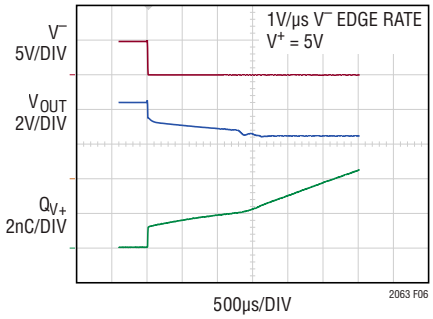


Figure 6. LTC2063 Charge Loss During Power-Up

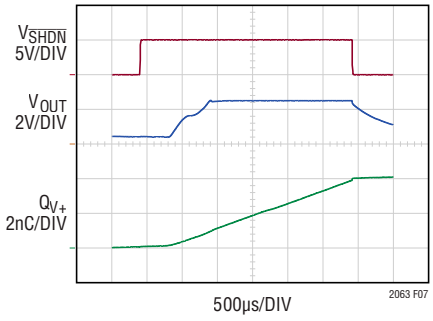


Figure 7. LTC2063 Charge Loss Due to Enabling and Disabling via $\overline{SHDN}$ Pin

APPLICATIONS INFORMATION

There are benefits when the $\overline{SHDN}$ pin is used to disable and enable the part in duty-cycled applications, rather than powering down the external supply voltage (V^+). Powering up and powering down the external supply will tend to waste charge due to charging and discharging the external decoupling capacitors. For these power-cycled applications, a relay or MOS device can be located after the decoupling capacitors to alleviate this, however there are drawbacks to this approach. The LTC2063 draws an initial charge of approximately 2nC when powered up. This recurring charge loss is unavoidable in power-cycled applications. Additionally, if the supply ramp rate exceeds 0.4V/µs, an internal transient ESD clamp will trigger, conducting additional current from V^+ to $V^–$. This will waste charge and can make insignificant any savings that may have been expected by power-cycling the supply. Figure 8 shows the charge loss at power-up.

The shutdown pin can be used to overcome these limitations in duty-cycled applications. The typical charge loss transitioning into and out of shutdown is only 1nC. Since the supply is not transitioned, the external decoupling capacitors do not draw charge from the supply.

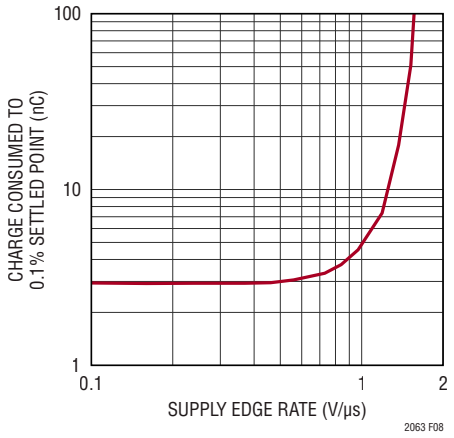


Figure 8. LTC2063 Power-Up Charge vs Supply Edge Rate

Gas Sensor

This low power precision gas sensor circuit operates in an oxygen level range of 0% to 30%, with a nominal output of 1V in normal atmospheric oxygen concentrations (20.9%) when the gas sensor has been fully initialized. Total active power consumption is less than 2.1µA on a single rail supply.

Since this gas sensor produces 100µA in a normal oxygen environment and requires a 100Ω load resistor, the resulting input signal is typically around 10mV. The LTC2063's rail-to-rail input means no additional DC level shifting is necessary, all the way down to very low oxygen concentrations.

Due to the extremely low input offset voltage of the LTC2063, which is 1µV typically and 5µV maximum, it is possible to gain up the mV-scale input signal substantially without introducing significant error. In the configuration shown in Figure 9, with a noninverting gain of 101V/V, the worst-case input offset results in a maximum of 0.5mV offset on the 1V output, or 0.05% error.

Although the 100kΩ resistor in series with the gas sensor does not strictly have the same precision requirement as the 10MΩ and 100kΩ resistors that set the gain, it is important to use a similar resistor at both input terminals. This helps to minimize additional offset voltage at the inputs due to thermocouple effects, hence the similar 0.1% precision requirement.

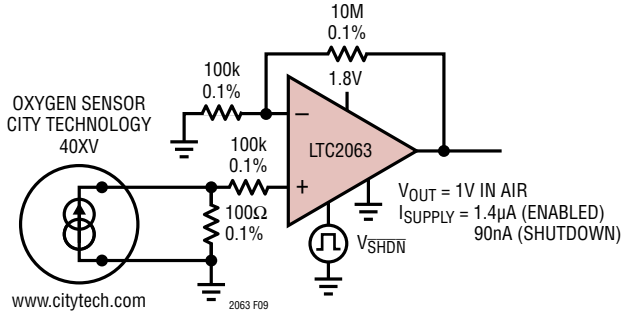


Figure 9. Micropower Precision Oxygen Sensor

APPLICATIONS INFORMATION

RTD Sensor

This low power platinum resistance temperature detector (RTD) sensor circuit draws only 35µA total supply current on a minimum 2.6V rail, and is accurate to within ±1°C at room temperature, including all error intrinsic to the Vishay PTS Class F0.3 Variant RTD. It covers the temperature range from –40°C to 85°C in 10mV/°C increments and produces an output of 1V at nominal room temperature of 25°C.

The LTC2063's extremely low typical offset of 1µV and typical input bias current of 3pA allows for the use of a very low excitation current in the RTD. Thus, self-heating is negligible, improving accuracy.

The LT5400-3, B-grade, is used to provide a ±0.025% matched resistor network that is effectively a precision 131:1 voltage divider. This precision divider forms one half of a bridge circuit, with the 0.1% 110kΩ and RTD in the other branch. Note that the 110kΩ's precision requirement is to ensure matching with the RTD. The 11kΩ R2 serves to provide a DC offset for the entire bridge so that the output is 1V at room temperature. Since bridge imbalances can lead to error, it is recommended to minimize the length of the leads connecting the RTD to reduce additional lead resistance.

The LT6656-2.048 reference helps create a known excitation current in the RTD at each temperature of operation, and also acts as a supply for the LTC2063, all while using less than 1µA itself. The LT6656 can accept input voltages anywhere between 2.6V and 18V, allowing for flexibility in selection of supply voltage while maintaining a fixed output range. The LT6656 reference can easily source the 35µA required to run the entire circuit, thanks to the LTC2063's 2µA maximum supply current and ability to handle microvolt signals produced by the RTD under low excitation current.

Care should be taken to minimize thermocouple effects by preventing significant thermal gradients between the two op amp inputs. It is also important to choose feedback and series resistors that are low-tempco to minimize error due to drift over the entire temperature range.

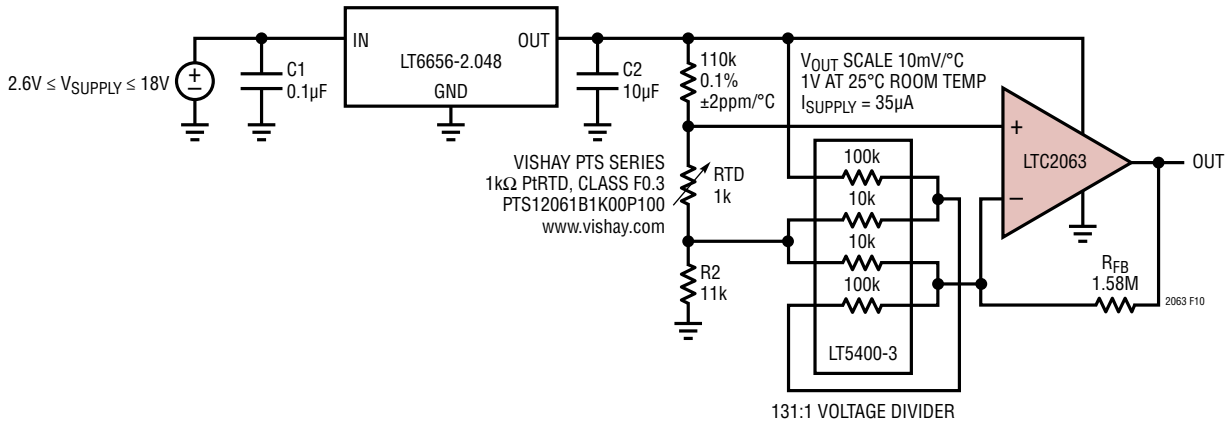


Figure 10. RTD Sensor

APPLICATIONS INFORMATION

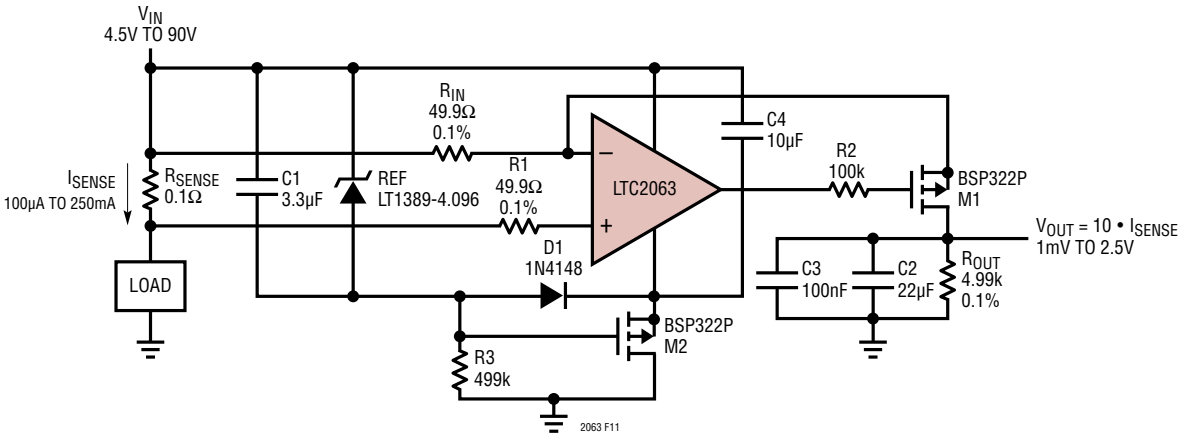


Figure 11. High Side Current Sense

90V High Side Current Sense

This micropower precision LTC2063 high side current sense circuit measures currents from 100µA to 250mA over a 4.5V to 90V input voltage range.

The output of this circuit is:

$$V_{OUT} = \frac{R_{OUT} \bullet R_{SHUNT}}{R_{IN}} I_{SENSE} = 500 \bullet I_{SENSE}$$

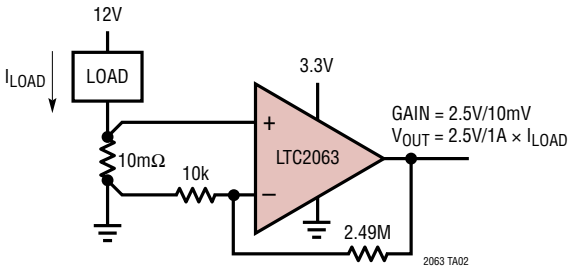
The LTC2063's low typical input offset voltage of 1µV and low input bias current of 3pA contribute output errors that are much smaller than the error due to precision limitations of the resistors used. Thus, output accuracy is mainly set by the accuracy of the resistors R_{SENSE}, R_{IN}, and R_{OUT}.

The LT1389-4.096V reference, along with the bootstrap circuit composed of M2, R3, and D1, establishes a very low power isolated 3V rail that protects the LTC2063 from reaching its absolute maximum voltage of 5.5V while allowing for much higher input voltages.

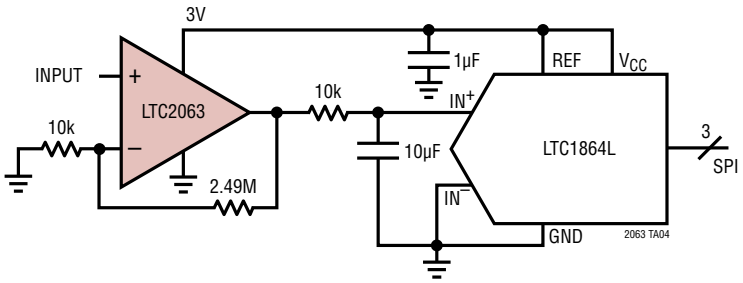
Since the LTC2063's gain-bandwidth product is 20kHz, it is recommended to use this circuit to measure signals that are 2kHz or slower. Note that the output filter as drawn will limit the frequency to 1.5Hz, which optimizes for lowest noise. If this output filter bandwidth is too narrow, removing C2 leads to an output filter with 318Hz bandwidth, created by C3 and R_{OUT}.

TYPICAL APPLICATIONS

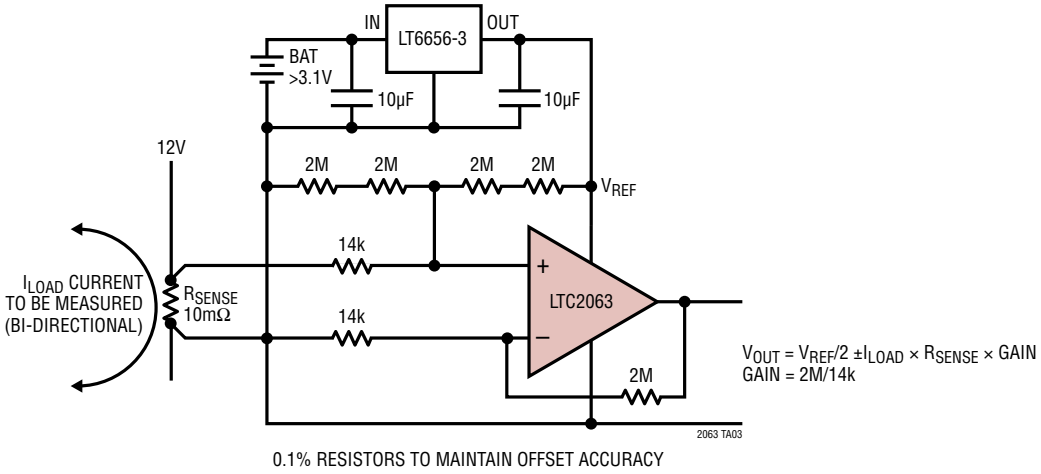
Precision Micropower Low Side Current Sense



Micropower 16-Bit Data Acquisition

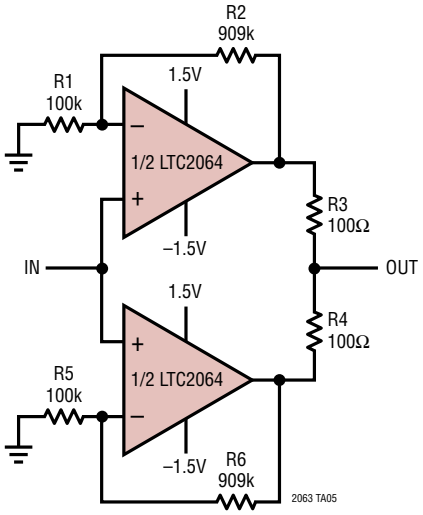


TYPICAL APPLICATIONS



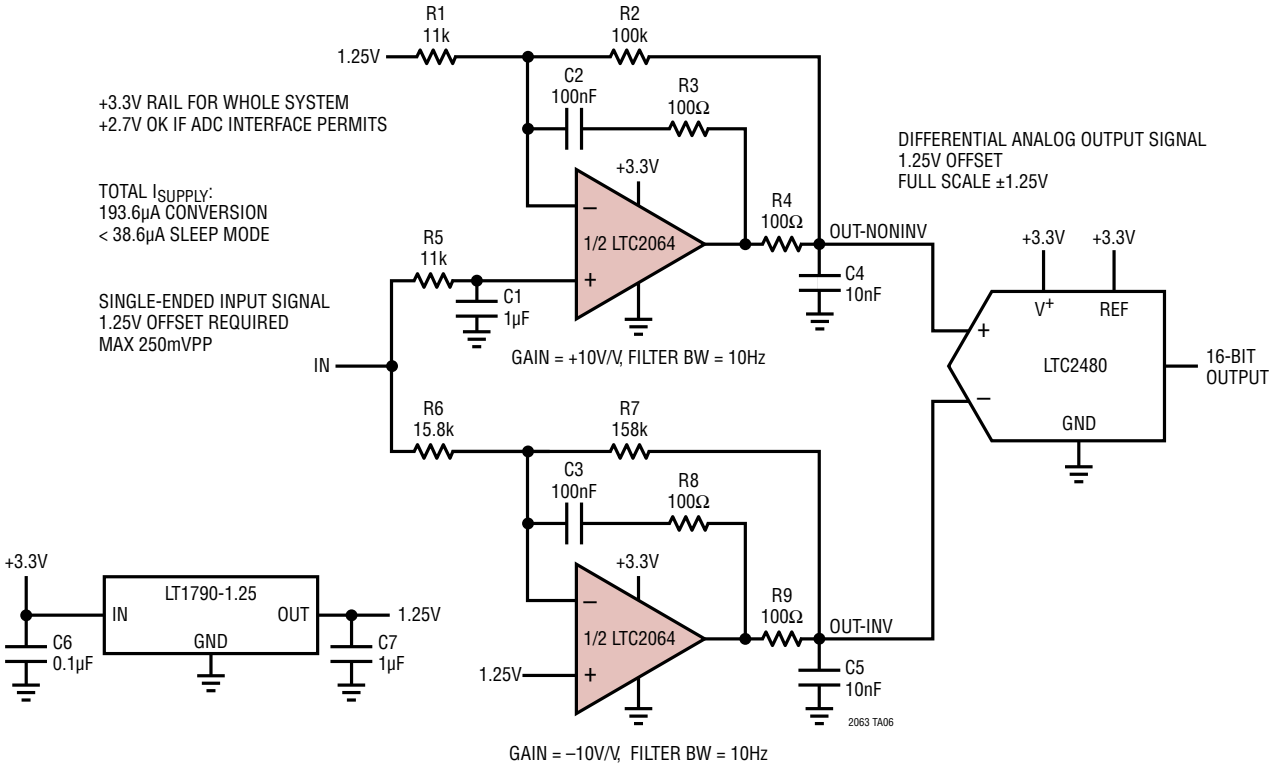
0.1% RESISTORS TO MAINTAIN OFFSET ACCURACY

Parallel LTC2064 Amplifiers to Reduce Noise by $\sqrt{2}$



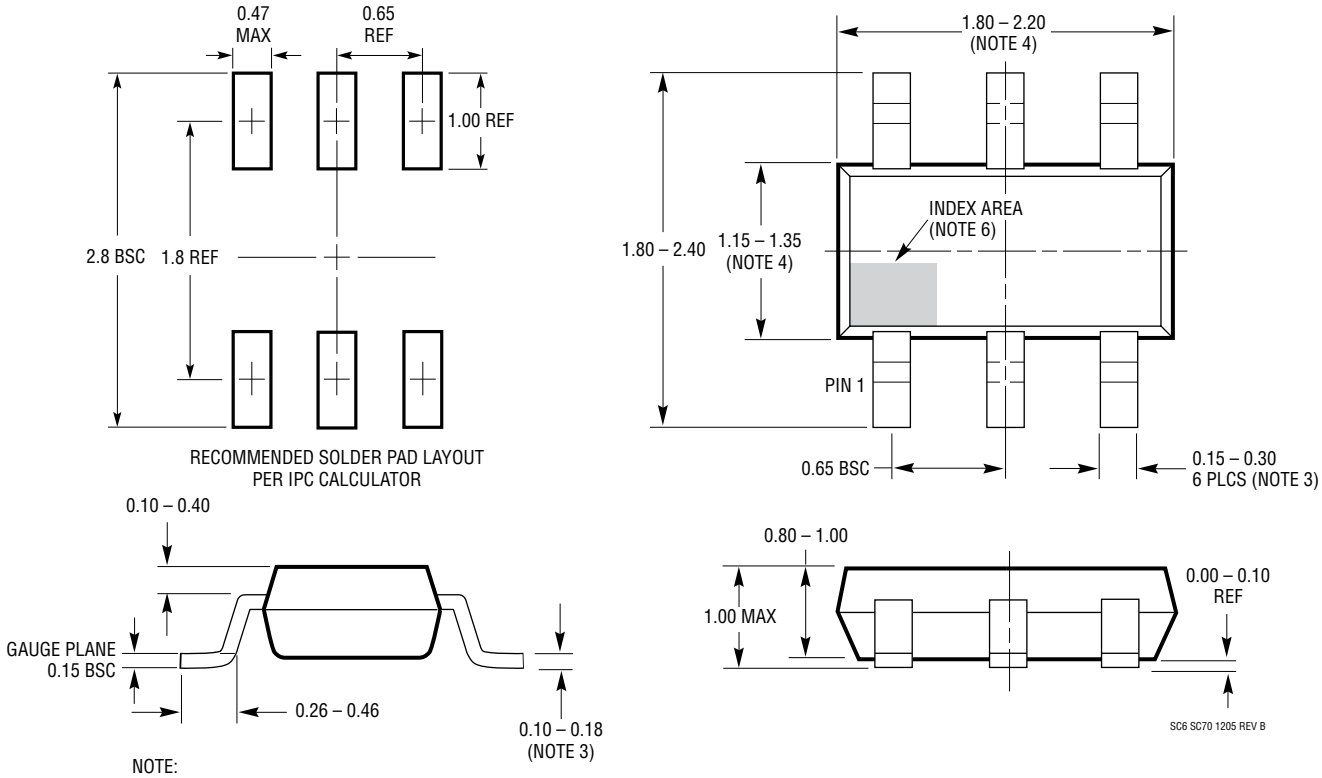
TYPICAL APPLICATIONS

Micropower 16-Bit Data Acquisition with Single-to-Differential Input Driver



PACKAGE DESCRIPTION

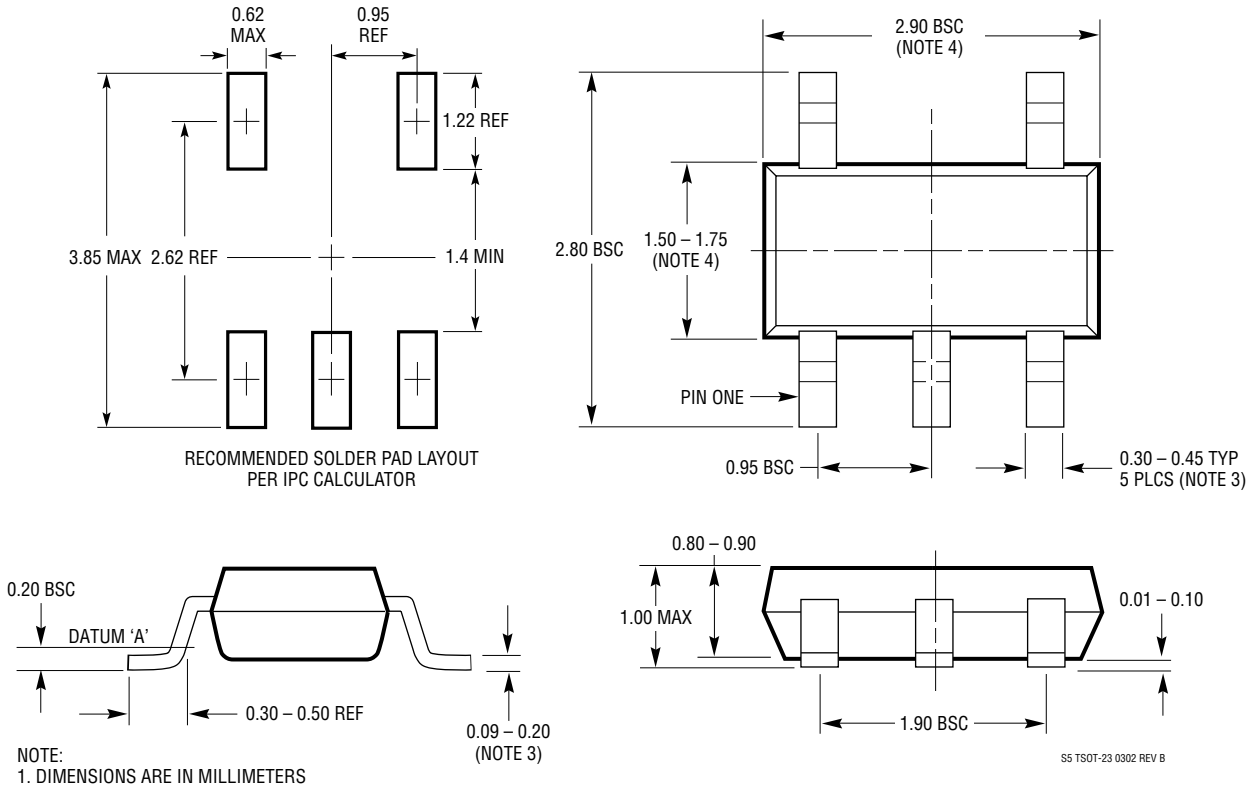
SC6 Package
6-Lead Plastic SC70
(Reference LTC DWG # 05-08-1638 Rev B)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. DETAILS OF THE PIN 1 IDENTIFIER ARE OPTIONAL,
   BUT MUST BE LOCATED WITHIN THE INDEX AREA
7. EIAJ PACKAGE REFERENCE IS EIAJ SC-70
8. JEDEC PACKAGE REFERENCE IS MO-203 VARIATION AB

PACKAGE DESCRIPTION

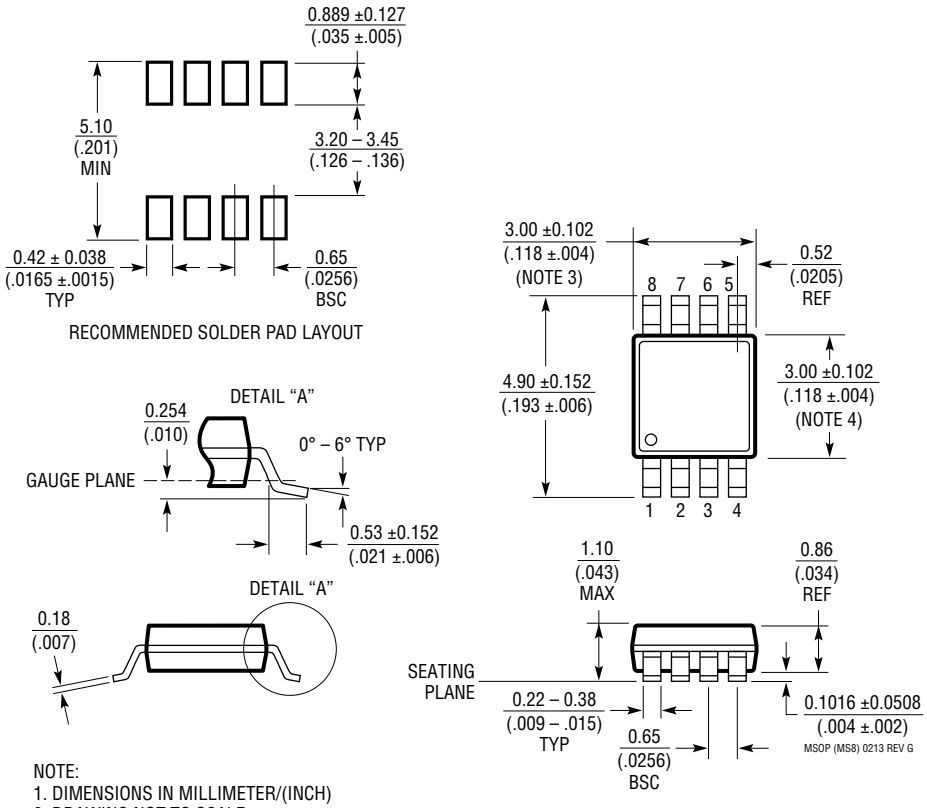
S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635 Rev B)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

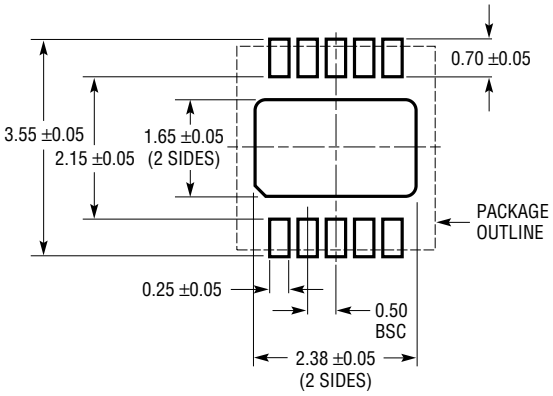
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



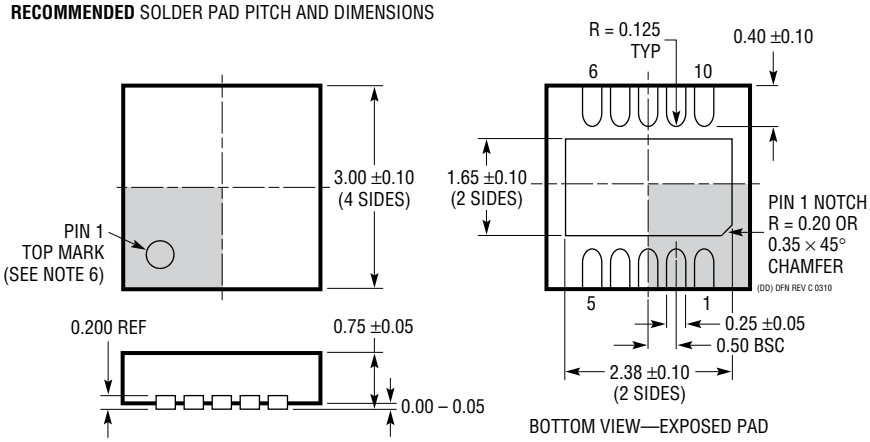
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

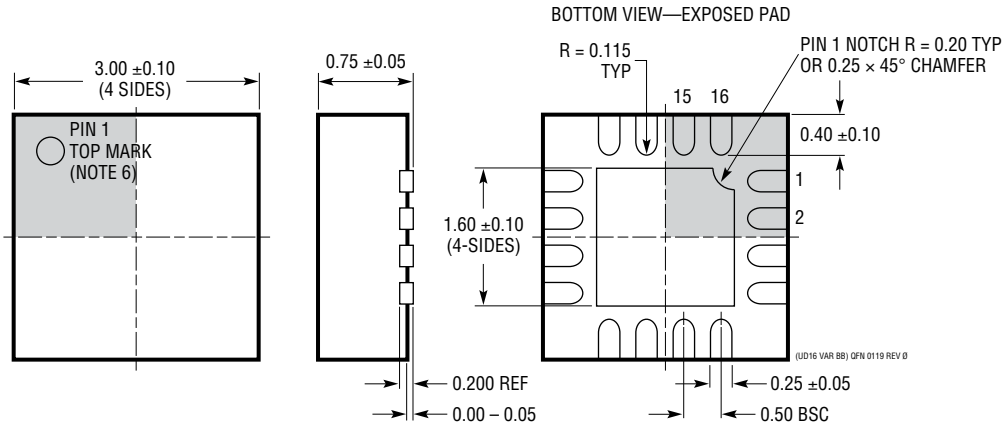


BOTTOM VIEW—EXPOSED PAD

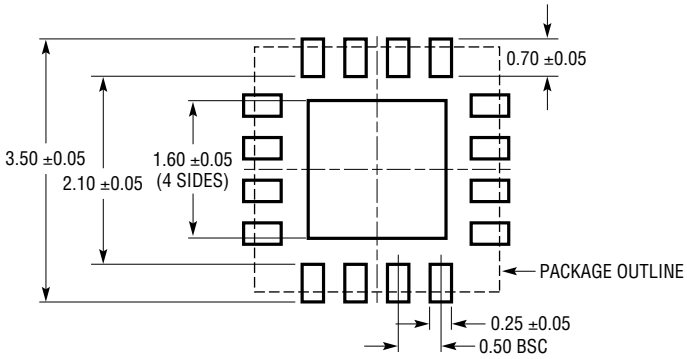
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1782 Rev Ø)
Exposed Pad Variation BB



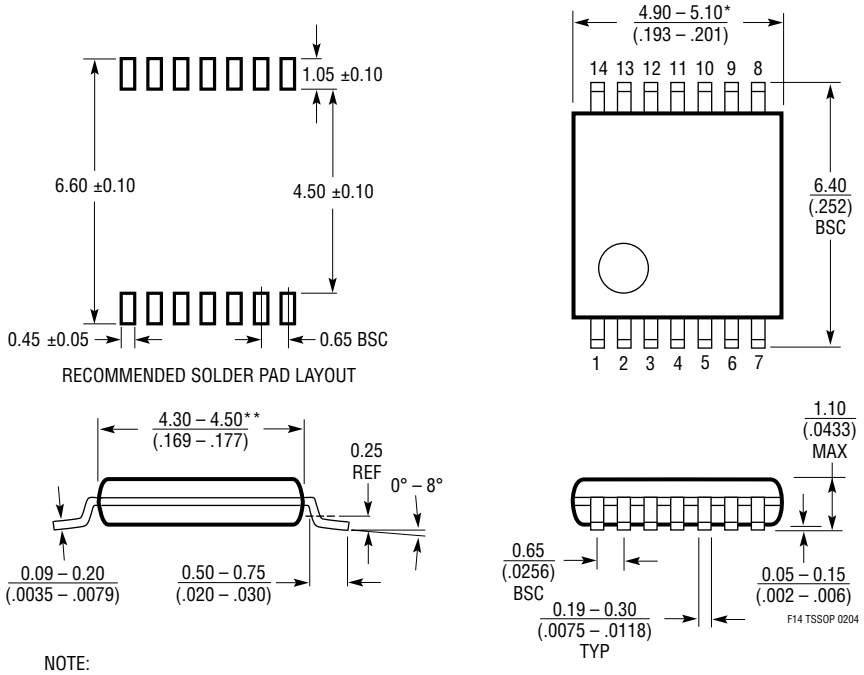
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. NiPdAu PPF TERMINAL FINISH
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

PACKAGE DESCRIPTION

F Package
14-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1650)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

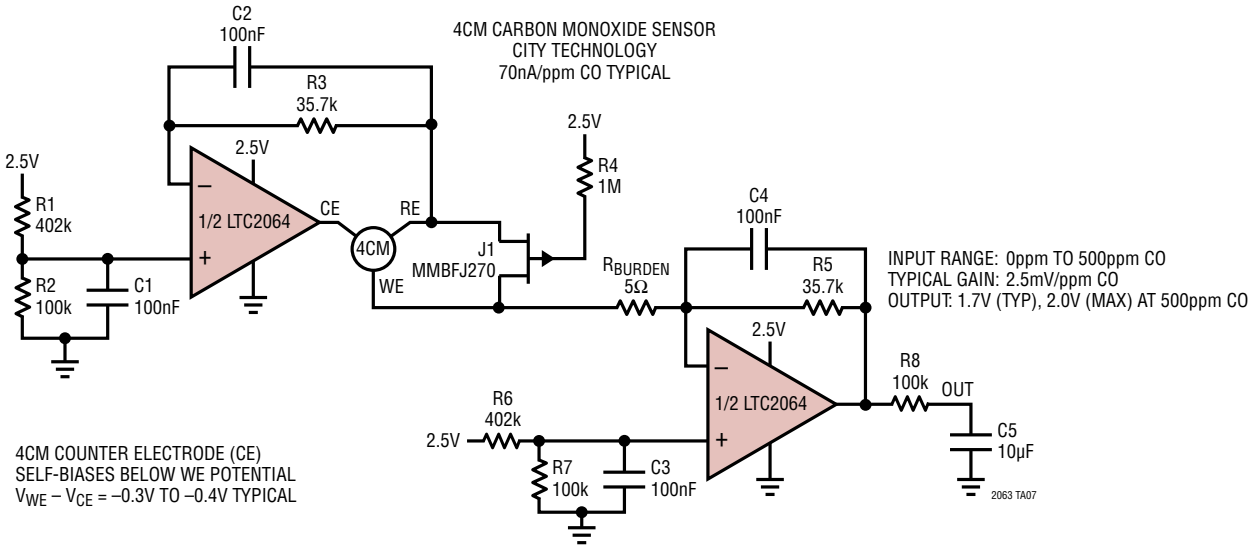
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/18	Added LTC2064, fixed typos.	All
B	4/20	Added LTC2065 to data sheet.	All
C	5/20	Corrected Order Information, QFN16 exposed pad, Figure 1 caption, minor typos.	2, 15, 18, 19, 21, 32

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TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADA4051-1/ADA4051-2	Micropower, Single/Dual, Zero-Drift Operational Amplifiers	7µA I_S, 15µV V_{OS}, 11.8V to 5.5V V_S, 115kHz, RRIO
LTC2066/LTC2067/ LTC2068	Micropower, Low IB Single/Dual/Quad, Zero-Drift Op Amps	2µA I_S, 5µV V_{OS}, 1.7V to 5.25V V_S, 20kHz, RRIO
LTC2054/LTC2055	Micropower, Single/Dual, Zero-Drift Operational Amplifier	130µA I_S, 5µV V_{OS}, 2.7V to 11 V V_S, 500kHz, RR Output
ADA4522-1/ADA4522-2/ ADA4522-4	55V, Low Noise Zero-Drift Operational Amplifier	900µA I_S, 5.8nV/$\sqrt{Hz}$, 5µV V_{OS}, 4.5V to 55V V_S, 3MHz, RR Output
LTC2057/LTC2057HV	High Voltage-Low Noise Zero-Drift Operational Amplifier	4µV V_{OS}, 1.2mA I_S, 4.75V to 60V V_S, 1.5MHz, RR Output
LTC2058	36V, Low Noise Zero-Drift Operational Amplifier	5µV V_{OS}, 1.2mA I_S, 4.75V to 36V V_S, 2.5MHz, RR Output
LTC2050/LTC2050HV	Zero-Drift Operational Amplifier	3µV V_{OS}, 1.5mA I_S, 2.7V to 12V V_S, 3MHz, RR Output
LTC2051/LTC2052	Dual/Quad Zero-Drift Operational Amplifier	3µV V_{OS}, 1.5mA I_S, 2.7V to 12V V_S, 3MHz, RR Output
ADA4528-1/ADA4528-2	5V Ultra Low Noise Zero-Drift Op Amps	5µV V_{OS}, 5.6nV/$\sqrt{Hz}$, 1.7mA I_S, 2.2V to 5.5V V_S, 4MHz, RRIO
LT®1494/LT1495/ LT1496	1.5µA Max, Over-The-Top Precision Operational Amplifier	1.5µA I_S, 375µV V_{OS}, 2.2V to 36V V_S, 2.7kHz, RRIO
LT6003/LT6004/LT6005	1.6V, 1µA Precision Rail-to-Rail Input and Output Op Amps	1µA I_S, 500µV V_{OS}, 1.6V to 16V V_S, 2kHz, RRIO
LT6023	Micropower, Enhanced Slew Op Amp	20µA I_S, 20µV V_{OS}, 3V to 30V V_S, 40kHz
LTC2053	Precision, Rail-to-Rail, Zero-Drift, PGIA	1.3mA I_S, 10µV V_{OS}, 2.7V to 12V V_S, 200kHz, RRIO
LT5400	Quad Matched Resistor Network	0.01% Matching, 8ppm/°C Temp Drift , 0.2ppm/°C Temp Matching

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