# Quad 17V, 1.25A Parallelable Synchronous Step-Down Regulator with Ultralow Quiescent Current

## FEATURES

- **Quad Step-down Outputs: 1.25A per Channel**
- **Wide $V_{IN}$ Range: 2.7V to 17V**
- **Wide $V_{OUT}$ Range: 0.6V to $V_{IN}$**
- **1.25A/2.5A/3.75A/5A $I_{OUT}$ Configurable with One Inductor**
- **Integrated 300mΩ P-Channel/80mΩ N-Channel MOSFETs Provide Up to 93% Efficiency**
- **No-Load Burst Mode Operation $I_Q$ < 10µA with All Channels Enabled**
- **Constant Frequency (1MHz/2.25MHz) with ±50% Frequency Synchronization Range**
- ±1% Output Voltage Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Full Dropout Operation (100% Duty Cycle)
- Phase Shift Programmable with External Clock
- 5mm × 5mm × 1.72mm BGA Package

## APPLICATIONS

- Battery Powered Systems
- Point-of-Load Supplies
- Portable – Handheld Scanners and Cameras

## DESCRIPTION

The LTC®3644/LTC3644-2 is a quad 1.25A output, high efficiency synchronous monolithic step-down regulator capable of operating from input supplies up to 17V. The switching frequency is internally fixed to 1MHz or 2.25MHz with a ±50% synchronization range. The regulator features ultralow quiescent current and high efficiency over a wide $V_{IN}$ and $V_{OUT}$ range.

The step-down regulator operates from an input voltage range of 2.7V to 17V and provides an adjustable output range from 0.6V to $V_{IN}$ while delivering up to 1.25A of output current per channel. LTC3644/LTC3644-2 can be configured for quad 1.25A outputs, triple 2.5A/1.25A/1.25A outputs, dual 2.5A outputs, or dual 3.75A/1.25A outputs. A user selectable mode input is provided to allow the user to trade off ripple noise for light load efficiency; Burst Mode® operation provides the highest efficiency at light loads, while forced-continuous mode provides the lowest ripple noise. The regulators can be synchronized to an external clock.

**LTC3644 Options**

| PART NAME | FREQUENCY | $V_{OUT}$ |
|---|---|---|
| LTC3644 | 1.00MHz | Adjustable |
| LTC3644-2 | 2.25MHz | Adjustable |

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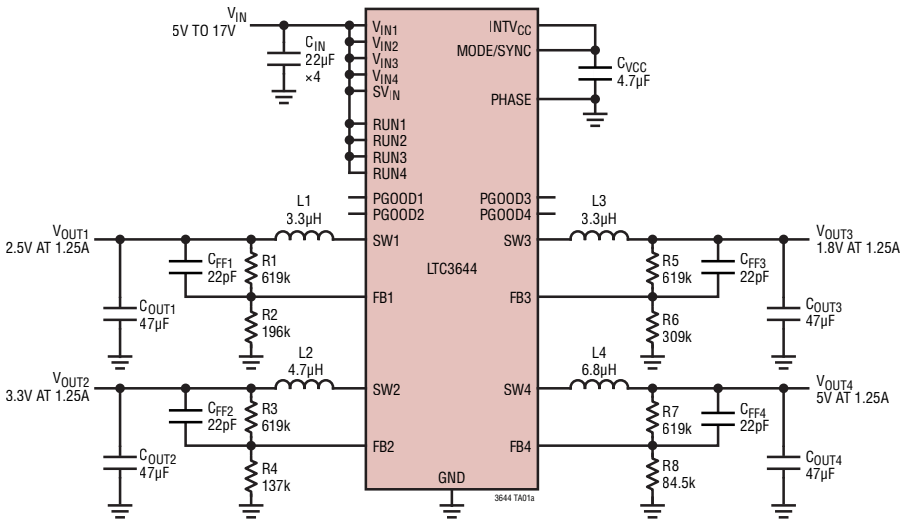
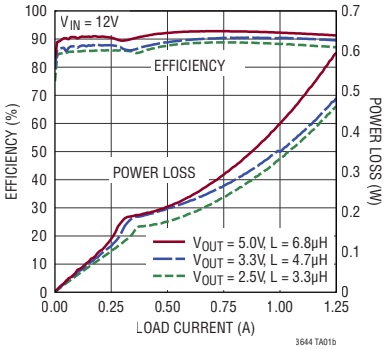
## TYPICAL APPLICATION

**4-Channel 1.25A Quad-Output 1MHz Step-Down Regulator**




**Efficiency and Power Loss vs Load at 1MHz in Burst Mode Operation**



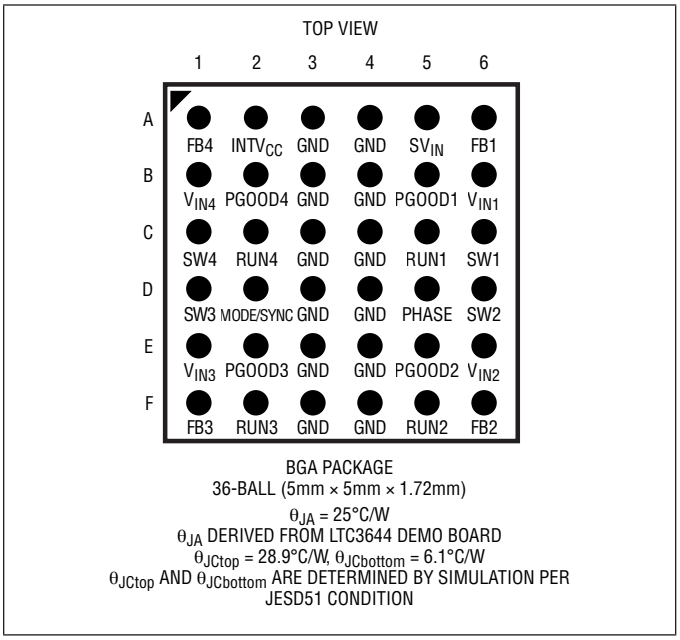

Rev. A

## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN1}$, $V_{IN2}$, $V_{IN3}$, $V_{IN4}$, $SV_{IN}$ ..... –0.3V to 17V
RUN1, RUN2, RUN3, RUN4 ..... –0.3V to $SV_{IN}$ + 0.3V
MODE/SYNC, FB1, FB2, FB3, FB4 .... –0.3V to $INTV_{CC}$ + 0.3V
PGOOD1, PGOOD2, PGOOD3, PGOOD4, PHASE .. –0.3V to 6V
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Peak Solder Reflow Body Temperature ..... 260°C

## PIN CONFIGURATION




BGA PACKAGE
36-BALL (5mm × 5mm × 1.72mm)
$\theta_{JA}$ = 25°C/W
$\theta_{JA}$ DERIVED FROM LTC3644 DEMO BOARD
$\theta_{JCtop}$ = 28.9°C/W, $\theta_{JCbottom}$ = 6.1°C/W
$\theta_{JCtop}$ AND $\theta_{JCbottom}$ ARE DETERMINED BY SIMULATION PER JESD51 CONDITION

## ORDER INFORMATION

| PART NUMBER | TAPE AND REEL | TERMINAL FINISH | PART MARKING* | | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (SEE NOTE 2) |
|---|---|---|---|---|---|---|---|
| | | | DEVICE | FINISH CODE | | | |
| LTC3644EY#PBF | LTC3644EY#TRPBF | SAC305(RoHS) | 3644Y | e1 | BGA | 3 | –40°C to 125°C |
| LTC3644IY#PBF | LTC3644IY#TRPBF | SAC305(RoHS) | 3644Y | e1 | BGA | 3 | –40°C to 125°C |
| LTC3644EY-2#PBF | LTC3644EY-2#TRPBF | SAC305(RoHS) | 3644Y2 | e1 | BGA | 3 | –40°C to 125°C |
| LTC3644IY-2#PBF | LTC3644IY-2#TRPBF | SAC305(RoHS) | 3644Y2 | e1 | BGA | 3 | –40°C to 125°C |

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings

For more information on tape and reel specifications, go to: Tape and reel specifications.

- This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $SV_{IN}$ = $V_{IN1}$ = $V_{IN2}$ = $V_{IN3}$ = $V_{IN4}$ = 12V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{INX}$, $SV_{IN}$ | Operating Voltage | | | 2.7 | | 17 | V |
| $V_{OUT}$ | Output Voltage | | | 0.6 | | $V_{IN}$ | V |
| $I_Q$ | Input Quiescent Current | Forced Continuous Mode (Note 3)<br>Burst Mode, No Load<br>Shutdown Mode; $V_{RUN1}$ = $V_{RUN2}$ = $V_{RUN3}$ = $V_{RUN4}$ = 0V | | | 5<br>10<br>0.1 | 8<br>14<br>1 | mA<br>µA<br>µA |
| $V_{FB}$ | Regulated Feedback Voltage | | ● | 0.594 | 0.6 | 0.606 | V |
| $I_{FB}$ | FB Input Current | | | | | 10 | nA |
| | Reference Voltage Line Regulation | $SV_{IN}$ = 2.7V to 17V (Note 4) | | | 0.01 | 0.025 | %/V |
| | Output Voltage Load Regulation | (Note 4) | | | 0.1 | 0.3 | % |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $SV_{IN}$ = $V_{IN1}$ = $V_{IN2}$ = $V_{IN3}$ = $V_{IN4}$ = 12V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| | NMOS Switch Leakage<br>PMOS Switch Leakage | | | | 0.1<br>0.1 | 1<br>1 | µA<br>µA |
| $R_{DS(ON)}$ | NMOS On Resistance<br>PMOS On Resistance | | | | 80<br>300 | | mΩ<br>mΩ |
| $t_{ON(MIN)}$ | Minimum On Time | (Note 6) | | | 60 | | ns |
| $V_{RUN}$ | RUN Input High<br>RUN Input Low | | | <br>0.35 | | 1.0 | V |
| | RUN Input Current | $V_{RUN}$ = 12V | | | 0.1 | 10 | nA |
| $V_{MODE/SYNC}$ | Pulse-Skipping Mode<br>Forced Continuous Mode<br>Burst Mode Operation | | | <br>1.0<br>$V_{INTVCC}$ – 0.4 | | 0.3<br>$V_{INTVCC}$ – 1.2<br>$V_{INTVCC}$ + 0.3V | V<br>V<br>V |
| | MODE/SYNC Input Current | | | | 0.1 | 100 | nA |
| | PHASE Input Threshold | Input Low<br>Input High | | <br>$V_{INTVCC}$ – 0.4 | | 0.4 | V<br>V |
| | PHASE Input Current | $V_{PHASE}$ = 6V | | | 0.1 | 100 | nA |
| $t_{SS}$ | Internal Soft Start Time | | | | 1.1 | | ms |
| $I_{LIM}$ | Peak Current Limit | 1.25A Regulator<br>2.5A Regulator (2-Channel Combined)<br>3.75A Regulator (3-Channel Combined) | | 1.8 | 2.2<br>4.4<br>6.6 | 2.6 | A<br>A<br>A |
| | $V_{INTVCC}$ Undervoltage Lockout | $SV_{IN}$ Ramping Up | | 2.35 | 2.5 | 2.65 | V |
| | $V_{INTVCC}$ Undervoltage Lockout Hysteresis | | | | 250 | | mV |
| | $V_{IN}$ Overvoltage Lockout Rising | | ● | 18 | 19 | 20 | V |
| | $V_{IN}$ Overvoltage Lockout Hysteresis | | | | 400 | | mV |
| $f_{OSC}$ | Oscillator Frequency | LTC3644-2<br>LTC3644 | ●<br>● | 1.8<br>0.82 | 2.25<br>1.00 | 2.60<br>1.16 | MHz<br>MHz |
| | SYNC Capture Range | % of Programmed Frequency | | 50 | | 150 | % |
| $V_{INTVCC}$ | $V_{INTVCC}$ Voltage | $SV_{IN}$ > 5.5V | | | 5 | | V |
| | Power Good Range | | | | ±7.5 | | % |
| $R_{PGOOD}$ | Power Good Resistance | | | | 275 | 350 | Ω |
| $t_{PGOOD}$ | PGOOD Delay | PGOOD Low to High<br>PGOOD High to Low | | | 0<br>32 | | Cycles<br>Cycles |
| | Phase Shift Between Channel 1/2 and Channel 3/4 | $V_{PHASE}$ = 0V<br>$V_{PHASE}$ = $INTV_{CC}$, $V_{MODE/SYNC}$ = 0V | | | 0<br>180 | | Deg<br>Deg |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3644/LTC3644-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3644E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3644I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

where $\theta_{JA}$ (in °C/W) is the package thermal impedance.

**Note 3:** The quiescent current in active mode does not include switching loss of the power FETs.

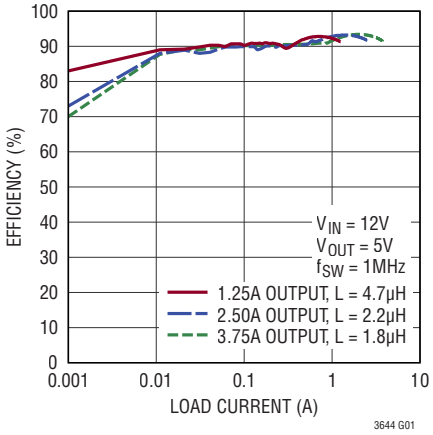
**Note 4:** The LTC3644 is tested in a proprietary test mode that connects $V_{FB}$ to the output of error amplifier.

**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

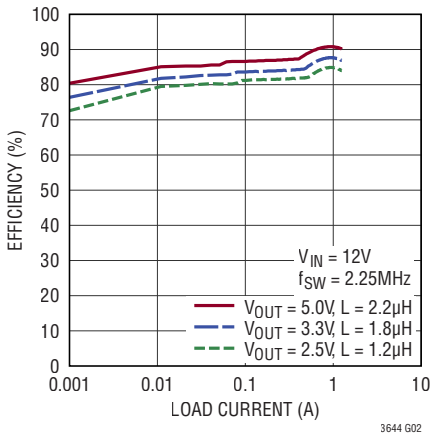
**Note 6:** The minimum on-time is determined by the speed of the top switch driver and peak current comparator. The typical value listed here is guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

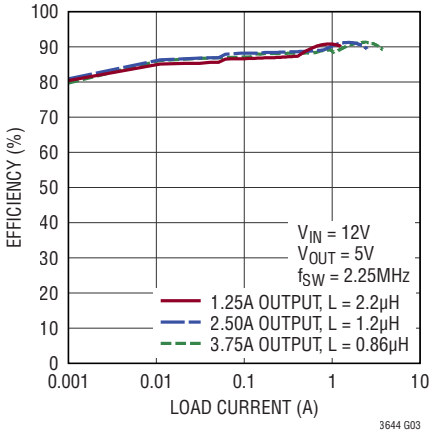
### Efficiency vs Load Current in Burst Mode Operation



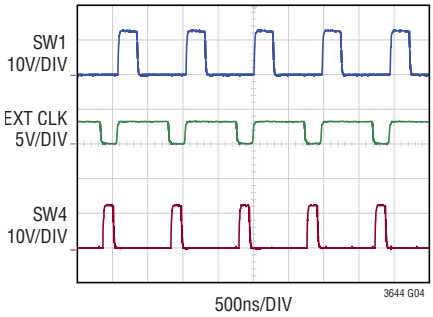

### Efficiency vs Load Current in Burst Mode Operation




### Efficiency vs Load Current in Burst Mode Operation

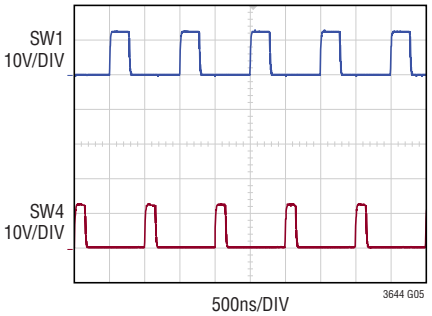



### Phase Shift with External Clock Frequency Sync



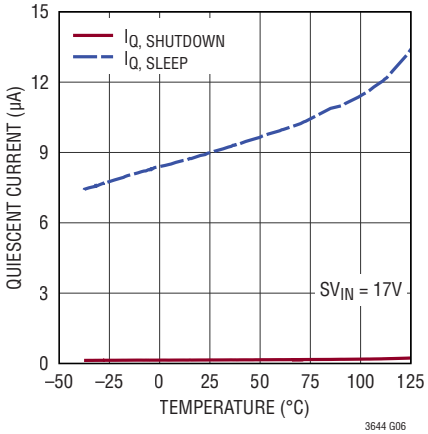

$V_{IN}$ = 12V
$V_{OUT1}$ = 3.3V, $V_{OUT4}$ = 1.8V
$L_1$ = 4.7µH, $L_4$ = 3.3µH
PHASE = $INTV_{CC}$
MODE/SYNC = EXT CLK

### 180° Phase Operation

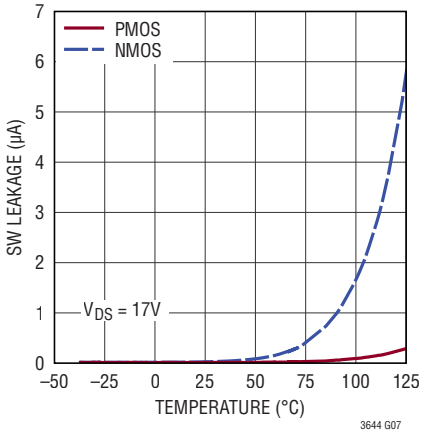



$V_{IN}$ = 12V
$V_{OUT1}$ = 3.3V, $V_{OUT4}$ = 1.8V
$L_1$ = 4.7µH, $L_4$ = 3.3µH
PHASE = $INTV_{CC}$
MODE/SYNC = 2.5V

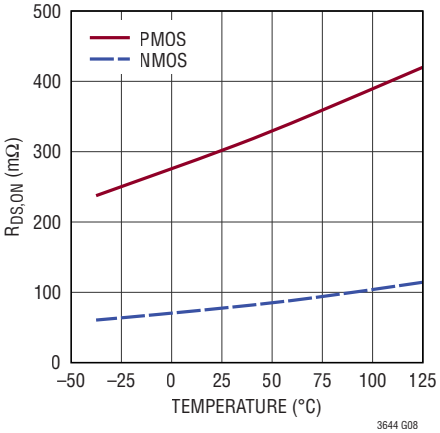
### $I_Q$ vs Temperature




### SW Leakage Current vs Temperature

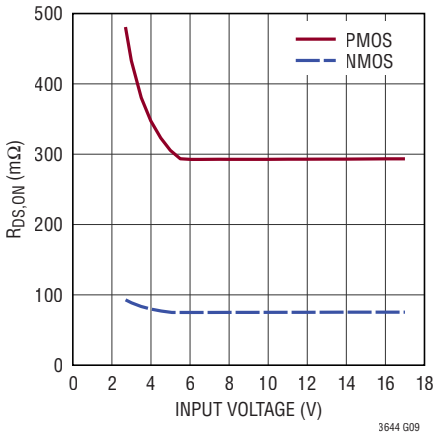



### $R_{DS(ON)}$ vs Temperature

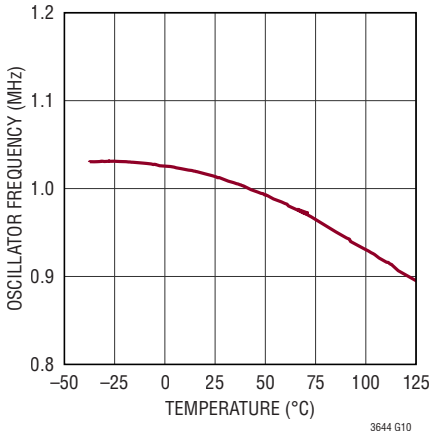


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

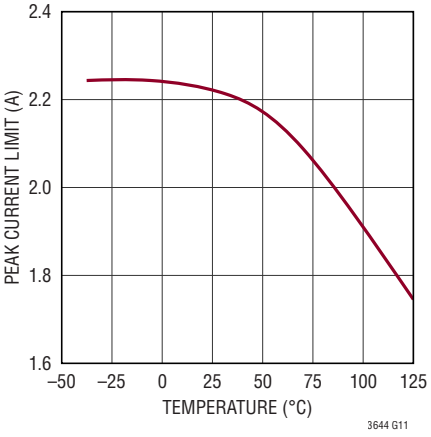
### $R_{DS(ON)}$ vs Input Voltage



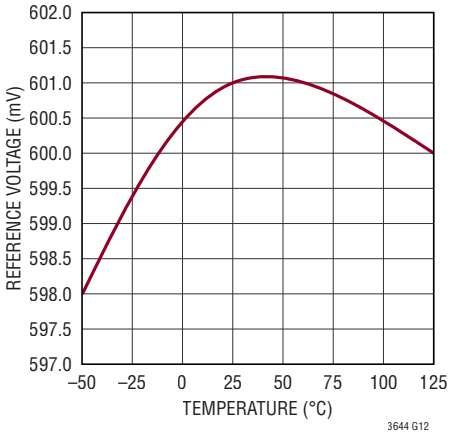

### Oscillator Frequency vs Temperature



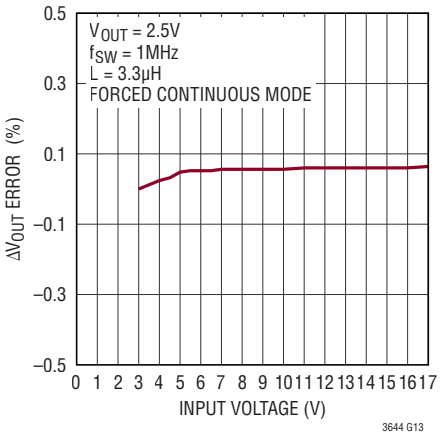

### Peak Current Limit vs Temperature



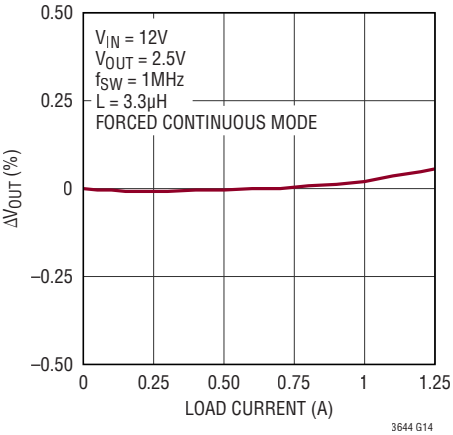

### Reference Voltage vs Temperature




### Line Regulation, No Load

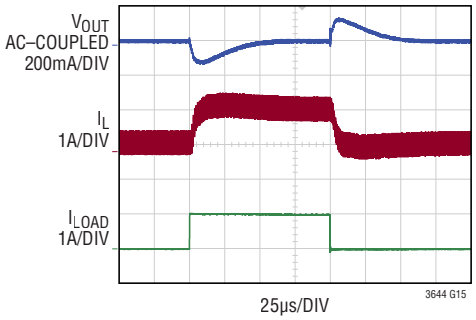



### Load Regulation



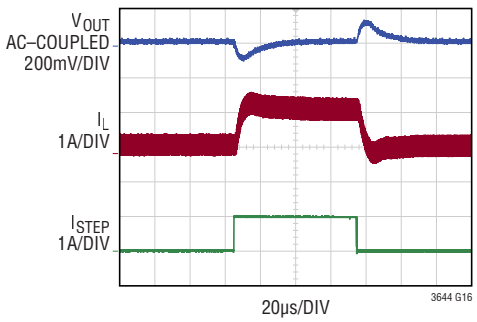
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

### Load Step at 1MHz



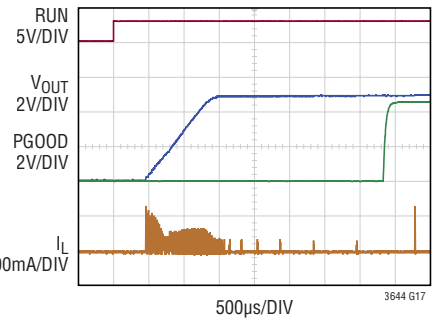

$V_{IN}$ = 12V
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 100mA to 1.1A
L = 3.3µH
$C_{OUT}$ = 47µF

### Load Step at 2.25MHz



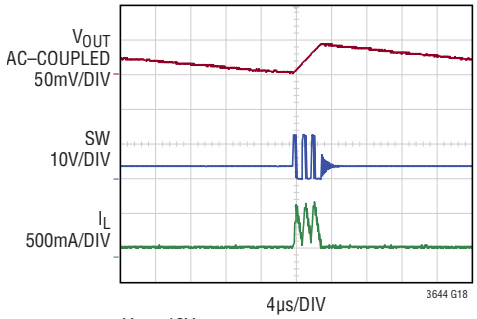

$V_{IN}$ = 12V
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 100mA to 1.1A
L = 1.8µH
$C_{OUT}$ = 47µF

### Start-Up Operation



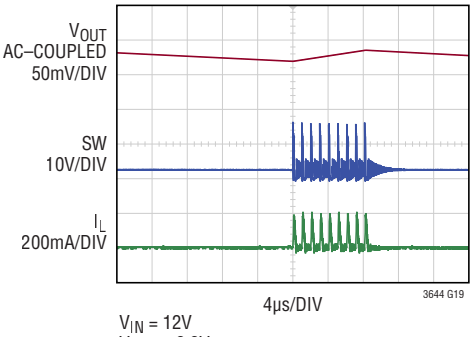

$V_{IN}$ = 12V
$V_{OUT}$ = 5V
$f_{SW}$ = 1MHz
L = 4.7µH
$C_{OUT}$ = 47µF

### Burst Mode Operation




$V_{IN}$ = 12V
$V_{OUT}$ = 3.3V
$I_{LOAD}$ = 25mA
$f_{SW}$ = 1MHz
L = 4.7µH

### Pulse-Skipping Operation




$V_{IN}$ = 12V
$V_{OUT}$ = 3.3V
$I_{LOAD}$ = 10mA
$f_{SW}$ = 1MHz
L = 4.7µH

## PIN FUNCTIONS

**FB1 (A6):** Feedback Input to the Error Amplifier of Channel 1 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to $V_{IN}$ by: $V_{OUT}$ = 0.6V • [1 + (R2/R1)].

**FB2 (F6):** Feedback Input to the Error Amplifier of Channel 2 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to $V_{IN}$ by: $V_{OUT}$ = 0.6V • [1 + (R2/R1)]. Connecting this pin to $INTV_{CC}$ turns this channel into a slave channel to channel 1.

**FB3 (F1):** Feedback Input to the Error Amplifier of Channel 3 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to $V_{IN}$ by: $V_{OUT}$ = 0.6V • [1 + (R2/R1)]. Connecting this pin to $INTV_{CC}$ turns this channel into a slave channel to channel 4.

**FB4 (A1):** Feedback Input to the Error Amplifier of Channel 4 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to $V_{IN}$ by: $V_{OUT}$ = 0.6V • [1 + (R2/R1)]. Connecting this pin to $INTV_{CC}$ turns this channel into a slave channel to channel 1.

## PIN FUNCTIONS

**$INTV_{CC}$ (A2):** Low Dropout Regulator. Bypass with a low ESR ceramic cap of at least 4.7µF to ground.

**MODE/SYNC (D2):** Burst Mode Select and External Clock Synchronization of the Step-Down Regulator. Tie MODE/SYNC to $INTV_{CC}$ for Burst Mode operation with a 550mA peak current clamp. Tie MODE/SYNC to GND for pulse skipping operation, and tie MODE/SYNC to a voltage between 1V and $INTV_{CC}$ – 1.2V for forced continuous mode. Furthermore, connecting this pin to an external clock will synchronize the switch clock to the external clock and put the part in forced continuous mode.

**GND (A3, A4, B3, B4, C3, C4, D3, D4, E3, E4, F3, F4):** Ground backplane for power and signal ground. These pins must be soldered to PCB ground for electrical contact and rated thermal performance. Connect all GND pins together with solid ground plane.

**PHASE (D5):** Phase Select Pin. Do not leave this pin floating. Tie this pin to GND to run the regulators in phase (0 degrees phase shift) between the SW rising edge of channel 1/2 and channel 3/4. Tie this pin to $INTV_{CC}$ to set 180 degrees phase shift between channel 1/2 and channel 3/4. When this pin is high, the phase shift may also be set by modulating the duty cycle of external clock on the MODE/SYNC pin (channel 1/2 edge synced to rising edge of clock, channel 3/4 edge synced to falling edge of clock). For 5A output configuration, this pin must be tied to ground. See the Applications Information section for more details.

**PGOOD1 (B5):** Open Drain Power Good Indicator for Channel 1.

**PGOOD2 (E5):** Open Drain Power Good Indicator for Channel 2.

**PGOOD3 (E2):** Open Drain Power Good Indicator for Channel 3.

**PGOOD4 (B2):** Open Drain Power Good Indicator for Channel 4.

**RUN1 (C5):** Logic Controlled RUN Input to Channel 1. Do not leave this pin floating. Logic High activates the step-down regulator.

**RUN2 (F5):** Logic Controlled RUN Input to Channel 2. Do not leave this pin floating. Logic High activates the step-down regulator.

**RUN3 (F2):** Logic Controlled RUN Input to Channel 3. Do not leave this pin floating. Logic High activates the step-down regulator.

**RUN4 (C2):** Logic Controlled RUN Input to Channel 4. Do not leave this pin floating. Logic High activates the step-down regulator.

**$SV_{IN}$ (A5):** Signal $V_{IN}$ Pin. This input powers the $INTV_{CC}$ LDO. May be a different voltage than $V_{IN1}$, $V_{IN2}$, $V_{IN3}$ or $V_{IN4}$. Connect $SV_{IN}$ to whichever $V_{INX}$ is highest; for applications where it is not known which $V_{IN}$ is highest, connect external diode between $SV_{IN}$ to all $V_{INX}$ to ensure that $SV_{IN}$ is less than a diode drop from the highest $V_{IN}$.

**SW1 (C6):** Switch Node Connection to the Inductor of Channel 1 Step-Down Regulator.

**SW2 (D6):** Switch Node Connection to the Inductor of Channel 2 Step-Down Regulator.

**SW3 (D1):** Switch Node Connection to the Inductor of Channel 3 Step-Down Regulator.

**SW4 (C1):** Switch Node Connection to the Inductor of Channel 4 Step-Down Regulator.

**$V_{IN1}$ (B6):** Input Voltage of Channel 1 Step-Down Regulator. May be a different voltage than other channels' $V_{IN}$.

**$V_{IN2}$ (E6):** Input Voltage of Channel 2 Step-Down Regulator. May be a different voltage than other channels' $V_{IN}$.

**$V_{IN3}$ (E1):** Input Voltage of Channel 3 Step-Down Regulator. May be a different voltage than other channels' $V_{IN}$.

**$V_{IN4}$ (B1):** Input Voltage of Channel 4 Step-Down Regulator. May be a different voltage than other channels' $V_{IN}$.

## BLOCK DIAGRAM

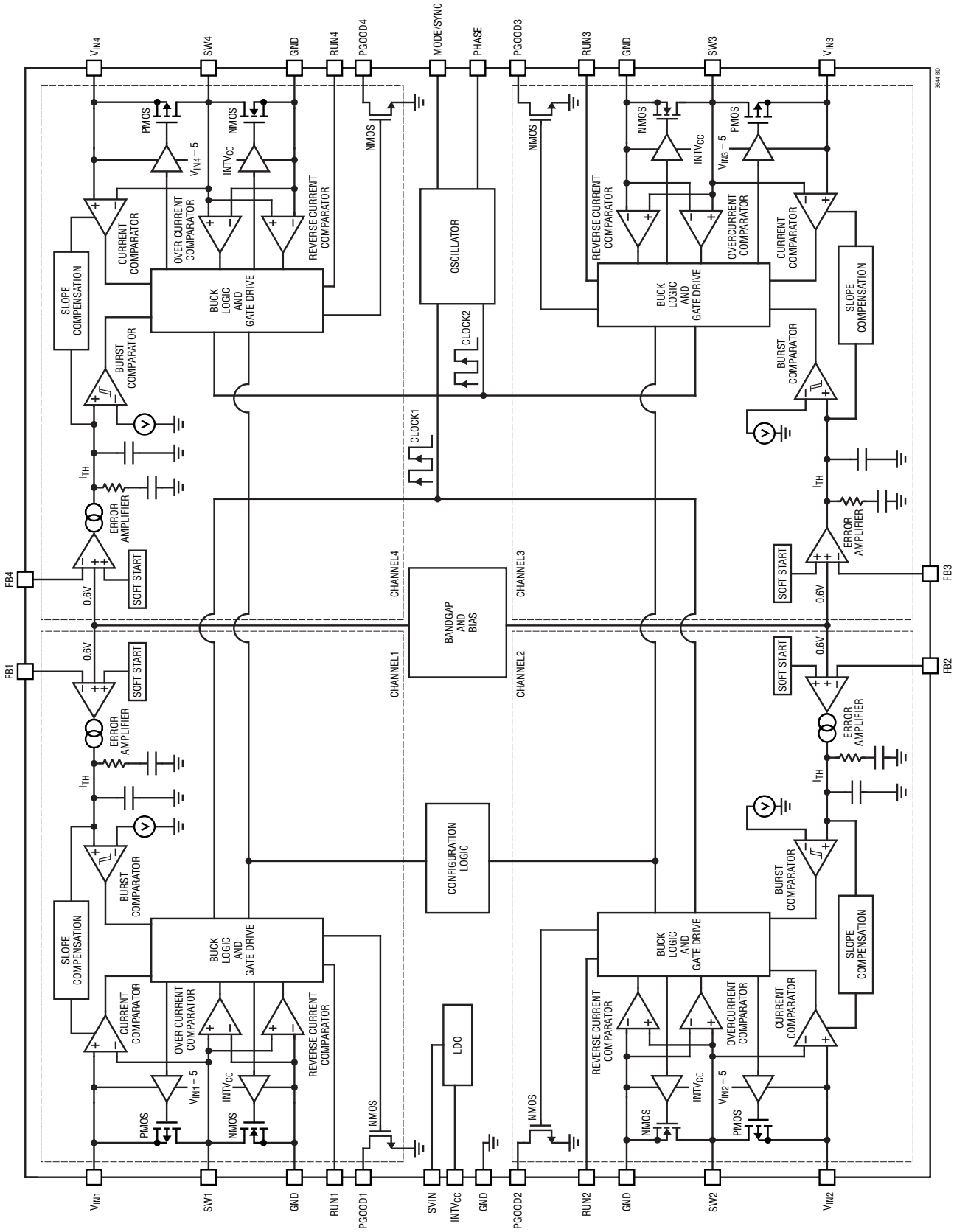



**Figure 1. Block Diagram**

## OPERATION

The LTC3644/LTC3644-2 is a quad high efficiency monolithic step-down regulator, which uses a constant frequency, peak current mode architecture. It operates through a wide $V_{IN}$ range and regulates with ultralow quiescent current. The operation frequency is set at either 1MHz or 2.25MHz and can be synchronized to an external oscillator ±50% of the inherent frequency. To suit a variety of applications, the selectable MODE/SYNC pin allows the user to trade off output ripple for efficiency.

For each channel, the output voltage is set by an external divider returned to the FB pin. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators pull the PGOOD output low if the output voltage is not within 7.5% of the programmed value. The PGOOD output goes high immediately after achieving regulation and goes low 32 clock cycles after falling out of regulation.

### Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle. The inductor current is allowed to ramp up to a peak level. Once the level is reached, the top power switch is turned off and the bottom switch (N-channel MOSFET) is turned on until the next clock cycle. The peak current level is controlled by the internally compensated ITH voltage, which is the output of the error amplifier. This amplifier compares the FB voltage to the 0.6V internal reference. When the load current increases, the FB voltage decreases slightly below the reference, which causes the error amplifier to increase the ITH voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground.

### Low Current Operation

Two discontinuous conduction modes (DCM) are available to control the operation of the LTC3644 at low currents. Both modes, Burst Mode operation and pulse-skipping mode, automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected by tying the MODE/SYNC pin to $INTV_{CC}$. In Burst Mode operation, the peak inductor current is set to be at least 550mA, even if the output of the error amplifier demands less. Thus, when the switcher is on at relatively light output loads, FB voltage will rise and cause the ITH voltage to drop. Once the ITH voltage goes below 0.2V, the switcher goes into sleep mode with both power switches off. The switchers remain in this sleep state until the external load pulls the output voltage below its regulation point. When all channels are in sleep mode, the part draws an ultralow 10µA of quiescent current from $SV_{IN}$.

To minimize $V_{OUT}$ ripple, pulse-skipping mode can be selected by grounding the MODE/SYNC pin. In LTC3644, pulse-skipping mode is implemented similarly to Burst Mode operation with the peak inductor current set to be at least 90mA. This results in lower ripple than in Burst Mode operation with the trade-off of slightly lower efficiency.

### Forced Continuous Mode Operation

The LTC3644 also has the ability to operate in the forced continuous mode by setting the MODE/SYNC voltage between 1V and $V_{INTVCC}$ – 1.2V. In forced continuous mode, the switcher switches cycle by cycle regardless of what the output load current is. If forced continuous mode is selected, the minimum peak current is set to be –250mA in order to ensure that the part can operate continuously at zero output load.

### High Duty Cycle/Dropout Operation

When the input supply voltage decreases towards the output voltage, the duty cycle increases and slope compensation is required to maintain the fixed switching frequency. The LTC3644 has internal circuitry to accurately maintain the peak current limit ($I_{LIM}$) of 2.2A even at high duty cycles.

As the duty cycle approaches 100%, the LTC3644 enters dropout operation. During dropout, the top PMOS switch is turned on continuously, and all active circuitry is kept alive.

## OPERATION

### $V_{IN}$ Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3644 constantly monitors the $V_{INX}$ pins for an overvoltage condition. When $V_{INX}$ rises above 19V, the corresponding regulator suspends operation by shutting off both power MOSFETs. Once $V_{INX}$ drops below 18.6V, the regulator immediately resumes normal operation. The regulators execute soft-start function when exiting an overvoltage condition.

### Low Supply Operation

To ensure that the regulators will operate properly, the LTC3644 incorporates an undervoltage lockout circuit that shuts down all channels if $SV_{IN}$ drops below 2.25V. Once $SV_{IN}$ rises above this lower limit, all switchers will resume normal operation if their respective RUN pins are enabled. However, the $R_{DS(ON)}$ of the top and bottom switch of each channels will be slightly higher than that specified in the electrical characteristics due to lack of gate drive. Refer to graph of $R_{DS(ON)}$ versus $V_{IN}$ for more details.

### Phase Selection

Channels 1,2 and channels 3,4 of the LTC3644 can operate in phase or 180° out-of-phase (anti-phase) depending on whether the PHASE pin is low or high, respectively. Anti-phase generally reduces input voltage and current ripple. Crosstalk between switch nodes SWx and components or sensitive lines connected to FBx can sometimes cause unstable switching waveforms and unexpectedly large input and output voltage ripple.

Crosstalk can generally be avoided by carefully choosing the phase shift such that the SW edges do not coincide. Depending on the duty cycle of the two channels, choose the phase option that keeps the SWx edges as far away from each other as possible. However, there are often situations where this is unavoidable, such as when all channels are operating at near 50% duty cycle. In such cases, the optimized phase shift can be set by modulating the duty cycle of an external clock on the MODE/SYNC pin (channel 1,2 edge synced to the rising edge of the external clock, channel 3,4 edge synced to the falling edge of the external clock), while keeping the PHASE pin voltage tied to $INTV_{CC}$. Figure 2 shows a 90° phase shift between channels 1, 2 and channels 3,4. Table 1 shows the phase options set by the PHASE and MODE/SYNC pins.

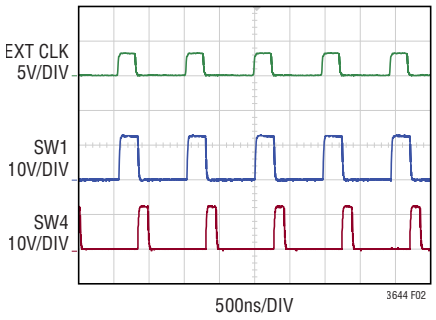



**Figure 2. 90° Phase Shift Set by External Clock**

**Table 1. Phase Selection**

| | No External CLK | External CLK |
|---|---|---|
| **PHASE = 0** | 0 degrees phase shift | 0 degrees phase shift |
| **PHASE = $INTV_{CC}$** | 180 degrees phase shift | Phase shift determined by clock edges |

### Soft-Start

The LTC3644 has an internal 1.1ms soft-start ramp for each channel. During soft-start operation, the switcher operates in pulse-skipping mode regardless of the mode programmed on the MODE/SYNC pin. Once the soft start period is complete, the part will transition into the desired mode of operation.

### Regulators with Combined Power Stages

The LTC3644 can be configured as the following:

1. Quad 1.25A outputs
2. Triple 2.5A/1.25A/1.25A outputs
3. Dual 2.5A outputs using only one inductor per output, or
4. Dual 3.75A/1.25A outputs

By connecting $V_{IN1,2}$ and $V_{IN3,4}$ together, SW1,2 and SW3,4 together, and connecting $FB_2$ and $FB_3$ to $INTV_{CC}$, LTC3644 supports dual 2.5A outputs using only one inductor per output. Even more, by connecting $V_{IN1,2,4}$ together, SW1,2,4 together, and FB2, FB4 to $INTV_{CC}$, LTC3644 supports 3.75A/1.25A outputs.

## APPLICATIONS INFORMATION

### Output Voltage Programming

The output voltage is set by external resistive divider according to the following equation:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 3.

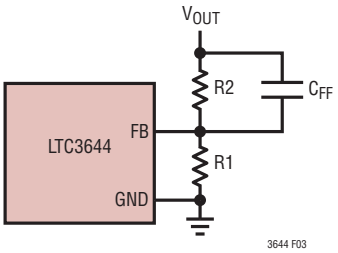



**Figure 3. Setting the Output Voltage**

### Input Capacitor ($C_{IN}$) Selection

The LTC3644 has individual input supply pins for each buck switching regulator and a separate $SV_{IN}$ pin that supplies power to all top level control and logic. Each of these pins must be decoupled with low ESR capacitors to GND. These capacitors must be placed as close to the pins as possible. Ceramic dielectric capacitors are a good compromise between high dielectric constant and stability versus temperature and DC bias. Note that the capacitance of a capacitor deteriorates at higher DC bias. It is important to consult manufacturer data sheets and obtain the true capacitance of a capacitor at the DC bias voltage it will be operated at. For this reason, avoid the use of Y5V dielectric capacitors. The X5R/X7R dielectric capacitors offer good overall performance.

### Output Capacitor ($C_{OUT}$) Selection

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LTC3644 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LTC3644's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For the LTC3644/LTC3644-2, a minimum $C_{OUT}$ of 47µF is recommended to ensure loop stability for $V_{OUT}$ lower than 2V. For good starting values, see the Typical Application section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between $V_{OUT}$ and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

### Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LTC3644 due to their piezoelectric nature. When in Burst Mode operation, the LTC3644's switching frequency depends on the load current, and at very light loads the LTC3644 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LTC3644 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

### Output Power Good

When the LTC3644's output voltages are within the ±7.5% window of the regulation point, the output voltages are good and the PGOOD pins are pulled high with external resistors. Otherwise, internal open-drain pull-down devices (275Ω) will pull the PGOOD pins low. To prevent unwanted PGOOD glitches during transients or dynamic $V_{OUT}$ changes, the LTC3644's PGOOD falling edge includes a blanking delay of approximately 32 switching cycles.

## APPLICATIONS INFORMATION

### Frequency Sync Capability

The LTC3644 has the capability to sync to a ±50% range of the internal programmed frequency. Once engaged in sync, the LTC3644 immediately runs at the external clock frequency in forced continuous mode.

### Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Lower ripple current reduces power losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current this is about 40% of $I_{OUT(MAX)}$. When calculating the ripple current, $I_{OUT(MAX)}$ refers to the maximum output current of the regulator, not the maximum load current of the intended application. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency in-creases, core loss decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that the inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coilcraft, Murata, Vishay, TDK and Würth Elektronik. Refer to Table 2 to Table 4 for more details.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2 etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources in the LTC3644 circuit are: 1) $I^2R$ losses, 2) switching and biasing losses, 3) other losses.

1. $I^2R$ losses are calculated from the DC resistances of the internal switches, $R_{SW}$, and external inductor, $R_L$. In continuous mode, the average output current flows through inductor L but is “chopped” between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both the top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain $I^2R$ losses:

   $$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

## APPLICATIONS INFORMATION

**Table 2. Recommended Inductors for 1.25A Buck Regulators**

| PART NUMBER | L (µH) | MAX DCR (mΩ) | MAX $I_{DC}$ (A) | SIZE IN mm (L × W × H) | MANUFACTURER |
|---|---|---|---|---|---|
| DFE201612E1R5MP2 | 1.5 | 72 | 3.2 | 2 × 1.6 × 1.2 | Murata |
| 74438356015 | 1.5 | 15 | 5.8 | 4.1 × 4.1 × 2.1 | Wurth Elektronik |
| IHLP1212BZER2R2M11 | 2.2 | 42.9 | 3.3 | 3 × 3 × 0.8 | Vishay |
| XAL4020222ME | 2.2 | 35.2 | 5.6 | 4 × 4 × 2.1 | Coilcraft |
| XAL4030332ME | 3.3 | 26 | 5.5 | 4 × 4 × 3.1 | Coilcraft |
| 74438356033 | 3.3 | 39.9 | 3.6 | 4.1 × 4.1 × 2.1 | Wurth Elektronik |
| IHLP2020CZER4R7M11 | 4.7 | 54 | 5.2 | 5.2 × 5.2 × 3 | Vishay |

**Table 3. Recommended Inductors for 2.5A Buck Regulators**

| PART NUMBER | L (µH) | MAX DCR (mΩ) | MAX $I_{DC}$ (A) | SIZE IN mm (L × W × H) | MANUFACTURER |
|---|---|---|---|---|---|
| XAL4020102ME | 1 | 13.25 | 8.7 | 4 × 4 × 2.1 | Coilcraft |
| 74437324010 | 1 | 27 | 5 | 4.5 × 4.1 × 1.8 | Wurth Elektronik |
| XAL4020152ME | 1.5 | 21.45 | 7.1 | 4 × 4 × 2.1 | Coilcraft |
| 74438356022 | 2.2 | 29 | 4.7 | 4.1 × 4.1 × 2.1 | Wurth Elektronik |
| IHLP2020CZER2R2M11 | 2.2 | 22.5 | 5.5 | 5.2 × 5.2 × 3 | Vishay |
| SPM6530T3R3M | 3.3 | 27 | 7.3 | 7.1 × 6.5 × 3 | TDK |

**Table 4. Recommended Inductors for 3.75A Buck Regulators**

| PART NUMBER | L (µH) | MAX DCR (mΩ) | MAX $I_{DC}$ (A) | SIZE IN mm (L × W × H) | MANUFACTURER |
|---|---|---|---|---|---|
| XAL4020601ME | 0.6 | 9.5 | 10.4 | 4 × 4 × 2.1 | Coilcraft |
| 744383560068 | 0.68 | 7.5 | 9.4 | 4.1 × 4.1 × 2.1 | Wurth Elektronik |
| XEL4020821ME | 0.82 | 11.8 | 10.2 | 4 × 4 × 2.1 | Coilcraft |
| IHLP2020CZER1E0M11 | 1 | 10 | 6.5 | 5.2 × 5.2 × 3 | Vishay |
| FDV0530H1R0M | 1 | 11.2 | 8.4 | 6.2 × 5.8 × 3 | Murata |
| SPM5030T2R2MHZ | 2.2 | 19.3 | 8.5 | 5.2 × 5 × 3 | TDK |

2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $V_{IN}$ to ground. The resulting dQ/dt is a current out of $V_{IN}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f_{OSC}(Q_T + Q_B)$, where $Q_T$ and $Q_B$ are the gate charges of the internal top and bottom power MOSFETs and $f_{OSC}$ is the switching frequency. The power loss is thus:

   Switching Loss = $I_{GATECHG} \bullet V_{IN}$

   The gate charge loss is proportional to $V_{IN}$ and $f_{OSC}$ and thus their effects will be more pronounced at higher supply voltages and higher frequencies.

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3644 internal power devices switch quickly enough that these loses are not significant compared to other sources. These losses plus other losses, including diode conduction losses

## APPLICATIONS INFORMATION

during dead-time and inductor core losses, generally account for less than 2% total additional loss.

### Thermal Conditions

In a majority of applications, the LTC3644 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3644 is running at high ambient temperature, high $V_{IN}$, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, all power switches will be turned off until the temperature drops about 15°C cooler.

To avoid the LTC3644 from exceeding the maximum junction temperature, the user need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC3644 is used in applications where $V_{IN}$ = 12V, $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 0.8A, f = 1MHz, $V_{OUT}$ = 1.8V. The equivalent power MOSFET resistance $R_{SW}$ is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 300m\Omega \bullet \frac{1.8V}{12V} + 80m\Omega \bullet \left(1 - \frac{1.8V}{12V}\right)$$

$$= 113m\Omega$$

The active current through $V_{IN}$ at 1MHz without load is about 5mA, which includes switching and internal biasing current loss, and transition loss. Therefore, the total power dissipated by the part is:

$$P_D = 4 \bullet I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet I_{IN(Q)}$$

$$= 4 \bullet 0.8A^2 \bullet 113m\Omega + 12V \bullet 5mA$$

$$= 349mW$$

For the BGA package, the $\theta_{JA}$ is 25°C/W as measured on the LTC3644 demo board. Therefore, the junction temperature of the regulator operating at 25°C ambient temperature is approximately:

$$T_J = 349mW \bullet 25°C/W + 25°C = 33.7°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that $R_{SW}$ increased 5% at 33.7°C yields a new junction temperature of 34.1°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or airflow.

### Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3644 (refer to Figure 4). Check the following in the layout:

1. Do the capacitors $C_{IN}$ connect to the $V_{IN}$ and GND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers. Does $C_{VCC}$ connect to $INTV_{CC}$ as close as possible?
2. Are $C_{OUT}$ and L closely connected? The (–) plate of $C_{OUT}$ returns current to GND and the (–) plate of $C_{IN}$.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of $C_{OUT}$ and a ground line terminated near GND. The feedback signal $V_{FB}$ should be routed away from noisy components and traces, such as the SW line, and its trace length should be minimized. Keep R1 and R2 close to the IC.
4. Keep sensitive components away from the SW pin. The input capacitor, $C_{IN}$, feedback resistors, and $INTV_{CC}$ bypass capacitors should be routed away from the SW trace and the inductor.
5. A ground plane is preferred. Use several vias connected to ground on the component side.
6. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

## APPLICATIONS INFORMATION

### Design Example

As a design example, consider using the LTC3644 in an application with the following specifications:

$SV_{IN} = V_{IN1} = V_{IN2} = V_{IN3} = V_{IN4}$ = 10.8V to 13.2V

$V_{OUT1}$ = 5V, $V_{OUT2}$ = 3.3V, $V_{OUT3}$ = 2.5V, $V_{OUT4}$ = 1.8V

$I_{LOAD1(MAX)} = I_{LOAD2(MAX)}$ = 400mA, $I_{LOAD3(MAX)}$ =1 A, $I_{LOAD4(MAX)}$ = 1.25A

$I_{OUT(MAX)}$ = 1.25A

$I_{OUT(MIN)}$ = 0

$f_{SW}$ = 1MHz

Because efficiency is important at both high and low load current, Burst Mode operation will be utilized.

To reduce input voltage and current ripple on the common input supply, the PHASE pin is tied to $INTV_{CC}$ for anti-phase operation between channels 1,2 and channels 3,4.

Given the internal oscillator of 1MHz, we can calculate the inductors value for about 40% ripple current at maximum $V_{IN}$:

$$L1 = \left(\frac{5V}{1MHz \bullet 0.5A}\right)\left(1 - \frac{5V}{13.2V}\right) = 6.21\mu H$$

$$L2 = \left(\frac{3.3V}{1MHz \bullet 0.5A}\right)\left(1 - \frac{3.3V}{13.2V}\right) = 4.95\mu H$$

$$L3 = \left(\frac{2.5V}{1MHz \bullet 0.5A}\right)\left(1 - \frac{2.5V}{13.2V}\right) = 4.05\mu H$$

$$L4 = \left(\frac{1.8V}{1MHz \bullet 0.5A}\right)\left(1 - \frac{1.8V}{13.2V}\right) = 3.11\mu H$$

Using standard values of L1 = 6.8µH, L2 = 4.7µH, L3 = 3.3µH and L4 = 3.3µH for inductors results in maximum ripple currents of:

$$\Delta I_{L1} = \left(\frac{5V}{1MHz \bullet 6.8\mu H}\right)\left(1 - \frac{5V}{13.2V}\right) = 0.46A$$

$$\Delta I_{L2} = \left(\frac{3.3V}{1MHz \bullet 4.7\mu H}\right)\left(1 - \frac{3.3V}{13.2V}\right) = 0.53A$$

$$\Delta I_{L3} = \left(\frac{2.5V}{1MHz \bullet 3.3\mu H}\right)\left(1 - \frac{2.5V}{13.2V}\right) = 0.61A$$

$$\Delta I_{L4} = \left(\frac{1.8V}{1MHz \bullet 3.3\mu H}\right)\left(1 - \frac{1.8V}{13.2V}\right) = 0.47A$$

$C_{OUT}$ will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, 47µF ceramic capacitors will be used.

To prevent large voltage transients, $C_{IN}$ should be sized based on the maximum RMS current:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

$$I_{RMS1} = 1.25A\left(\frac{5V}{13.2V}\right)\sqrt{\frac{13.2V}{5V} - 1} = 0.606A$$

$$I_{RMS2} = 1.25A\left(\frac{3.3V}{13.2V}\right)\sqrt{\frac{13.2}{3.3V} - 1} = 0.541A$$

$$I_{RMS3} = 1.25A\left(\frac{2.5V}{13.2V}\right)\sqrt{\frac{13.2}{2.5V} - 1} = 0.490A$$

$$I_{RMS4} = 1.25A\left(\frac{1.8V}{13.2V}\right)\sqrt{\frac{13.2}{1.8V} - 1} = 0.429A$$

$$I_{RMS} = I_{RMS1} + I_{RMS2} + I_{RMS3} + I_{RMS4} = 2.07A$$

Decoupling the $V_{INX}$ pins each with 22µF ceramic capacitors is adequate for most applications.

## APPLICATIONS INFORMATION

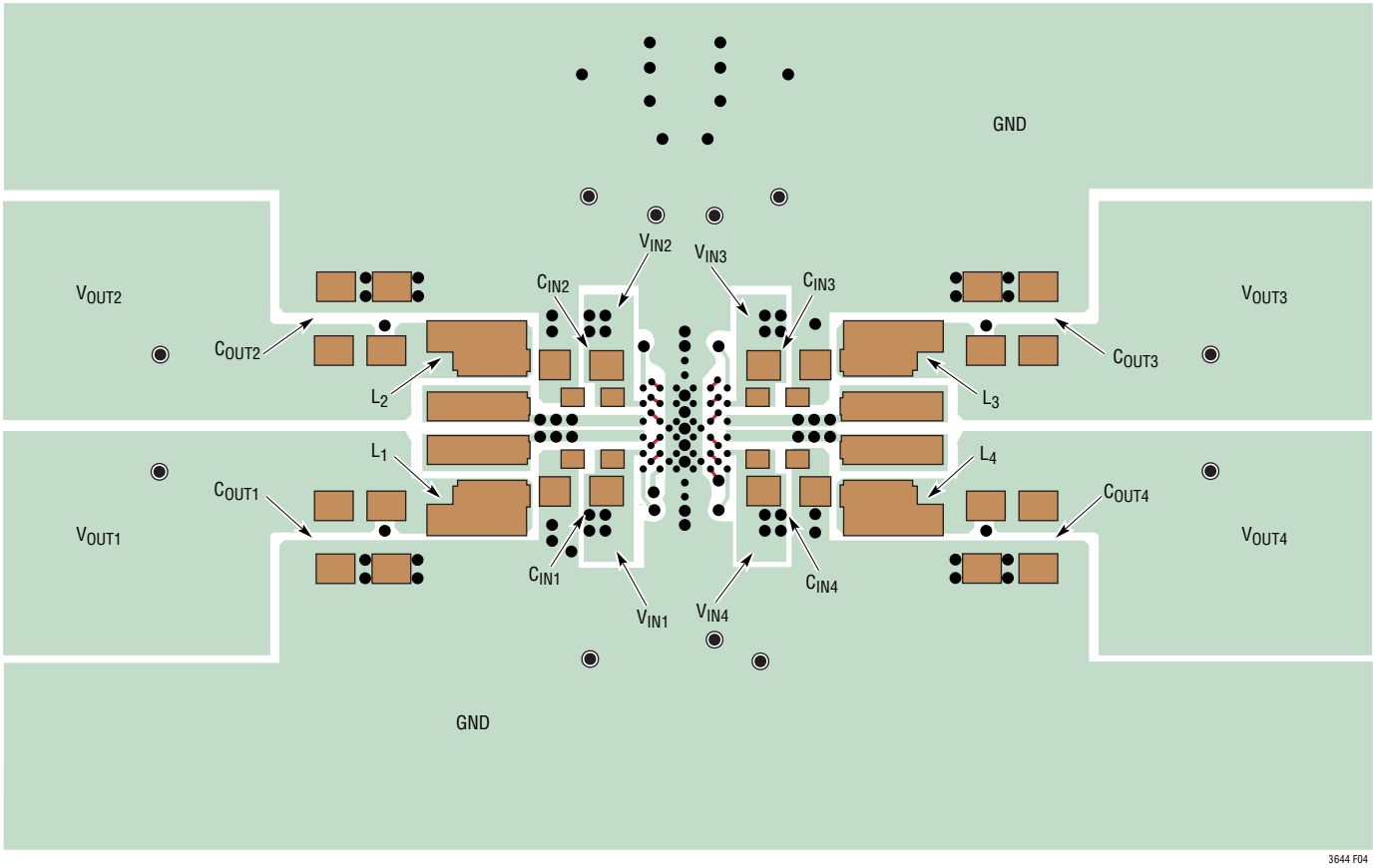



**Figure 4. Recommended Layout**

## APPLICATIONS INFORMATION

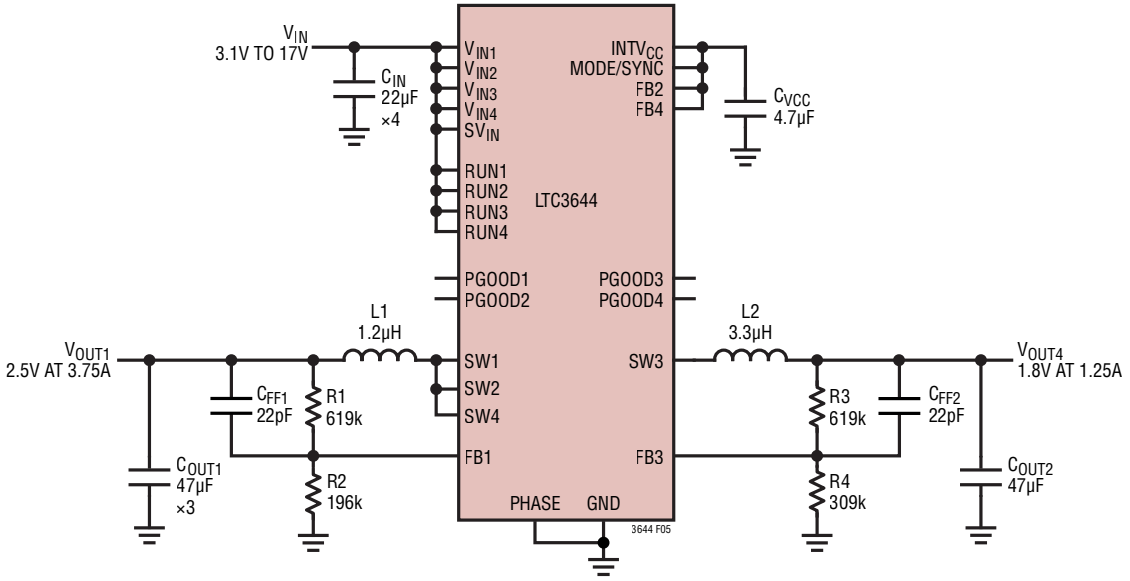



**Figure 5. Dual 3.75A/1.25A 1MHz Step-Down Regulator with Common Input Supply**

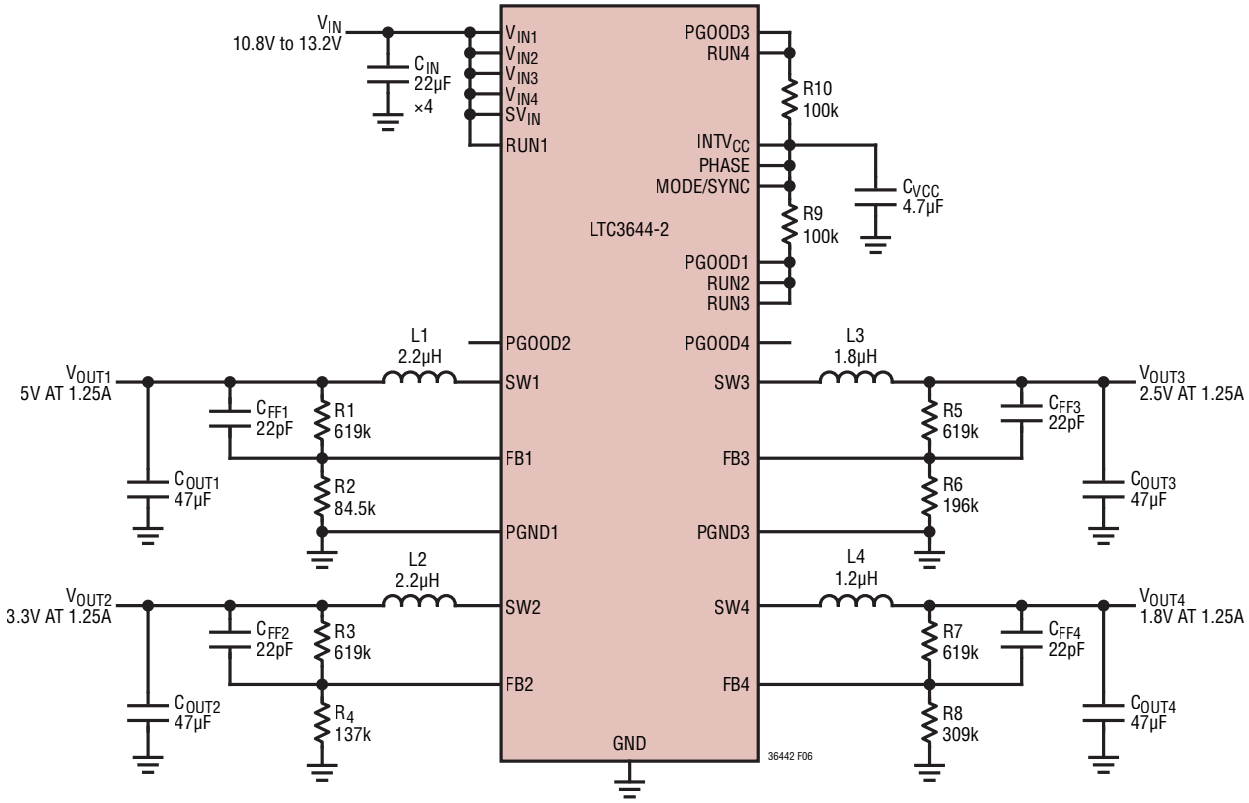



**Figure 6. 5V/3.3V/2.5V/1.8V Output 2.25MHz Step-Down Regulator with Common Input Supply and Sequenced Turn-On**

## TYPICAL APPLICATIONS

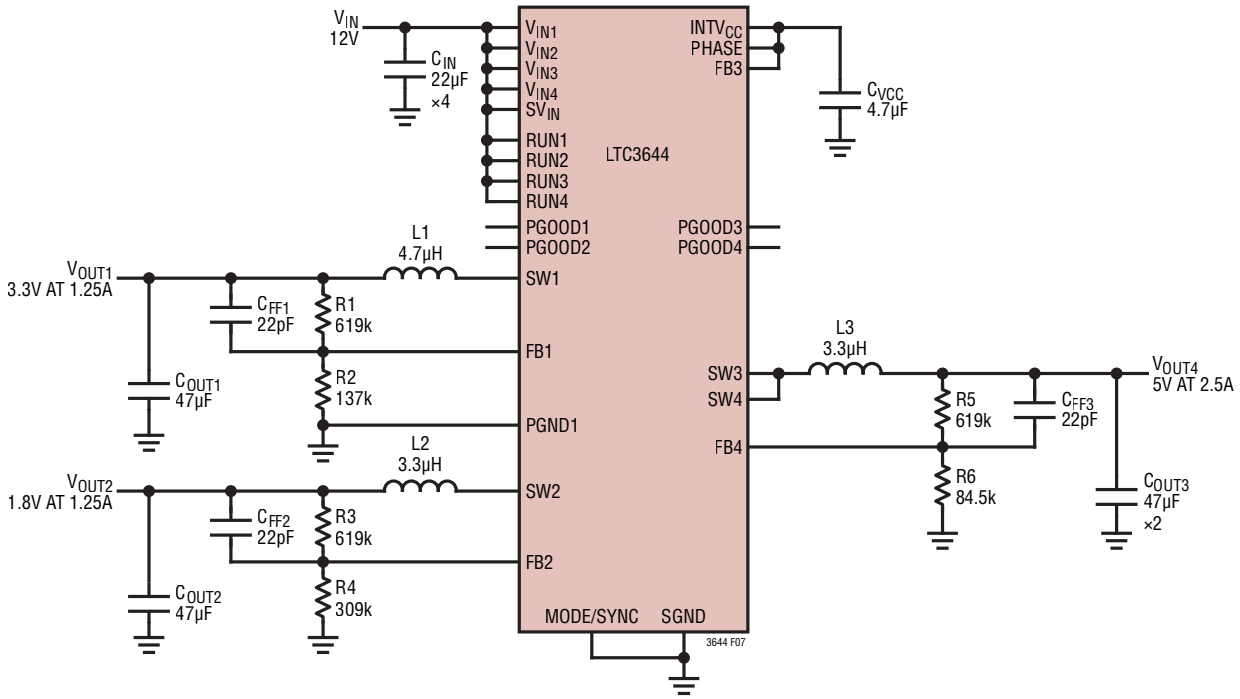
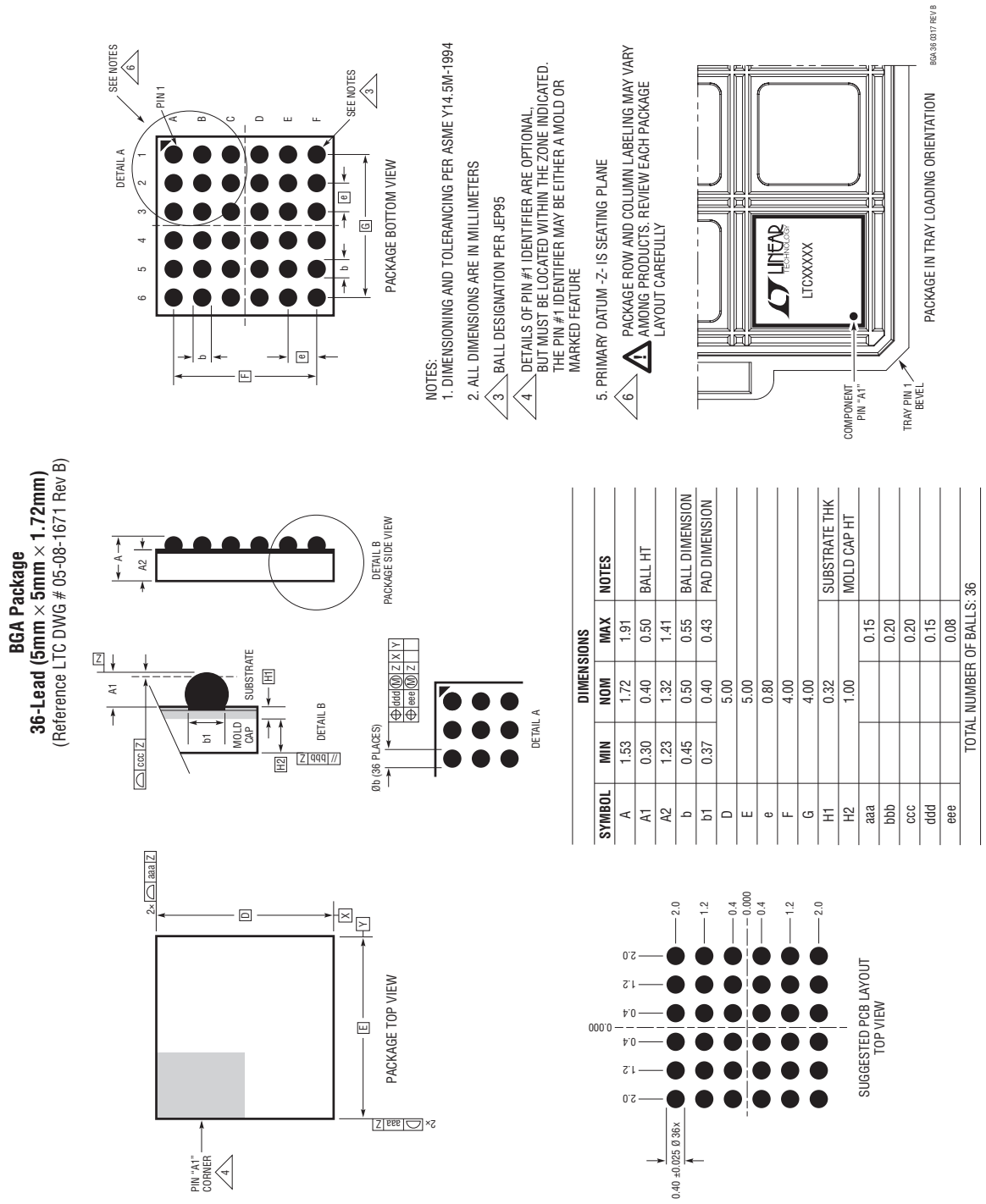



**Figure 7. 2.5A/1.25A/1.25A 1MHz Step-Down Regulator with Common Input Supply**

# PACKAGE DESCRIPTION




| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTES |
| A | 1.53 | 1.72 | 1.91 | |
| A1 | 0.30 | 0.40 | 0.50 | BALL HT |
| A2 | 1.23 | 1.32 | 1.41 | |
| b | 0.45 | 0.50 | 0.55 | BALL DIMENSION |
| b1 | 0.37 | 0.40 | 0.43 | PAD DIMENSION |
| D | | 5.00 | | |
| E | | 5.00 | | |
| e | | 0.80 | | |
| F | | 4.00 | | |
| G | | 4.00 | | |
| H1 | | 0.32 | | SUBSTRATE THK |
| H2 | | 1.00 | | MOLD CAP HT |
| aaa | | | 0.15 | |
| bbb | | | 0.20 | |
| ccc | | | 0.20 | |
| ddd | | | 0.15 | |
| eee | | | 0.08 | |
| TOTAL NUMBER OF BALLS: 36 | | | | |

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 03/24 | Added Tape and Reel versions | 2 |
| | | Rewrote Regulators with Combined Power Stages | 10 |



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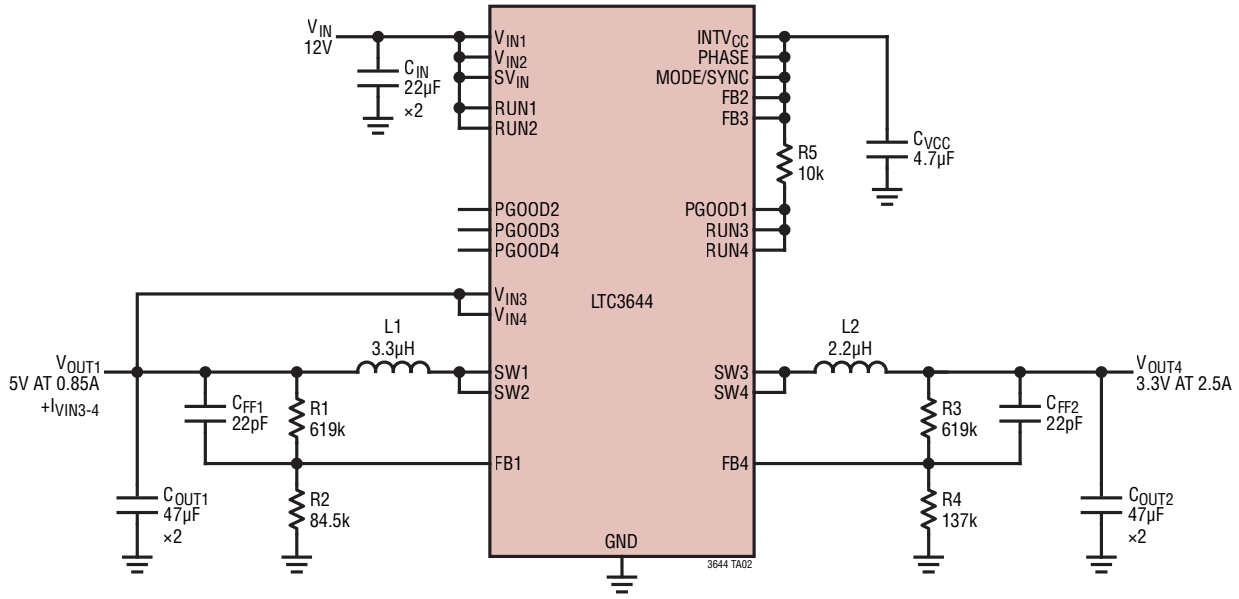
## TYPICAL APPLICATION

**0.85A/2.5A Series Output 1MHz Step-Down Regulator**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3621/ LTC3621-2 | 1A, 17V, 1MHz/2.25MHz, Synchronous Step-Down Regulator | 95% Efficiency, $V_{IN}$: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 3.5µA, $I_{SD}$ < 1µA, 2mm × 3mm DFN-6, MSOP-8E Packages |
| LTC3600 | 1.5A, 15V, 4MHz Synchronous Rail-to-Rail Single Resistor Step-Down Regulator | 95% Efficiency, $V_{IN}$: 4V to 15V, $V_{OUT(MIN)}$ = 0V, $I_Q$ = 700µA, $I_{SD}$ < 1µA, 3mm × 3mm DFN-12, MSOP-12E Packages |
| LTC3601 | 15V, 1.5A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 300µA, $I_{SD}$ < 1µA, 4mm × 4mm QFN-20, MSOP-16E Packages |
| LTC3603 | 15V, 2.5A ($I_{OUT}$) 3MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 75µA, $I_{SD}$ < 1µA, 4mm × 4mm QFN-20, MSOP-16E Packages |
| LTC3633A | 20V, Dual 3A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 3.6V to 20V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 500µA, $I_{SD}$ < 15µA, 4mm × 5mm QFN-28, TSSOP-28E Packages. A Version Up to 20$V_{IN}$ |
| LTC3605A | 20V, 5A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 4V to 20V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 2mA, $I_{SD}$ < 15µA, 4mm × 4mm QFN-24 Package. A Version Up to 20$V_{IN}$ |
| LTC3604 | 15V, 2.5A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 300µA, $I_{SD}$ < 14µA, 3mm × 3mm QFN-16, MSOP-16E Packages |
| LTC3624/ LTC3624-2 | 2A, 17V, 1MHz/2.25MHz Synchronous Step-Down Regulator | 95% Efficiency, $V_{IN}$: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 3.5µA, $I_{SD}$ < 1µA, 3mm × 3mm DFN-8, MSOP-12E Packages |
| LTC3622/ LTC3622-2/ LTC3622-23/5 | Dual 1A, 17V 1MHz/2.25MHz Synchronous Step-Down Regulator | 95% Efficiency, $V_{IN}$: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 5µA, $I_{SD}$ ≤ 1µA, 3mm × 4mm DFN-14, MSOP-16E Packages |
| LTC7124 | Dual Channel 3.5A, 17V Monolithic Synchronous Step-Down Regulator | 95% Efficiency, $V_{IN}$: 3.1V to 17V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ < 8µA, $I_{SD}$ < 1µA, 3mm × 5mm QFN-24 |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