Dual Output PolyPhase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management

FEATURES

- **PMBus/I²C Compliant Serial Interface**
  - **Monitor Voltage, Current, Temperature and Faults**
  - **Program Voltage, Soft-Start/Stop, Sequencing, Margining, AVP and UV/OV/OC Limits**
- **3V ≤ VINSNS ≤ 38V, 0.1V ≤ V_{OUT} ≤ 5.25V**
- **±0.5% Output Voltage Error**
- **Programmable PWM Frequency or External Clock Synchronization from 250kHz to 1.25MHz (2.5MHz-2)**
- **Accurate PolyPhase® Current Sharing**
- **Internal EEPROM with Fault Logging and ECC**
- IC Supply Range: 3V to 13.2V
- Resistor or Inductor DCR Current Sensing
- Power Good Output Voltage Monitor
- Optional Resistor Programming for Key Parameters
- 40-Pin (6mm × 6mm) QFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- High Current Distributed Power Systems
- Servers, Network and Storage Equipment
- Intelligent Energy Efficient Power Regulation

DESCRIPTION

The LTC®3882-1/LTC3882-2 is a dual, PolyPhase DC/DC synchronous step-down switching regulator controller with PMBus compliant serial interface. It uses a constant frequency, leading-edge modulation, voltage mode architecture for excellent transient response and output regulation. Each PWM channel can produce output voltages from 0.1V to 5.25V using a wide range of 3.3V compatible power stages, including power blocks, DrMOS or discrete FET drivers. Up to four LTC3882-1 devices can operate in parallel for 2-, 3-, 4-, 6- or 8-phase operation.

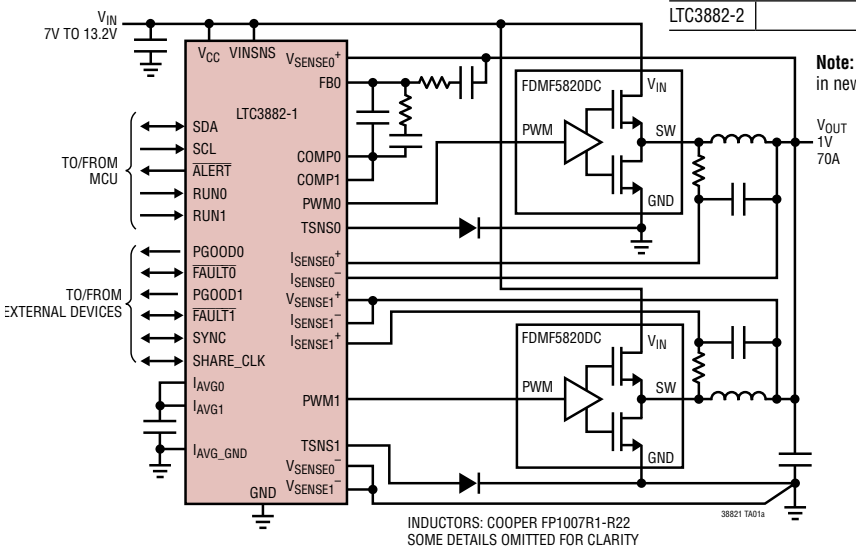
System configuration and monitoring is supported by the LTpowerPlay™ software tool. The LTC3882-1/LTC3882-2 serial interface can read back input voltage, output voltage and current, temperature and fault status. Most operating parameters can be set via the digital interface or stored in internal EEPROM for use at power up. Switching frequency and phase, output voltage and device address can also be set using external configuration resistors.

In this document, statements related to the LTC3882-1 apply to the LTC3882-2 unless specifically noted.

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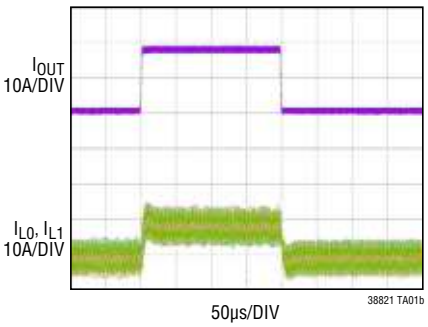
TYPICAL APPLICATION

	PWM ENABLE OUTPUT	TG/BG CONTROL	HW WRITE PROTECT	DEDICATED PGOOD OUTPUT	DIFFERENTIAL V_{OUT} SENSE	MAX PWM FREQUENCY
LTC3882	•	•	•		V_{OUT0}	1.25MHz
LTC3882-1				•	V_{OUT0} & V_{OUT1}	1.25MHz
LTC3882-2				•	V_{OUT0} & V_{OUT1}	2.5MHz



Note: Analog Devices, Inc., does not recommend using the following PWM frequencies in new designs: 600kHz, 750kHz, 900kHz, and 1MHz.

Load Step Transient Current Sharing (Using FDMF5820DC DrMOS)



Rev. D

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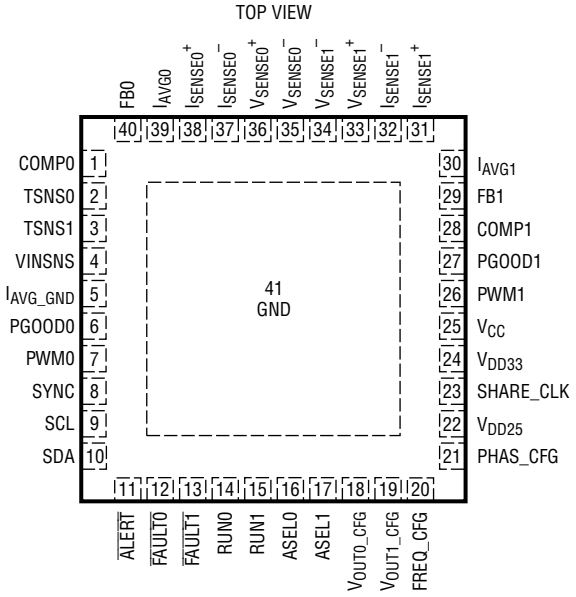
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage ..... –0.3V to 15V
VINSNS Voltage ..... –0.3V to 40V
V_{SENSEn^-} ..... –0.3V to 1V
V_{SENSEn^+}, I_{SENSEn^+}, I_{SENSEn^-} ..... –0.3V to 6V
FB*n*, COMP*n*, TSNS*n*, I_{AVG_GND}, I_{AVGn} ..... –0.3V to 3.6V
SYNC, $\overline{FAULT}$n, PGOOD*n*, SHARE_CLK.....–0.3V to 3.6V
SCL, SDA, RUN*n*, $\overline{ALERT}$ ..... –0.3V to 5.5V
ASEL*n*, VOUT*n*_CFG, FREQ_CFG,
PHAS_CFG..... –0.3V to 2.75V
PWM*n*, V_{DD25} ..... (Note 13)
V_{DD33} ..... (Note 14)
Operating Junction Temperature
(Notes 2, 3) ..... –40°C to 125°C*
Storage Temperature Range ..... –65°C to 150°C*
ABSMAX T_J ..... 125°C*

*See Derating EEPROM Retention at Temperature in the Applications Information section for junction temperatures in excess of 125°C.

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W , θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3882IUJ-1#PBF	LTC3882IUJ-1#TRPBF	LTC3882UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3882IUJ-2#PBF	LTC3882IUJ-2#TRPBF	LTC3882UJ-2	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC3882IUJ-1#WPBF	LTC3882IUJ-1#WTRPBF	LTC3882UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{CC} = 5V, V_{SENSE0}^+ = V_{SENSE1}^+ = 1.8V, V_{SENSE0}^- = V_{SENSE1}^- = I_{AVG_GND} = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IC Supply							
V_{CC}	V_{CC} Voltage Range	V_{DD33} = Internal LDO		4.5		13.8	V
V_{DD33_EXT}	V_{DD33} Voltage Range	V_{CC} = V_{DD33} (Note 6)	●	3		3.6	V
V_{UVLO}	Undervoltage Lockout Threshold	V_{DD33} Rising Hysteresis	●		 42	3	V mV
I_Q	IC Operating Current				32		mA
t_{INIT}	Controller Initialization Time	Delay from RESTORE_USER_ALL, MFR_RESET or V_{DD33} > V_{UVLO} Until TON_DELAY Can Begin			35		ms
V_{DD33} Linear Regulator							
V_{DD33}	V_{DD33} Regulator Output Voltage	V_{CC} ≥ 4.5V		3.2	3.3	3.4	V
I_{DD33}	V_{DD33} Current Limit	V_{DD33} = 2.8V V_{DD33} = 0V			85 40		mA mA
V_{DD25} Linear Regulator							
V_{DD25}	V_{DD25} Regulator Output Voltage			2.25	2.5	2.75	V
I_{DD25}	V_{DD25} Current Limit				95		mA
PWM Control Loops							
VINSNS	V_{IN} Sense Voltage Range			3		38	V
R_{VINSNS}	VINSNS Input Resistance				278		kΩ
V_{OUT_R0}	Range 0 Maximum V_{OUT} Range 0 Set Point Error (Note 7) Range 0 Set Point Resolution	 0.6V ≤ V_{OUT} ≤ 5V 0.6V ≤ V_{OUT} ≤ 5V	 ●	 –0.5	5.25 ±0.2 1.375	 0.5	V % % mV
V_{OUT_R1}	Range 1 Maximum V_{OUT} Range 1 Set Point Error (Note 7) Range 1 Set Point Resolution	 0.6V ≤ V_{OUT} ≤ 2.5V 0.6V ≤ V_{OUT} ≤ 2.5V	 ●	 –0.5	2.65 ±0.2 0.6875	 0.5	V % % mV
I_{VSENSE}	V_{SENSE} Input Current	V_{SENSE}^+ = 5.5V V_{SENSE}^- = 0V			235 –335		µA µA
$V_{LINEREG}$	V_{CC} Line Regulation, No Output Servo	4.5V ≤ V_{CC} ≤ 13.2V (See Test Circuit)		–0.02		0.02	%/V
AVP	AVP ΔV_{OUT}	AVP = 10%, VOUT_COMMAND = 1.8V, I_{SENSE} Differential Step 3mV to 12mV with IOUT_OC_WARN_LIMIT = 15mV	●	–118	–108	–96	mV
$A_{V(OL)}$	Error Amplifier Open-Loop Voltage Gain				87		dB
SR	Error Amplifier Slew Rate				9.5		V/µs
f_{0dB}	Error Amplifier Bandwidth	(Note 12)			30		MHz
I_{COMP}	Error Amplifier Output Current	Sourcing Sinking			–2.6 34		mA mA
R_{VSFB}	Resistance Between V_{SENSE}^+ and FB	Range 0 Range 1	● ●	52 37	67 49	83 61	kΩ kΩ
V_{ISENSE}	I_{SENSE} Differential Input Range				±70		mV
I_{ISENSE}	$I_{SENSE}^{\pm}$ Input Current	0V ≤ V_{PIN} ≤ 5.5V		–1	±0.1	1	µA
I_{AVG_VOS}	I_{AVG} Current Sense Offset	Referred to I_{SENSE} Inputs	 ●	 –600	±175 	 650	µV µV
V_{SIOS}	Slave Current Sharing Offset	Referred to I_{SENSE} Inputs	 ●	 –800	±300 	 700	µV µV
f_{SYNC}	SYNC Frequency Error	250kHz ≤ f_{SYNC} ≤ 1.25MHz LTC3882-1, 250kHz ≤ f_{SYNC} ≤ 2.5MHz LTC3882-2	●	–10		10	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{CC} = 5V, V_{SENSE0}^+ = V_{SENSE1}^+ = 1.8V, V_{SENSE0}^- = V_{SENSE1}^- = I_{AVG_GND} = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Supervisor							
V_{ON_TOL}	Input ON/OFF Threshold Error	15V ≤ V_{IN_ON} ≤ 35V	●	–2		2	%
N_{VON}	Input ON/OFF Threshold Resolution				143		mV
Output Voltage Supervisors							
V_{UVOV_R0}	Range 0 Maximum Threshold Range 0 Error Range 0 Threshold Resolution Range 0 Threshold Hysteresis	2V ≤ V_{OUT} ≤ 5V (Falling for UV and Rising for OV)	 ● 	 –1 	5.5 11 	 1 50	V % mV mV
V_{UVOV_R1}	Range 1 Maximum Threshold Range 1 Error Range 1 Threshold Resolution Range 1 Threshold Hysteresis	1V ≤ V_{OUT} ≤ 2.5V (Falling for UV and Rising for OV)	 ● 	 –1 	2.75 5.5 	 1 25	V % mV mV
Output Current Supervisors							
V_{ILIM_TOL}	Output Current Limit Tolerance $I_{SENSE}^+ – I_{SENSE}^-$	15mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 30mV 30mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 50mV 50mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 70mV	● ● ●	–1.7 –2.5 –5.2		1.7 2.5 5.2	mV mV mV
N_{ILIM}	$I_{SENSE}^+ – I_{SENSE}^-$ Threshold Resolution	1LSB			0.4		mV
ADC Readback Telemetry (Note 8)							
N_{VIN}	VINSNS Readback Resolution	(Note 9)			10		Bits
V_{IN_TUE}	VINSNS Total Unadjusted Readback Error	4.5V ≤ VINSNS ≤ 38V	 ●			0.5 2	% %
N_{DC}	PWM Duty Cycle Resolution	(Note 9)			10		Bits
DC_{TUE}	PWM Duty Cycle Total Unadjusted Readback Error	PWM Duty Cycle = 12.5%		–2		2	%
N_{VOUT}	V_{OUT} Readback Resolution				244		µV
V_{OUT_TUE}	V_{OUT} Total Unadjusted Readback Error	0.6V ≤ V_{OUT} ≤ 5.5V, Constant Load	 ●	 –0.5	±0.2 	 0.5	% %
N_{ISENSE}	I_{OUT} Readback Resolution LSB Step Size (at $I_{SENSE}^±$)	(Note 9) 0mV ≤ $\|I_{SENSE}^+ – I_{SENSE}^-\|$ < 16mV 16mV ≤ $\|I_{SENSE}^+ – I_{SENSE}^-\|$ < 32mV 32mV ≤ $\|I_{SENSE}^+ – I_{SENSE}^-\|$ < 63.9mV 63.9mV ≤ $\|I_{SENSE}^+ – I_{SENSE}^-\|$ ≤ 70mV			10 15.625 31.25 62.5 125		Bits µV µV µV µV
I_{SENSE_TUE}	I_{OUT} Total Unadjusted Readback Error	$\|I_{SENSE}^+ – I_{SENSE}^-\|$ ≥ 6mV, 0V ≤ V_{OUT} ≤ 5.5V	●	–1		1	%
I_{SENSE_OS}	I_{OUT} Zero-Code Offset Voltage				±32		µV
N_{TEMP}	Temperature Resolution				0.25		°C
T_{EXT_TUE}	External Temperature Total Unadjusted Readback Error	TSNS0, TSNS1 ≤ 1.85V (Note 10) MFR_PWM_MODE_LTC3882-1[6] = 0 MFR_PWM_MODE_LTC3882-1[6] = 1	 ● ●	 –3 –7	 	 3 7	 °C °C
T_{INT_TUE}	Internal Temperature Total Unadjusted Readback Error	Internal Diode (Note 10)			±1		°C
$t_{CONVERT}$	Update Rate	(Note 11)			90		ms
Internal EEPROM (Notes 4, 6)							
Endurance	Number of Write Operations	0°C ≤ T_J ≤ 85°C During All Write Operations		10,000			Cycles
Retention	Stored Data Retention	T_J ≤ 125°C		10			Years
Mass Write Time	STORE_USER_ALL Execution Duration	0°C ≤ T_J ≤ 85°C During All Write Operations			0.2	2	s

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{CC} = 5V, V_{SENSE0}^+ = V_{SENSE1}^+ = 1.8V, V_{SENSE0}^- = V_{SENSE1}^- = I_{AVG_GND} = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs (SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*, SYNC, SHARE_CLOCK)							
V_{IH}	Input High Voltage	SCL, SDA, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$ SYNC, SHARE_CLK	● ●	1.35 1.8			V V
V_{IL}	Input Low Voltage	SCL, SDA, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$ SYNC, SHARE_CLK	● ●			0.8 0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA			80		mV
C_{IN}	Input Capacitance	SCL, SDA, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, SYNC, SHARE_CLK (Note 12)				10	pF
t_{FILT}	Input Digital Filter Delay	$\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$ RUN0, RUN1			3 10		µs µs
Digital Outputs (SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*, SYNC, SHARE_CLOCK, $\overline{\text{ALERT}}$, PWM*n*, PGOOD*n*)							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA; SDA, SCL, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, SYNC, SHARE_CLK, $\overline{\text{ALERT}}$, I_{SINK} = 2mA; PWM*n*, PGOOD*n*	● ●		0.2	0.4 0.3	V V
V_{OH}	PWM*n* Output High Voltage	I_{SOURCE} = 2mA	●	2.7			V
I_{LKG}	Output Leakage Current	0V ≤ PWM0, PWM1, PGOOD0, PGOOD1 ≤ V_{DD33} 0V ≤ $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, SYNC, SHARE_CLK ≤ 3.6V 0V ≤ RUN0, RUN1 ≤ 5.5V 0V ≤ SCL, SDA, $\overline{\text{ALERT}}$ ≤ 5.5V	 ●	–1 –5 –5		1 5 5	µA µA µA
t_{RO}	PWM*n* Output Rise Time	C_{LOAD} = 30pF, 10% to 90%			5		ns
t_{FO}	PWM*n* Output Fall Time	C_{LOAD} = 30pF, 90% to 10%			4		ns
Serial Bus Timing							
f_{SMB}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition. After This Period, the First Clock Is Generated		●	0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		●	0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD,DAT}$	Data Hold Time: Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 ns µs
$t_{SU,DAT}$	Input Data Setup Time		●	100			ns
$t_{TIMEOUT}$	Clock Low Timeout		●	25		35	ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3882-1/LTC3882-2 is specified over the –40°C to 125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: EEPROM endurance, retention and mass write times are guaranteed by design, characterization and correlation with statistical process controls. Minimum retention applies only for devices cycled less than the minimum endurance specification. EEPROM read commands (e.g. RESTORE_USER_ALL) are valid over the entire specified operating junction temperature range.

Note 5: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 6: Minimum EEPROM endurance, retention and mass write time specifications apply when writing data with $3.15V \le V_{DD33} \le 3.45V$. EEPROM read commands are valid over the entire specified V_{DD33} operating range.

Note 7: Specified V_{OUT} error with AVP = 0% requires servo mode to be set with MFR_PWM_MODE_LTC3882-1 command bit 6. Performance is guaranteed by testing the LTC3882-1 in a feedback loop that servos V_{OUT} to a specified value.

Note 8: ADC tested with PWMs disabled. Comparable capability demonstrated by in-circuit evaluations. Total Unadjusted Error includes all gain and linearity errors, as well as offsets.

Note 9: Internal 32-bit calculations using 16-bit ADC results are limited to 10-bit resolution by PMBus Linear 11-bit data format.

Note 10: Limits guaranteed by TSNS voltage and current measurements during test, including ADC readback.

Note 11: Data conversion is done in round robin fashion. All inputs signals are continuously scanned in sequence resulting in a typical conversion latency of 90ms.

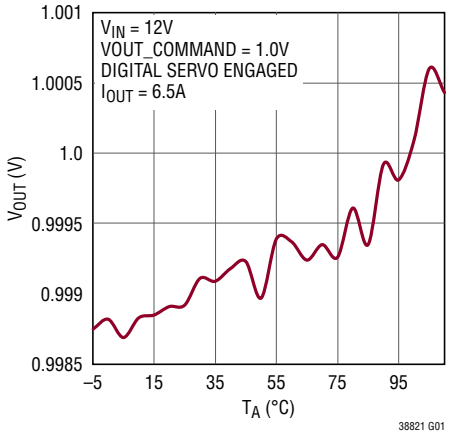
Note 12: Guaranteed by design.

Note 13: Do not apply a voltage or current source directly to these pins. They should only be connected to passive RC loads, otherwise permanent damage may occur.

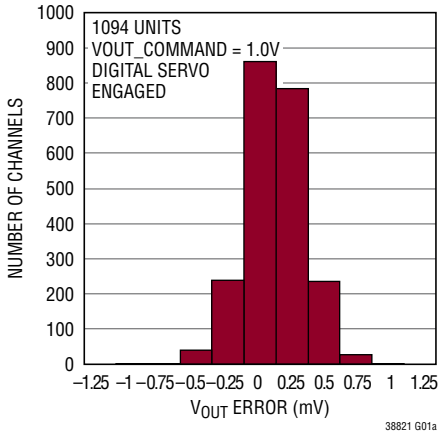
Note 14: Do not apply a voltage source to this pin unless shorted to V_{CC}. See Electrical Characteristics for applicable limits beyond which permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

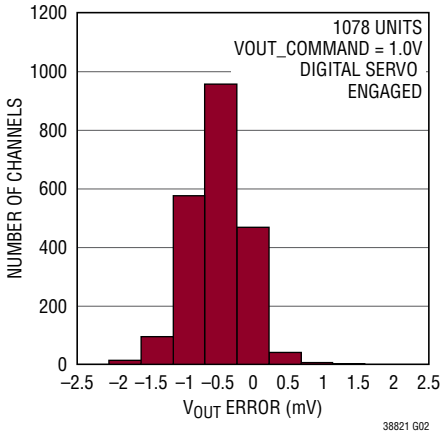
LTC3882-1 1.0V Regulated Output vs Temperature



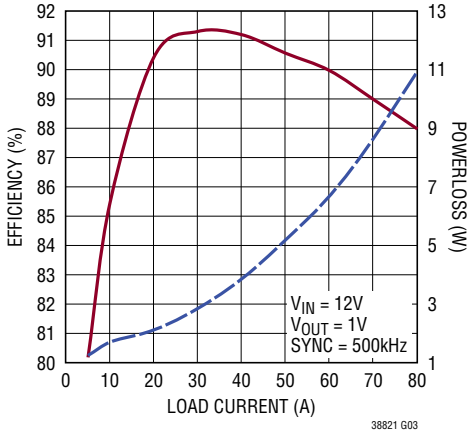
Typical LTC3882-1 Output Voltage Distribution at 0°C



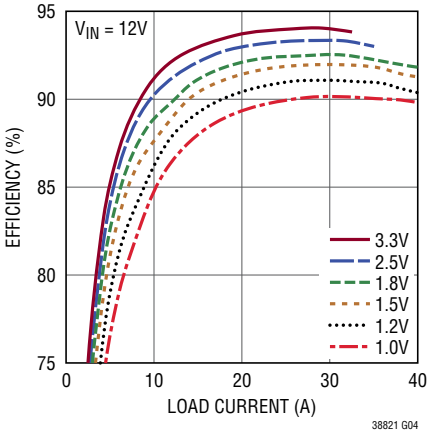
Typical LTC3882-1 Output Voltage Distribution at 105°C



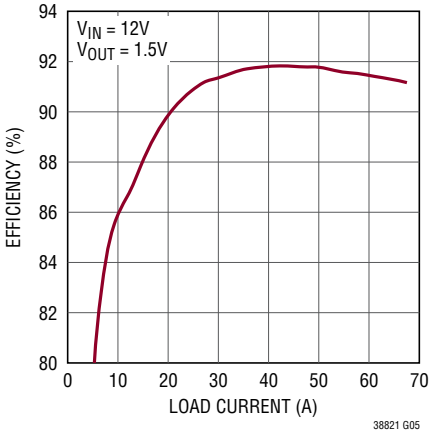
Efficiency and Loss vs Load (2-Phase Using FDMF5820DC DRMOS)



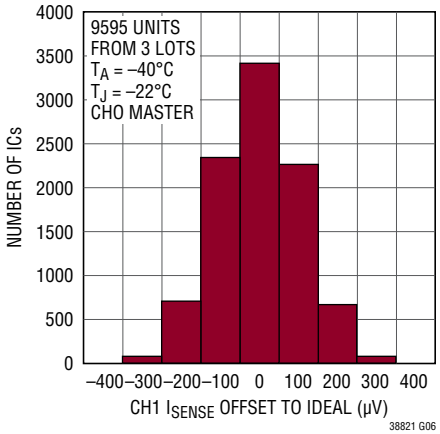
Efficiency vs Load Current (1-Phase Using D12S1R880A Power Block)



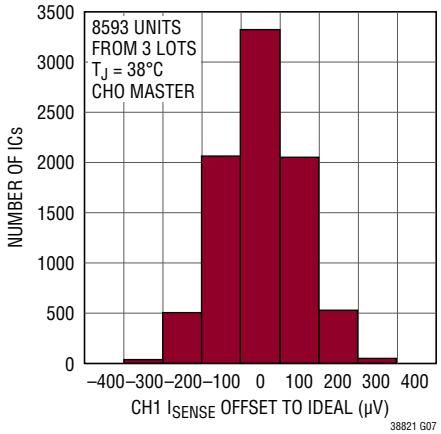
Efficiency vs Load Current (3-Phase Using D12S1R845A Power Block)



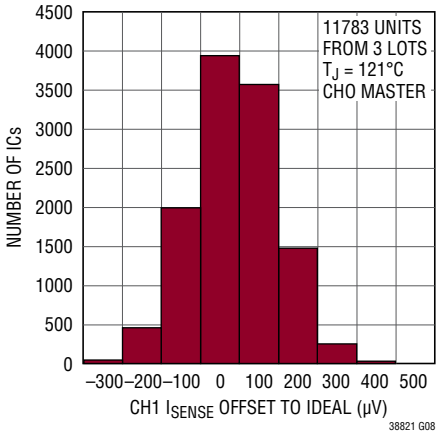
Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)



Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)



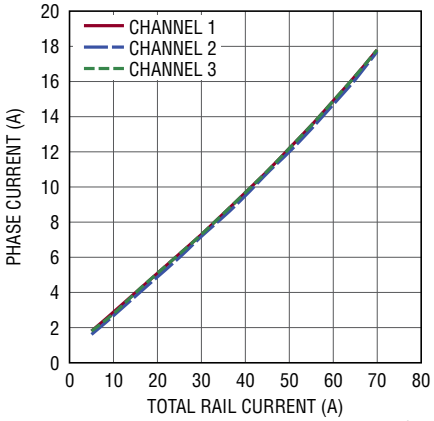
Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)



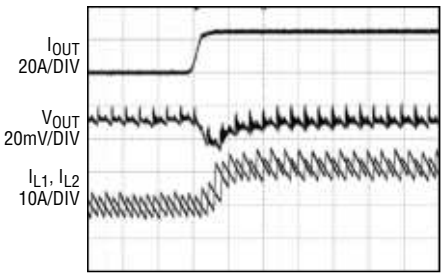
Rev. D

TYPICAL PERFORMANCE CHARACTERISTICS

3-Phase DC Output Current Sharing (Using D12S1R845A Power Block

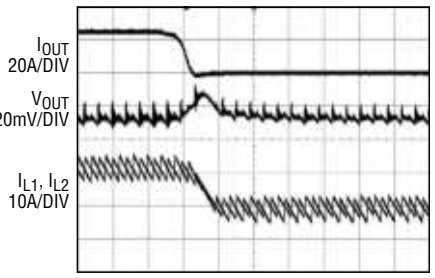


Load Step Transient Current Sharing (Using FDMF6707B DrMOS)



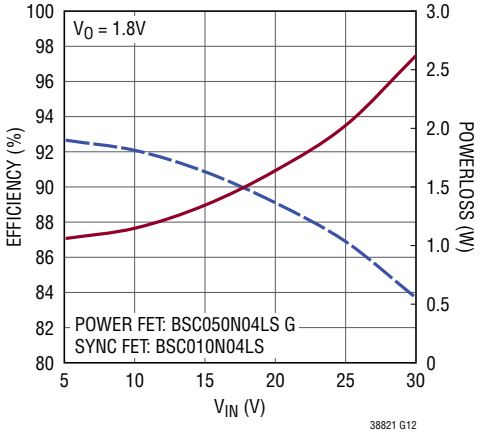
V_{OUT} = 1V
V_{IN} = 12V
SYNC = 500kHz
L = 320nH

Load Dump Transient Current Sharing (Using FDMF6707B DrMOS)

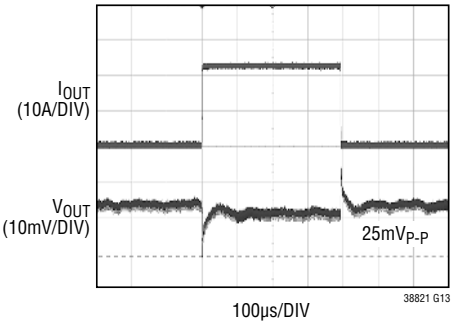


V_{OUT} = 1V
V_{IN} = 12V
SYNC = 500kHz
L = 320nH

Efficiency and Power Loss vs Input Voltage (1-Phase Using LTC4449)

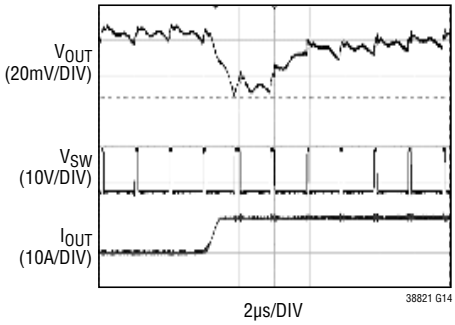


3-Phase Transient Response (Using D12S1R860A Power Block)



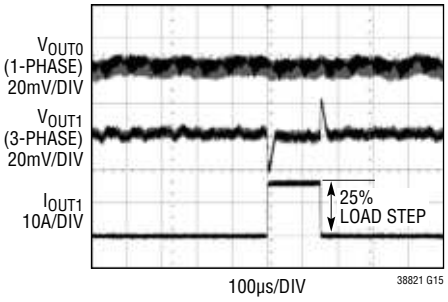
V_{OUT} = 0.9V/90A
V_{IN} = 12V
SYNC = 500kHz
L = 210nH

1-Phase Single Cycle Response (Using D12S1R860A Power Block with C_{OUT} = 6 × 100µF X5R 1210)

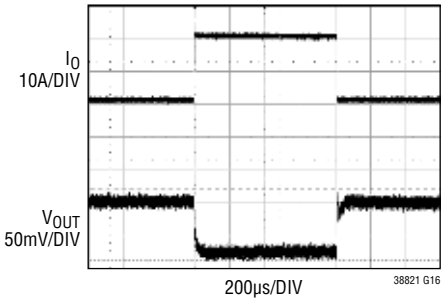


V_{OUT} = 1V/25A
V_{IN} = 12V
SYNC = 1MHz
L = 210nH

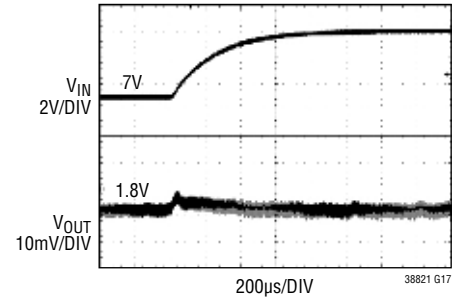
3+1 Channel Crosstalk (Using D12S1R845A Power Blocks)



Load Step Transient Response Using AVP

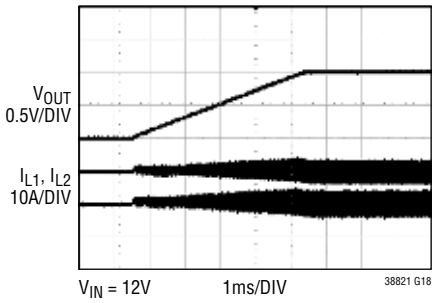


Line Step Transient Response (1-phase Using LTC4449)

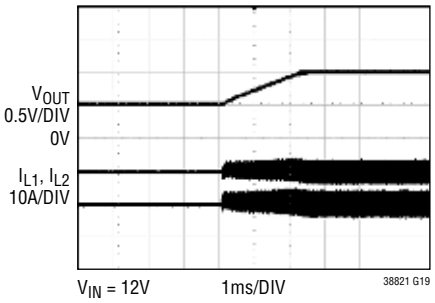


TYPICAL PERFORMANCE CHARACTERISTICS

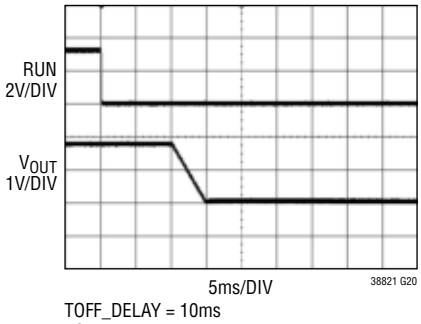
Soft-Start Ramp



Start-Up Into a Prebiased Load

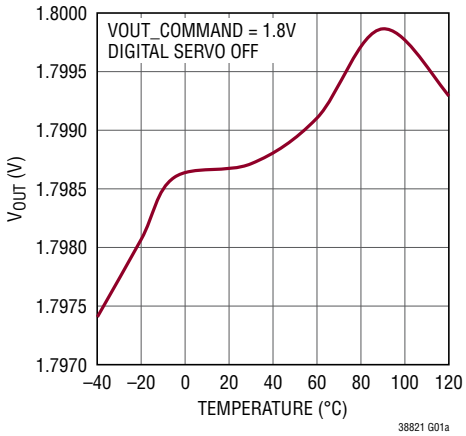


Soft-Off Ramp

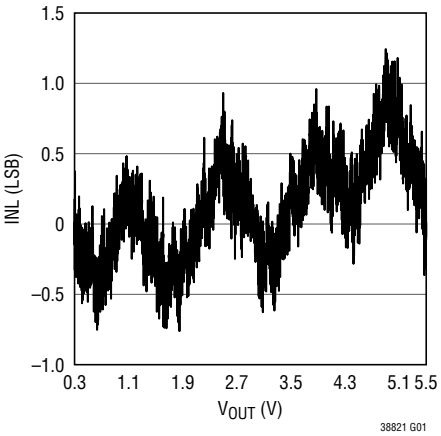


TOFF_DELAY = 10ms
TOFF_FALL = 5ms

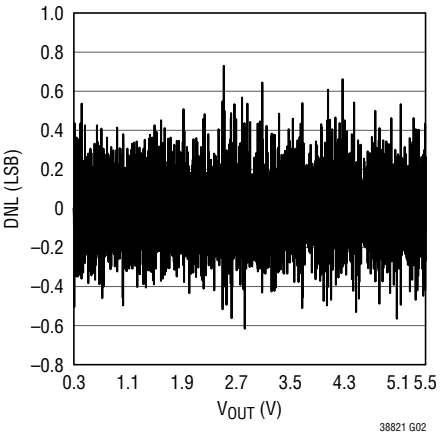
Regulated Output vs Temperature



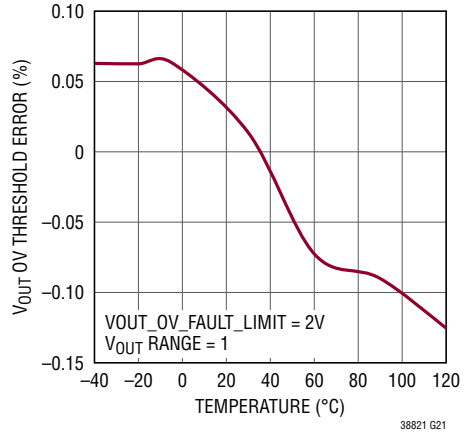
VOUT_COMMAND INL



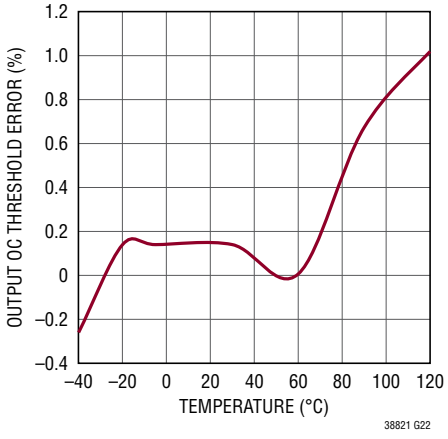
VOUT_COMMAND DNL



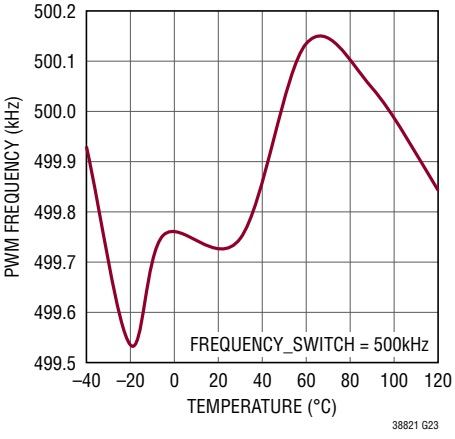
Output Overvoltage Threshold Error vs Temperature



Output Overcurrent Threshold Error vs Temperature



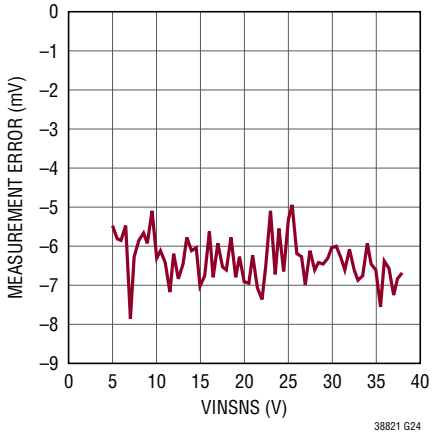
PWM Frequency vs Temperature



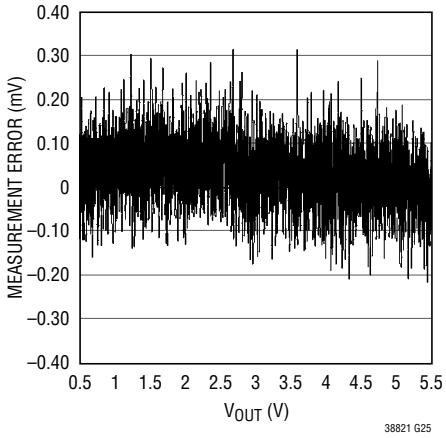
Rev. D

TYPICAL PERFORMANCE CHARACTERISTICS

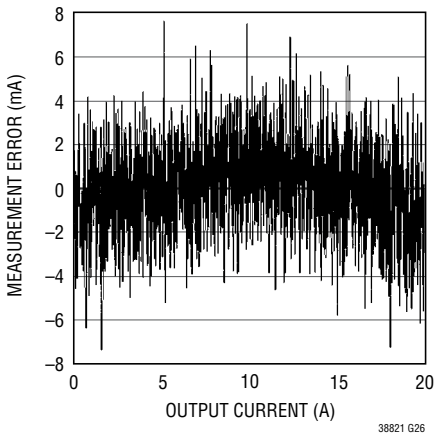
$V_{IN(SNS)}$ ADC TUE



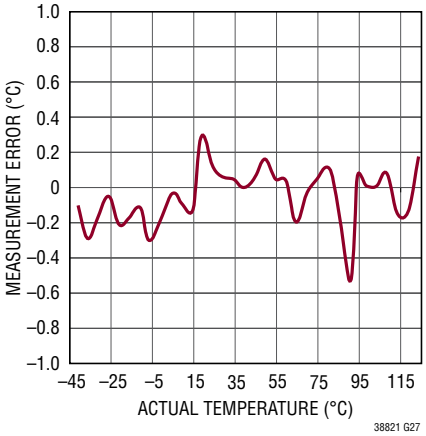
V_{OUT} ADC TUE



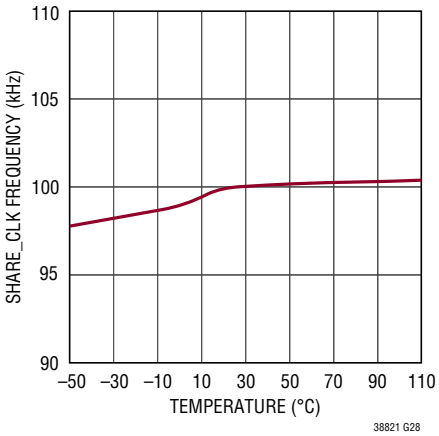
I_{OUT} ADC TUE



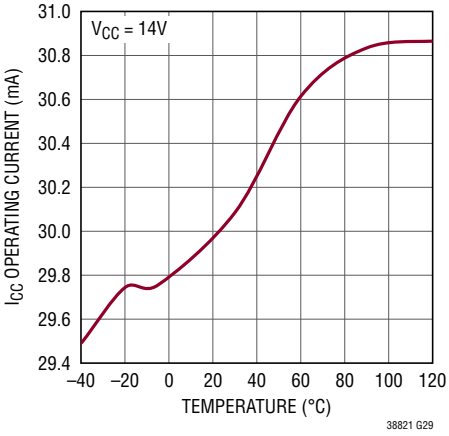
Temperature ADC TUE



SHARE_CLK Frequency vs Temperature



IC Operating Current vs Temperature



PIN FUNCTIONS

COMP0/COMP1 (Pin 1/Pin 28): Error Amplifier Outputs. PWM duty cycle increases with this control voltage. These are true low impedance outputs and cannot be directly connected together when active. For PolyPhase operation, wiring FB to V_{DD33} will three-state the error amplifier output of that channel, making it a slave. PolyPhase control is then implemented in part by connecting all slave COMP pins together to one master error amplifier output.

TSNS0/TSNS1 (Pin 2/Pin 3): External Temperature Sense Inputs. The LTC3882-1 supports two methods of calculation of external temperature based on forward-biased P/N junctions between these pins and GND.

VINSNS (Pin 4): V_{IN} Supply Sense. Connect to the V_{IN} power supply to provide line feedforward compensation. A change in V_{IN} immediately modulates the input to the PWM comparator and inversely changes the pulse width to provide excellent transient line regulation and fixed modulator voltage gain. An external lowpass filter can be added to this pin to prevent noisy signals from affecting the loop gain.

I_{AVG_GND} (Pin 5): I_{AVG} Ground Reference. The same I_{AVG_GND} should be shared between all channels of a PolyPhase rail and connected to system ground at a single point. I_{AVG_GND} may be wired directly to GND on ICs that do not share phases with other chips.

PGOOD/PGOOD1 (Pin 6/Pin 27): Power Good Indicator Open-Drain Outputs. These outputs are driven low through a 30µs filter when the respective channel output is below its programmed UV fault limit or above its programmed OV fault limit. If used, a pull-up resistor is required in the application. Operating voltage range is GND to V_{DD33}.

PWM0/PWM1 (Pin 7/Pin 26): PWM Three-State Control Outputs. These pins provide single-wire PWM switching control for each channel to an external gate driver, DrMOS or power block. Operating voltage range is GND to V_{DD33}.

SYNC (Pin 8): External Clock Synchronization Input and Open-Drain Output. If desired, an external clock can be applied to this pin to synchronize the internal PWM channels. If the LTC3882-1 is configured as a clock master, this pin will also pull to ground at the selected PWM switching frequency with a 125ns pulse width. A pull-up resistor to 3.3V is required in the application if SYNC is driven by any LTC3882-1. Minimize the capacitance on this line to ensure its time constant is fast enough for the application.

SCL (Pin 9): Serial Bus Clock Input. A pull-up resistor to 3.3V is required in the application.

SDA (Pin 10): Serial Bus Data Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{ALERT}}$ (Pin 11): Open-Drain Status Output. This pin may be connected to the system $\overline{\text{SMBALERT}}$ wire-AND interrupt signal and should be left open if not used. If used, a pull-up resistor is required in the application. Operating voltage range is GND to V_{DD33}.

$\overline{\text{FAULT0}}$/$\overline{\text{FAULT1}}$ (Pin 12/Pin 13): Programmable Digital Inputs and Open-Drain Outputs for Fault Sharing. Used for channel-to-channel fault communication and propagation. These pins should be left open if not used. If used, a pull-up resistor to 3.3V is required in the application.

RUN0/RUN1 (Pin 14/Pin 15): Run Control Inputs and Open-Drain Outputs. A voltage above 2V is required on these pins to enable the respective PWM channel. The LTC3882-1 will drive these pins low under certain reset/restart conditions regardless of any PMBus command settings. A pull-up resistor to 3.3V is required in the application.

ASEL0/ASEL1 (Pin 16/Pin 17): Serial Bus Address Select Pins. Connect optional 1% resistor dividers between V_{DD25} and GND to these pins to select the serial bus interface address. Refer to the Applications Information section for more detail.

V_{OUT0_CFG}/V_{OUT1_CFG} (Pin 18/Pin 19): Output Voltage Configuration Pins. Connect optional 1% resistor dividers between V_{DD25} and GND to these pins to select the output voltage for each channel. Refer to the Applications Information section for more detail.

FREQ_CFG (Pin 20): Frequency Configuration Pin. Connect an optional 1% resistor divider between V_{DD25} and GND to this pin to configure PWM switching frequency. Refer to the Applications Information section for more detail.

PIN FUNCTIONS

PHAS_CFG (Pin 21): Phase Configuration Pin. Connect an optional 1% resistor divider between V_{DD25} and GND to this pin to configure the phase of each PWM channel relative to SYNC. Refer to the Applications Information section for more detail.

V_{DD25} (Pin 22): Internal 2.5V Regulator Output. Bypass this pin to GND with a low ESR 1µF capacitor. Do not load this pin with external current beyond that required for local LTC3882-1 configuration pins, if any.

SHARE_CLK (Pin 23): Share Clock Open-Drain Output (bussed). Share Clock, nominally 100kHz, is used to sequence multiple rails in a power system utilizing more than one LTC PSM controller. A pull-up resistor is required in the application. Minimize the capacitance on this line to ensure the time constant is fast enough for the application. Operating voltage range is GND to V_{DD33}.

V_{DD33} (Pin 24): Internal 3.3V Regulator Output. Bypass this pin to GND with a low ESR 2.2µF capacitor. The LTC3882-1 may also be powered from an external 3.3V rail attached to this pin, if also shorted to V_{CC}. Do not overload this pin with external system current. Local pull-up resistors for the LTC3882-1 itself may be powered from V_{DD33}. Refer to the Applications Information section for more detail.

V_{CC} (Pin 25): 3.3V Regulator Input. Bypass this pin to GND with a capacitor (0.1µF to 1µF ceramic) in close proximity to the IC.

V_{SENSE0}^-/V_{SENSE1}^- (Pin 35/Pin 34): Negative Output Voltage Sense Inputs. These pins must still be properly connected on slave channels for accurate output current telemetry.

V_{SENSE0}^+/V_{SENSE1}^+ (Pin 36/Pin 33): Positive Output Voltage Sense Inputs. These pins must still be properly connected on slave channels for accurate output current telemetry.

I_{SENSE0}^-/I_{SENSE1}^- (Pin 37/Pin 32): Current Sense Amplifier Inputs. The (–) inputs to the amplifiers are normally connected to the low side of a DCR sensing network or output current sense resistor for each phase.

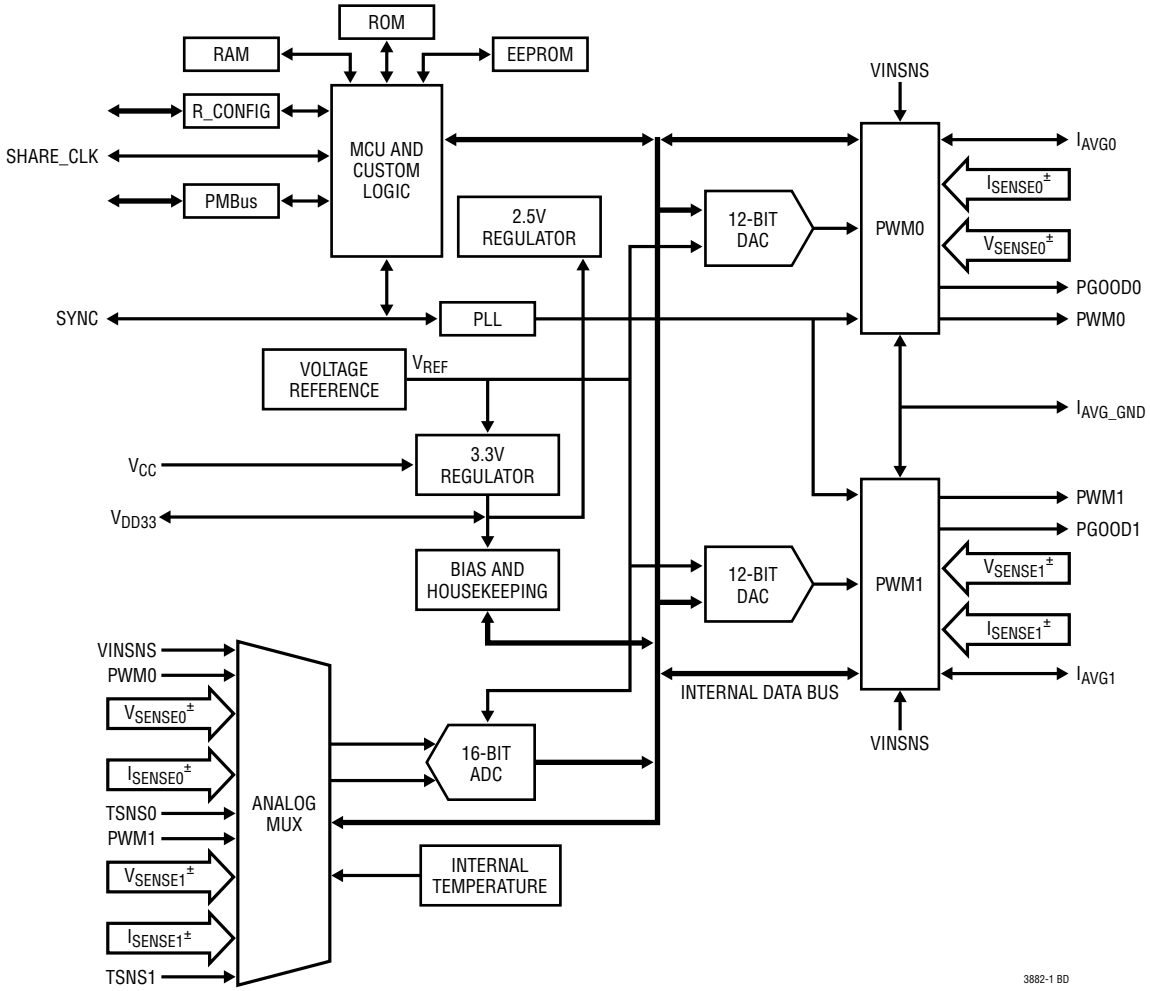
I_{SENSE0}^+/I_{SENSE1}^+ (Pin 38/Pin 31): Current Sense Amplifier Inputs. The (+) inputs are normally connected to the high side of an output current sense resistor or the R-C midpoint of a parallel DCR sense circuit.

I_{AVG0}/I_{AVG1} (Pin 39/Pin 30): Average Current Control Pins. A capacitor connected between these pins and I_{AVG_GND} stores a voltage proportional to the average output current of the master channel. PolyPhase control is then implemented in part by connecting all slave I_{AVG} pins together to the master I_{AVG} output. This pin should be left open on channels that control single-phase outputs. Operating voltage range is GND to 2.1V.

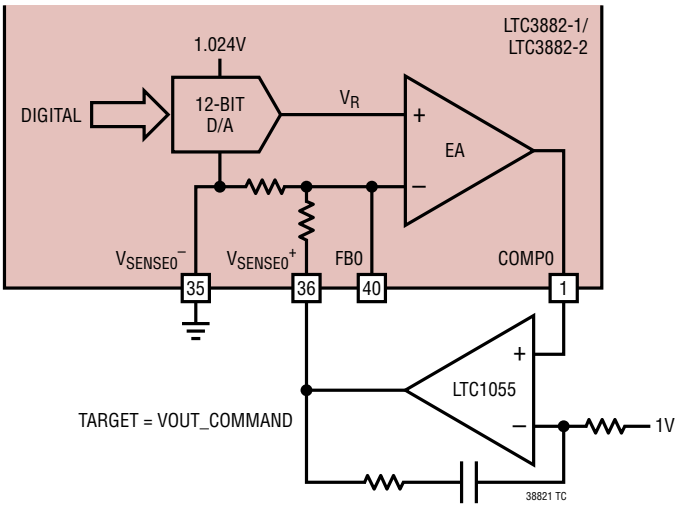
FB0/FB1 (Pin 40/Pin 29): Error Amplifier Inverting Inputs. These pins provide an internally scaled version of the output voltage for use in loop compensation. Refer to the Applications Information section for additional details on compensating the output voltage control loop with external components.

GND (Exposed Pad Pin 41): Ground. All small-signal and compensation components should connect to this pad. *The exposed pad must be soldered to a suitable PCB copper ground plane for proper electrical operation and to obtain the specified package thermal resistance.*

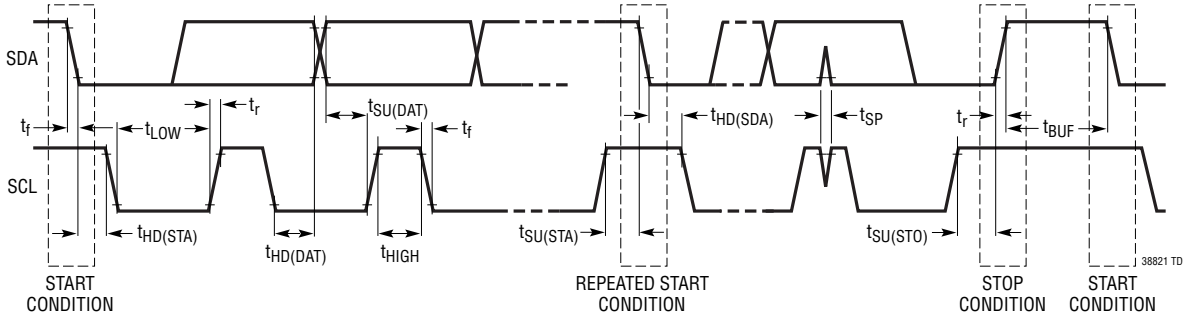
BLOCK DIAGRAM



TEST CIRCUIT (Channel 0 Example)



TIMING DIAGRAM



OPERATION

Overview

The LTC3882-1/LTC3882-2 is a dual channel/dual phase, constant frequency analog voltage mode controller for DC/DC step-down applications. The LTC3882-1 operates to 1.25MHz and the LTC3882-2 operates to 2.5MHz. In this document, statements related to the LTC3882-1 apply to the LTC3882-2 unless specifically noted. It features a PMBus compliant digital interface for monitoring and control of important power system parameters. The chip operates from an IC power supply between 3V and 13.2V and is intended for conversion from V_{IN} between 3V and 38V to output voltages between 0.5V and 5.25V. It is designed to be used in a switching architecture with external FET drivers, including higher level integrations such as non-isolated power blocks.

Major features include:

- Digitally Programmable Output Voltage
- Digitally Programmable Output Current Limit
- Digitally Programmable Input Voltage Supervisor
- Digitally Programmable Output Voltage Supervisors
- Digitally Programmable Switching Frequency
- Digitally Programmable On and Off Delay Times
- Digitally Programmable Soft-Start/Stop
- Operating Condition Telemetry
- Phase Locked Loop for Synchronous PolyPhase Operation (2, 3, 4, 6, or 8 phases)
- Fully Differential Load Sense
- Non-Volatile Configuration Memory with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Controllers
- Fault Event Data Logging
- Capable of Standalone Operation with Default Factory Configuration
- PMBus Revision 1.2 Compliant Interface up to 400kHz

The PMBus interface provides access to important power management data during system operation including:

- Average Input Voltage
- Average Output Voltages
- Average Output Currents
- Average PWM Duty Cycles
- Internal LTC3882-1 Temperature
- External Sensed Temperatures
- Warning and Fault Status, Including Input and Output Undervoltage and Overvoltage

The LTC3882-1 supports four serial bus addressing schemes to access the individual PWM channels separately or jointly.

Fault communication, reporting and system response behavior are fully configurable. Two fault I/Os are provided ($\overline{FAULT0}$, $\overline{FAULT1}$) that can be controlled independently. A separate $\overline{ALERT}$ pin also provides for a maskable SMBALERT#. Fault responses for each channel may be individually programmed, depending on the fault type. PMBus status commands allow fault reporting over the serial bus to identify a specific fault event.

Main Control Loop

The LTC3882-1 utilizes constant frequency voltage mode control with leading-edge modulation. This provides improved response to a load step increase, especially at larger V_{IN}/V_{OUT} ratios found in the low voltage, high current solutions demanded by modern digital subsystems. The LTC3882-1 leading-edge modulation architecture does not have a minimum on-time requirement. Minimum duty cycle will be determined by performance limits of the external power stage. The IC is also capable of active voltage positioning (AVP) to afford the smallest output capacitors possible for a given output voltage accuracy over the anticipated full load range. The LTC3882-1 error amplifiers have high bandwidth, low offset and low output impedance, allowing the control loop compensation network to be optimized for very high crossover frequencies and excellent transient response. The controller also achieves outstanding line transient response by using

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input feedforward compensation to instantaneously adjust PWM duty cycle and significantly reduce output under/overshoot during supply voltage changes. This also has the added advantage of making the DC loop gain independent of input voltage.

The main PWM control loop used for each channel is illustrated in Figure 1. During normal operation the top MOSFET (power switch) driving choke L1 is commanded off when the clock for that channel resets the RS latch. The power switch is commanded back on when the main PWM comparator VC, sets the RS latch. The error amplifier EA output (COMP) controls the PWM duty cycle to match the FB voltage to the EA positive terminal voltage in steady state. A patented circuit adjusts this output for VINSNS line feedforward.

The positive terminal of the EA is connected to the output of a 12-bit DAC with values ranging from 0V to 1.024V. The DAC value is determined by the resistor configuration pins detailed in application Table 8, by values retrieved from internal EEPROM, or by a combination of PMBus commands to synthesize the desired output voltage. Refer to the following PMBus Command Details section of this document for more information. The LTC3882-1 supports two output ranges. EA can regulate the output voltage to 5.5x the DAC output (Range 0) or 2.75x the DAC output (Range 1).

VC discriminates its positive input against an internally generated PWM voltage ramp. The positive input is a composite control based on COMP voltage with line feedforward compensation, and current sharing if the channel controls a slave phase. When the ramp falls below this voltage the comparator trips and sets the PWM latch.

If load current increases, V_{SENSE}^+ and FB will droop slightly with respect to the 12-bit DAC output. This causes the COMP voltage to increase until the average inductor current matches the new load current and the desired output voltage is restored. Programmable comparators I_{LIM} and I_{REV} monitor peak instantaneous forward and reverse inductor current for pulse-by-pulse protection. The top power MOSFET is immediately commanded off if the programmed positive limit is reached, and the bottom MOSFET is immediately commanded off if the negative limit is reached. Repeated peak overcurrent events cause an overcurrent fault to be set.

When the top MOSFET is commanded off, the bottom MOSFET is normally commanded on. In continuous conduction mode (CCM) the bottom MOSFET stays on until comparator VC turns the top MOSFET back on. Otherwise in discontinuous conduction mode (DCM, also known as diode emulation) the bottom MOSFET is commanded off if the I_{REV} comparator detects that the inductor current has decayed to approximately 0A. In any case the next PWM cycle starts when the clock for that channel again clears the RS latch.

Power-Up and Initialization

The LTC3882-1 is designed to provide stand-alone supply sequencing with controlled turn-on and turn-off functions. It operates from a single IC input supply of 3V to 13.2V while two on-chip linear regulators generate internal 2.5V and 3.3V. If V_{CC} is below 4.5V, the V_{CC} and V_{DD33} pins must be shorted together and limited to a maximum operating voltage of 3.6V. Controller configuration is reset by the internal UVLO threshold, where V_{DD33} must be at or above 3V and the internal 2.5V supply must be within about 20% of its regulated value. At that point the internal microcontroller begins initialization. A PMBus RESTORE_USER_ALL or MFR_RESET command forces this same initialization.

The LTC3882-1 features an internal RAM built-in self-test (BIST) that runs during initialization. Should RAM BIST fail, the following steps are taken.

- Device responds only at device address 0x7C and global addresses 0x5A and 0x5B
- A persistent Memory Fault Detected is indicated by STATUS_CML
- Internal EEPROM is not accessed
- RUN*n* and SHARE_CLK are driven low continuously

Normal operation can be restored if the RAM BIST subsequently passes, for instance as the result of another MFR_RESET command issued to address 0x7C.

OPERATION

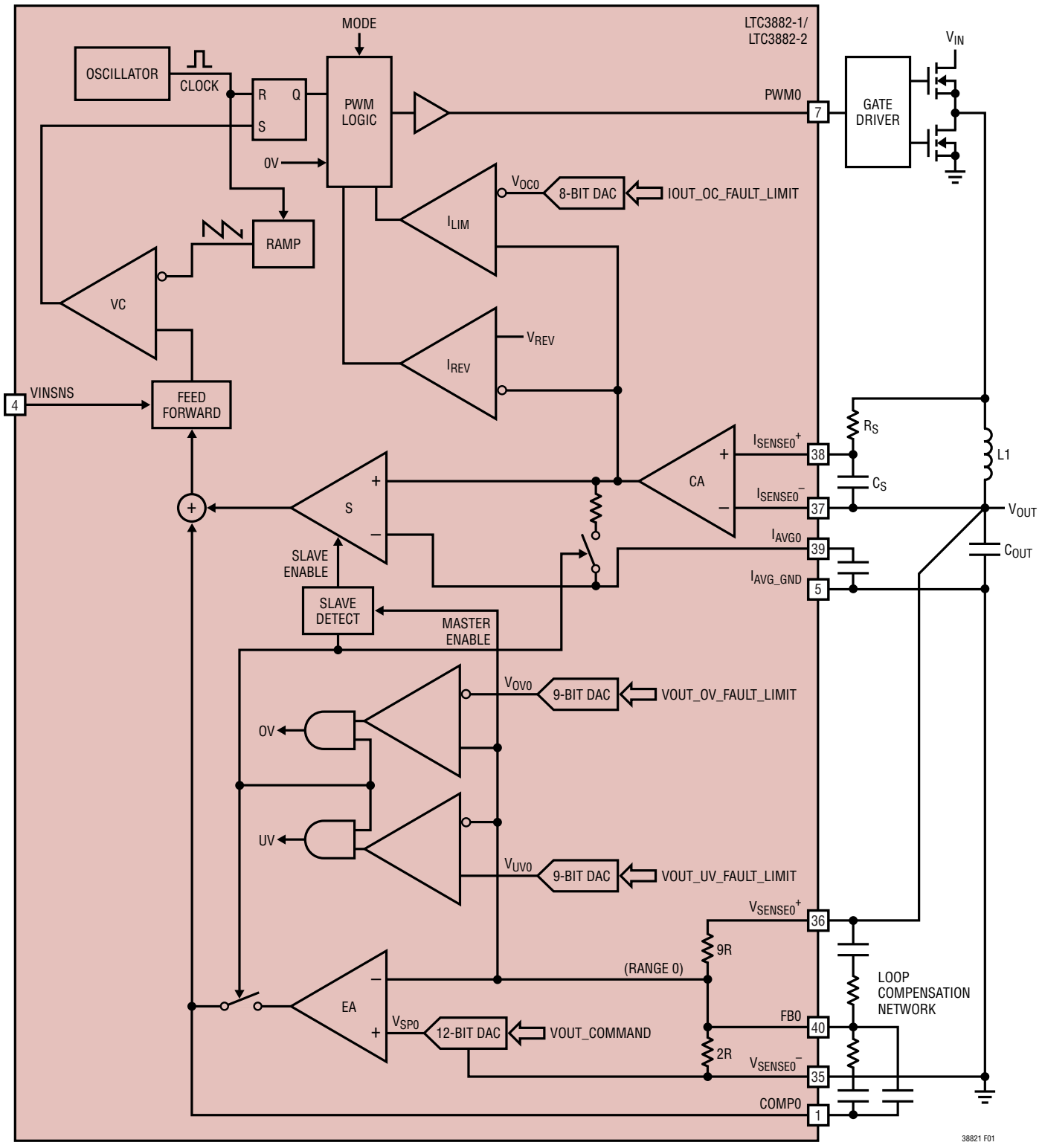


Figure 1. PWM Control Loop Diagram

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During initialization all PWM outputs are disabled. The RUN*n* pins and SHARE_CLK are held low and $\overline{\text{FAULT}}$*n* pins are high impedance. External configuration resistors are identified and the contents of the onboard EEPROM are read into the controller command memory space. The LTC3882-1 can determine key operating parameters from external configuration resistors according to application Table 8 through Table 11. See the following Resistor Configuration Pins section for more detail. The resistor configuration pins only determine some of the preset values of the controller. The remaining values, retrieved from internal EEPROM, are programmed at the factory or with PMBus commands.

If the configuration resistor pins are all open, the LTC3882-1 will use only EEPROM contents to determine all operating parameters. If Ignore Resistor Configuration Pins is set (bit 6 of MFR_CONFIG_ALL_LTC3882-1), the LTC3882-1 will use only its EEPROM contents to determine all operating parameters except device address. Unless both ASEL pins are completely open, the LTC3882-1 will always determine some portion of its device address from the resistors on these pins. See Serial Bus Addressing later in this section.

The internal microcontroller typically requires 35ms to complete initialization from VDD33 ≥ 3V. At that point, an internal comparator monitors VINSNS, which must exceed the VIN_ON threshold before output power sequencing can begin (SHARE_CLK released, ready for TON_DELAY). Accurate readback telemetry can then require an additional 90ms for initial round-robin A/D conversions.

Soft-Start

The RUN pins are released for external control after the part initializes and VINSNS is greater than the VIN_ON threshold. If multiple LTC3882-1 ICs are used in an application, shared RUN pins are held low until all units initialize and VINSNS exceeds the VIN_ON threshold for all devices. A common SHARE_CLK signal can also ensure all connected devices use the same time reference for initial start-up even if RUN pins cannot be shared due to other design requirements. SHARE_CLK is not released by each IC until the conditions for power sequencing have been fully satisfied.

After a channel RUN pin rises above 2V and any specified turn on delay (TON_DELAY) has expired, the LTC3882-1 performs an initial monotonic soft-start ramp on that channel. This is carried out with a digitally controlled ramp of the regulated output voltage from 0V to the commanded voltage set point over the programmed TON_RISE period, allowing inrush current control. During the soft-start ramp, the LTC3882-1 does not initiate PWM operation until the commanded output exceeds the actual rail voltage. This allows the regulator to start up into a pre-biased load even when using gate drivers or power blocks that do not support discontinuous operation. The soft-start feature is disabled by setting the value of TON_RISE to any time less than 0.25ms.

Time-Based Output Sequencing

The LTC3882-1 supports time-based on and off output sequencing using a shared time reference (SHARE_CLK). Following a valid qualified command to turn on, each output is enabled after waiting its programmed TON_DELAY. This can be used to sequence outputs in a prescribed order that can be preprogrammed as needed without hardware modification. Channel off-sequencing is accomplished in a similar way with the TOFF_DELAY command.

Output Ramping Control

The LTC3882-1 supports synchronized output on and off ramping control using a shared time reference (SHARE_CLK). Power rail on and off relationships similar to those of conventional analog tracking functions can be achieved by using programmed delays and TON_RISE and TOFF_FALL times. However, with LTC3882-1 digital control, on and off ramping methods need not be the same, and ramping configurations can be reprogrammed as needed without hardware modification.

Programmable fault responses and fault sharing can ensure that any desired time-based output sequencing and ramping control is properly accomplished each time the system powers up or down. Refer to the Applications Information section for various LTC3882-1 hardware and PMBus command configurations needed to fully support synchronization for time-based sequencing and output ramping when using multiple ICs.

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Voltage-Based Output Sequencing

It is also possible to sequence outputs using cascaded voltage events. To do this, the PGOOD status output from one PWM channel can be used to control the RUN pin of a downstream channel. This keeps the downstream channel off unless acceptable output conditions exist on the controlling channel.

Output Disable

Both PWM channels are disabled any time VINSNS is below the VIN_OFF threshold. The power stages are immediately shut off to stop the transfer of energy to the load(s) as quickly as possible.

A PWM channel may also be disabled in response to certain internal fault conditions, an external fault propagated into a $\overline{\text{FAULT}}$ pin, or loss of SHARE_CLK. In these cases the power stage is immediately shut off to stop the transfer of energy to the load as quickly as possible. Refer to the following Fault Detection and Handling section for additional details related to fault recovery.

Each PWM channel can be disabled with a PMBus OPERATION command at any time if enabled by ON_OFF_CONFIG. This will force a controlled turn-off response with defined delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will maintain the programmed mode of operation for TOFF_FALL. In DCM, the controller will not draw current from the load and fall time will be set by output capacitance and load current.

Finally, each PWM channel can be commanded off by pulling the associated RUN pin low. Pulling the RUN pin low can force the channel to perform a controlled turn off or immediately disable the power stage, depending on the programming of the ON_OFF_CONFIG command.

Minimum Output Disable Times

When a PMBus OPERATION command is used to turn off an LTC3882-1 channel, a minimum output disable time of 120ms is imposed regardless of how quickly the channel is commanded back on. If bit 4 of MFR_CHAN_CONFIG is clear, a PMBus command to turn the channel off also pulses the RUN pin low. Once the RUN pin is pulled low internally or externally, a minimum output disable time (RUN forced low) of TOFF_DELAY + TOFF_FALL + 136ms is enforced. If MFR_RESTART_DELAY is greater than this mandatory minimum, the larger value of MFR_RESTART_DELAY is used. In either case the LTC3882-1 holds its own RUN pin low during the entire disable period. These minimum off times allow a consistent channel restart with coherent monitor ADC values and make the LTC3882-1 highly compatible with other LTC PMBus digital power system management products.

Output Short Cycle

An output short cycle condition is created when a master channel is commanded back on while waiting for TOFF_DELAY or TOFF_FALL to expire. Any time this occurs, the LTC3882-1 asserts the Short Cycle bit in STATUS_MFR_SPECIFIC. Device response at that point is governed by bits in MFR_CHAN_CONFIG_LTC3882-1 and SMBALERT_MASK. Refer to the detailed descriptions of those commands for additional details. Generally, the LTC3882-1 should be controlled so that short cycle conditions are not created during normal operation.

Light Load Current Operation

The LTC3882-1 has two modes of PWM operation: discontinuous conduction mode (DCM) and forced continuous conduction mode (CCM). Mode selection is made with the MFR_PWM_MODE command.

In DCM, the inductor current is not allowed to reverse. The reverse current comparator I_{REV} disables the external bottom MOSFET (synchronous rectifier) when the inductor current reaches approximately 0A, preventing it from going substantially negative. The external gate driver or power block must have short delays to a high impedance output, relative to the PWM cycle, to support DCM.

Efficiency at light loads in CCM is lower than in DCM. Continuous conduction mode exhibits less interference with audio circuitry but may result in reverse inductor current, for instance at light loads or under large transient conditions.

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Switching Frequency and Phase

There is a high degree of flexibility for setting the PWM operating frequency of the LTC3882-1. The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the master clock to other ICs through PMBus command, EEPROM setting, or external configuration resistors as outlined in application Table 10. For PMbus or EEPROM configuration, the LTC3882-1 is designated as a clock master by clearing bit 4 of MFR_CONFIG_ALL_LTC3882-1. As clock master, the LTC3882-1 will drive its open-drain SYNC pin at the selected rate with a pulse width of 125ns. An external pull-up resistor between SYNC and V_{DD33} is required in this case. Only one device connected to SYNC should be designated to drive the pin. If more than one LTC3882-1 sharing SYNC is programmed as clock master, just one of the devices is automatically elected to provide the clock. The others disable their SYNC outputs and indicate this with bit 10 of MFR_PADS_LTC3882-1.

The LTC3882-1 will automatically accept an external SYNC input, disabling is own SYNC drive if necessary, as long as the external clock frequency is greater than 1/2 of the programmed internal oscillator. Whether configured to drive SYNC or not, the LTC3882-1 can continue PWM operation at the selected frequency (FREQUENCY_SWITCH) using its own internal oscillator, if an external clock signal is subsequently lost.

The MFR_PWM_CONFIG_LTC3882-1 command can be used to configure the phase of each channel. Desired phase can also be set from EEPROM or external configuration resistors as outlined in Table 10. Phase designates the relationship between the falling edge of SYNC and the internal clock edge that resets the PWM latch. That reset turns off the top power switch, producing a PWM falling edge. Additional small propagation delays to the PWM control pins will apply.

The phase relationships and frequency are independent of each other, providing numerous application options. Multiple LTC3882-1 ICs can be synchronized to realize a PolyPhase array. In this case the phases should be separated by 360/n degrees, where n is the number of phases driving the output voltage rail.

PolyPhase Load Sharing

Multiple LTC3882-1 ICs can be combined to provide a balanced load-share solution by configuring the necessary pins. The SHARE_CLK and SYNC pins of all load-sharing channels should be bussed together. Connecting the SYNC pins synchronizes the PWM controllers with each other. Bussing the SHARE_CLK pins together allows the phases to start synchronously. Refer to the discussion in the previous Power-Up and Initialization section. The last device to see all start-up conditions satisfied controls the initiation of power sequencing for all phases.

Due to the low output impedance of the LTC3882-1 error amplifiers, PolyPhase applications should use the error amplifier of only one phase as the master. The FB pins of each slave channel must be wired to V_{DD33}, and the COMP pins of each slave phase must be connected to the master error amplifier COMP output. This disables the slave error amplifiers and provides a single point of voltage control and loop stabilization for the PolyPhase output rail.

For PolyPhase load sharing the LTC3882-1 also incorporates an auxiliary current sharing loop. Referring back to Figure 1, the instantaneous current of each slave phase is sensed by current amplifier CA and compared to the I_{AVG} pin. The I_{AVG} and I_{AVG_GND} pins of each phase are wired together, and a small capacitor (50pF to 200pF) between I_{AVG} and I_{AVG_GND} stores a voltage corresponding to the average master phase output current. The difference in this average and the instantaneous phase current is integrated. The output of integrator S of each slave phase is then proportionally summed with the master error amplifier COMP output to adjust the duty cycle and balance the current contribution of that phase. Additional hardware configuration and digital programming requirements apply in PolyPhase systems. Refer to the Applications Information section for complete details on building PolyPhase rails with the LTC3882-1.

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Active Voltage Positioning

Load slope is programmable in the LTC3882-1 via the MFR_VOUT_AVP PMBus command. The inductor current measured at the I_{SENSE} pins is converted to a voltage which is then subtracted from the voltage reference at the positive input of the error amplifier. The final load slope is defined by the inductor current sense element and the bits set in the MFR_VOUT_AVP PMBus command. Setting MFR_VOUT_AVP to a value greater than 0.0% automatically disables output servo mode for that channel.

Input Supply Monitoring

The input supply voltage is sensed by the LTC3882-1 at the VINSNS pin. Undervoltage, overvoltage, valid on and off levels can be programmed for V_{IN}. Refer to the following PMBus Command Details section for more information on programming the input supply thresholds. In addition, the telemetry ADC monitors the VINSNS voltage relative to GND. Conversion results are returned by the READ_VIN PMBus command.

Output Voltage Sensing and Monitoring

Both PWM channels allow remote, differential sensing of the load voltage with V_{SENSE} pins. The channel 1 output sense pin V_{SENSE1}^- is internally shorted to GND (the exposed pad). The telemetry ADC is fully differential and makes its measurements of the output voltages of channels 0 and 1 at $V_{SENSE0}^{\pm}$ and $V_{SENSE1}^{\pm}$, respectively. Conversion results are returned by the READ_VOUT PMBus command.

Output Current Sensing and Monitoring

Both channels allow differential sensing of the inductor current using either the inductor DCR or a resistor in series with the inductor across the I_{SENSE} pins. When the I_{SENSE} pins for a channel are multiplexed to the differential inputs of the LTC3882-1 monitor ADC, they have an input range of approximately ±128mV and a noise floor of $7\mu V_{RMS}$. Peak-peak noise is approximately 46.5µV. The internal ADC anti-aliasing filter and conversion rate produce an average reading of the I_{SENSE} differential voltage. The resulting value is returned by the READ_IOUT PMBus command. Refer to the Applications Information section for details on sensing output current using inductor DCR or discrete resistors.

External and Internal Temperature Sense

External temperature can best be measured using a remote, diode-connected PNP transistor such as the MMBT3906. The emitter should be connected to a TSNS pin while the base and collector terminals of the PNP transistor must be shorted together and returned directly to the LTC3882-1 GND pin. Two different currents are applied to the diode (nominally 2µA and 32µA) and the temperature is calculated from a ΔV_{BE} measurement made with the internal 16-bit monitor ADC.

The LTC3882-1 also supports direct V_{BE} based external temperature measurements. In this case the diode or diode network is trimmed to a specific voltage at a specific current and temperature. In general this method does not yield as accurate a result as the ΔV_{BE} measurement. Refer to MFR_PWM_MODE_LTC3882-1 in the PMBus Command Details section for additional information on programming the LTC3882-1 for these two external temperature sense configurations.

The calculated temperature is returned by the PMBus READ_TEMPERATURE_1 command. Refer to the Applications Information section for details on proper layout of external temperature sense elements and PMBus commands that can be used to improve the accuracy of calculated temperatures.

The READ_TEMPERATURE_2 command returns the internal junction temperature of the LTC3882-1 using an on-chip diode with a ΔV_{BE} measurement and calculation.

Resistor Configuration Pins

Six input pins can be used to configure key operating parameters with selected 1% resistors arranged between V_{DD25} and GND as a divider to the pin(s). The pins are ASEL0, ASEL1, V_{OUT0_CFG}, V_{OUT1_CFG}, FREQ_CFG, and PHAS_CFG. If any of these pins are left open the value stored in the corresponding EEPROM command is used. The resistor configuration pins are only measured during power-up and execution of RESTORE_USER_ALL or MFR_RESET commands. If bit 6 of the MFR_CONFIG_ALL_LTC3882-1

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command is set in EEPROM, all resistor inputs **except** ASEL*n* are ignored. Per the PMBus specification, all pin-programmed parameters can be overridden at any time by commands from the digital interface.

The ASEL*n* pin settings are described in application Table 11. These pins can be used to select the entire LTC3882-1 device address. ASEL0 always programs the bottom four bits of the device address for the LTC3882-1 unless left open. ASEL1 can be used to program the three most-significant bits. Either portion of the address can also be retrieved from the MFR_ADDRESS value in EEPROM. If both pins are left open, the full 7-bit MFR_ADDRESS value stored in EEPROM is used to determine the device address. The LTC3882-1 always responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS should not be set to either of these values.

The V_{OUTn_CFG} pin settings are described in application Table 8. These pins select the output voltages for the related channel.

The following parameters are also set as a percentage of the programmed V_{OUT} if resistor configuration pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT: +10%
- VOUT_OV_WARN_LIMIT: +7.5%
- VOUT_MAX: +7.5%
- VOUT_MARGIN_HIGH: +5%
- VOUT_MARGIN_LOW: –5%
- VOUT_UV_WARN_LIMIT: –6.5%
- VOUT_UV_FAULT_LIMIT: –7%

The FREQ_CFG pin settings are described in application Table 9. This pin selects the switching frequency of the internal oscillator and enables the SYNC output if not left open, shorted to GND or ignored by EEPROM setting.

The PHAS_CFG pin settings are described in Table 10. This pin selects the phase relationships between the two channels and the selected clock source.

Internal EEPROM with CRC and ECC

The LTC3882-1 contains internal EEPROM with Error Correcting Coding (ECC) to store user configuration settings and fault log information. EEPROM endurance and retention for user space and fault log pages are specified in the Absolute Maximum Ratings and Electrical Characteristics table.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the EEPROM CRC Error bit in the STATUS_MFR_SPECIFIC command is set, and the $\overline{\text{ALERT}}$ and RUN pins pulled low (PWM channels off). At that point the device will only respond at special address 0x7C, which is activated only after an invalid CRC has been detected. The chip will also respond at the global addresses 0x5A and 0x5B, but use of these addresses when attempting to recover from a CRC issue is not recommended. All power supply rails associated with either PWM channel of a device reporting an invalid CRC should remain disabled until the issue is resolved.

LTC recommends that the EEPROM not be written when die temperature is greater than 85°C. If internal die temperature exceeds 130°C, all EEPROM operations except RESTORE_USER_ALL and MFR_RESET are disabled. Full EEPROM operation is not re-enabled until die temperature falls below 125°C. Refer to the Applications Information section for equations to predict retention degradation due to elevated operating temperatures.

See the Applications Information section or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming, which the LTC3882-1 also supports.

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Fault Detection

A variety of fault and warning detection, reporting and handling mechanisms are provided by the LTC3882-1. Fault or warning detection capabilities include:

- Input Under/Overvoltage
- Output Under/Overvoltage
- Output Overcurrent (Peak and Average)
- Internal and External Overtemperature and External Undertemperature
- CML Fault (Communication, Memory, or Logic)
- External Fault Detection via Bidirectional $\overline{\text{FAULT}}$ Pins

Reporting is covered in following sections on status commands (registers) and $\overline{\text{ALERT}}$ pin function. Fault handling mechanisms include hardwired, low-level PWM safety responses that always occur, and higher-level programmable event management. Both types are covered in the following sections.

Input Supply Faults

Input undervoltage and overvoltage limits are determined from multiplexed monitor ADC conversions. Therefore the input UV/OV response is naturally deglitched by the 90ms typical conversion cycle of the ADC. There is no hardwired low-level PWM response for any input supply fault.

Hardwired PWM Response to V_{OUT} Faults

V_{OUT} undervoltage (UV) and overvoltage (OV) faults are detected by supervisor comparators. The OV and UV fault limits can be set in three ways:

- As a Percentage of V_{OUT} if Using the Resistor Configuration Pins
- From Stored EEPROM Values
- By PMBus Command

The output overvoltage comparator guards against transient overshoots as well as long term overvoltages at the output. When an output OV fault is detected the top MOSFET for that channel is commanded off and the bottom MOSFET is commanded on until the overvoltage condition is cleared or for PWM control protocol 0, reverse overcurrent is detected. See I_{OUT} faults below.

UV faults and warnings are masked if the channel has been commanded off or until all of the following criteria are achieved.

- TON_DELAY Has Expired
- TON_RISE Ramp Has Completed
- TON_MAX_FAULT_LIMIT Has Been Reached
- IOUT_OC_FAULT_LIMIT Has Not Been Reached
- TOFF_FALL Is Not in Progress

Output UV warnings are determined from multiplexed monitor ADC conversions. The LTC3882-1 has no hardwired PWM response for output UV faults or warnings.

Power Good Indication (Master)

An LTC3882-1 master phase indicates Power Good on its PGOOD pin and in PMBus commands STATUS_WORD (paged) and MFR_PADS_LTC3882-1 based on programmed UV and OV fault limits. Power Good is indicated on a master phase as long as it is enabled to run and V_{OUT} is between the UV and OV fault limits. If a master channel is off for any reason, its PGOOD pin is driven low and Power Not Good is indicated in the status commands.

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Power Good Indication (Slave)

As long as they are enabled, slave phases indicate Power Good on PGOOD and in PMBus status commands, unless a master error amplifier (EA) fault is detected. An EA fault indicates the bussed COMP voltage appears to be too high.

When a slave detects an EA fault, its output is immediately disabled and OV is indicated (see Figure 2). Any valid higher-level OV fault response and propagation may be set for a slave channel to handle a detected EA fault. If the OV fault response is set to ignore, the slave output is re-enabled when the EA/COMP condition clears.

A slave indicates Power Not Good with PMBus status commands during an EA fault, but its PGOOD pin remains high impedance. If a slave phase is off for any other reason, its PGOOD pin is also driven low.

Hardwired PWM Response to I_{OUT} Faults

The LTC3882-1 measures average I_{OUT} from the voltage across the I_{SENSE} pins, taking into account the sense resistor or DCR value and its associated temperature coefficient. Both are provided by PMBus command or EEPROM values.

An output overcurrent (OC) fault condition is detected by a supervisor comparator for each PWM output when the sensed instantaneous current for that channel reaches its maximum allowed value. Refer to the IOUT_OC_FAULT_LIMIT PMBus command for details. When an OC fault is detected the controller immediately disables the top FET, and the bottom FET is normally commanded on for the remainder of that PWM cycle.

If programmed to operate in CCM, the LTC3882-1 also uses the negative of IOUT_OC_FAULT_LIMIT to detect a reverse overcurrent (ROC) fault. When an ROC fault occurs the controller immediately disables both top and bottom FETs, unless PWM output protocol 1 is selected with MFR_PWM_MODE_LTC3882-1.

OC and ROC faults are both handled according to the IOUT_OC_FAULT_RESPONSE for that channel. Either hardware response can result in current-limited operation using pulse truncation or skipping. Because the LTC3882-1 uses leading edge modulation, this will cause a shift in average phase toward 0° on the faulted channel and an increase in input ripple current

Output OC warnings are determined from multiplexed monitor ADC conversions. The LTC3882-1 has no hardwired PWM response if an output OC warning occurs.

Hardwired PWM Response to Temperature Faults

An internal temperature sensor measured by the monitor ADC protects against EEPROM and other IC damage. When die temperature rises above 130°C, the LTC3882-1 will NACK any EEPROM-related command except RESTORE_USER_ALL and MFR_RESET and issue a CML fault for Invalid/Unsupported Command. Normal EEPROM access is re-enabled when die temperature drops below 125°C. Above 160°C, the part shuts down all PWM outputs until die temperature is below 150°C. Internal temperature fault limits cannot be adjusted. Writing to the EEPROM above a die temperature of 85°C is strongly discouraged. Refer to the Absolute Maximum Ratings for other important temperature limitations on internal EEPROM use.

External temperature sensors may also be monitored by the onboard ADC. There is no hardwired PWM response for sensed external temperature faults or warnings.

Hardwired PWM Response to Timing Faults

There is no hardwired PWM response to any timing faults.

TON_MAX_FAULT_LIMIT is the time allowed for V_{OUT} to rise and settle at start-up. The TON_MAX_FAULT_LIMIT timer, which has a resolution of 10µs, is started after TON_DELAY has been reached and a soft-start sequence is started. If the VOUT_UV_FAULT_LIMIT is not reached or an OC remains within the specified time, fault response is determined by the value of TON_MAX_FAULT_RESPONSE.

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An internal watchdog detects if SHARE_CLK remains low for more than 64µs. The part then actively holds SHARE_CLK low for 120ms, ensuring all devices connected to this shared control observe a minimum RETRY_DELAY event.The LTC3882-1 sets the SHARE_CLK_LOW bit in MFR_COMMON to indicate this fault condition.

External Faults

There are no hardware-level responses to any external faults propagated into the IC through the $\overline{\text{FAULT}}n$ pins.

Fault Handling

Higher-level input and output fault event handling (response) can be programmed as described in the following PMBus Command Details section. For most faults, the LTC3882-1 can manage response in one of three ways: ignore, autonomous recovery (hiccup), or latch off. The device takes no additional action beyond previously discussed hardware-level responses when programmed to ignore a fault.

For autonomous recovery a new soft-start is attempted if the fault condition is not present after the MFR_RETRY_DELAY interval has elapsed. MFR_RETRY_DELAY can be set from 120ms to 83 seconds in 1ms increments. If the fault persists, the controller will continue to retry with an interval specified by the MFR_RETRY_DELAY command. This avoids damage to external regulator components caused by repetitive, rapid power cycling.

No retry is attempted for a latch off fault response. In the latch off state the gate drivers for the external MOSFETs are immediately disabled to stop the transfer of energy to the load as quickly as possible. The output remains disabled until the channel is commanded off and then on, or IC supply power is cycled. Commanding a PWM channel off and on may require software and/or hardware intervention depending on its programmed configuration.

The RUN pin must be released by any controlling external application circuits for that channel to restart from the latch off state. As the RUN pin for a given channel rises, associated internal fault indications are cleared automatically. The LTC3882-1 can also be programmed to clear faults for both outputs based solely on the RUN voltage of just one channel. See the MFR_CONFIG_ALL_LTC3882-1 command. The CLEAR_FAULTS PMBus command can also be used to clear all fault bits at any time, independent of PWM channel state.

Handling of some internally generated faults can be digitally deglitched. See Table 12. External faults propagated into the chip using $\overline{\text{FAULT}}n$ pins are not deglitched. Refer to the following section on $\overline{\text{FAULT}}$ functions.

Status Registers and $\overline{\text{ALERT}}$ Masking

Figure 2 summarizes the internal LTC3882-1 status registers accessible by PMBus command. These contain indication of various faults, warnings and other important operating conditions. As shown, the STATUS_BYTE and STATUS_WORD commands also summarize contents of other status registers. Refer to PMBus Command Details for specific information.

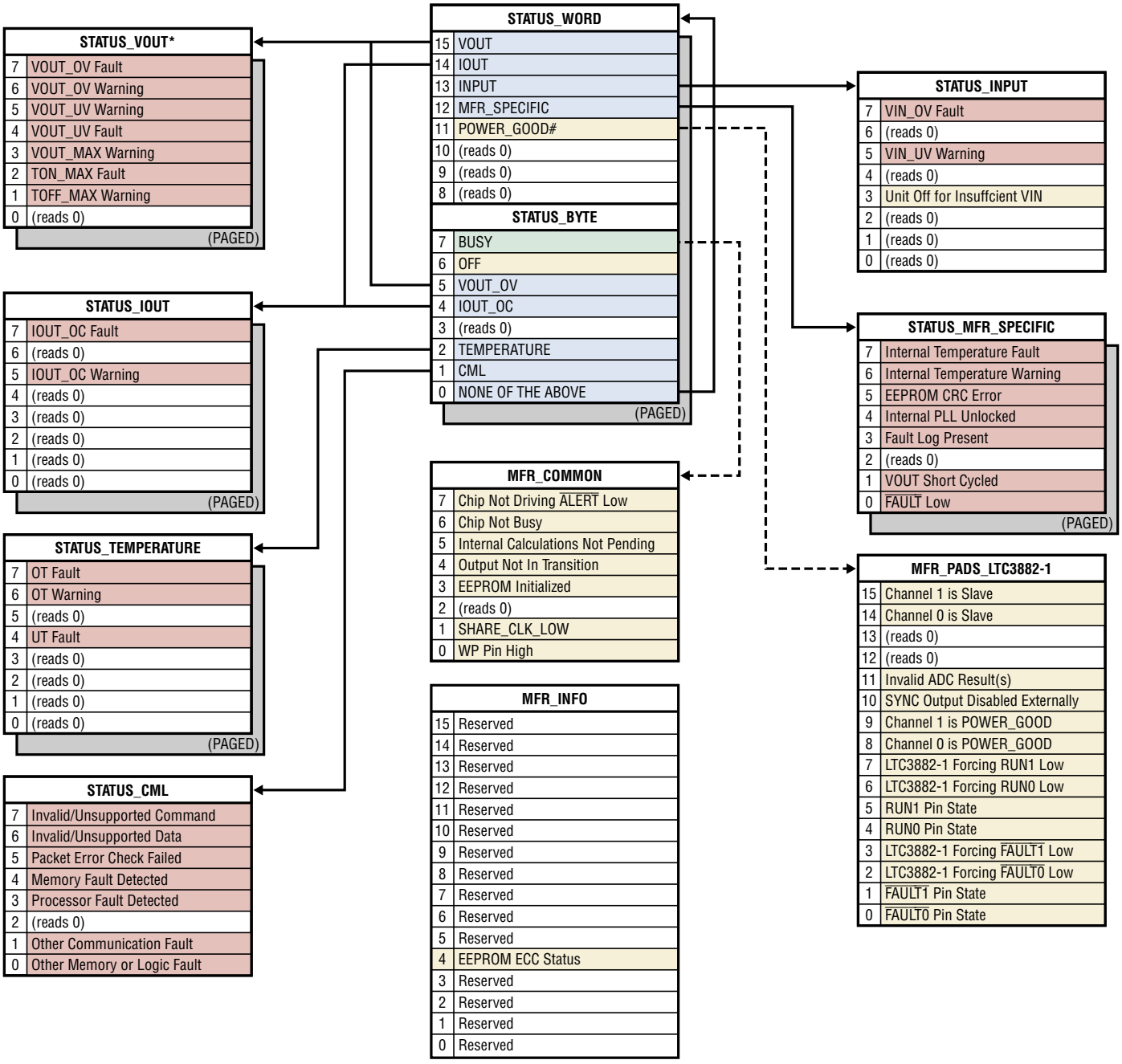
NONE OF THE ABOVE in STATUS_BYTE indicates that one or more of the bits in the most-significant nibble of STATUS_WORD are also set.

In general, any asserted bit in a STATUS_x register also pulls the $\overline{\text{ALERT}}$ pin low. Once set, $\overline{\text{ALERT}}$ will remain low until one of the following occurs.

- A CLEAR_FAULTS, RESTORE_USER_ALL or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- The LTC3882-1 Successfully Transmits Its Address During a PMBus Alert Response Address (ARA)
- IC Supply Power Is Cycled

With some exceptions, the SMBALERT_MASK command can be used to prevent the LTC3882-1 from asserting $\overline{\text{ALERT}}$ for bits in these registers on a bit-by-bit basis. These mask settings are promoted to STATUS_WORD and STATUS_BYTE in the same fashion as the status bits themselves. For example, if $\overline{\text{ALERT}}$ is masked for all bits in Channel 0 STATUS_VOUT, then $\overline{\text{ALERT}}$ is effectively masked for the VOUT bit in STATUS_WORD for PAGE 0.

OPERATION



DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
General Non-Maskable Event	No	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

*IF THE CHANNEL IS CONFIGURED AS A SLAVE AS INDICATED BY MFR_PADS_LTC3882-1[15:14], VOUT_OV FAULT INDICATES A DETECTED MASTER ERROR AMPLIFIER FAULT (COMP VOLTAGE TOO HIGH). NO OTHER BITS IN STATUS_VOUT ARE ACTIVE ON SLAVE CHANNELS

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Figure 2. LTC3882-1/LTC3882-2 Status Register Summary

OPERATION

The BUSY bit in STATUS_BYTE also asserts $\overline{\text{ALERT}}$ low and cannot be masked. This bit can be set as a result of interaction between internal operation and PMBus communication. This fault occurs when a command is received that cannot be safely executed with one or both channels enabled. As discussed in Application Information, BUSY faults can be avoided by polling MFR_COMMON before executing some commands.

Status information contained in MFR_COMMON and MFR_PADS_LTC3882-1 can be used to clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of these registers do not affect the state of the $\overline{\text{ALERT}}$ pin and may not directly influence bits in STATUS_BYTE or STATUS_WORD.

$\overline{\text{FAULT}}$ Pin I/O

The LTC3882-1 can map various fault indicators to their respective $\overline{\text{FAULT}}$ pin using the MFR_FAULT_PROPAGATE_LTC3882-1 command.

Channel-to-channel fault dependencies and communication can be created by connecting $\overline{\text{FAULT}}$ pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{FAULT}}$ pins low. All channels are then configured to shut down when the bussed $\overline{\text{FAULT}}$ pins are pulled low (MFR_FAULT_RESPONSE set to 0xc0). If latch off is the programmed response on the faulted channel, the $\overline{\text{FAULT}}$ pin remains low until one of the following occurs:

- A CLEAR_FAULTS, RESTORE_USER_ALL or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- IC Supply Power Is Cycled

For autonomous group retry, the faulted channel is configured to release the $\overline{\text{FAULT}}$ pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence.

As noted above, $\overline{\text{FAULT}}$ pins may be configured as inputs to detect faults external to the controller that require an immediate response. External faults propagated into the chip using $\overline{\text{FAULT}}$ pins are not deglitched.

Refer to the MFR_FAULT_PROPAGATE command for additional details.

Fault Logging

The LTC3882-1 features a fault log, providing telemetry recording capability. During normal operation log data is continuously updated in internal RAM. When a fault occurs that disables either PWM controller, recording to internal memory is halted, the fault log information is made available from RAM via the MFR_FAULT_LOG command, and the contents of the RAM log are copied into EEPROM. Refer to the Fault Log Operation section for more detail.

EEPROM fault logging is allowed above a die temperature of 85°C, but 10 years of retention is not guaranteed. When die temperature exceeds 130°C EEPROM fault logging is delayed until the temperature drops below 125°C. Faults generating a log should be fully cleared before the log is erased to prevent generation of spurious fault logs. Faults propagated into the IC through $\overline{\text{FAULT}}$*n* pins do not trigger a fault logging event.

When the LTC3882-1 powers up it checks the EEPROM for a valid fault log. If one is found the Valid Fault Log bit in the STATUS_MFR_SPECIFIC PMBus command is set. Additional fault logging will be disabled until the LTC3882-1 receives a CLEAR_FAULTS command. If the Memory Fault Detected bit is also set in STATUS_CML, then the stored fault log is partial. Data in one or more event records may be incomplete or incorrect and MFR_FAULT_LOG_CLEAR should also be commanded after all faults are cleared in order to fully enable additional logging functions.

The MFR_FAULT_LOG command uses a block read protocol with a fixed length of 147 bytes. The LTC3882-1 returns a block byte count of zero if a fault log is not present.

OPERATION

Table 1. LTC3882-1/LTC3882-2 Fault Log Contents

RECORD TYPE	STARTING BYTE	ENDING BYTE	COMMENTS
Header Information	0	26	See Table 2.
Fault Event Record	27	46	Fault may have occurred anywhere during this event record. See byte 4 of Table 2 and all of Table 3 and Table 4.
Event Record N-1	47	66	Last complete cyclical data read before the fault was detected.
Event Record N-2	67	86	Older data record.
Event Record N-3	87	106	
Event Record N-4	107	126	
Event Record N-5	127	146	Oldest recorded data.

Contents of a fault log are shown in Table 1 through Table 4. Refer to Table 6 for an explanation of data formats. Each event record represents one complete conversion cycle through all multiplexed monitor ADC inputs and related status. The six most recent event records are maintained in internal memory in reverse chronological order unless the part is reset. Then the four most recent events are maintained in EEPROM. When a fault log is created the present ADC input cycle is completed and the ADC input being converted at the time of the fault is noted in the log header record.

Table 2. Fault Log Header Information

RECORD	BITS	FORMAT	BLOCK BYTE COUNT	DETAILS
Fault Log Preface	[7:0]	ASC	0	Returns LTxx beginning at byte 0 if a partial or complete fault log exists. Word xx is a factory identifier that may vary part to part.
	[7:0]		1	
	[15:8]	Reg	2	
	[7:0]		3	
Fault Source	[7:0]	Reg	4	Refer to Table 3.
MFR_REAL_TIME	[7:0]	Reg	5	48 bit share-clock counter value when fault occurred (200µs resolution).
	[15:8]		6	
	[23:16]		7	
	[31:24]		8	
	[39:32]		9	
	[47:40]		10	
MFR_VOUT_PEAK (PAGE 0)	[15:8]	L16	11	Peak READ_VOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		12	
MFR_VOUT_PEAK (PAGE 1)	[15:8]	L16	13	Peak READ_VOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		14	
MFR_IOUT_PEAK (PAGE 0)	[15:8]	L11	15	Peak READ_IOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		16	
MFR_IOUT_PEAK (PAGE 1)	[15:8]	L11	17	Peak READ_IOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		18	
MFR_VIN_PEAK	[15:8]	L11	19	Peak READ_VIN since last power-on or CLEAR_PEAKS command.
	[7:0]		20	
READ_TEMPERATURE1 (PAGE 0)	[15:8]	L11	21	External temperature sensor 0 during last event.
	[7:0]		22	
READ_TEMPERATURE1 (PAGE 1)	[15:8]	L11	23	External temperature sensor 1 during last event.
	[7:0]		24	
READ_TEMPERATURE2	[15:8]	L11	25	Internal temperature sensor during last event.
	[7:0]		26	

OPERATION

Table 3. Fault Source Values

FAULT SOURCE VALUE	CAUSE OF FAULT LOG	CHANNEL
0x00	TON_MAX	0
0x01	VOUT_OV	
0x02	VOUT_UV	
0x03	IOUT_OC	
0x05	Over temperature	
0x06	Under temperature	
0x07	VIN_OV	
0x0A	Internal temperature	
0x10	TON_MAX	1
0x11	VOUT_OV	
0x12	VOUT_UV	
0x13	IOUT_OC	
0x15	Over temperature	
0x16	Under temperature	
0x17	VIN_OV	
0x1A	Internal temperature	
0xFF	MFR_FAULT_LOG_STORE	

Table 4. Fault Log Event Record

DATA	BITS	FORMAT	RECORD BYTE INDEX
READ_VOUT (PAGE 0)	[15:8]	L16	0
	[7:0]		1
READ_VOUT (PAGE 1)	[15:8]	L16	2
	[7:0]		3
READ_IOUT (PAGE 0)	[15:8]	L11	4
	[7:0]		5
READ_IOUT (PAGE 1)	[15:8]	L11	6
	[7:0]		7
READ_VIN	[15:8]	L11	8
	[7:0]		9
(Not used)	[15:8]	L11	10
	[7:0]		11
STATUS_VOUT (PAGE 0)	[7:0]	Reg	12
STATUS_VOUT (PAGE 1)	[7:0]	Reg	13
STATUS_WORD (PAGE 0)	[15:8]	Reg	14
	[7:0]		15
STATUS_WORD (PAGE 1)	[15:8]	Reg	16
	[7:0]		17
STATUS_MFR_SPECIFIC (PAGE 0)	[7:0]	Reg	18
STATUS_MFR_SPECIFIC (PAGE 1)	[7:0]	Reg	19

OPERATION

Factory Default Operation

The LTC3882-1 ships from the factory with a default configuration stored in its non-volatile memory, unless custom programming has been requested. These command values are loaded into volatile RAM when the chip is initialized. Prior to receiving any PMBus commands, a stock LTC3882-1 will operate in the factory default mode. If a STORE_USER_ALL command is executed, the contents of the non-volatile memory are replaced with active command values from internal RAM, and that will permanently overwrite the factory defaults. Table 5 summarizes the default factory operation settings of the LTC3882-1 if all resistor configuration pins are left open. These defaults allow parameters listed in bold text in the table to be overridden with configuration resistor programming. Warning limits are given in Table 5 because exceeding them will cause the $\overline{\text{ALERT}}$ pin to be asserted even if the PMBus interface is not being utilized.

Table 5. Factory Default Operation Summary

PARAMETER*	DEFAULT SETTING	UNITS
PMBus Address	All writes enabled to Channel 0 at address 0x4F (no PEC).	–
Operation	OPERATION enabled with RUN pin control and soft-off.	–
Input Voltage OFF Threshold	6.0	V
Input Voltage UV Warning Limit	6.3	V
Input Voltage ON Threshold	6.5	V
Input Voltage OV Fault Limit	15.5	V
Input Voltage OV Fault Response	Latch off.	–
Soft-Start Time	8 (with no delay).	ms
Maximum Start-Up Time (TMAX)	10	ms
TMAX Fault Response	Retry every 350ms.	–
Output Voltage UV Fault/Warning Limits	0.900/0.925	V
Output Voltage UV Fault Response	Retry every 350ms.	–
Output Voltage	1.000	V
Active Voltage Positioning	Disabled.	–
Output Voltage OV Warning/Fault Limits	1.075/1.100	V
Output Voltage OV Fault Response	Retry every 350ms.	–
Shut Down	8ms soft-off.	–
Output Current Sense Element	0.63mΩ with 3930ppm/°C TC.	–
Output Current OC Warning/Fault Limits	20/29.75	A
Output Current OC Fault Response	Ignore	–
PWM Switching Mode	Continuous inductor current only.	–
PWM Control Protocol	Three-State PWM.	–
PWM Switching Frequency	500	kHz
Channel 0/1 Phase	0/180	Degrees
Internal Overtemperature Warning/Fault Limits	130/160	°C
Internal Overtemperature Responses	Warning: EEPROM disabled; Fault: PWM disabled.	–
External Undertemperature Fault Limit	–40	°C
External Undertemperature Fault Response	Retry every 350ms.	–
External Overtemperature Warning/Fault Limits	85/100	°C
External Overtemperature Fault Response	Retry every 350ms.	–
FAULT	Asserts low for the following faults: V_{OUT} UV or OV, V_{IN} OV, external or internal OT, external UT, TON_MAX, or output short cycle.	–
$\overline{\text{ALERT}}$ Masking	ALERTs are masked for loss of PLL lock and external $\overline{\text{FAULT}}$ inputs.	–

*bold entries can be changed with external configuration resistors

OPERATION

Serial Interface

The LTC3882-1 has a PMBus compliant serial interface that can operate at any frequency between 10kHz and 400kHz. The LTC3882-1 is a bus slave device that communicates bidirectionally with a host (master) using standard PMBus protocols. The Timing Diagram found earlier in this document, along with related Electrical Characteristics table entries, define the timing relationships of the SDA and SCL bus signals. SDA and SCL must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

PMBus, an incremental extension of the SMBus standard, offers more robust operation than a 2-wire I^2C interface. In addition to adding a protocol layer to improve interoperability and facilitate reuse, PMBus supports bus timeout recovery for system reliability, optional packet error checking to ensure data integrity, and peripheral hardware alerts for system fault management. In general, a programmable device capable of functioning as an I^2C bus master can be configured for PMBus management with little or no change to hardware. However, not all I^2C controllers support repeat start (restart) required for PMBus reads.

For a description of the minor extensions and exceptions PMBus makes to the SMBus standard, refer to PMBus Specification Part I Revision 1.2 Paragraph 5 on Transport.

For a description of the differences between SMBus and I^2C, refer to System Management Bus (SMBus) Specification Version 2.0 Appendix B on Differences Between SMBus and I^2C.

The user is encouraged to reference Part I of the latest PMBus Power System Management Protocol Specification to understand how to interface the LTC3882-1 to a PMBus system. This specification can be found at http://www.pmbus.org/specs.html.

The LTC3882-1 uses the following standard serial interface protocols defined in the SMBus and PMBus specifications:

- Quick Command
- Send Byte
- Write Byte
- Write Word
- Read Byte
- Read Word
- Block Read
- Block Write – Block Read Process Call
- Alert Response Address

The LTC3882-1 does not require PEC for Quick Command under any circumstances. The LTC3882-1 also supports group command protocol (GCP) as required by PMBus specification Part I, section 5.2.3. GCP is used to send commands to more than one PMBus device in one continuous transmission. It should not be used with commands that require the receiving device to respond with data, such as a STATUS_BYTE command. Refer to Part I of the PMBus specification for additional details on using GCP.

All LTC3882-1 message transmission types allow for packet error checking. The later section on Serial Communication Errors provides more detail on packet error checking.

Figure 4 to Figure 20 illustrate these protocols. Figure 3 provides a key to the protocol diagrams. Not all protocol elements will be present in every data packet. For instance, not all packets are required to include the packet error code. A number shown above a field in these diagrams indicates the number of bits in that field. All data transfers are initiated by the present bus master regardless of how many times data direction flow may change during the subsequent transmission. The LTC3882-1 never functions as a bus master.

This device includes handshaking features to ensure robust system communication. Please refer to the PMBus Communication and Command Processing section in Applications Information for more details.

Serial Bus Addressing

The LTC3882-1 supports four types of serial bus addressing:

- Global Bus Addressing
- Power Rail Addressing
- Individual Device Addressing
- Page+ Channel Addressing

OPERATION

Global addressing provides a means for the bus master to communicate with all LTC3882-1 devices on the bus simultaneously. The LTC3882-1 global addresses of 0x5A and 0x5B cannot be changed or disabled. Commands sent to address 0x5A are applied to both channels, as if the PAGE command were set to 0xFF. Global address 0x5B is paged, allowing channel-specific control of all LTC3882-1 devices on the bus. Other LTC device types may respond at one or both of these global addresses. Reading from global addresses is strongly discouraged.

Rail addressing provides a means for the bus master to simultaneously communicate with all channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Rail addresses should be unique for each single-phase or PolyPhase rail. Different voltage rails should not attempt to share a rail address. Reading from rail addresses is also strongly discouraged.

Device addressing is the most common means used by a bus master to communicate with an LTC3882-1. The value of the device address is set by the combination of ASEL pin programming and the MFR_ADDRESS command. Refer to the previous section on Resistor Configuration Pins for details.

Individual channel addressing allows the bus master to communicate directly with a specific LTC3882-1 PWM channel without first using a PAGE command. Refer to the PAGE_PLUS commands for additional details.

Use of any of the four types of addressing requires careful planning to avoid address-related bus conflicts. Communication to LTC3882-1 devices at global and rail addresses should be limited to command write operations.

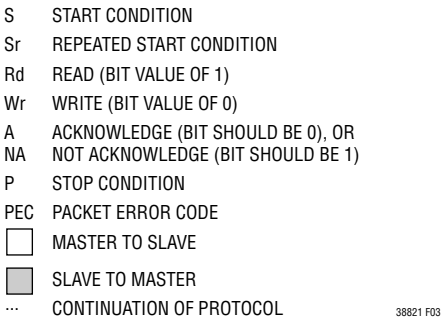


Figure 3. PMBus Packet Protocol Diagram Element Key



Figure 4. Quick Command Protocol

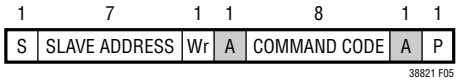


Figure 5. Send Byte Protocol

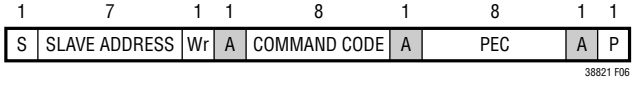


Figure 6. Send Byte Protocol with PEC

OPERATION

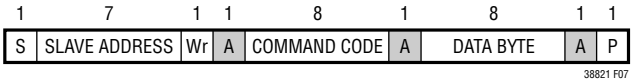


Figure 7. Write Byte Protocol

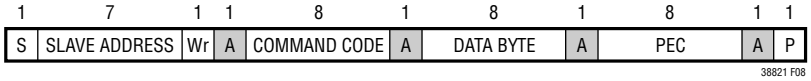


Figure 8. Write Byte Protocol with PEC

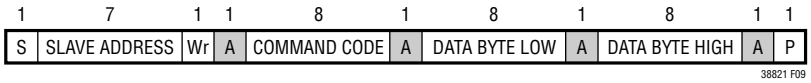


Figure 9. Write Word Protocol

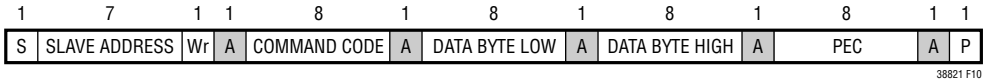


Figure 10. Write Word Protocol with PEC

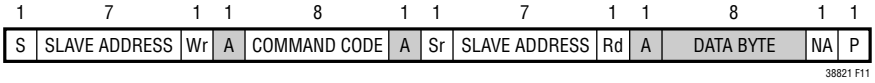


Figure 11. Read Byte Protocol

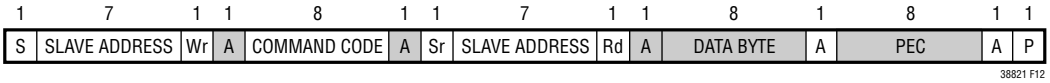


Figure 12. Read Byte Protocol with PEC

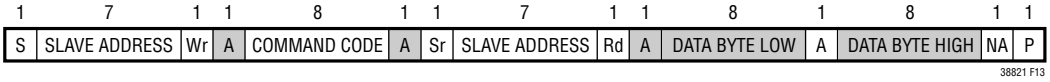


Figure 13. Read Word Protocol

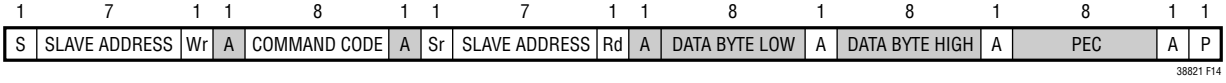


Figure 14. Read Word Protocol with PEC

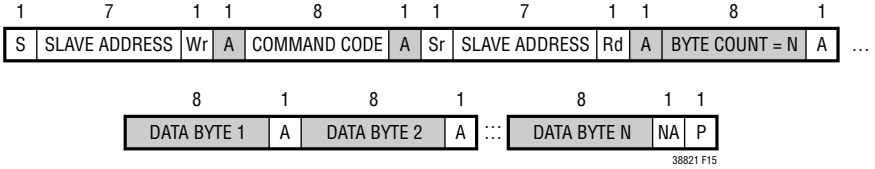


Figure 15. Block Read Protocol

OPERATION

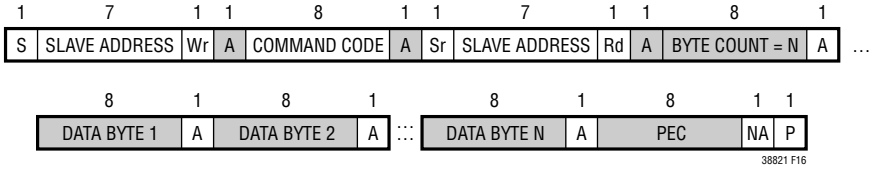


Figure 16. Block Read Protocol with PEC

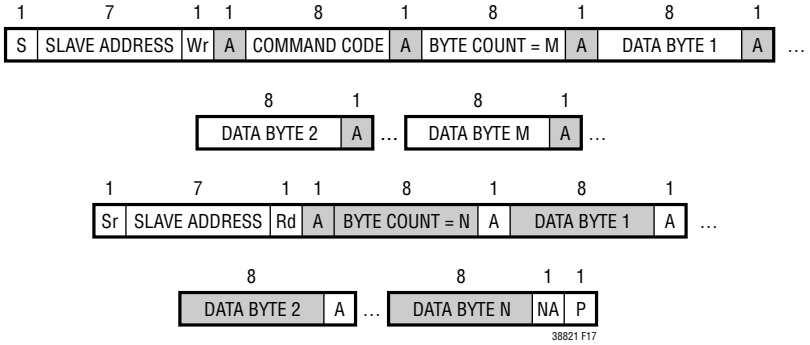


Figure 17. Block Write – Block Read Process Call

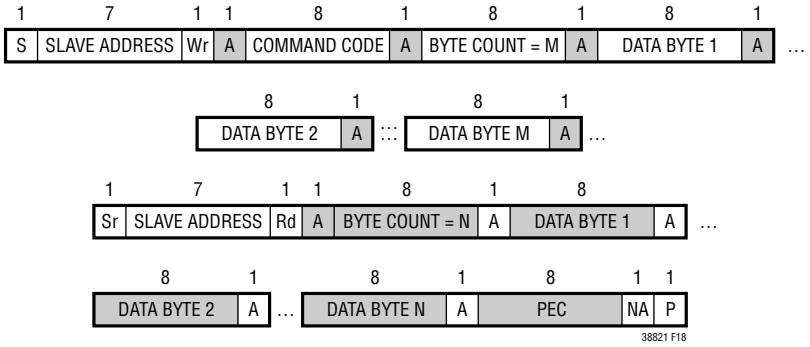


Figure 18. Block Write – Block Read Process Call with PEC

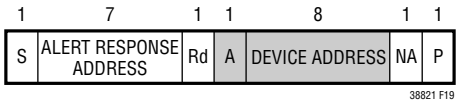


Figure 19. Alert Response Address Protocol

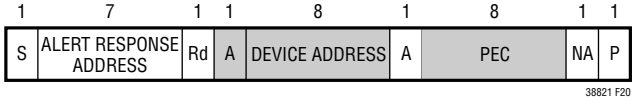


Figure 20. Alert Response Address Protocol with PEC

OPERATION

Serial Bus Timeout

The LTC3882-1 implements a timeout feature to avoid hanging the serial interface. The data packet timer begins running at the first START event before the SLAVE ADDRESS write byte and ends with the STOP bit. Packet transmission must be completed before the timer expires, or the LTC3882-1 will tri-state the bus and ignore all message data. The data packet includes the SLAVE ADDRESS byte, COMMAND CODE byte, repeated START and SLAVE ADDRESS byte (if a read operation), all ACKNOWLEDGE and flow control bits (R/$\overline{W}$) and all data bytes.

The packet timer is typically set to 30ms. If bit 3 of MFR_CONFIG_ALL_LTC3882-1 is set, this period is extended to 255ms. The LTC3882-1 automatically allows a packet transmission time of 255ms for MFR_FAULT_LOG block reads regardless of the setting of this bit. In no circumstances will the timeout period be less than the $t_{TIMEOUT}$ specification (25ms minimum).

The LTC3882-1 supports the full PMBus frequency range of 10kHz to 400kHz.

Serial Communication Errors

The LTC3882-1 supports the optional PMBus packet error checking protocol. This protocol appends a packet error code (PEC) to the end of applicable message transfers to improve communication reliability. The PEC is a CRC-8 error-checking byte calculated by the bus device sending the last data byte. Refer to SMBus specification 1.2 or higher for additional implementation details. All LTC3882-1 read operations will return a valid PEC if the bus master requests it. If bit 2 in the MFR_CONFIG_ALL_LTC3882-1 command is set, the IC will not act in response to a bus write operation unless a valid PEC is also received from the host.

PEC errors on command writes, attempts to access unsupported commands, or writing invalid data to supported commands all cause the LTC3882-1 to generate a CML fault. The CML bit is then set in the STATUS_BYTE and STATUS_WORD commands, and the appropriate bit is set in the STATUS_CML command.

PMBus COMMAND SUMMARY

PMBus Commands

Table 7 lists supported PMBus commands and manufacturer specific commands. Additional information about these commands can be found in Revision 1.2 of Part II of the PMBus Power System Management Protocol Specification that can be found at http://www.pmbus.org/specs.html. Users are encouraged to reference that manual. Exceptions or manufacturer-specific implementations are detailed in the tables below. All standard PMBus commands from 0x00 through 0xCF not listed in this table are implicitly not supported by the LTC3882-1. All commands from 0xD0 through 0xFF not listed in this table are implicitly reserved by the manufacturer. The LTC3882-1 may execute additional commands not listed in this table, and these can change without notice. Reading these unlisted commands is harmless to the operation of the IC. Writes to any unsupported or reserved command should be avoided, as they may result in a CML fault and/or undesired operation of the part.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these cases the LTC3882-1 follows the protocols defined in the PMBus Specification V1.2, Part II, Section 10.8.7, to communicate that it is busy. This device includes handshaking features to eliminate busy responses, simplify error handling software and ensure robust communication and system behavior. Please refer to PMBus Communication and Command Processing in the Applications Information section for further details.

LTC has made an effort to establish PMBus command compatibility and functional uniformity among its family of parts. However, differences may occur due to specific product requirements. Compatibility of PMBus commands among any ICs should not be assumed based simply on command name. Always refer to the manufacturer's data sheet of each device for a complete definition of a command function.

Data Formats

PMBus supports specific floating point number formats and allows for a wide range of other data formats.

Table 6 describes the data formats used by the LTC3882-1. Abbreviations of these formats appear throughout this document.

Table 6. Abbreviations of Supported Data Formats

	PMBus				
	TERMINOLOGY	SPECIFICATION REFERENCE	LTC TERMINOLOGY	DEFINITION	EXAMPLE
L11	Linear	Part II ¶7.1	Linear_5s_11s	Floating point 16-bit data: value = Y • 2^N, where N = b[15:11] and Y = b[10:0], both two's compliment binary integers.	b[15:0] = 0x9807 = 10011_000_0000_0111 value = 7 • 2^{-13} = 854E-6
L16	Linear VOUT_MODE	Part II ¶8.2	Linear_16u	Floating point 16-bit data: value = Y • 2^{-12}, where Y = b[15:0], an unsigned integer.	b[15:0] = 0x4C00 = 0100_1100_0000_0000 value = 19456 • 2^{-12} = 4.75
CF	DIRECT	Part II ¶7.2	varies	16-bit data with a custom format defined in the detailed PMBus command description.	Often an unsigned or two's compliment integer.
Reg	register bits	Part II ¶10.3	Reg	Per-bit meaning defined in detailed PMBus command description.	PMBus STATUS_BYTE command.
ASC	text characters	Part II ¶22.2.1	ASCII	ISO/IEC 8859-1 [A05]	LTC (0x4C5443)

PMBus COMMAND SUMMARY

Table 7. PMBus Command Summary

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	SEE PAGE
PAGE	0x00	Channel (page) presently selected for any paged command.	R/W Byte	N	Reg			0x00	72
OPERATION	0x01	On, off and margin control.	R/W Byte	Y	Reg		●	0x80	76
ON_OFF_CONFIG	0x02	RUN pin and PMBus on/off command configuration.	R/W Byte	Y	Reg		●	0x1E	75
CLEAR_FAULTS	0x03	Clear all set fault bits.	Send Byte	N					93
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N					72
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W Process	N					73
WRITE_PROTECT	0x10	Protect the device against unintended PMBus modifications.	R/W Byte	N	Reg		●	0x00	73
STORE_USER_ALL	0x15	Store entire operating memory in EEPROM.	Send Byte	N					105
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N					105
CAPABILITY	0x19	Summary of supported optional PMBus features.	R Byte	N	Reg			0xB0	74
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ activity	Block R/W	Y	Reg		●	see CMD details	101
VOUT_MODE	0x20	Voltage-related format (Linear) and exponent.	R Byte	Y	Reg			0x14 2^{-12}	82
VOUT_COMMAND	0x21	Nominal V_{OUT} value.	R/W Word	Y	L16	V	●	1.0V 0x1000	82
VOUT_MAX	0x24	Maximum V_{OUT} that can be set by any command, including margin.	R/W Word	Y	L16	V	●	2.75V 0x2C00	83
VOUT_MARGIN_HIGH	0x25	V_{OUT} at high margin, *must be greater than VOUT_COMMAND.*	R/W Word	Y	L16	V	●	1.05V 0x10CD	83
VOUT_MARGIN_LOW	0x26	V_{OUT} at low margin, *must be less than VOUT_COMMAND.*	R/W Word	Y	L16	V	●	0.95V 0x0F33	83
VOUT_TRANSITION_RATE	0x27	V_{OUT} slew rate for programmed output changes.	R/W Word	Y	L11	V/ms	●	0.25 0xAA00	87
FREQUENCY_SWITCH	0x33	PWM frequency control.	R/W Word	N	L11	kHz	●	500kHz 0xFBE8	77
VIN_ON	0x35	Minimum input voltage to begin power conversion.	R/W Word	N	L11	V	●	6.5V 0xCB40	81
VIN_OFF	0x36	Decreasing input voltage at which power conversion stops.	R/W Word	N	L11	V	●	6.0V 0xCB00	81
IOUT_CAL_GAIN	0x38	Ratio of $I_{SENSE}^{\pm}$ voltage to sensed current.	R/W Word	Y	L11	mΩ	●	0.63mΩ 0xB285	85
VOUT_OV_FAULT_LIMIT	0x40	V_{OUT} overvoltage fault limit.	R/W Word	Y	L16	V	●	1.1V 0x119A	83
VOUT_OV_FAULT_RESPONSE	0x41	V_{OUT} overvoltage fault response.	R/W Byte	Y	Reg		●	0xB8	98
VOUT_OV_WARN_LIMIT	0x42	V_{OUT} overvoltage warning limit.	R/W Word	Y	L16	V	●	1.075V 0x1133	84
VOUT_UV_WARN_LIMIT	0x43	V_{OUT} undervoltage warning limit.	R/W Word	Y	L16	V	●	0.925V 0x0ECD	84

PMBus COMMAND SUMMARY

Table 7. PMBus Command Summary

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	SEE PAGE
VOUT_UV_FAULT_LIMIT	0x44	V_{OUT} undervoltage fault limit.	R/W Word	Y	L16	V	●	0.9V 0x0E66	84
VOUT_UV_FAULT_RESPONSE	0x45	V_{OUT} undervoltage fault response.	R/W Byte	Y	Reg		●	0xB8	98
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	●	29.75A 0xDBB8	85
IOUT_OC_FAULT_RESPONSE	0x47	Output overcurrent fault response.	R/W Byte	Y	Reg		●	0x00	99
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	●	20.0A 0xDA80	85
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	°C	●	100.0°C 0xEB20	88
OT_FAULT_RESPONSE	0x50	External overtemperature fault response.	R/W Byte	Y	Reg		●	0xB8	100
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	°C	●	85.0°C 0xEAA8	88
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	°C	●	–40.0°C 0xE580	89
UT_FAULT_RESPONSE	0x54	External undertemperature fault response.	R/W Byte	Y	Reg		●	0xB8	100
VIN_OV_FAULT_LIMIT	0x55	V_{IN} overvoltage fault limit.	R/W Word	N	L11	V	●	15.5V 0xD3E0	81
VIN_OV_FAULT_RESPONSE	0x56	V_{IN} overvoltage fault response.	R/W Byte	Y	Reg		●	0x80	97
VIN_UV_WARN_LIMIT	0x58	V_{IN} undervoltage warning limit.	R/W Word	N	L11	V	●	6.3V 0xCB26	81
TON_DELAY	0x60	Delay from RUN pin or OPERATION ON command to TON_RISE ramp start.	R/W Word	Y	L11	ms	●	0.0ms 0x8000	86
TON_RISE	0x61	Time for V_{OUT} to rise from 0.0V to VOUT_COMMAND after TON_DELAY.	R/W Word	Y	L11	ms	●	8.0ms 0xD200	86
TON_MAX_FAULT_LIMIT	0x62	Maximum time for V_{OUT} to rise above VOUT_UV_FAULT_LIMIT after TON_DELAY.	R/W Word	Y	L11	ms	●	10.0ms 0xD280	87
TON_MAX_FAULT_RESPONSE	0x63	Fault response when TON_MAX_FAULT_ LIMIT is exceeded.	R/W Byte	Y	Reg		●	0xB8	101
TOFF_DELAY	0x64	Delay from RUN pin or OPERATION OFF command to TOFF_FALL ramp start.	R/W Word	Y	L11	ms	●	0.0ms 0x8000	87
TOFF_FALL	0x65	Time for V_{OUT} to fall to 0.0V from VOUT_COMMAND after TOFF_DELAY.	R/W Word	Y	L11	ms	●	8.0ms 0xD200	87
TOFF_MAX_WARN_ LIMIT	0x66	Maximum time for V_{OUT} to decay below 12.5% of VOUT_COMMAND after TOFF_FALL completes.	R/W Word	Y	L11	ms	●	150ms 0xF258	87
STATUS_BYTE	0x78	One-byte channel status summary.	R/W Byte	Y	Reg				89
STATUS_WORD	0x79	Two-byte channel status summary.	R/W Word	Y	Reg				90
STATUS_VOUT	0x7A	V_{OUT} fault and warning status.	R/W Byte	Y	Reg				90
STATUS_IOUT	0x7B	I_{OUT} fault and warning status.	R/W Byte	Y	Reg				90
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg				91
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status.	R/W Byte	Y	Reg				91

PMBus COMMAND SUMMARY

Table 7. PMBus Command Summary

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	SEE PAGE
STATUS_CML	0x7E	Communication, memory and logic fault and warning status.	R/W Byte	N	Reg				91
STATUS_MFR_ SPECIFIC	0x80	LTC3882-1-specific status.	R/W Byte	Y	Reg				92
READ_VIN	0x88	Measured V_{IN}.	R Word	N	L11	V			94
READ_VOUT	0x8B	Measured V_{OUT}.	R Word	Y	L16	V			94
READ_IOUT	0x8C	Measured I_{OUT}.	R Word	Y	L11	A			95
READ_TEMPERATURE_1	0x8D	Measured external temperature.	R Word	Y	L11	°C			95
READ_TEMPERATURE_2	0x8E	Measured internal temperature.	R Word	N	L11	°C			95
READ_DUTY_CYCLE	0x94	Measured commanded PWM duty cycle.	R Word	Y	L11	%			96
READ_FREQUENCY	0x95	Measured PWM input clock frequency.	R Word	Y	L11	kHz			96
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W			95
PMBUS_REVISION	0x98	Supported PMBus version.	R Byte	N	Reg			0x22 V1.2	74
MFR_ID	0x99	Manufacturer identification.	R String	N	ASC			LTC	106
MFR_MODEL	0x9A	LTC model number.	R String	N	ASC			LTC3882-1 LTC3882-2	106
MFR_SERIAL	0x9E	Device serial number.	R Block	N	ASC				106
IC_DEV_ID (LTC3882-2 only)	0xAD	LTC3882-2 model number	R String	N	ASC			LTC3882-2	106
IC_DEVICE_REV (LTC3882-2 only)	0xAE	LTC3882-2 device revision code	R String	N	ASC			A4802	106
LTC3882-1/LTC3882-2 Custom Commands									
MFR_VOUT_MAX	0xA5	Maximum value of any V_{OUT} related command.	R Word	Y	L16	V		5.6V 0x599A	82
USER_DATA_00	0xB0	EEPROM word reserved for LTpowerPlay.	R/W Word	N	Reg		●		106
USER_DATA_01	0xB1	EEPROM word reserved for LTpowerPlay.	R/W Word	Y	Reg		●		106
USER_DATA_02	0xB2	EEPROM word reserved for OEM use.	R/W Word	N	Reg		●		106
USER_DATA_03	0xB3	EEPROM word available for general data storage.	R/W Word	Y	Reg		●	0x0000	106
USER_DATA_04	0xB4	EEPROM word available for general data storage.	R/W Word	N	Reg		●	0x0000	106
MFR_INFO	0xB6	Manufacturing Specific Information	R Word	N	Reg			NA	93
MFR_EE_UNLOCK	0xBD	(contact the factory)							106
MFR_EE_ERASE	0xBE	(contact the factory)							106
MFR_EE_DATA	0xBF	(contact the factory)							106
MFR_CHAN_CONFIG_LTC3882-1	0xD0	LTC3882-1 channel-specific configuration.	R/W Byte	Y	Reg		●	0x1D	79
MFR_CONFIG_ALL_LTC3882-1	0xD1	LTC3882-1 device-level configuration.	R/W Byte	N	Reg		●	0x21	75
MFR_FAULT_PROPAGATE_ LTC3882-1	0xD2	Configure LTC3882-1 status propagation via $\overline{FAULT}n$ pins.	R/W Word	Y	Reg		●	0x6993	102
MFR_VOUT_AVP	0xD3	Specify V_{OUT} load line.	R/W Word	Y	L11	%	●	0% 0x8000	83
MFR_PWM_MODE_LTC3882-1	0xD4	LTC3882-1 channel-specific PWM mode control.	R/W Byte	Y	Reg		●	0xC8	80

PMBus COMMAND SUMMARY

Table 7. PMBus Command Summary

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	SEE PAGE
MFR_FAULT_RESPONSE	0xD5	PWM response when $\overline{FAULT}n$ pin is low.	R/W Byte	Y	Reg		●	0xC0	103
MFR_OT_FAULT_RESPONSE	0xD6	Internal overtemperature fault response.	R Byte	N	Reg			0xC0	100
MFR_IOUT_PEAK	0xD7	Maximum I_{OUT} measurement since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A			95
MFR_RETRY_DELAY	0xDB	Minimum time before retry after a fault.	R/W Word	Y	L11	ms	●	350ms 0xFABC	101
MFR_RESTART_DELAY	0xDC	Minimum time RUN pin is held low by the LTC3882-1.	R/W Word	Y	L11	ms	●	500ms 0xFBE8	86
MFR_VOUT_PEAK	0xDD	Maximum V_{OUT} measurement since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V			94
MFR_VIN_PEAK	0xDE	Maximum V_{IN} measurement since last MFR_CLEAR_PEAKS.	R Word	N	L11	V			94
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum external temperature measurement since last MFR_CLEAR_PEAKS.	R Word	Y	L11	°C			95
MFR_CLEAR_PEAKS	0xE3	Clear all peak values.	Send Byte	N					96
MFR_PADS_LTC3882-1	0xE5	State of selected LTC3882-1 pads.	R Word	N	Reg				92
MFR_ADDRESS	0xE6	Specify right-justified 7-bit device address.	R/W Byte	N	Reg		●	0x4F	74
MFR_SPECIAI_ID	0xE7	Manufacturer code representing the LTC3882-1	R Word	N	Reg			0x424X(-1) 0x452X(-2)	107
MFR_FAULT_LOG_STORE	0xEA	Force transfer of fault log from operating memory to EEPROM.	Send Byte	N					106
MFR_FAULT_LOG_CLEAR	0xEC	Clear existing EEPROM fault log.	Send Byte	N					104
MFR_FAULT_LOG	0xEE	Read fault log data.	R Block	N	Reg				104
MFR_COMMON	0xEF	LTC-generic device status reporting.	R Byte	N	Reg				93
MFR_COMPARE_USER_ALL	0xF0	Compare operating memory with EEPROM contents.	Send Byte	N					105
MFR_TEMPERATURE_2_PEAK	0xF4	Maximum internal temperature measurement since last MFR_CLEAR_PEAKS.	R Word	N	L11	°C			96
MFR_PWM_CONFIG_LTC3882-1	0xF5	LTC3882-1 PWM configuration common to both channels.	R/W Byte	N	Reg		●	0x14	78
MFR_IOUT_CAL_GAIN_TC	0xF6	Output current sense element temperature coefficient.	R/W Word	Y	CF	ppm/°C	●	3900ppm/°C 0x0F3C	85
MFR_TEMP_1_GAIN	0xF8	Slope for external temperature calculations.	R/W Word	Y	CF		●	1.0 0x4000	88
MFR_TEMP_1_OFFSET	0xF9	Offset addend for external temperature calculations.	R/W Word	Y	L11	°C or V	●	0.0 0x8000	88
MFR_RAIL_ADDRESS	0xFA	Specify unique right-justified 7-bit address for channels comprising a PolyPhase output.	R/W Byte	Y	Reg		●	0x80	74
MFR_RESET	0xFD	Force full reset without removing power.	Send Byte	N					76

NVM ● Indicates a command value stored to internal EEPROM using STORE_USER_ALL or restored to RAM from internal EEPROM at power-up or execution of RESTORE_USER_ALL or MFR_RESET.

APPLICATIONS INFORMATION

Efficiency Considerations

Normally, one of the primary goals of any LTC3882-1 application will be to obtain the highest practical conversion efficiency. The efficiency of a switching regulator is equal to the output power divided by the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and to ascertain which change would produce the most improvement. Balancing or limiting these individual losses plays a dominant role in the component selection process outlined over the next few sections.

Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, et al, are the individual losses as a percentage of input power: $100 \bullet P_{Ln}/P_{IN}$.

Although all dissipative elements in the system produce losses, four main sources usually account for most of the losses in LTC3882-1 applications: IC supply current, I^2R losses, topside power MOSFET transition losses and total gate drive current.

1. The LTC3882-1 IC supply current is a DC value given in the Electrical Characteristics table. The absolute loss created by the IC itself is approximately this current times the V_{CC} supply voltage. IC supply current typically results in a small loss (<0.1%).
2. I^2R losses occur mainly in the DC resistances of the MOSFET, inductor, PCB routing, and input and output capacitor ESR. Since each MOSFET is only on for part of the cycle, its on-resistance is effectively multiplied by the percentage of the cycle it is on. Therefore the bottom MOSFET should have a much lower on-resistance $R_{DS(ON)}$ than the top MOSFET in high step-down ratio applications. It is crucial that careful attention is paid to the layout of the power path on the PCB to minimize its resistance. In a 2-phase 1.2V system, 1mΩ of PCB resistance at the output costs 5% in efficiency with the output running at 60A.
3. Transition losses apply only to the topside MOSFET and become significant when operating at high input voltages (typically above 12V). This loss can be minimized by choosing a driver with very low drive resistance and a MOSFET with low gate charge Q_G, gate resistance R_G and Miller capacitance C_{MILLER}. Absolute transition loss can be estimated by:

$$P_{TRANS} = (1.7) \bullet V_{IN}^2 \bullet I_{OUT} \bullet C_{MILLER} \bullet f_{PWM}$$

4. Gate drive current is equal to the sum of the top and bottom MOSFET gate charges multiplied by the frequency of operation. These charges are based on the gate voltage applied by the FET driver and can be determined from manufacturer curves like the one shown in Figure 21. Many driver ICs employ asymmetrical gate voltages for top and bottom FETs.

Other sources of loss include body or Schottky diode conduction during the driver dependent non-overlap time and inductor core losses. These latter categories generally account for less than 2% total additional loss.

PWM Frequency and Inductor Selection

The selection of the PWM switching frequency is a trade-off between efficiency, transient response and component size. High frequency operation reduces the size of the inductor and output capacitor as well as increasing the maximum practical control loop bandwidth. However, efficiency is generally lower due to increased transition and switching losses. The inductor value is related to the switching frequency f_{PWM} and step-down ratio. It should be selected to meet choke ripple current requirements. The inductor value can be calculated using the following equation:

$$L = \left(\frac{V_{OUT}}{f_{PWM} \bullet \Delta I_L}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Allowing a larger value of choke ripple current (ΔI_L) leads to smaller L, but results in greater core loss and higher output voltage ripple for a given output capacitance and/or ESR. A reasonable starting point for setting the ripple current is 30% of the maximum output current.

The inductor saturation current rating needs to be higher than the peak inductor current during transient conditions. If I_{OUT} is the maximum rated load current, then the maximum transient current I_{MAX} would normally be chosen to be some factor greater than I_{OUT} (e.g., $1.6 \bullet I_{OUT}$).

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The minimum saturation current rating should be chosen to allow margin due to manufacturing and temperature variation in the sense resistor or inductor DCR. A reasonable I_{SAT} value would be 2.2 • I_{OUT}.

The programmed current limit IOUT_OC_FAULT_LIMIT must be low enough to ensure that the inductor never saturates and high enough to allow increased current during transient conditions with margin for DCR variation. For example, if

I_{SAT} = 2.2 • I_{OUT}, and

I_{MAX} = 1.6 • I_{OUT}

a reasonable output current limit would be

IOUT_OC_FAULT_LIMIT = 1.8 • I_{OUT}

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core losses found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Also, core losses decrease as inductance increases. Unfortunately, increased inductance requires more turns of wire, larger inductance and larger copper losses.

Ferrite designs have very low core loss and are preferred at high switching frequencies. However, these core materials exhibit hard saturation, causing an abrupt reduction in the inductance when the peak current capability is exceeded. Do not allow the core to saturate!

Power MOSFET Selection

The LTC3882-1 requires at least two external N-channel power MOSFETs per channel, one for the top (main) switch and one or more for the bottom (synchronous) switch. The number, type and on-resistance of the MOSFETs selected should take into account the voltage step-down ratio and the FET circuit position (main or synchronous switch). A much smaller and lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than one-third of the input voltage. At operating frequencies above 300kHz and where V_{IN} >> V_{OUT}, the top MOSFET on-resistance is normally less important for overall efficiency than its input capacitance. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

Selection criteria for the power MOSFETs include on-resistance, gate charge, Miller capacitance, breakdown voltage and maximum output current.

For maximum efficiency, $R_{DS(ON)}$ and Q_G should be minimized. Low $R_{DS(ON)}$ minimizes conduction losses and low Q_G minimizes switching and transition losses. MOSFET gate charge can be taken from the typical gate charge curve included on most data sheets (Figure 21).

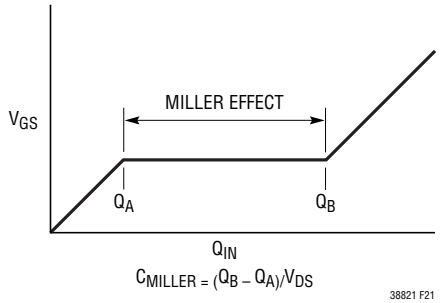


Figure 21. Typical MOSFET Gate Charge Curve

C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{MILLER} is equal to the increase in gate charge along the horizontal axis of Figure 21 while the curve is approximately flat, divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the actual application V_{DS} to the V_{DS} specified on the gate charge curve. When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

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The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + V_{IN}\ ^2\frac{I_{MAX}}{2}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{GG}-V_{TH(IL)}}+\frac{1}{V_{TH(IL)}}\right](f_{PWM})$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance, V_{IN} is the drain potential and the change in drain potential in the particular application. V_{GG} is the applied gate voltage, $V_{TH(IL)}$ is the typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current, and C_{MILLER} is the capacitance calculated using the technique previously described.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ versus temperature curve. Typical values for δ range from 0.005/°C to 0.01/°C depending on the particular MOSFET used.

Both MOSFETs have I^2R losses while the topside N-channel losses also include transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ and meet the current and thermal requirements if desired.

If using discrete drivers and MOSFETs, check the stress on the MOSFETs by independently measuring the drain-to-source voltages directly across the device terminals. Beware of inductive ringing that could exceed the maximum voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, choose a higher voltage rated MOSFET.

MOSFET Driver Selection

Gate driver ICs, DrMOS devices and power blocks with an interface compatible with the LTC3882-1 3.3V three-state PWM control output(s) can be used. An external resistor divider may be needed to set three-state control voltage outputs to mid-rail while in the high impedance state, depending on the driver selected. These external driver/power circuits do not typically present a heavy capacitive load to the LTC3882-1 PWM outputs. Suitable drivers such as the LTC4449 are capable of driving large gate capacitances at high transition rates. In fact, when driving MOSFETs with very low gate charge, it is sometimes helpful to slow down the drivers by adding small gate resistors (5Ω or less) to reduce noise and EMI caused by fast transitions.

Using PWM Protocols

For successful utilization of the driver selected, the appropriate LT3882-1 PWM control protocol must be programmed. The LTC3882-1 supports two three-state PWM control protocols. See bit 1, of the MFR_PWM_MODE_LTC3882-1 PMBus command.

The first of these protocols (bit 1=0) is for drivers controlled by a single 3-state input that have sufficiently short delay to the diode emulation state (both top and bottom power MOSFETs disabled in a fraction of a PWM cycle), such as the LTC4449. The second protocol (bit 1=1) handles all other 3.3V compatible drivers with a single 3-state control input.

C_{IN} Selection

The input bypass capacitance for an LTC3882-1 circuit needs to have ESR low enough to keep the supply drop low as the top MOSFETs turn on, RMS current capability adequate to withstand the ripple current at the input, and a capacitance value large enough to maintain the input voltage until the input supply can make up the difference. Generally, a capacitor that meets the first two requirements (particularly a non-ceramic type) will have far more

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capacitance than is required to keep capacitance-based droop under control.

The input capacitance voltage rating should be at least 1.4 times the maximum input voltage. Power loss due to ESR occurs as I^2R dissipation in the capacitor itself. The input capacitor RMS current and its impact on any preceding input network is reduced by PolyPhase architecture. It can be shown that the worst case RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product should be used to determine the maximum RMS current requirement. Increasing the output current drawn from the other out-of-phase controller will decrease the input RMS ripple current from this maximum value. Two channel out-of-phase operation typically reduces the input capacitor RMS ripple current by a factor of 30% to 70%.

In continuous inductor conduction mode, the source current of the top power MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. The maximum RMS capacitor current in this case is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \frac{\sqrt{V_{OUT}\left(V_{IN}-V_{OUT}\right)}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where

$$I_{RMS} = I_{OUT}/2$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Note that manufacturer ripple current ratings for capacitors are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

Ceramic, tantalum, semiconductor electrolyte (OS-CON), hybrid conductive polymer (SUNCON) and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks. Ceramics have high voltage coefficients of capacitance and may have audible piezoelectric effects; tantalums need to be surge-rated; OS-CONs suffer from higher inductance, larger case size and limited surface mount applicability; and electrolytic capacitors have higher ESR and can dry out. Sanyo OS-CON SVP(D) series, Sanyo POSCAP TQC series, or Panasonic EE-FT series aluminum electrolytic capacitors can be used in parallel with a couple of high performance ceramic capacitors as an effective means of achieving low ESR and high bulk capacitance.

In addition to PWM bulk input capacitance, a small (0.01µF to 1µF) bypass capacitor between the chip VINSNS pin and ground, placed close to the LTC3882-1, is also suggested. A small resistor placed between the bulk C_{IN} and the VINSNS pin provides further isolation between the two channels. However, if the time constant of any such R-C network on the VINSNS pin exceeds 30ns, dynamic line transient response can be adversely affected.

C_{OUT} Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8 \bullet f_{PWM} \bullet C_{OUT}} \right)$$

where ΔI_L is the inductor ripple current.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{PWM}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Since ΔI_L increases with input voltage, the output ripple voltage is highest at maximum input voltage. Typically once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Manufacturers such as Sanyo, Panasonic and Cornell Dubilier should be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has a good (ESR)(size) product. An additional ceramic capacitor in parallel with polarized capacitors is recommended to offset the effect of lead inductance.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or transient current

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handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent output capacitor choices include the Sanyo POSCAP TPD/E/F series, the Kemet T520, T530 and A700 series, NEC/Tokin NeoCapacitors and Panasonic SP series. Other suitable capacitor types include Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations.

Feedback Loop Compensation

The LTC3882-1 is a voltage mode controller with a second, dedicated current sharing loop to provide excellent phase-to-phase current sharing in PolyPhase applications. The current sharing loop is internally compensated.

While Type 2 compensation for the voltage control loop may be adequate in some applications (such as with the use of high ESR bulk capacitors), Type 3 compensation and ceramic capacitors are recommended for optimum transient response.

Figure 22 shows a simplified view of the error amplifier EA for one LTC3882-1 channel. The positive input of the error amplifier is connected to the output of an internal 12-bit DAC fed by a 1.024V reference, while the negative input is connected to the FB pin and other internal circuits (not all shown). R1 is internal to the IC with a value range given by the R_{VSFB} parameter in the Electrical Characteristics table. The output is connected to COMP, from which the PWM controller derives the required output duty cycle. To speed up overshoot recovery time, the maximum potential at the COMP pin is internally clamped.

Unlike many regulators that use a transconductance (g_m) amplifier, the LTC3882-1 is designed to use an inverting summing amplifier topology with the FB pin configured as a virtual ground. This allows feedback gain to be tightly controlled by external components, which is not possible with a simple g_m amplifier. The voltage feedback amplifier also provides flexibility in choosing pole and zero locations. In particular, it allows the use of Type 3 compensation to provide phase boost at the LC pole frequency for significantly improving the control loop phase margin, as shown in Figure 23.

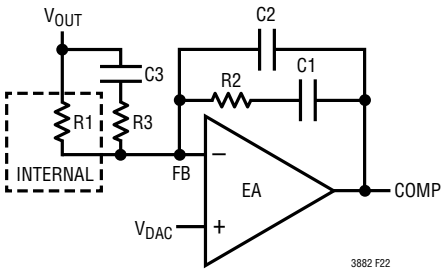


Figure 22. Type 3 Compensation Circuit

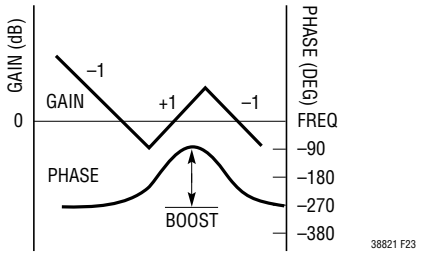


Figure 23. Type 3 Compensation Frequency Response

In a typical LTC3882-1 circuit, the feedback loop closed around this control amplifier and compensation network consists of the line feedforward circuit, the modulator, the external inductor and the output capacitor. All these components affect loop behavior and need to be accounted for in the frequency compensation.

The modulator consists of the PWM generator, the output MOSFET drivers and the external MOSFETs themselves. Step-down modulator gain varies linearly with the input voltage. The line feedforward circuit compensates for this change in gain, and provides a constant gain A_{MOD} of 4V/V from the error amplifier output COMP to the inductor input (average DC voltage) regardless of V_{IN}. The combination of the line feedforward circuit and the modulator looks like a linear voltage transfer function from COMP to the inductor input with a fairly benign AC behavior at typical loop compensation frequencies. Significant phase shift will not begin to occur in this transfer function until half the switching frequency.

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The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a 2nd order amplitude roll-off that filters the PWM waveform, resulting in the desired DC output voltage. But the additional 180° phase shift produced by this filter causes stability issues in the feedback loop and must be frequency compensated. At higher frequencies, the reactance of the output capacitor will approach its ESR, and the roll-off due to the capacitor will stop, leaving –20dB/decade and 90° of phase shift.

The transfer function of the Type 3 circuit shown in Figure 22 is given by the following equation:

$$\frac{V_{COMP}}{V_{OUT}} = \frac{-(1+sC1R2)[1+s(R1+R3)C3]}{sR1(C1+C2)[1+s(C1//C2)R2](1+sC3R3)}$$

The RC network across the error amplifier and the feed-forward components R3 and C3 introduce two pole-zero pairs to obtain a phase boost at the system unity-gain (crossover) frequency, f_C. In theory, the zeros and poles are placed symmetrically around f_C, and the spread between the zeros and the poles is adjusted to give the desired phase boost at f_C. However, in practice, if the crossover frequency is much higher than the LC double-pole frequency, this method of frequency compensation normally generates a phase dip within the unity bandwidth and creates some concern regarding conditional stability.

If conditional stability is a concern, move the error amplifier zero to a lower frequency to avoid excessive phase dip. The following equations can be used to compute the feedback compensation component values:

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR}C_{OUT}}$$

choose:

$$f_C = \text{crossover frequency} = \frac{f_{PWM}}{10}$$

$$f_{Z1(ERR)} = f_{LC} = \frac{1}{2\pi R2C1}$$

$$f_{Z2(RES)} = \frac{f_C}{5} = \frac{1}{2\pi(R1+R3)C3}$$

$$f_{P1(ERR)} = f_{ESR} = \frac{1}{2\pi R2(C1//C2)}$$

$$f_{P2(RES)} = 5f_C = \frac{1}{2\pi R3C3}$$

Required error amplifier gain at frequency f_C is:

$$\approx 40\log\sqrt{1+\left(\frac{f_C}{f_{LC}}\right)^2} - 20\log\sqrt{1+\left(\frac{f_C}{f_{ESR}}\right)^2} - 15.56$$

Once the value of resistor R1 (function of selected V_{OUT} range) and pole/zero locations have been decided, the value of R2, C1, C2, R3 and C3 can be obtained from the previous equations.

Compensating a switching power supply feedback loop is a complex task. The applications shown in this data sheet provide typical values, optimized for the power components shown. Though similar power components should suffice, substantially changing even one major power component may degrade performance significantly. Stability also may depend on circuit board layout. To verify the calculated component values, all new circuit designs should be prototyped and tested for stability.

The LTPowerCAD software tool can be used as a guide through the entire power supply design process, including optimization of circuit component values according to system requirements.

PCB Layout Considerations

To prevent magnetic and electrical field radiation or high frequency resonant problems and to ensure correct IC operation, proper layout of the components connected to the LTC3882-1 is essential. Refer to Figure 24, which also illustrates current waveforms typically present in the circuit branches. R_{SENSE} will be replaced with a dead short if DCR sensing is used. For maximum efficiency, the switch

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node rise and fall times should be minimized. The following PCB design priority list will help ensure proper topology.

1. Place a ground or DC voltage layer between a power layer and a small-signal layer. Generally, power planes should be placed on the top layer (4-layer PCB), or top and bottom layer if more than 4 layers are used. Use wide/short copper traces for power components and avoid improper use of thermal relief around power plane vias to minimize resistance and inductance.
2. Low ESR input capacitors should be placed as close as possible to switching FET supply and ground connections with the shortest copper traces possible. The switching FETs must be on the same layer of copper as the input capacitors with a common topside drain connection at C_{IN}. Do not attempt to split the input decoupling for the two channels, as a large resonant loop can result. Vias should not be used to make these connections. Avoid blocking forced air flow to the switching FETs with large size passive components.
3. If using a discrete FET driver, place that IC close to the switching FET gate terminals, keeping the connecting traces short to produce clean drive signals. This rule also applies to driver IC supply and ground pins that connect to the switching FET source pins. The driver IC can be placed on the opposite side of the PCB from the switching FETs.
4. Place the inductor input as close as possible to the switching FETs. Minimize the surface area of the switch node. Make the trace width the minimum needed to support the maximum output current. Avoid copper fills or pours. Avoid running the connection on multiple copper layers in parallel. Minimize capacitance from the switch node to any other trace or plane.
5. Place the output current sense resistor (if used) immediately adjacent to the inductor output. PCB traces for remote voltage and current sense should be run together back to the LTC3882-1 in pairs with the smallest spacing possible on any given layer on which they are routed. Avoid high frequency switching signals and ideally shield with ground planes. Locate any filter component on these traces next to the LTC3882-1, and not at the Kelvin sense location. However, if DCR sensing is used, place the top resistor (R1, Figure 25) close to the switch node.
6. Place low ESR output capacitors adjacent to the sense resistor output and ground. Output capacitor ground connections must feed into the same copper that connects to the input capacitor ground before connecting back to system ground.
7. Connection of switching ground to system ground, small-signal analog ground or any internal ground plane should be single-point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection. This cluster should be located directly beneath the IC GND paddle, which serves as both analog signal ground and the negative sense for V_{OUT1}. A useful CAD technique is to make separate ground nets and use a 0Ω resistor to connect them to system ground.
8. Place all small-signal components away from high frequency switching nodes. Place decoupling capacitors for the LTC3882-1 immediately adjacent to the IC.
9. A good rule of thumb for via count in a given high current path is to use 0.5A per via. Be consistent when applying this rule.
10. Copper fills or pours are good for all power connections except as noted above in rule 3. Copper planes on multiple layers can also be used in parallel. This helps with thermal management and lowers trace inductance, which further improves EMI performance.

Output Current Sensing

The I_{SENSE}^+ and I_{SENSE}^- pins are high impedance inputs to internal current comparators, the current-sharing loop and telemetry ADC. The common mode range of the current sense inputs is approximately 0V to 5.5V. Continuous linear operation is provided throughout this range. Maximum differential current sense input ($I_{SENSE}^+ – I_{SENSE}^-$) is 70mV, including any variation over temperature. These inputs must be properly connected in the application at all times.

To maximize efficiency at full load the LTC3882-1 is designed to sense current through the inductor's DCR, as shown in Figure 25. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which

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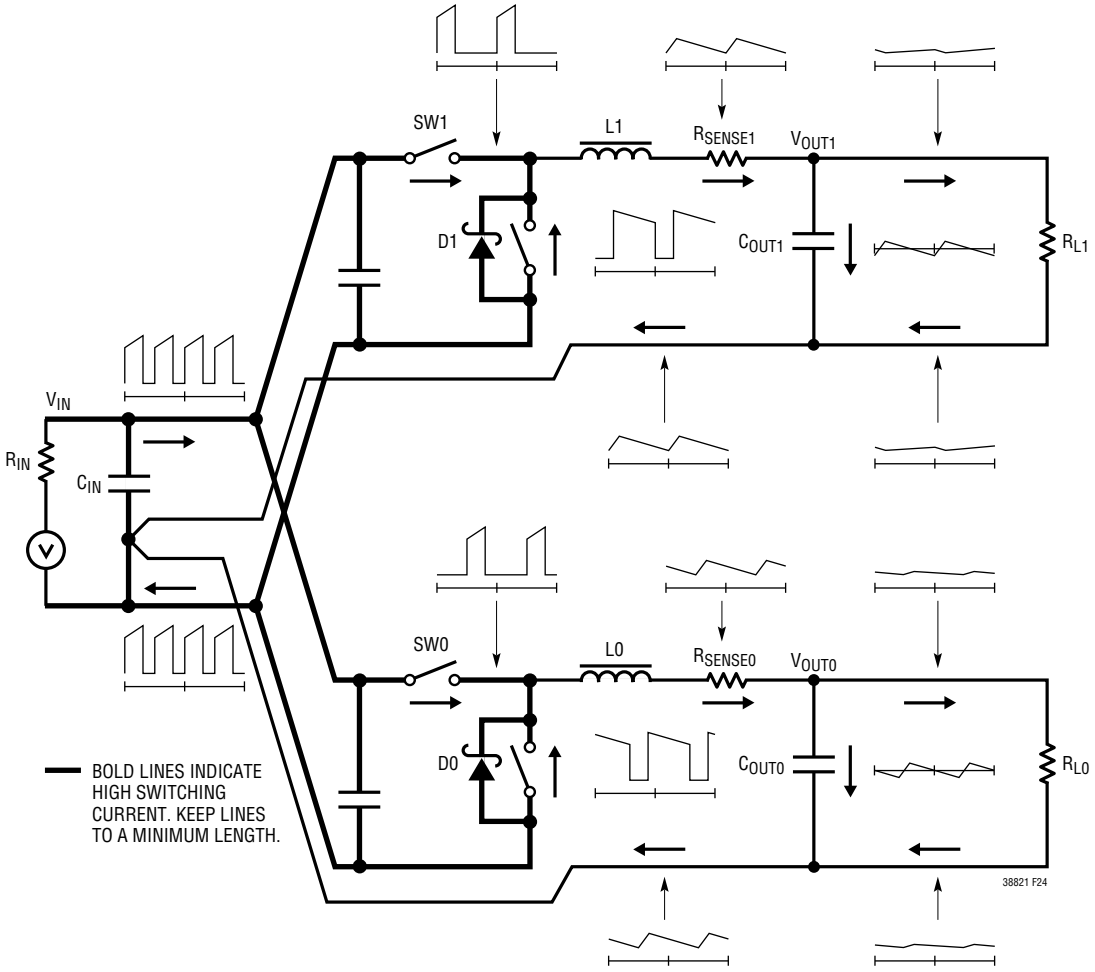


Figure 24. High Frequency Paths and Branch Current Waveforms

for most inductors suitable to LTC3882-1 applications, is between 0.3mΩ and 1mΩ. If the filter RC time constant is chosen to be exactly equal to the L/DCR time constant of the inductor, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR. Check the manufacturer's data sheet for specifications regarding the inductor DCR in order to properly dimension the external filter components. The DCR of the inductor can also be measured using a good RLC meter.

Use the nominal or measured value of DCR to program IOUT_CAL_GAIN (in mΩ). The temperature coefficient of the inductor's DCR is typically high, like copper. Again, consult the manufacturer's data sheet. The LTC3882-1 can adjust for this non-ideality if the correct MFR_IOUT_CAL_GAIN_TC value is programmed. Typically this coefficient is around 3900ppm/°C.

Resistor R1 should be placed close to the switch node, to prevent noise from coupling into sensitive small-signal nodes. Capacitor C1 should be placed close to the IC pins.

An example of discrete resistor sensing of output current is shown in Figure 26. Previously, the parasitic inductance of the sense resistor could represent a relatively small error. New high current density solutions may utilize low sense resistor values producing sense voltages less than 20mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common.

Under these conditions, the voltage drop across the sense resistor's parasitic inductance is no longer negligible. An RC filter can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 27 illustrates the voltage

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waveform across a 2mΩ resistor with a 2010 footprint. The waveform is the superposition of a purely resistive component and a purely inductive component. If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resultant waveform looks resistive, as shown in Figure 28.

For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and the following equation to determine the ESL:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \bullet \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}}$$

If low value (<5mΩ) sense resistors are used, verify that the signal across C_F resembles the current through the inductor, and reduce R_F to eliminate any large step associated with the turn-on of the primary switch.

Output Voltage Sensing

Accurate Kelvin sensing techniques should be used to connect the output voltage differentially back to the LTC3882-1 $V_{SENSE}^{\pm}$ pins of the master channel for the best output voltage regulation at the point of load. These pins also provide the ADC inputs for output voltage telemetry.

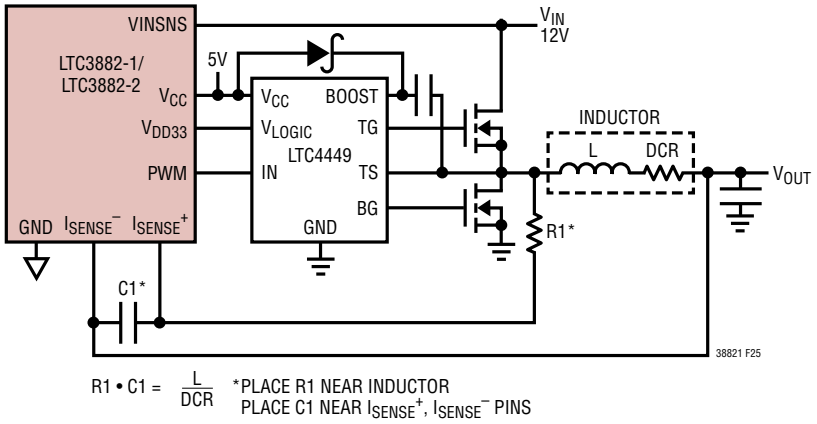


Figure 25. Inductor DCR Output Current Sense

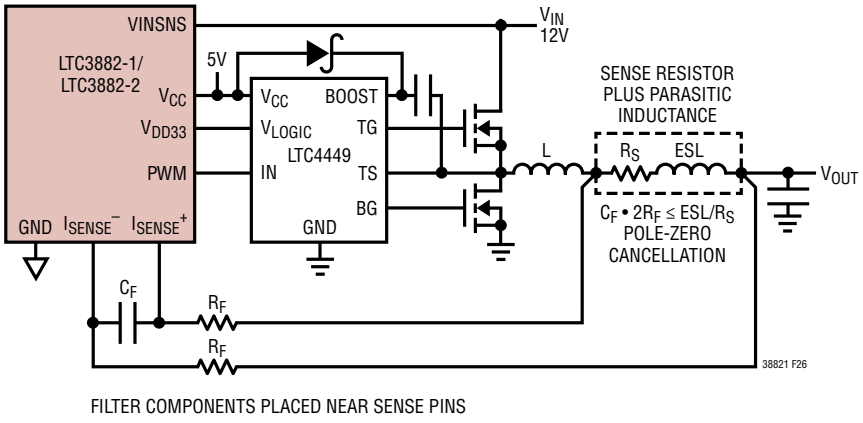


Figure 26. Discrete Resistor Output Current Sense

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While these considerations may or may not be important for slave channels, V_{OUT} must be connected back to the slave channel V_{SENSE} pin(s) in order for the I_{OUT} telemetry of those phases to be accurate. So in general, sound Kelvin V_{OUT} sensing techniques for all LTC3882-1 channels is recommended.

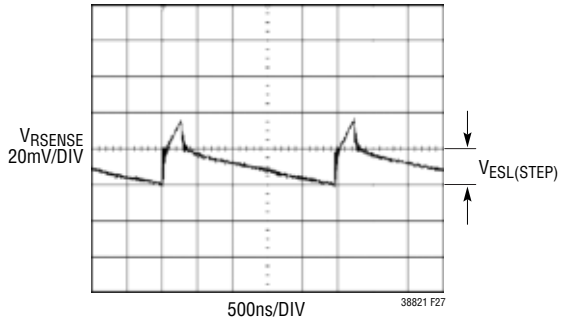


Figure 27. Voltage Measured Directly Across R_{SENSE}

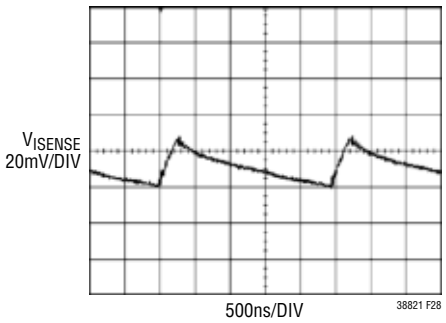


Figure 28. Voltage Measured at I_{SENSE} Pins

Soft-Start and Stop

The LTC3882-1 uses digital ramp control to create both soft-start and soft-stop.

The LTC3882-1 must enter the run state prior to soft-start. The RUN pins are released after the part initializes and VINSNS is determined to be greater than the VIN_ON threshold.

Once in the run state, soft-start is performed after any additional prescribed delay (next section) by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set point. Rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with start-up voltage ramp. The maximum rate at which the LTC3882-1 can move the output in this fashion is 100µs/step. Soft-start is disabled by setting TON_ RISE to any value less than 0.250ms. The LTC3882-1 will perform the necessary math internally to assure the voltage ramp is controlled to the desired slope. However, the voltage slope cannot be any faster than the fundamental limits of the power stage. The smaller TON_RISE becomes, the more noticeable an output voltage stair-step may become.

The LTC3882-1 also supports soft turn off in the same manner it controls turn on. TOFF_FALL is processed when the RUN pin goes low or if the part is commanded off. If the part faults off or $\overline{\text{FAULT}}$ is pulled low and the part is programmed to respond to this, the PWM instantly commands the output off. The output will then decay as a function of load current.

The LTC3882-1 can produce a controlled ramp off as long as the power stage is configured to run in CCM and the TOFF_FALL time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL time can only be met if the power stage can sink sufficient current under closed loop control to assure the output is at 0V by the end of the fall time. If TOFF_FALL is shorter than the time required to discharge the load capacitance, the output will not reach 0V. In this case, the power stage will still be commanded off at the end of TOFF_FALL and V_{OUT} will decay at a rate determined by the load. If the controller is set to run DCM, the controller will not pull negative current and the output will only be pulled low by the load, not the power stage. The maximum fall time is limited to 1.3 seconds. The smaller TOFF_FALL becomes, the more noticeable an output voltage stair-step may become.

Time-Based Output Sequencing and Ramping

The LTC3882-1 TON_DELAY and TOFF_DELAY commands can be used in combination with the rise and fall time commands covered in the previous section to implement a wide range of versatile sequencing and ramping schemes. The key to time-based sequencing and ramping is the ability of LTC3882-1 master phases to move their outputs up and down according to PMBus command values as shown in Figure 29 and Figure 30.

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As shown in Figure 29, it is important to remember that the hysteresis given in the Electrical Characteristics (EC) table applies above VOUT_UV_FAULT_LIMIT, which specifies the UV limit when the output is falling out of regulation. For turn-on, the output must rise above this programmed limit plus the hysteresis to avoid exceeding TON_MAX_FAULT_LIMIT. PGOOD is indicated at that point. For this reason, VOUT_UV_FAULT_LIMIT should be more than 27mV below the programmed output voltage in low range and more than 54mV below V_{OUT} in high range. There is a fixed delay and other timing uncertainty associated with all changes in output voltage controlled by the LTC3882-1. A nominal fixed timing delay of 270µs exists to process any change in output voltage, including soft start/stop, margining and general changes in VOUT_COMMAND value. The start of all time-based output operations occur with an uncertainty of ±50µs and have a nominal step resolution of 100µs. This means the minimum TON_DELAY or TOFF_DELAY that the LTC3882-1 can produce will range from 220µs to 320µs, not including basic oscillator tolerances. For software-based output changes (e.g., margining), this algorithmic delay begins when the STOP bit is received on the serial bus. An example of this minimum turn on/off delay and step-wise output control can be seen in Figure 31, where TON_DELAY = 0s and TON_RISE = 1ms.

To effectively implement sequencing and synchronized ramping between rails controlled by LTC digital power products, two signals should be shared between all controlling ICs: SHARE_CLK and RUN (CONTROL pin on LTC297x products). This facilitates synchronized rail sequencing on or off based on shared input supply state (VIN_ON threshold), external hardware control (RUN pin), or PMBus commands (possibly using global addressing).

Figure 32 shows an example of output supply sequencing using TON_DELAY.

Using this scheme, conventional coincident and ratiometric tracking can also be emulated by setting equivalent turn-on/off delays and appropriate rise and fall times as shown in Figure 33 and Figure 34.

In addition, these schemes can easily be mixed and matched to create any necessary ramping controls, some of which might prove difficult to implement with conventional analog-only controllers. These programmable features

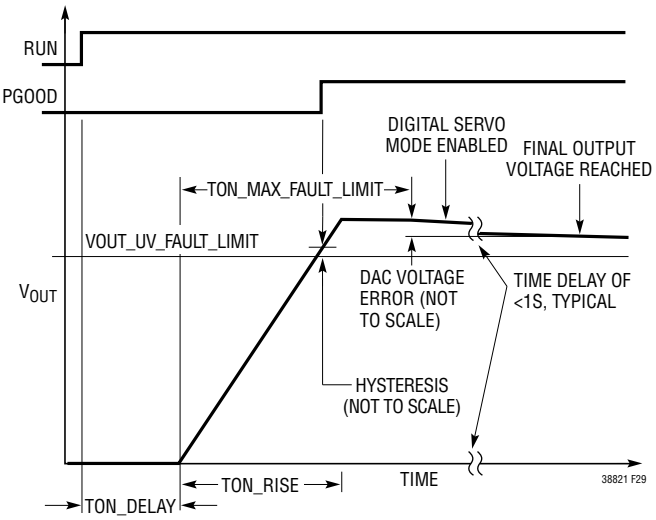


Figure 29. Time-Based V_{OUT} Turn-On

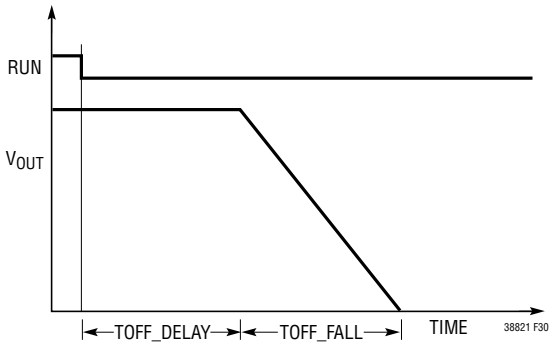


Figure 30. Time-Based V_{OUT} Turn-Off

greatly simplify actual system development because rails can be re-sequenced without a hardware change as final product requirements evolve. The LTpowerPlay GUI and LTC3882-1 onboard EEPROM can be used for this task, avoiding the need for firmware development to modify turn on/off relationships between rails. Entire power systems can then easily be scaled up or down, facilitating reuse of proven hardware macro designs.

Voltage-Based Output Sequencing

The LTC3882-1 is capable of voltage-based output sequencing. For concatenated events between members of the LTC388x family, it is possible to control one RUN pin from a PGOOD pin of a different controller as shown in

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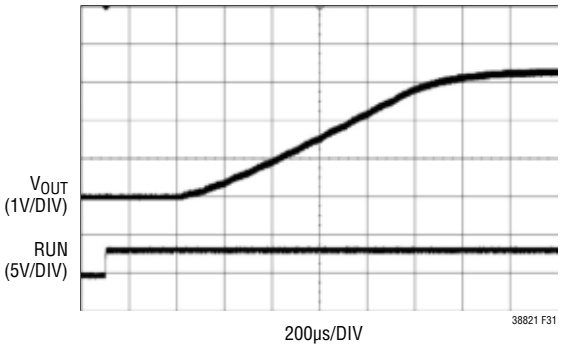


Figure 31. Example of 1ms TON_RISE

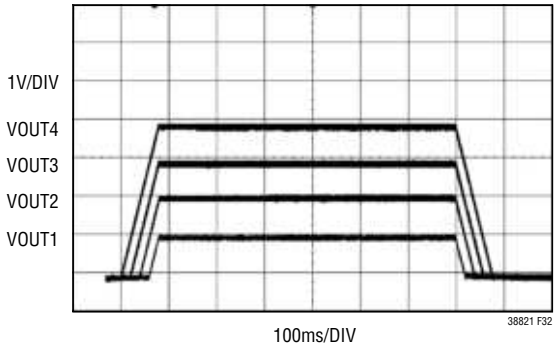


Figure 32. LTC3882-1 Time-Based Supply Sequencing

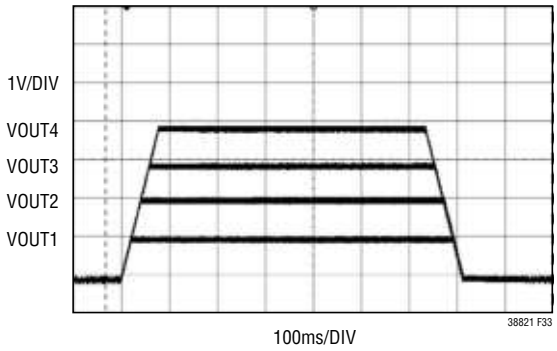


Figure 33. LTC3882-1 Time-Based Coincident Supply Ramping

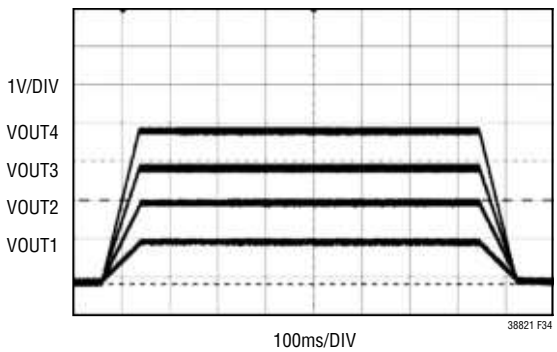


Figure 34. LTC3882-1 Time-Based Ratiometric Ramping

Figure 35. This configuration hardware disables the next downstream controller anytime the output is not within the specified UV and OV limits, or the upstream controller is disabled. When indicating power is not good, there is a 30µs deglitching filter on the PGOOD output to assure the signal does not toggle repeatedly at lower values of TON_RISE/FALL due to noise on V_{OUT}. If unwanted transitions still occur on PGOOD due to noise or longer rise/fall settings, place a capacitor to ground on the PGOOD pin to further filter the waveform. The RC time-constant of the filter should be low enough to assure no appreciable delay is incurred. A value of 300µs to 500µs will provide some additional filtering without significantly delaying the trigger event.

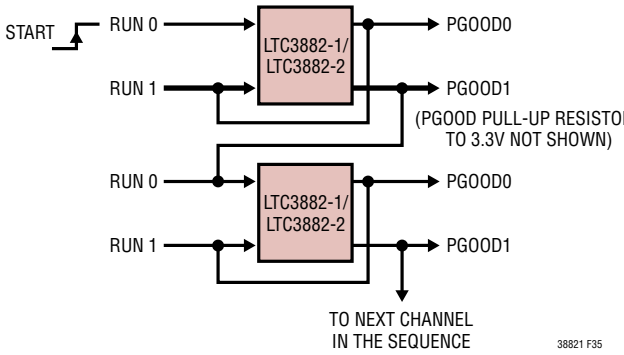


Figure 35. Cascade Sequencing Configuration

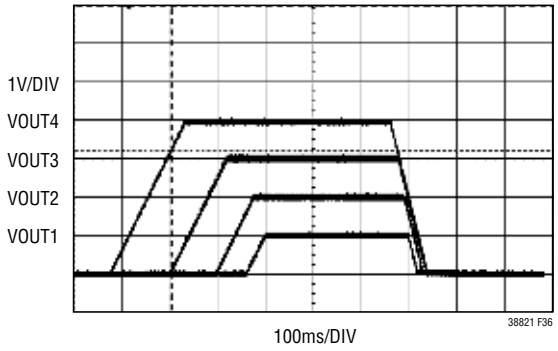


Figure 36. Cascade Sequencing Waveforms

When the system is turned off, rails will shut down in the same order as they turn on, as shown in Figure 36. If a different sequence is required, the circuit must be rewired or delays must be added by programming TON_DELAY or TOFF_DELAY. A fundamental limitation of this application is the inability of upstream rails to detect a start-up failure of

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downstream rails. Due to this, cascade sequencing should not be implemented without an external fast supervisor to monitor downstream rails and assert a system fault if problems occur.

Using Output Voltage Servo

For best output voltage accuracy, enable digital servo mode on the master phase by setting bit 6 of MFR_PWM_MODE_LTC3882-1. In digital servo mode, the LTC3882-1 will adjust the regulated output voltage based on its related ADC voltage reading. Every 90ms the digital servo loop will step the LSB of the DAC (nominally 1.375mV or 0.6875mV depending on the voltage range bit) until the output is at the correct ADC reading.

When the master channel is turned on, digital servo is enabled after all of the following conditions are satisfied.

- MFR_PWM_MODE_LTC3882-1 Bit 6 Is Set
- The TON_RISE Sequence Is Complete
- A VOUT_UV_FAULT Is Not Present
- An IOUT_OC_FAULT Is Not Present
- MFR_AVP = 0%

Digital servo mode then engages after TON_MAX_FAULT_LIMIT has expired as shown in Figure 29, unless that limit is set to 0s (infinite). In that case, the mode is engaged as soon as the above conditions are satisfied.

Using AVP

The LTC3882-1 features digitally programmable active voltage positioning (AVP), where output voltage set point is automatically adjusted as a function of output current at the full bandwidth of the converter. AVP normally entails specifying an output load line for a voltage mode switcher to allow current sharing between master phases connected in parallel. While AVP can be used to this effect in LTC3882-1 applications, use of the LTC3882-1 I_{AVG} current sharing control loop is recommended instead. This will produce more accurate sharing across a wider number of phases without degrading supply output impedance.

However, AVP can still be used to great benefit in LTC3882-1 applications. AVP can be applied to minimize the size of output filter capacitance for some allowed output voltage variation over the anticipated load range. An example of AVP is shown in Figure 37. Refer to LTC Design Solution 10 for additional examples of using AVP to advantage.

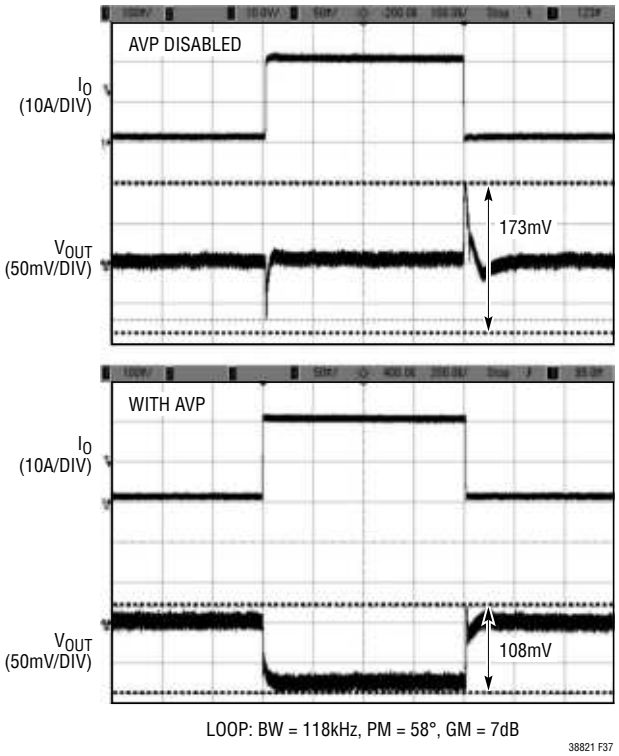


Figure 37. Active Voltage Positioning

MFR_VOUT_AVP specifies the percent reduction in programmed V_{OUT} from no load at an output current value equal to IOUT_WARN_LIMIT. LTC3882-1 AVP supports a maximum reduction in V_{OUT} of 15%, corresponding to a ±7.5% tolerance about a nominal output voltage at roughly 50% load. In order to effectively use AVP, apply the following steps.

1. Set IOUT_OC_WARN_LIMIT. This specifies the master phase output current at which the programmed AVP level will apply. Generally this is above the 100% load point to avoid spurious warnings at full load.
2. VOUT_COMMAND should be set to the value of V_{OUT} desired with no load on the output. VOUT_MARGIN_HIGH/LOW also specify no-load values when AVP is enabled. AVP on the LTC3882-1 can only reduce the output from these levels.

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3. Set MFR_VOUT_AVP to a percentage that produces the desired output excursion as a function of current.

For example, if the goal is to allow a 2.5% output change on a 3.3V 6-phase supply rated at 120A during an output load step from 20% to 80%, the following parameters should be programmed.

First set an output current warning level for the master (one of six phases) just slightly higher than the rated full load to avoid spurious warnings. Typically this same setting would also be applied to the five slave phases.

$$IOUT_OC_WARN_LIMIT = 1.1 \bullet 120A/6 = 22A$$

The open circuit output voltage calculation for the master phase must reflect that the AVP specification in this case only covers an output load swing of 60%.

$$VOUT_COMMAND = 3.3V(1 + 0.5 \bullet 0.025/0.6)$$

$$= 3.3687V$$

The AVP calculation must then account for the fact that IOUT_OC_WARN_LEVEL is set higher than the 100% load point.

$$MFR_VOUT_AVP = \frac{100\% \bullet 1.1 \bullet 2 \bullet (3.3687 - 3.3)}{3.3687}$$

$$= 4.487\%$$

With the output voltage at 3.3V at 50% load these settings will move V_{OUT} from approximately 3.34V to about 3.26V when the output load of the rail moves from 24A to 96A. Note that V_{OUT} will drop to 3.23V at full load in this design example.

Digital output servo mode is automatically disabled if AVP is enabled on a master phase. AVP is active during all output ramping when enabled (e.g., a TON_RISE sequence). AVP is disabled on master phases by programming MFR_VOUT_AVP to 0.0% (factory default). AVP is automatically disabled on phases configured as slaves (FB tied to V_{DD33}).

Because of related ISENSE input offsets, increased output voltage error can occur at all operating currents when AVP is engaged. To minimize this error a calibration offset can be added to the master phase VOUT_COMMAND value based on the READ_VOUT value obtained when operating at a known output current of at least 20% of full load (READ_IOUT). The necessary correction, which will typically be less than several percent of the no load output voltage, is calculated as:

$$VOS = VOUT_COMMAND \bullet \left(1 - \frac{MFR_VOUT_AVP \bullet READ_IOUT}{100 \bullet IOUT_OC_WARN_LIMIT}\right) - READ_VOUT$$

PWM Frequency Synchronization

The LTC3882-1/LTC3882-2 incorporates an internal phase-locked loop (PLL) which enables synchronization of both PWM channels (falling edge PWM) to an external CMOS clock from 250kHz to 1.25MHz (LTC3882-1), 250kHz to 2.5MHz (LTC3882-2). The PLL is locked to the falling edge of the SYNC pin clock signal. This PLL also generates very accurate channel phase relationships which can be selected with the MFR_PWM_CONFIG_LTC3882-1 command. For PolyPhase applications, all phases should be spaced evenly in the phase diagram for best results. For instance, a 4-phase system should use a separation of 90° between channels.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{ALERT}$ pin is pulled low, unless masked. The fault can be cleared by writing a 1 to STATUS_MFR_SPECIFIC bit 4. A spurious $\overline{ALERT}$ for an unlocked PLL may occur at start-up or during a reset if this fault is not masked.

Neither PWM channel will transition from off to the RUN state until PLL lock is indicated. When transitioning a channel from off to RUN, bit 4 of STATUS_MFR_SPECIFIC will be set if the PWM ramp generator for that channel is not also locked to the desired PLL output frequency.

If the SYNC pin is not externally clocked in the application, the PWMs will operate at the frequency specified by a non-zero FREQUENCY_SWITCH command. In the LTC3882-1 if FREQUENCY_SWITCH is set to 0x0000 (external clock only) in EEPROM or with RCONFIG (FREQ_CFG pin grounded), then at power-up, or MFR_RESET, or RESTORE_USER_ALL, the PWM will not start without an external clock input. The LTC3882-2 does not support frequencies <250kHz. In the LTC3882-1 if the external

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clock is lost while programmed for external clock only, or if the PWM is simply switched to this setting under power with no external clock present, the PLL will start/run at the lowest free running frequency created by the internal VCO. This can be well below the intended PWM frequency of the application and may cause undesirable operation of the converter. For this reason, it is generally recommended that a useable PWM frequency be programmed for each channel, regardless of whether that particiular LTC3882-1 unit serves as clock master, or not.

All channels of a PolyPhase rail are required to share SYNC pins. Between rails and for other configurations, such synchronization is optional. If the SYNC pin is shared between LTC3882-1s, only one LTC3882-1 should be programmed to control the SYNC output.

PolyPhase Operation and Load Sharing

When the LTC3882-1 is used in a PolyPhase application, the slave phases must be configured as such by connecting their FB pins to V_{DD33}. Among other things, this disables the error amplifiers of the slave phases. Five other pins must then also be shared between all channels of a PolyPhase rail:

- VINSNS
- COMP
- I_{AVG}
- I_{AVG_GND}
- SYNC

Using a common VINSNS connection reduces the dynamic range required by the current loop and helps maintain well-controlled master modulator gain.

The shared COMP signal allows the master phase error amplifier to control the duty cycle of all slave phases to produce the commanded output voltage.

Slave phases can detect system faults that cause the master COMP (error amplifier) output to be too high. A slave phase detecting this kind of error amplifier fault immediately shuts off its PWM output, indicates the fault on its VOUT_OV Fault bit, and takes whatever additional action may be indicated by VOUT_OV_FAULT_RESPONSE for that channel. If this response is set to only provide hardware-level response (0x00), then normal channel operation will automatically resume when the fault condition is cleared.

The shared I_{AVG} and I_{AVG_GND} signals actively balance the amount of output current delivered from each channel using a secondary current sharing loop. A capacitor with a value between 100pF and 200pF should be placed between I_{AVG} and I_{AVG_GND}. This capacitance can be distributed across LTC3882-1 devices/pins for improved noise immunity. All I_{AVG_GND} pins for a PolyPhase rail should be tied together and connected to a single ground point at or near the package paddle of the master phase.

Load sharing accuracy is based primarily on the current sense amplifier offset of each phase (I_{AVG_VOS}) and the offset of slave current error amplifiers (V_{SIOS}). These are given in the EC table. Current sense gain errors between LTC3882-1 channels will be negligible. The secondary current sharing loop acts to average any errors among the phases. Because of this error averaging and the random nature of these variables, the EC table limits ensure actual per-phase offset will be less than or equal to ±300µV for most designs over the full operating temperature range. This signifies better than ±2% matching when ΔI_{SENSE} = 15mV, not including external factors such as DCR make tolerance.

It is necessary to properly connect V_{SENSE}^+ on a slave phase for accurate I_{OUT} telemetry, even though slave phases do use need this information for PWM control. While not strictly required, the $V_{SENSE}^{\pm}$ lines of slave phases can simply share with the master to provide additional output voltage telemetry. If the only concern is accurate slave I_{OUT} telemetry, V_{SENSE}^+ for that channel may be locally wired to I_{SENSE}^-. V_{SENSE}^- on a slave phase should always be shorted to V_{SENSE}^- for its master channel. I_{OUT} OC/ROC function is not affected by $V_{SENSE}^{\pm}$ wiring.

All phases must be synchronized to the same shared SYNC clock and should be programmed to run at the same default PWM frequency. Phases should be selected to be evenly spaced around a 360° phasor diagram, and all phases on a PolyPhase rail should be selected to have the same maximum duty cycle. Refer to details for MFR_

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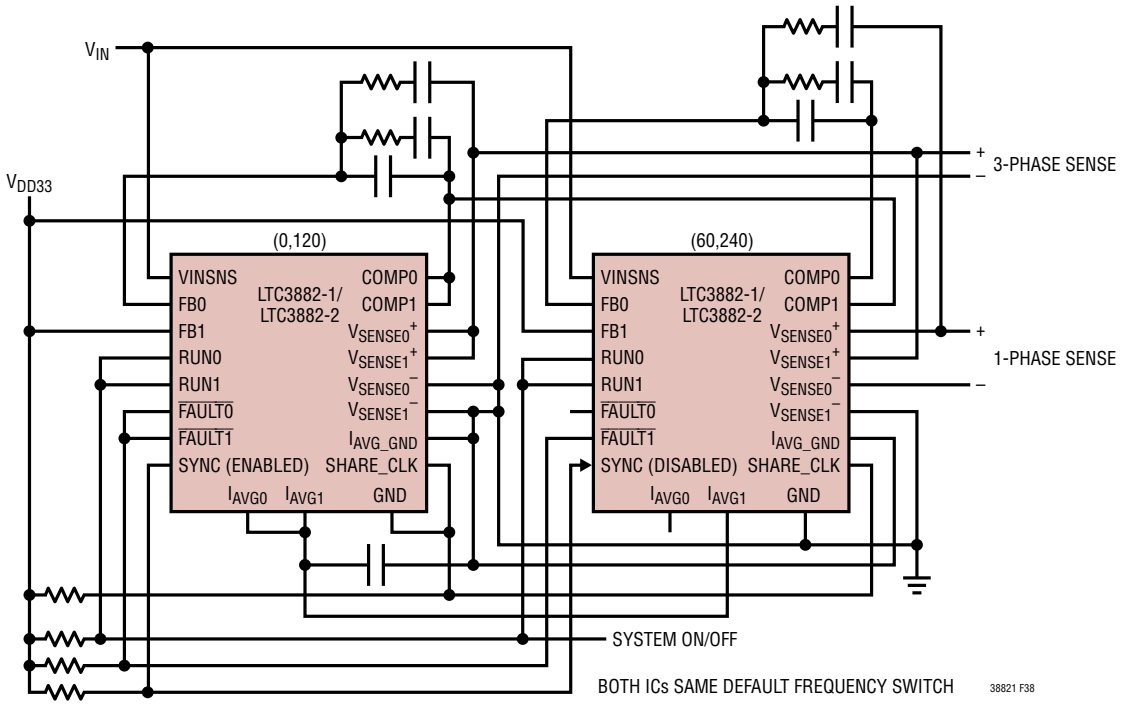


Figure 38. 3+1-Phase Application

PWM_CONFIG_LTC3882-1. Figure 38 shows an example of connections for three phases and Figure 39 shows an example of an 8-phase rail. Additional shared signals in these figures highlight the ability of the LTC3882-1 to communicate fault status between phases and rails, perform synchronized time-based rail sequencing and ramping and report accurate output current telemetry for all phases.

In general, only the PGOOD pin of the master phase needs to be used for external Power Good indication. However, PGOOD pins of slave phases may be shorted to a master PGOOD bus to indicate full output power is available, unless the slave channel is used in active phase shedding. In that case, the slave PGOOD should be left disconnected or used only to indicate operating status for that phase.

Output current fault and warning limits should each be set to the same values across all PolyPhase channels using IOUT_FAULT_LIMIT and IOUT_WARN_LIMIT. The correct sense resistance and related temperature coefficient should also be set for each phase (IOUT_CAL_GAIN, MFR_IOUT_CAL_GAIN_TC) to achieve accurate I_{OUT} telemetry and consistent fault handling across phases. Because the LTC3882-1 current sharing loop operates by matching sensed voltage, it is important that well-matched sense elements be used in the system. Current matching parameters specified for the LTC3882-1 do not include these external sources of error, such as inductor DCR tolerance. Programming of V_{OUT} related parameters is not required for slave phases.

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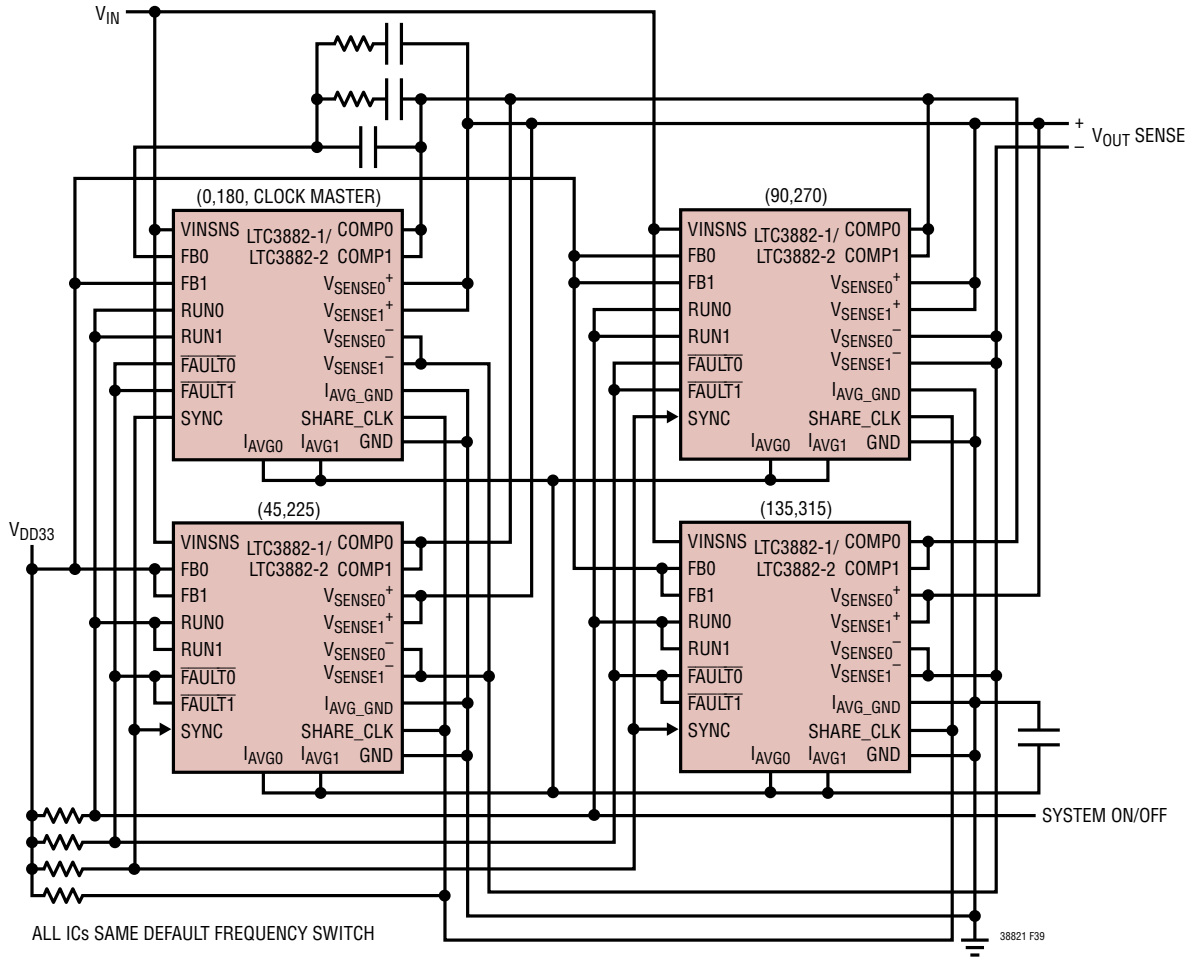


Figure 39. 8-Phase Application

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A PolyPhase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied by, the number of phases used as long as the input voltage is greater than the number of phases used times the output voltage. The output ripple amplitude is also reduced by the number of phases used. Figure 40 graphically illustrates the principle.

The worst-case RMS ripple current for a single stage design peaks at an input voltage of twice the output voltage. The worst case RMS ripple current for a 2-phase design peaks at output voltages of 1/4 and 3/4 of the input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the current in each stage is balanced. Refer to Application Note 19 at http://www.linear.com/designtools/app_notes for a detailed description of how to calculate RMS current for the single stage switching regulator. Figure 41 and Figure 42 illustrate how the input and output currents are reduced by using an additional phase. For a 2-phase converter, the input current peaks drop in half and the frequency is doubled. The input capacitor requirement is then theoretically reduced by a factor of four.

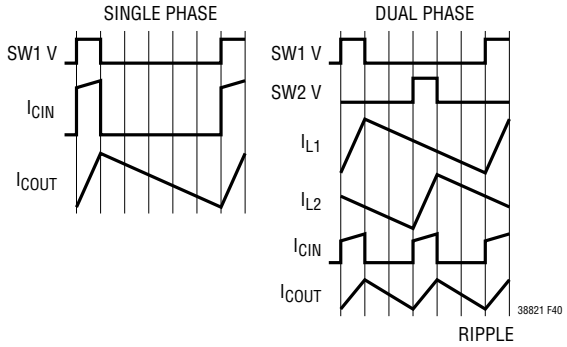


Figure 40. Single and 2-Phase Current Waveforms

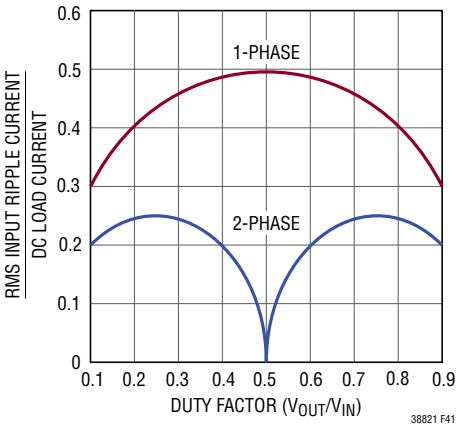


Figure 41. Normalized RMS Input Ripple Current

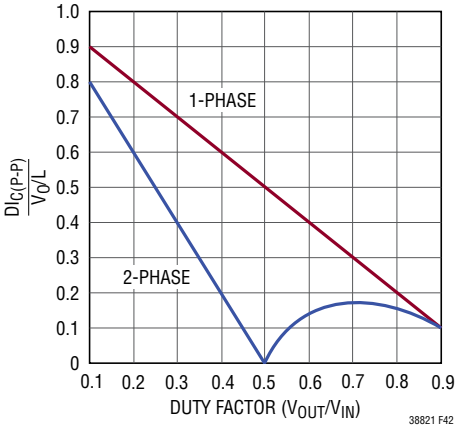


Figure 42. Normalized Output Ripple Current [I_{RMS} ~ 0.3($DI_{C(PP)}$)]

External Temperature Sense

The LTC3882-1 facilitates external measurement of the power stage temperature of each channel with several silicon-junction-based means. The voltage produced by the remote sense circuit is digitized by the internal ADC, and the computed temperature value is returned by the paged READ_TEMPERATURE_1 telemetry command.

The most accurate external temperature measurement can be made using a diode-connected PNP transistor such as the MMBT3906 as shown in Figure 43 with bit 5 of MFR_PWM_MODE_LTC3882-1 set to 0 (ΔV_{BE} method). The BJT should be placed in contact with or immediately adjacent to the power stage inductor. Its emitter should be connected to the TSNS*n* pin while the base and collector terminals of the PNP transistor must be returned to the LTC3882-1 GND paddle using a Kelvin connection. For best noise immunity, the connections should be routed differentially and a 10nF capacitor should be placed in parallel with the diode-connected PNP.

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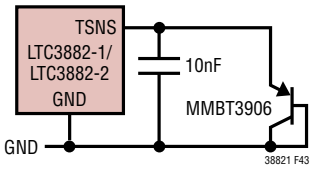


Figure 43. External ΔV_{BE} Temperature Sense

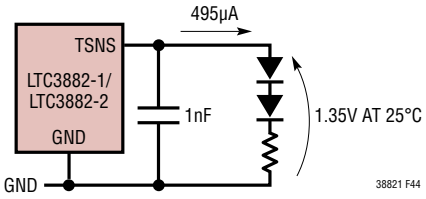


Figure 44. 2D+R Temperature Sense

The LTC3882-1 also supports direct junction voltage measurements when bit 5 of MFR_PWM_MODE_LTC3882-1 is set to one. The factory defaults support a resistor-trimmed dual diode network as shown in Figure 44. However, this measurement method can be applied to simple single-diode circuits of the type shown in Figure 43 with parameter adjustments as described below. This second measurement method is not generally as accurate as the first, but it supports legacy power blocks or may prove necessary if high noise environments prevent use of the ΔV_{BE} approach with its lower signal levels.

For either method, the slope of the external temperature sensor can be modified with the coefficient stored in MFR_TEMP_1_GAIN. With the ΔV_{BE} approach, typical PNPs require temperature slope adjustments slightly less than 1. The MMBT3906 has a recommended value in this command of approximately MFR_TEMP_1_GAIN = 0.991 based on the ideality factor of 1.01. Simply invert the ideality factor to calculate the MFR_TEMP_1_GAIN. Different manufacturers and different lots may have different ideality factors. Consult with the manufacturer to set this value. Bench characterization over temperature is recommended when adjusting MFR_TEMP_1_GAIN for the direct p-n junction measurement.

The offset of the external temperature sense can be adjusted by MFR_TEMP_1_OFFSET. For the ΔV_{BE} method a value of 0 in this register sets the temperature offset to –273.15°C. For a direct p-n junction measurement, this parameter adjusts the nominal circuit voltage at 25°C away from that shown in Figure 44.

To ensure proper use of these temperature adjustment parameters, refer to the specific formulas given for the two methods by the MFR_PWM_MODE_LTC3882-1 command in the later section covering PMBus command details, as well as Application Note 137.

Resistor Configuration Pins

As a factory default, the LTC3882-1 is programmed to use external resistor configuration, allowing output voltage, PWM frequency and phasing, and the PMBus address to be set without programming the part through its serial interface or purchasing devices with custom EEPROM contents. The RCONFIG pins all require a resistor divider between V_{DD25} and GND. The RCONFIG pins are only interrogated at initial power up and during a reset, so modifying their values on the fly is not recommended. RCONFIG pins on the same IC can be shared with a single resistor divider if they require identical programming. Resistors with a tolerance of 1% or better must be used to assure proper operation. In the following tables, R_{TOP} is connected between V_{DD25} and the RCONFIG pin, while R_{BOT} is connected between the pin and GND. Noisy clock signals should not be routed near these pins.

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Table 8. V_{OUTn_CFG} Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	V_{OUT} (V)	
		LTC3882-1	LTC3882-2
0 or Open	Open	NVM	NVM
10	23.2	5	5
10	15.8	3.3	3.3
16.2	20.5	2.5	2.5
16.2	17.4	1.8	1.8
20	17.8	1.5	1.5
20	15	1.35	1.35
20	12.7	1.25	1.25
20	11	1.2	1.2
24.9	11.3	1.15	1.15
24.9	9.09	1.1	1.1
24.9	7.32	1.05	1.0
24.9	5.76	0.9	0.9
24.9	4.32	0.75	0.75
30.1	3.57	0.65	0.65
30.1	1.96	0.6	0.6
open	0	output off* (V_{OUT} from NVM)	output off* (V_{OUT} from NVM)

*OPERATION value and RUNn pin must both command the channel to start from this configuration.

Output voltage can be set as shown in Table 8. For example, setting R_{TOP} to 16.2kΩ and R_{BOT} to 17.4kΩ is equivalent to programming a VOUT_COMMAND value of 1.8V. Refer to the Operations section for related parameters that are also automatically set as a percentage of the programmed V_{OUT} if resistor configuration pins are used to determined output voltage.

Table 9. FREQ_CFG Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	SWITCHING FREQUENCY (kHz)	
		LTC3882-1	LTC3882-2
0 or Open	Open	NVM	NVM
10	23.2		2500
10	15.8		2250
16.2	20.5		2000
16.2	17.4		1750
20	17.8	1250	1500
20	15	1000	1250
20	12.7	900	1000
20	11	750	900
24.9	11.3	600	750
24.9	9.09	500	600
24.9	7.32	450	500
24.9	5.76	400	450
24.9	4.32	350	400
30.1	3.57	300	350
30.1	1.96	250	300
open	0	External Sync	250

Note: Analog Devices does not recommend using the following PWM frequencies in new designs: 600kHz 750kHz, 900kHz, and 1MHz.

Note that if SYNC pins are shared between LTC3882-1s, only one SYNC output should be enabled. All other SYNC outputs should be disabled. For example, if configuring two LTC3882-1s as a 4-phase rail operating at a frequency of 600kHz, both devices should have R_{TOP} of 24.9kΩ and R_{BOT} of 11.3kΩ on the FREQ_CFG pin. In this case, selecting R_{TOP} of 24.9kΩ and R_{BOT} of 9.09kΩ for PHAS_CFG on the first IC (clock master) affords 180° of phase separation and enables the SYNC output. The second device should have R_{TOP} of 20kΩ and R_{BOT} of 12.7kΩ on PHAS_CFG, to disable its SYNC output and run its phases with 180° of separation in quadrature with the first IC. Only mix

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Table 10. PHAS_CFG Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	LTC3882-1				LTC3882-2			
		θ_{SYNC} TO θ_0	θ_{SYNC} TO θ_1	MAXIMUM DUTY CYCLE	SYNC OUTPUT DISABLED	θ_{SYNC} TO θ_0	θ_{SYNC} TO θ_1	MAXIMUM DUTY CYCLE	SYNC OUTPUT DISABLED
0 or Open	Open	NVM	NVM	See MFR_ PWM_CONFIG	NVM	NVM	NVM	See MFR_ PWM_CONFIG	NVM
10	23.2					135°	315°	87.5	Yes
10	15.8					90°	270°		
16.2	20.5					45°	225°		
16.2	17.4					0°	180°		
20	17.8					120°	300°	83.3	Yes
20	15	135°	315°	87.5	Yes	60°	240°		
20	12.7	90°	270°			0°	180°		
20	11	45°	225°			0°	120°		
24.9	11.3	0°	180°			135°	315°	87.5	No
24.9	9.09	0°	180°		No	90°	270°		
24.9	7.32	120°	300°	83.3	Yes	45°	225°		
24.9	5.76	60°	240°			0°	180°		
24.9	4.32	0°	180°			120°	300°	83.3	No
30.1	3.57	0°	120°			60°	240°		
30.1	1.96	0°	180°		No	0°	180°		
open	0	0°	120°			0°	120°		

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phase selections that have the same maximum duty cycle specified. Refer to Table 9 and 10.

The LTC3882-1 address is selected based on the programming of the two configuration pins ASEL0 and ASEL1 according to Table 11. ASEL0 programs the bottom four bits of the device address for the LTC3882-1, and ASEL1 programs the three most-significant bits. Either portion of the address can also be retrieved from the MFR_ADDRESS value in EEPROM. If both pins are left open, the full 7-bit MFR_ADDRESS value stored in EEPROM is used to determine the device address. In the 4-phase example above, it is recommended that one or both ASEL*n* pins on both parts be programmed to create two unique addresses. The LTC3882-1 also responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS and MFR_RAIL_ADDRESS should not be set to either of these values.

Refer to AN-152: Power System Management Addressing.

Table 11. ASEL*n* Resistor Programming

R_{TOP} (kΩ)	R_{BOT} (kΩ)	ASEL1		ASEL0	
		LTC3882-1 DEVICE ADDRESS BITS[6:4]		LTC3882-1 DEVICE ADDRESS BITS[3:0]	
		BINARY	HEX	BINARY	HEX
0 or Open	Open	from EEPROM		from EEPROM	
10	23.2			1111	F
10	15.8			1110	E
16.2	20.5			1101	D
16.2	17.4			1100	C
20	17.8			1011	B
20	15			1010	A
20	12.7			1001	9
20	11			1000	8
24.9	11.3	111	7	0111	7
24.9	9.09	110	6	0110	6
24.9	7.32	101	5	0101	5
24.9	5.76	100	4	0100	4
24.9	4.32	011	3	0011	3
30.1	3.57	010	2	0010	2
30.1	1.96	001	1	0001	1
Open	0	000	0	0000	0

Internal Regulator Outputs

The V_{DD33} pin provides supply current for much of the internal LTC3882-1 analog circuitry at a nominal value of 3.3V. The LTC3882-1 features an internal linear regulator that can be used to supply 3.3V to V_{DD33} from a higher voltage V_{CC} supply (up to 12V nominal). Use of this LDO is optional. The LTC3882-1 will also accept an external 3.3V supply attached to this pin if V_{CC} and V_{DD33} are shorted. If the internal 3.3V LDO is used, it can supply a peak current of 85mA (including internal consumption), and the V_{DD33} regulator output must be bypassed to GND with a low ESR X5R or X7R ceramic capacitor with a value of 2.2µF. If an external source supplies V_{DD33}, a local low ESR bypass capacitor with a value between 0.01µF and 0.1µF should be placed directly between the V_{DD33} and GND pins.

Do not draw more than 20mA from the internal 3.3V regulator for the host system, governed by IC power dissipation as discussed in the next section. This limit includes current required for external pull up resistors for the LTC3882-1 that are terminated to V_{DD33}.

V_{DD33} powers a second internal 2.5V LDO whose output is present on V_{DD25}. This 2.5V supply provides power for much of the internal processor logic on the LTC3882-1. The V_{DD25} output should be bypassed directly to GND with a low ESR X5R or X7R ceramic capacitor with a value of 1µF or greater. Do not draw any external system current from this supply beyond that required for LTC3882-1 specific configuration resistor dividers.

IC Junction Temperature

The user must ensure that the maximum rated junction temperature is not exceeded under all operating conditions. The thermal resistance of the LTC3882-1 package (θ_{JA}) is 33°C/W, provided the exposed pad is in good thermal contact with the PCB. The actual thermal resistance in the application will depend on forced air cooling and other heat sinking means, especially the amount of copper on the PCB to which the LTC3882-1 is attached. The following formula may be used to estimate the maximum average power dissipation P_D (in watts) of the LTC3882-1 when V_{CC} is supplied externally.

$$P_D = V_{CC}(0.024 + f_{PWM} \bullet 1.6e\text{-}5 + I_{EXT} + I_{RC25})$$

where:

I_{EXT} = total external load drawn from V_{DD33}, including local pull-up resistors, in amps

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I_{RC25} = total current drawn from V_{DD25} by LTC3882-1 configuration resistor dividers, in amps

and the $_{PWM}$ frequency f_{PWM} is given in kHz

If an external source supplies V_{DD33} directly, the following formula may be used to estimate the maximum average power dissipation P_D (in watts) of the LTC3882-1

$$P_D = V_{DD33}(0.024 + f_{PWM} \bullet 1.6e\text{-}5 + I_{RC25})$$

The maximum junction temperature of the LTC3882-1 in °C may then be found from the following equation

$$T_J = T_A + 33 \bullet P_D$$

with ambient temperature T_A expressed in °C

Derating EEPROM Retention at Temperature

EEPROM read operations between 85°C and 125°C will not affect data storage. But retention will be degraded if the EEPROM is written above 85°C or stored above 125°C. If an occasional fault log is generated above 85°C, the slight reduction in data retention in the EEPROM fault log area will not affect the use of the function or other EEPROM storage. See the Operation section for other high temperature EEPROM functional details. Degradation in data can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273} - \frac{1}{T_{STRESS}+273}\right)\right]}$$

Where:

AF = acceleration factor

Ea = activation energy = 1.4eV

$k = 8.617 \bullet 10^{-5}$ eV/°K

T_{USE} = is the specified junction temperature

T_{STRESS} = actual junction temperature in °C

As an example, if the device is stored at 130°C for 10 hours,

T_{STRESS} = 130°C, and

$$AF = e^{\left[\left(\frac{1.4}{8.617\bullet10^{-5}}\right)\bullet\left(\frac{1}{398} - \frac{1}{403}\right)\right]} = 1.66$$

indicating the effect is the same as operating the device at 125°C for 10 • 1.66 = 16.6 hours, resulting in a retention derating of 6.6 hours.

Configuring Open-Drain Pins

The LTC3882-1 has the following open-drain pins:

3.3V Pins

1. PGOOD*n*
2. $\overline{\text{FAULT}}$*n*
2. SYNC
3. SHARE_CLK

5V-Capable Pins

(These pins operate correctly when pulled to 3.3V.)

1. RUN*n*
2. $\overline{\text{ALERT}}$
3. SCL
4. SDA

All of the above pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low-state threshold on these pins provides ample noise margin exists with 3mA of current. For 3.3V pins, 3mA of current is produced by a 1.1k pull-up resistor. Unless there are transient speed issues associated with the RC time constant of the net, a 10k resistor or larger is generally recommended.

The pull-up resistor for PGOOD should be terminated to the LTC3882-1 V_{DD33} pin or a separate bias supply under 3.6V that is up before the LTC3882-1 is enabled. Otherwise, power-not-good may be falsely indicated after the PWM outputs are running.

The SYNC pin has an on-chip pull-down transistor with the output held low for nominally 250ns when driven by the LTC3882-1. If the internal oscillator is set for 500kHz and the load is 100pF with a 1/3 rise time required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 250ns}{3 \bullet 100pF} = 5.83k$$

The closest 1% resistor is 5.76k.

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If timing errors are occurring or if the SYNC amplitude is not as large as required, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. Otherwise reduce the pull-up resistor sufficiently to assure proper operation.

The SHARE_CLK output has a nominal period of 10µs and is pulled low for about 1µs. If the system load on this shared line is 100pF, the resistor calculation for this line with a 1/3 rise time is:

$$R_{PULLUP} = \frac{9\mu s}{3 \bullet 100pF} = 30k$$

The closest 1% resistor is 30.1k.

For high speed signals such as SDA, SCL and SYNC, a lower value resistor may be required. The RC time constant should be set to 1/3 to 1/5 the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the resistor pull-up on the SDA and SCL pins with the time constant set to 1/3 the rise time equals

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k$$

The closest 1% resistor value is 1k.

Be careful to minimize parasitic capacitance on the SDA and SCL lines to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is one time constant.

PMBus Communication and Command Processing

The LTC3882-1 has a one deep buffer to hold the last data written for each supported command prior to processing, as shown in Figure 45. Two distinct parallel sections of the LTC3882-1 manage command buffering and command processing to ensure the last data written to any command is never lost. When the part receives a new command from the bus, command data buffering copies the data into the write command data buffer and indicates to the internal processor that data for that command should be handled. The internal processor runs in parallel and performs the sometimes slower task of fetching, converting (to internal format) and executing commands so marked for processing.

Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and a new command(s) arrives, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process with bit 5 of MFR_COMMON (LTC3882-1 Calculations Not Pending). When the internal processor is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 46, which ensures that commands are processed in order while simplifying error handling routines. MFR_COMMON always returns valid data at PMBus speeds between 10kHz and 400kHz.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and ALERT notification, or stretch the SCL clock low. For more information refer to PMBus Specification V1.2, Part II, Section 10.8.7 and SMBus V2.0 section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL_LTC3882-1. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

PMBus protocols for busy devices are well accepted

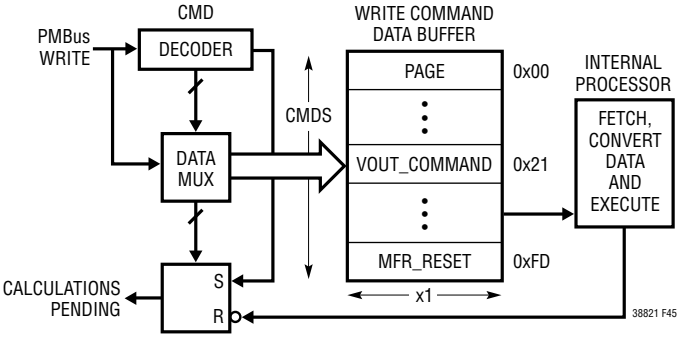


Figure 45. Write Command Data Processing

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standards but can make writing system level software somewhat complex. The part provides three handshaking status bits which reduce this complexity while enabling robust system level communication. The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it

```
// wait until bits 6, 5, and 4 of MFR_COMMON are all set
do
{
        mfrCommonValue = PMBUS_READ_BYTE(0xEF);
        partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)

// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

Figure 46. Example of a Polling Loop to Write VOUT_COMMAND

will clear bit 6 of MFR_COMMON (LTC3882-1 Not BUSY). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON (LTC3882-1 Calculations Not Pending). When the part is busy specifically because it is transitioning V_{OUT} (margining, off/on, moving to a new VOUT_COMMAND, etc.) it will clear bit 4 of MFR_COMMON (LTC3882-1 Output Not In Transition). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following all these status bits being set will be accepted without a NACK, BUSY fault or ALERT notification. The part can NACK commands for other reasons, however, as required by the PMBus specification (e.g., an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 46.

It is recommended that all command writes be preceded with such a polling loop to avoid the extra complexity of dealing with busy behavior or unwanted ALERT notifications. A simple way to achieve this is to embed the polling in subroutines to write command bytes and words. This polling mechanism will allow system software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases please refer to the application note section located at www.linear.com/designtools/app_notes.

When communicating using bus speeds at or below 100kHz, the polling mechanism previously shown provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be enabled to use clock stretching, requiring a PMBus master that supports that function. Clock stretching does not allow the LTC3882-1 to communicate reliably on busses operating above 400kHz. Operating the LTC3882-1 with PMBus SCL rates above 400kHz is not recommended. System software that detects and properly recovers from the standard PMBus NACK responses or BUSY faults described in PMBus Specification V1.2, Part II, Section 10.8.7 is required to communicate above 100kHz without clock stretching.

Refer to Application Note 135 for techniques that may also apply to implement a robust PMBus interface to the LTC3882-1.

Status and Fault Log Management

Due to internal operation, very infrequently the LS byte of STATUS_WORD may be inconsistent with the state of bits in the MS byte. This condition is quite transient and can normally be resolved by simply re-reading STATUS_WORD.

If power is lost during an internal store of a fault log to EEPROM, a partial write of the log can result. In this situation, the LTC3882-1 will not indicate that a fault log is present the next time adequate supply voltage is applied (bit 3 of STATUS_MFR_SPECIFIC). The existence of a partial fault log can be detected by examining the header of the log (MFR_FAULT_LOG). If the first two words of the Fault Log Preface contain valid data as specified by Table 2, and STATUS_MFR_SPECIFIC does not indicate the presence of a complete fault log, then a partial log existed in EEPROM at boot and has been retrieved to RAM. The only way to then determine how much of the log is actually valid is by subjective evaluation of the contents of each log event record. MFR_FAULT_LOG_CLEAR will permanently erase a partial fault log, allowing a subsequent log to be written. It is a good practice to always check for a partial fault log at power-up if fault logging is enabled (bit 7 of MFR_CONFIG_ALL_LTC3882-1).

LTpowerPlay – An Interactive Digital Power GUI

LTpowerPlay is a powerful Windows-based development

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environment that supports Linear Technology Power System Management ICs, including the LTC3882-1. LTpowerPlay can be used to evaluate LTC products by connecting to a Linear Technology demo circuit or user application. LTpowerPlay can also be used offline (no hardware present) to build multiple IC configuration files that can be saved and later reloaded. LTpowerPlay uses the DC1613 USB-to-I^{2}C/SMBus/PMBus controller to communicate with a system for evaluation, development or debug. The software also features automatic update to remain up-to-date with the latest device drivers and documentation available from Linear Technology. A great deal of context sensitive help is available within LTpowerPlay, along with several tutorials. Complete information is available here.

. Interfacing to the DC1613

The LTC DC1613 USB-to-I^{2}C/SMBus/PMBus controller can be interfaced to the LTC3882-1 on any board for programming, telemetry and system debug. This includes the DC1936 from Linear Technology, or any customer target system. The controller, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status registers and the fault log. The final configuration can be quickly developed and stored to the LTC3882-1 EEPROM and/or LTpowerPlay configuration file.

The DC1613 can communicate with, program and even power one or more LTC3882-1s, regardless of whether system supplies are up. The DC2086 Powered Programming Adapter can be used to extend the power sourcing capability of the DC1613. Figure 47 illustrates an application schematic for in-system programming of multiple LTC3882-1s normally powered from a V_{CC} system supply (5V to 12V). If V_{CC} is applied, the DC1613 will not supply the LTC3882-1s on the board. If the DC2086 is used, PFETs with lower $R_{DS(ON)}$, such as the SiA907EDJT, should be used in place of the TP0101K devices. Figure 48 shows an example when the system normally provides 3.3V directly to the LTC3882-1(s).

If system supplies are not up in either of these circuits, the DC1613 will power the LTC3882-1 V_{DD33} supply, allowing in-circuit configuration or manufacturing customization. These circuits also facilitate remote diagnostics, control and reprogramming of the LTC3882-1 while the host system is fully operational, permitting very flexible in-system debugging.

If the system supply is restored while power is still applied by the DC1613 or DC2086, the LTC3882-1 can often be ready to initiate output soft-start before sufficient supply bias for the power stage has been established. Create additional LTC3882-1 delay with TON_DELAY or use a common system RUN line to control both the LTC3882-1 and its related power stages based on acceptable operating parameters, as shown in Figure 55. The DC1613 I^{2}C connections are opto-isolated from the host PC USB. The DC1613 3.3V current limit is only 100mA, so it should only be used to power one or two LTC3882-1s in-system. Because of this limited current sourcing capability, only the LTC3882-1s, their associated pull-up resistors and the I^{2}C pull-up resistors should be powered from the isolated 3.3V supply provided by the DC1613. Using the DC2086 will enable in-system programming of several tens of LTC3882-1 devices without normal system power applied. Any other device sharing the I^{2}C bus with the LTC3882-1 should not have body diodes between their SDA/SCL pins and their respective logic supply, because this will interfere with bus communication in the absence of system power. Hold the RUN pins low externally to avoid providing power to the load until the part is fully configured.

Design Example

As a design example, consider a 132W 2-phase application such as the one shown in Figure 53, where V_{IN} = 36V, V_{OUT} = 3.3V, and I_{OUT} = 40A. A fully discrete power stage design is employed to allow better optimization given these demanding requirements. Assume that a secondary 5V supply will be available in the system for the LTC3882-1 V_{CC} supply. The necessary local bypassing is then provided for the V_{DD33} (2.2µF) and V_{DD25} (1µF) LDO outputs. These LDO outputs should not be shared with other ICs that might have outputs of the same name, because they have independent, internal control loops. When V_{DD33} is used as the LTC3882-1 supply input, it may be shared

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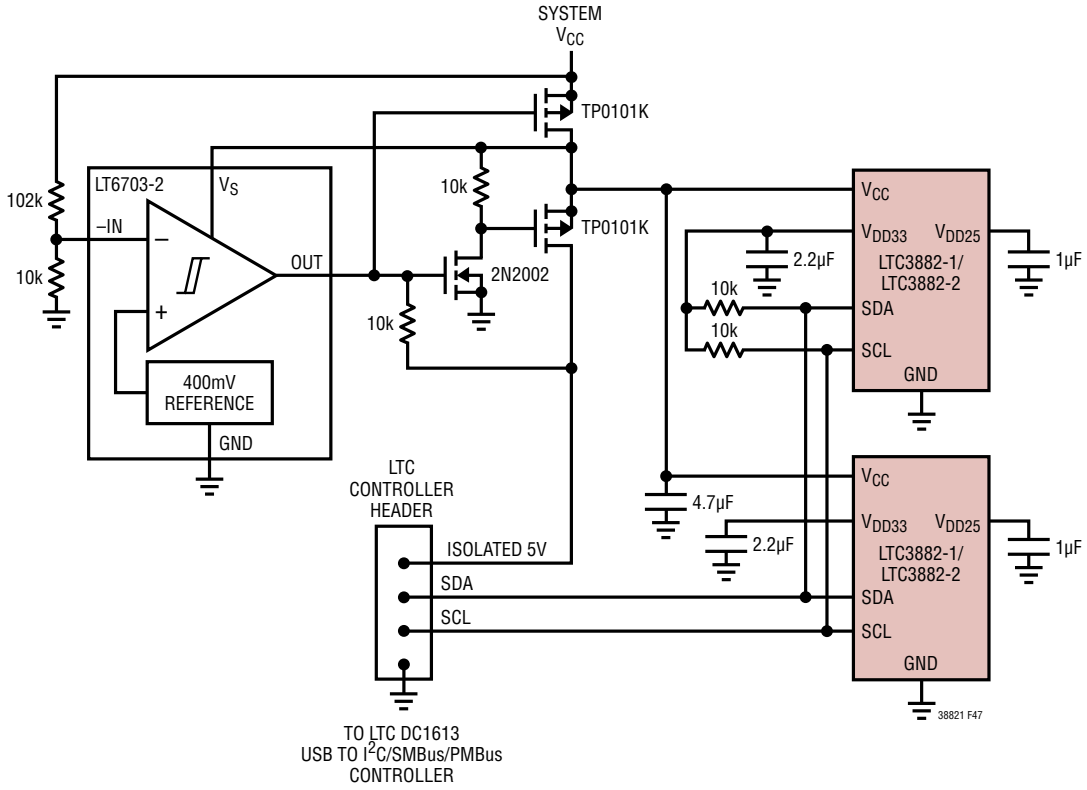


Figure 47. DC1613 Connection (V_{CC} Supply)

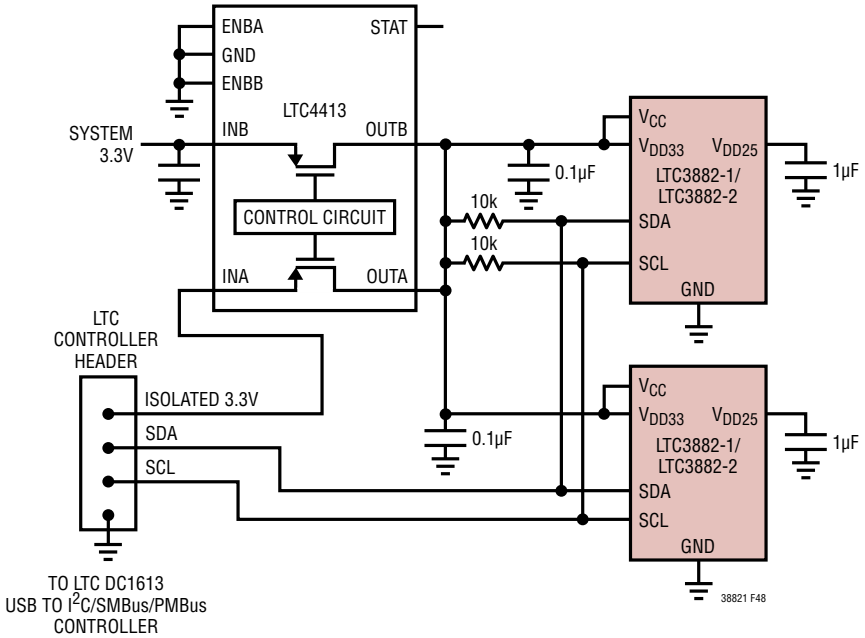


Figure 48. DC1613 Connections (V_{DD33} Supply)

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with other ICs operating from that 3.3V supply. Local HF bypassing of at least 0.1µF is still required on V_{DD33} in this case.

First, the regulated output is established by programming the VOUT_COMMAND stored in EEPROM to 3.3V.

The frequency and phase are also set by EEPROM values. Assume that solution footprint or vertical clearance is an issue, so operating frequency will need to be increased in an effort to minimize inductor value (size). This choice could also result from the need to have above average transient performance, although efficiency may be reduced slightly. FREQUENCY_SWITCH is set to 1.0MHz. As a 2-phase system, MFR_PWM_CONFIG_LTC3882-1 is programmed to 0x14 to put Channel 0 phase at 0° and Channel 1 phase at 180°. This produces the lowest input ripple possible with this configuration and allows this output to synchronize with other rails via SHARE_CLK.

The design will plan on a nominal output ripple of 70% of I_{OUT} to minimize the magnetics volume, and the inductance value is chosen based on this assumption. Each channel supplies an average 20A to the output at full load, resulting in a ripple of $14A_{P-P}$. A 200nH inductor per phase would create this peak-to-peak ripple at 1.0MHz. A Pulse PA0513.22LT 210nH inductor with a DCR of 0.32mΩ typical is selected. Setting IOUT_FAULT_LIMIT to 35A per phase leaves plenty of headroom for transient conditions while still adequately protecting against the rated inductor saturation current of 45A at temperature.

For top and bottom power FETs, the 40V rated Infineon BSC050N04LSG and BSC010N04LS are chosen, respectively. These afford both low $R_{DS(ON)}$ and low gate charge Q_G. Two of each of these could be paralleled to achieve improved efficiency at full load, if desired.

The LTC4449 gate driver is chosen for its fast response (13ns), suitable gate drive, V_{IN} capability (38V) and the ease with which it can be interfaced to the LTC3882-1. Basic three-state control, CCM operation, fast boost refresh, low V_{OUT} range and digital output voltage servo are selected by programming MFR_PWM_MODE_LTC3882-1 to 0xC0 for both channels.

For input filtering, a 47µF SUNCON capacitor and four 22µF ceramic capacitors are selected to provide acceptable AC impedance against the designed converter ripple current. Four 470µF 9mΩ POSCAPs and two 100µF ceramic capacitors are chosen for the output to maintain supply regulation during severe transient conditions and to minimize output voltage ripple.

A loop crossover frequency of 100kHz provides good transient performance while still being well below the switching frequency of the converter. The values of R29, R30 and C25 to C27 were determined to produce a nominal system phase margin of about 65° at this bandwidth.

For the DCR sense filter network, R = 3.09k and C = 220nF are chosen to match the L/DCR time constant of the inductor. PolyPhase connections (I_{AVG}, et al) are shown in the schematic to ensure good output current sharing between the two power stages.

External temperature sense will employ an accurate ΔV_{BE} method, and Q1 and Q2 serve to sense the temperature of L1 and L2, respectively. These components will be located immediately adjacent to their chokes and the 10nF filter capacitors placed with the BJTs.

Resistor configuration is used on the ASEL*n* pins to program PMBus address (MFR_ADDRESS) to 0x4C. Each LTC3882-1 must be configured for a unique address. Using both ASEL*n* pins to accomplish this programming is recommended for simpliest in-system programming. Check the selected address to avoid collision with global addresses other any other specific devices. Identical MFR_RAIL_ADDRESS can be set in EEPROM for both channels to allow single-command control of common rail parameters such as IOUT_OC_FAULT_LIMIT. The LTC3882-1 also responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS and MFR_RAIL_ADDRESS should not be set to either of these values.

PMBus connection (three signals), as well as shared RUN control and fault propagation ($\overline{FAULT}$) are provided. SYNC can be used to synchronize other PWMs to this rail if required.

Pull-ups are provided on all these shared open-drain signals assuming a maximum 100pF line load and PMBus rate of 100kHz. These pins should not be left floating. Termination to 3.3V ensures the absolute maximum ratings for the pins are not exceeded. All other operating parameters such as soft start/stop and desired faults responses are programmed via PMBus command values stored in internal LTC3882-1 EEPROM.

PMBus COMMAND DETAILS (by functional groups)

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PAGE	0x00	Channel (page) presently selected for any paged command.	R/W Byte	N	Reg			0x00
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N				
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W Process	N				
WRITE_PROTECT	0x10	Protect the device against unintended PMBus modifications.	R/W Byte	N	Reg		●	0x00
MFR_ADDRESS	0xE6	Specify right-justified 7-bit device address.	R/W Byte	N	Reg		●	0x4F
MFR_RAIL_ADDRESS	0xFA	Specify unique right-justified 7-bit address for channels comprising a PolyPhase output.	R/W Byte	Y	Reg		●	0x80

Related commands: MFR_COMMON.

PAGE

The PAGE command provides the ability to configure, control and monitor both PWM channels through only one physical address, either the MFR_ADDRESS or GLOBAL device address. Each PAGE contains the operating memory for one PWM channel.

Pages 0x00 and 0x01 correspond to Channel 0 and Channel 1, respectively, in this device.

Setting PAGE to 0xFF applies any following paged commands to both outputs. With PAGE set to 0xFF the LTC3882-1 will respond to read commands as if PAGE were set to 0x00 (Channel 0 results).

This command has one data byte.

PAGE_PLUS_WRITE

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command that has two data bytes is shown in Figure 49.

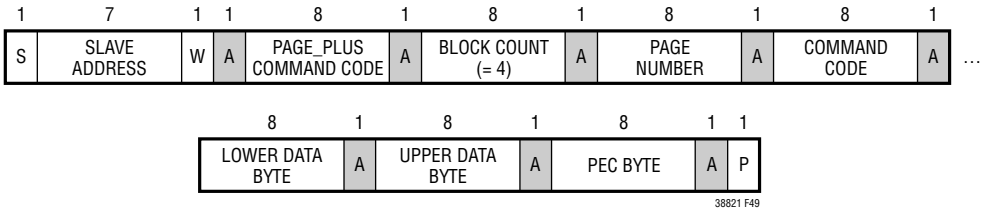


Figure 49. Example of PAGE_PLUS_WRITE

PMBus COMMAND DETAILS (Addressing and Write Protect)

PAGE_PLUS_READ

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command and then read the data returned by the command, all in one communication packet .

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses Block Write – Block Read Process Call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 50.

NOTE: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTC3882-1 will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

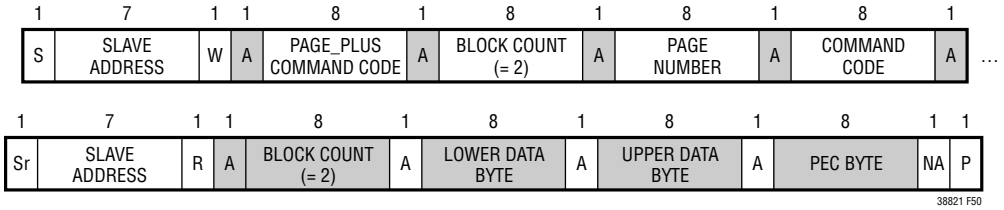


Figure 50. Example of PAGE_PLUS_READ

WRITE_PROTECT

The WRITE_PROTECT command is used to control PMBus write access to the LTC3882-1.

Supported Values:

VALUE	MEANING
0x80	Disable all writes except WRITE_PROTECT, PAGE, STORE_USER_ALL and MFR_EE_UNLOCK commands.
0x40	Disable all writes except WRITE_PROTECT, PAGE, STORE_USER_ALL, MFR_EE_UNLOCK, OPERATION, CLEAR_PEAKS and CLEAR_FAULTS commands. Individual faults can also be cleared by writing a 1 to the respective status bit.
0x20	Disable all writes except WRITE_PROTECT, PAGE, STORE_USER_ALL, MFR_EE_UNLOCK, OPERATION, CLEAR_PEAKS, CLEAR_FAULTS, ON_OFF_CONFIG and VOUT_COMMAND commands. Individual faults can be cleared by writing a 1 to the respective status bit.
0x00	Enables writes to all commands.

This command has one data byte.

PMBus COMMAND DETAILS (Addressing and Write Protect)

MFR_ADDRESS

The MFR_ADDRESS command sets the seven bits of the PMBus device address for this unit (right justified).

Setting this command to a value of 0x80 disables device-level addressing. The GLOBAL device addresses 0x5A and 0x5B cannot be disabled. The LTC3882-1 always responds at these addresses. Even if bit 6 of MFR_CONFIG_ALL_LTC3882-1 is set to ignore the device resistor configuration pins, any valid address, or portion of an address, specified with external resistors on ASEL0 or ASEL1 is applied. If both of these pins are open, the device address is determined strictly by the MFR_ADDRESS value stored in EEPROM. Refer to the Operation section on Resistor Configuration Pins for additional details.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command sets a direct 7-bit PMBus address (right justified) for the active channel(s) as determined by the PAGE command. This address should be common to all channels attached to a single power supply rail. Setting this command to a value of 0x80 disables rail device addressing for the selected channel. Only command writes should be made to the rail address. If a read is performed from this address, a CML fault may result.

This command has one data byte.

GENERAL DEVICE CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PMBUS_REVISION	0x98	Supported PMBus version.	R Byte	Y	Reg			0x22 V1.2
CAPABILITY	0x19	Summary of supported optional PMBus features.	R Byte	N	Reg			0xB0
MFR_CONFIG_ALL_LTC3882-1	0xD1	LTC3882-1 device-level configuration.	R/W Byte	N	Reg		●	0x21

PMBUS_REVISION

The PMBUS_REVISION command returns the revision of the PMBus Specification that the device supports. The LTC3882-1 is compliant with PMBus Version 1.2, both Part I and Part II.

This read-only command has one data byte.

CAPABILITY

The CAPABILITY command reports some key LTC3882-1 features to the PMBus host device.

The LTC3882-1 supports packet error checking, 400kHz bus speeds and has an $\overline{\text{ALERT}}$ output.

This read-only command has one data byte.

PMBus COMMAND DETAILS (General Device Configuration)

MFR_CONFIG_ALL_LTC3882-1

The MFR_CONFIG_ALL_LTC3882-1 command provides device-level configuration common to multiple LTC PMBus products.

Bit Definitions:

BIT	MEANING
7	Enable fault logging.
6	Ignore resistor configuration pins. Does not apply to ASEL0 or ASEL1.
5	Disable CML fault for Quick Command message.
4	Disable SYNC output.
3	Enable 255ms PMBus timeout.
2	Require valid PEC for PMBus write.
1	Enable PMBus clock stretching.
0	Execute CLEAR_FAULTS on rising edge of either RUN pin.

If a legal command is received with an invalid PEC, the LTC3882-1 will not execute the command, regardless of the state of bit 2. If clock stretching is enabled, the LTC3882-1 only uses it as required, generally above SCL rates of 100kHz.

This command has one data byte.

ON, OFF AND MARGIN CONTROL

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
ON_OFF_CONFIG	0x02	RUN pin and PMBus on/off command configuration.	R/W Byte	Y	Reg		●	0x1E
OPERATION	0x01	On, off and margin control.	R/W Byte	Y	Reg		●	0x80
MFR_RESET	0xFD	Force full reset without removing power.	Send Byte	N				

ON_OFF_CONFIG

The ON_OFF_CONFIG command specifies the combination of RUN*n* pin input state and PMBus commands needed to turn the PWM channel on and off.

Supported Values:

VALUE	MEANING
0x1F	OPERATION value and RUN*n* pin must both command the device to start/run. Device executes immediate off when commanded off with the RUN pin.
0x1E	OPERATION value and RUN*n* pin must both command the device to start/run. Device uses TOFF_ command values when commanded off.
0x17	RUN*n* pin control with immediate off when commanded off. OPERATION on/off control ignored.
0x16	RUN*n* pin control using TOFF_ command values when commanded off. OPERATION on/off control ignored.

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault and the command will be ignored.

This command has one data byte.

PMBus COMMAND DETAILS (On, Off and Margin Control)

OPERATION

The OPERATION command is used to turn the PWM channel on and off in conjunction with RUN pin hardware control. This command may also be used to move the output voltage to margin levels. V_{OUT} changes commanded by OPERATION margin commands occur at the programmed VOUT_TRANSITION_RATE. The unit stays in the commanded operating state until an OPERATION command or RUN pin voltage instructs the device to change to another state.

Execution of margin commands is delayed until any on-going TON_RISE or TOFF_FALL output sequencing is completed. Margin values are affected by AVP function, if enabled. Margin operations that ignore faults are not supported by the LTC3882-1.

Supported Values:

VALUE	MEANING
0xA8	Margin high.
0x98	Margin low.
0x80	On (V_{OUT} back to nominal even if bit 3 of ON_OFF_CONFIG is not set).
0x40*	Soft off (with sequencing).
0x00*	Immediate off (no sequencing).

*Device does not respond to these commands if bit 3 of ON_OFF_CONFIG is not set.

Programming an unsupported OPERATION value will generate a CML fault and the command will be ignored.

This command has one data byte.

MFR_RESET

This command provides a means to reset the LTC3882-1 from the serial bus. This forces the LTC3882-1 to turn off both PWM channels, load the operating memory from internal EEPROM, clear all faults and then perform a soft-start of both PWM channels, if enabled.

This write-only command has no data bytes.

PMBus COMMAND DETAILS (PWM Configuration)

PWM CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
FREQUENCY_SWITCH	0x33	PWM frequency control.	R/W Word	N	L11	kHz	●	500kHz 0xFBE8
MFR_PWM_CONFIG_LTC3882-1	0xF5	LTC3882-1 PWM configuration common to both channels.	R/W Byte	N	Reg		●	0x14
MFR_CHAN_CONFIG_LTC3882-1	0xD0	LTC3882-1 channel-specific configuration.	R/W Byte	Y	Reg		●	0x1D
MFR_PWM_MODE_LTC3882-1	0xD4	LTC3882-1 channel-specific PWM mode control.	R/W Byte	Y	Reg		●	0xC8

Related commands MFR_TEMP_1_GAIN_ADJUST, MFR_TEMP_1_OFFSET.

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the switching frequency of both LTC3882-1 PWM channels in kilohertz. At most only one IC sharing SYNC should be programmed as clock master. See bit 4 in MFR_CONFIG_ALL_LTC3882-1. FREQUENCY_SWITCH value will determine the free-running frequency of PWM operation if an expected external clock source is not present or the bussed SYNC line becomes stuck due an external fault or conflict. Both PWM channels must be turned off by the RUN*n* pins, OPERATION command, or their combination, to process this command. If this command is sent while either PWM controller is operating, the LTC3882-1 will NACK the command byte, ignore the command and its data, and assert a BUSY fault. A PLL Unlocked status may be reported after changing the value of this command until the new frequency is established. Below is the table of the supported frequencies for the LTC3882-1. The LTC3882-2 supports all frequencies from 250kHz to 2500kHz.

Supported Frequencies LTC3882-1:

VALUE	PWM FREQUENCY (TYPICAL)
0x0A71	1.25MHz
0x03E8	1MHz
0x0384	900kHz
0x02EE	750kHz
0x0258	600kHz
0xFBE8	500kHz
0xFB84	450kHz
0xFB20	400kHz
0xFABC	350kHz
0XFA58	300kHz
0xF3E8	250kHz
0x0000	External SYNC Only

Note: Analog Devices does not recommend using the following PWM frequencies in new designs: 600kHz 750kHz, 900kHz, and 1MHz.

The LTC3882-2 valid range for this command is 250kHz to 2500kHz inclusive.

This command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS (PWM Configuration)

MFR_PWM_CONFIG_LTC3882-1

The MFR_PWM_CONFIG_LTC3882-1 command controls PWM-related clocking for the LTC3882-1. Both PWM channels must be turned off by the RUN*n* pins, OPERATION command, or their combination, to process this command. If this command is sent while either PWM controller is operating, the LTC3882-1 will NACK the command byte, ignore the command and its data, and assert a BUSY fault.

Supported Values:

<table>
<tr><th>BIT</th><th colspan="4">MEANING</th></tr>
<tr><td>7</td><td colspan="4">(Reserved, must write as 0).</td></tr>
<tr><td>6</td><td colspan="4">(Reserved, must write as 0).</td></tr>
<tr><td>5</td><td colspan="4">(Reserved).</td></tr>
<tr><td>4</td><td colspan="4">SHARE_CLK configuration:
0: SHARE_CLK continuously enabled once VINSNS ≥ VIN_ON after initialization.
1: SHARE_CLK always forced low if VINSNS ≤ VIN_OFF, then held low until VINSNS ≥ VIN_ON.</td></tr>
<tr><td>3</td><td colspan="4">(Reserved).</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="2">Value</td><td colspan="2">Phase</td><td rowspan="2">Maximum Duty Cycle</td></tr>
<tr><td>Channel 0</td><td>Channel 1</td></tr>
<tr><td>111b</td><td>135°</td><td>315°</td><td rowspan="4">87.5%</td></tr>
<tr><td>110b</td><td>90°</td><td>270°</td></tr>
<tr><td>101b</td><td>45°</td><td>225°</td></tr>
<tr><td>100b</td><td>0°</td><td>180°</td></tr>
<tr><td>011b</td><td>120°</td><td>300°</td><td rowspan="4">83.3%</td></tr>
<tr><td>010b</td><td>60°</td><td>240°</td></tr>
<tr><td>001b</td><td>0°</td><td>180°</td></tr>
<tr><td>000b</td><td>0°</td><td>120°</td></tr>
</table>

Phase is expressed from the falling edge of SYNC to the falling edge of PWM.

This command has one data byte.

PMBus COMMAND DETAILS (PWM Configuration)

MFR_CHAN_CONFIG_LTC3882-1

The MFR_CHAN_CONFIG_LTC3882-1 command provides per-channel configuration common to multiple LTC PMBus products.

Bit Definitions:

BIT	MEANING
7:5	(Reserved).
4	RUN pin control: 0: When the channel is commanded off, the associated RUN pin is pulsed low for TOFF_DELAY + TOFF_FALL + 136ms (or MFR_RESTART_DELAY, if longer) regardless of the state of bit 3. 1: RUN pin is not pulsed low if channel is commanded off.
3	Short cycle control: 0: No special control. Device attempts to follow on/off commands exactly as issued. 1: Output is immediately disabled if commanded back on while waiting for TOFF_DELAY or TOFF_FALL to expire. A minimum off time of 120ms is then enforced before the channel is turned back on. Additional delay will apply if bit 4 is clear.
2	SHARE_CLK output control: 0: No special control. 1: Output disabled if SHARE_CLK is held low.
1	(Reserved, must write as 0).
0	MFR_RETRY_DELAY control: 0: Output decay to 12.5% of programmed value required for retry after ANY action that turns off the rail. 1: Output decay not required for retry.

This command has one data byte.

PMBus COMMAND DETAILS (PWM Configuration)

MFR_PWM_MODE_LTC3882-1

The MFR_PWM_MODE_LTC3882-1 command sets important PWM controls for each channel. The addressed channel(s) must be turned off by its RUN pin, OPERATION command, or their combination, when this command is issued. Otherwise the LTC3882-1 will NACK the command byte, ignore the command and its data, and assert a BUSY fault.

When bit 5 is cleared, the LTC3882-1 computes temperature in °C from ΔV_{BE} measured by the ADC at the TSNS*n* pin as

$$T = (G \bullet \Delta V_{BE} \bullet q/(K \bullet \ln(16))) - 273.15 + O$$

When bit 5 is set, the LTC3882-1 computes temperature in °C from TSNS*n* voltage measured by the ADC as

$$T = (G \bullet (1.35 - V_{TSNSn} + O)/4.3e\text{-}3) + 25$$

For both equations,

G = MFR_TEMP_1_GAIN $\bullet 2^{-14}$, and

O = MFR_TEMP_1_OFFSET

Supported Values:

BIT	MEANING
7	Output voltage range select: 0: Maximum V_{OUT} = 5.25V. 1: Maximum V_{OUT} = 2.65V.
6*	Enable V_{OUT} servo.
5	External temperature sense: 0: ΔV_{BE} measurement. 1: Direct voltage measurement.
4:3	BOOST refresh width: 11b: 250ns 10b: 125ns 01b: 50ns 00b: 25ns
2	(Reserved).
1	PWM control protocol: 0: 3-State PWM output. 1: 3-State PWM output with no DCM (including soft-start) or hardware ROC response (including OV).
0	PWM mode: 0: Forced continuous inductor current. 1: Discontinuous inductor current.

*This bit is ignored (servo disabled) if MFR_VOUT_AVP for this channel is programmed to a value greater than 0.0%.

This command has one data byte.

PMBus COMMAND DETAILS (Input Voltage and Limits)

INPUT VOLTAGE AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_ON	0x35	Minimum input voltage to begin power conversion.	R/W Word	N	L11	V	●	6.5V 0xCB40
VIN_OFF	0x36	Decreasing input voltage at which power conversion stops.	R/W Word	N	L11	V	●	6.0V 0xCB00
VIN_OV_FAULT_LIMIT	0x55	V_{IN} overvoltage fault limit.	R/W Word	N	L11	V	●	15.5V 0xD3E0
VIN_UV_WARN_LIMIT	0x58	V_{IN} undervoltage warning limit.	R/W Word	N	L11	V	●	6.3V 0xCB26

Related commands: STATUS_INPUT, SMBALERT_MASK, READ_VIN, VIN_OV_FAULT_RESPONSE

VIN_ON

The VIN_ON command sets the input voltage, in volts, required to start power conversion.

This command has two data bytes in Linear_5s_11s format.

VIN_OFF

The VIN_OFF command sets the minimum input voltage, in volts, at which power conversion stops.

This command has two data bytes in Linear_5s_11s format.

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured by the ADC, in volts, that causes an input overvoltage fault.

This command has two data bytes in Linear_5s_11s format.

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of input voltage measured by the ADC that causes an input undervoltage warning. This warning is disabled until the input exceeds the input startup threshold value set by the VIN_ON command and the unit has been enabled. If the VIN_UV_WARN_LIMIT is then exceeded, the device:

- Sets the INPUT Bit in the STATUS_WORD
- Sets the V_{IN} Undervoltage Warning Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

PMBus COMMAND DETAILS (Output Voltage and Limits)

OUTPUT VOLTAGE AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_MODE	0x20	Output voltage format and exponent.	R Byte	Y	Reg			2^{-12} 0x14
VOUT_COMMAND	0x21	Nominal V_{OUT} value.	R/W Word	Y	L16	V	●	1.0V 0x1000
MFR_VOUT_MAX	0xA5	Maximum value of any V_{OUT}-related command.	R Word	Y	L16	V	●	5.6V 0x599A
VOUT_MAX	0x24	Maximum V_{OUT} that can be set by any command, including margin.	R/W Word	Y	L16	V	●	2.75V 0x2C00
MFR_VOUT_AVP	0xD3	Specify V_{OUT} load line.	R/W Word	Y	L11	%	●	0% 0x8000
VOUT_MARGIN_HIGH	0x25	V_{OUT} at high margin, *must be greater than VOUT_COMMAND.*	R/W Word	Y	L16	V	●	1.05V 0x10CD
VOUT_MARGIN_LOW	0x26	V_{OUT} at low margin, *must be less than VOUT_COMMAND.*	R/W Word	Y	L16	V	●	0.95V 0x0F33
VOUT_OV_FAULT_LIMIT	0x40	V_{OUT} overvoltage fault limit.	R/W Word	Y	L16	V	●	1.1V 0x119A
VOUT_OV_WARN_LIMIT	0x42	V_{OUT} overvoltage warning limit.	R/W Word	Y	L16	V	●	1.075V 0x1133
VOUT_UV_WARN_LIMIT	0x43	V_{OUT} undervoltage warning limit.	R/W Word	Y	L16	V	●	0.925V 0x0ECD
VOUT_UV_FAULT_LIMIT	0x44	V_{OUT} undervoltage fault limit.	R/W Word	Y	L16	V	●	0.9V 0x0E66

Related commands: OPERATION, STATUS_WORD, STATUS_VOUT, SMBALERT_MASK, READ_VOUT, MFR_VOUT_PEAK, READ_POUT, VOUT_OV_FAULT_RESPONSE, VOUT_UV_FAULT_RESPONSE

VOUT_MODE

The VOUT_MODE command gives the format used by the LTC3882-1 for output voltage related commands. Only Linear Mode is supported, with a mantissa expressed in microvolts. Sending the VOUT_MODE command to the LTC3882-1 using a write protocol will result in a CML fault.

This read-only command has one data byte.

VOUT_COMMAND

The VOUT_COMMAND is used to set the output voltage in volts (no load value if AVP is enabled). Execution of this command is delayed until any on-going TON_RISE or TOFF_FALL output sequencing is completed, otherwise the output voltage moves to a new value at VOUT_TRANSITION_RATE.

This command has two data bytes in Linear_16u format.

MFR_VOUT_MAX

The MFR_VOUT_MAX command returns the maximum value, in volts, allowed for any V_{OUT}-related command, including VOUT_OV_FAULT_LIMIT. This value represents the maximum regulated voltage the selected channel could be capable of producing.

This read-only command has two data bytes in Linear_16u format.

PMBus COMMAND DETAILS (Output Voltage and Limits)

VOUT_MAX

The VOUT_MAX command sets an upper limit, in volts, on the allowed value of any command that sets the output voltage, including VOUT_MARGIN_HIGH. Setting VOUT_MAX to a value greater than MFR_VOUT_MAX will result in a CML fault and VOUT_MAX will be set to the value of MFR_VOUT_MAX. A VOUT_MAX warning may also be generated if VOUT_MAX is set above 5.5V in output range 0 or above 2.75V in range 1. This command ensures that any combination of commands attempting to set V_{OUT} above VOUT_MAX will result in a warning with the output clamped at VOUT_MAX. When a VOUT_MAX warning occurs, the device takes the following actions:

- Sets The Offending Command Value to the Voltage Specified by VOUT_MAX
- Sets the VOUT Bit in the STATUS_WORD
- Sets the VOUT_MAX Warning Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has two data bytes in Linear_16u format.

MFR_VOUT_AVP

The MFR_VOUT_AVP command sets the change in output voltage, in percent, for a full-scale change in output current. MFR_VOUT_AVP can be used for active voltage positioning (AVP) requirements or passive current sharing schemes. The LTC3882-1 interprets the IOUT_OC_WARN_LIMIT value as full-scale current for AVP. If MFR_VOUT_AVP is non-zero, VOUT_COMMAND sets the maximum, no-load output voltage and servo mode for that channel is automatically disabled. Setting MFR_VOUT_AVP to 0.0% automatically disables the AVP function. Refer to the Applications Information section for additional details on range and resolution when using MFR_VOUT_AVP.

This command has two data bytes in Linear_5s_11s format.

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command programs the output voltage, in volts, to be produced when Margin High is set with the OPERATION command (no load value if AVP is enabled). The value must be greater than VOUT_ COMMAND.

This command has two data bytes in Linear_16u format.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command programs the output voltage, in volts, to be produced when Margin Low is set by the OPERATION command (no load value if AVP is enabled). The value must be less than VOUT_COMMAND.

This command has two data bytes in Linear_16u format.

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured by the OV supervisor at the $V_{SENSE}^{\pm}$ pins, in volts, which causes an output overvoltage fault. If VOUT_OV_FAULT_LIMIT is modified while the channel is on, 10ms should be allowed for the new value to take effect. Modifying V_{OUT} during that time can result an erroneous OV fault. The LTC3882-1 sets MFR_COMMON bits[6:5] low while it establishes the new VOUT_OV_FAULT_LIMIT value.

This command has two data bytes in Linear_16u format.

PMBus COMMAND DETAILS (Output Voltage and Limits)

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value, in volts, of the output voltage measured by the ADC at the $V_{SENSE}^{\pm}$ pins that causes an output overvoltage warning. If the VOUT_OV_WARN_LIMIT is exceeded, the device:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the V_{OUT} Overvoltage Warning Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has two data bytes in Linear_16u format.

VOUT_UV_WARN_LIMIT

The VOUT_UV_WARN_LIMIT command sets the value, in volts, of the output voltage measured by the ADC at the $V_{SENSE}^{\pm}$ pins that causes an output undervoltage warning. If the VOUT_UV_WARN_LIMIT is exceeded, the device:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the V_{OUT} Undervoltage Warning Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has two data bytes in Linear_16u format.

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage measured by the UV supervisor at the $V_{SENSE}^{\pm}$ pins, in volts, which causes an output undervoltage fault.

This command has two data bytes in Linear_16u format.

PMBus COMMAND DETAILS (Output Current and Limits)

OUTPUT CURRENT AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_CAL_GAIN	0x38	Ratio of $I_{SENSE}^{\pm}$ voltage to sensed current.	R/W Word	Y	L11	mΩ	●	0.63mΩ 0xB285
MFR_IOUT_CAL_GAIN_TC	0xF6	Output current sense element temperature coefficient.	R/W Word	Y	CF	ppm/°C	●	3900ppm/°C 0x0F3C
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	●	29.75A 0xDBB8
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	●	20.0A 0xDA80

Related commands: STATUS_IOUT, SMBALERT_MASK, READ_IOUT, MFR_IOUT_PEAK, READ_POUT, IOUT_OC_FAULT_RESPONSE, MFR_VOUT_AVP

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the resistance value of the output current sense element in milliohms.

This command has two data bytes in Linear_5s_11s format.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC command sets the temperature coefficient of the output current sense element in ppm/°C. Effective sense resistance, in milliohms, is computed by the LTC3882-1 as

$$R_{SENSE} = IOUT_CAL_GAIN \bullet (1 + 1E\text{-}6 \bullet MFR_IOUT_CAL_GAIN_TC \bullet (READ_TEMPERATURE_1 - 27))$$

This command has two data bytes representing a 2's compliment integer.

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the instantaneous peak output current, in amperes, which will cause the OC supervisor to detect an output overcurrent fault. The LTC3882-1 uses the computed effective sense resistance and the voltage across the $I_{SENSE}^{\pm}$ inputs to determine the output current. The programmed limit voltage is rounded to the nearest 0.4mV in a range from 0.0mV to 80.0mV. Output overcurrent faults are ignored during TON_RISE and TOFF_FALL output sequencing.

This command has two data bytes in Linear_5s_11s format.

IOUT_OC_WARN_LIMIT

The IOUT_OC_WARN_LIMIT command sets the value of the output current measured by the ADC, in amperes, that causes an output overcurrent warning. To provide meaningful responses, this value should be set below IOUT_OC_FAULT_LIMIT minus 1/2 of the maximum anticipated ripple current. If the IOUT_OC_WARN_LIMIT is exceeded, the device:

- Sets the IOUT Bit in the STATUS_WORD
- Sets the I_{OUT} Overcurrent Warning Bit in the STATUS_IOUT Command
- Notifies the Host by Asserting $\overline{ALERT}$, Unless Masked

Output overcurrent warnings are ignored during TON_RISE and TOFF_FALL output sequencing.

This command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS (Output Timing, Delays, and Ramping)

OUTPUT TIMING, DELAYS, AND RAMPING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RESTART_DELAY	0xDC	Minimum time RUN pin is held low by the LTC3882-1.	R/W Word	Y	L11	ms	●	500ms 0xFBE8
TON_DELAY	0x60	Delay from RUN pin or OPERATION on command to TON_RISE ramp start.	R/W Word	Y	L11	ms	●	0.0ms 0x8000
TON_RISE	0x61	Time for V_{OUT} to rise from 0V to VOUT_COMMAND after TON_DELAY.	R/W Word	Y	L11	ms	●	8.0ms 0xD200
TON_MAX_FAULT_LIMIT	0x62	Maximum time for V_{OUT} to rise above VOUT_UV_FAULT_LIMIT after TON_DELAY.	R/W Word	Y	L11	ms	●	10.0ms 0xD280
VOUT_TRANSITION_RATE	0x27	V_{OUT} slew rate for programmed output changes.	R/W Word	Y	L11	V/ms	●	0.25V/ms 0xAA00
TOFF_DELAY	0x64	Delay from RUN pin or OPERATION off command to TOFF_FALL ramp start.	R/W Word	Y	L11	ms	●	0.0ms 0x8000
TOFF_FALL	0x65	Time for V_{OUT} to fall to 0V from VOUT_COMMAND after TOFF_DELAY.	R/W Word	Y	L11	ms	●	8.0ms 0xD200
TOFF_MAX_WARN_LIMIT	0x66	Maximum time for V_{OUT} to decay below 12.5% of VOUT_COMMAND after TOFF_FALL completes.	R/W Word	Y	L11	ms	●	150ms 0xF258

Related commands: MFR_RETRY_DELAY, STATUS_VOUT, SMBALERT_MASK, TON_MAX_FAULT_RESPONSE, MFR_CHAN_CONFIG_LTC3882-1, MFR_PWM_MODE_LTC3882-1

These commands can be used to establish required on/off sequencing for any number of system power supply rails.

MFR_RESTART_DELAY

The MFR_RESTART DELAY command specifies the minimum PWM off time (RUN low) in milliseconds. The LTC3882-1 will actively hold its RUN pin low for this length of time if a falling RUN edge is detected. After this delay, a standard start-up sequence can be initiated. A minimum of TOFF_DELAY + TOFF_FALL + 136ms is recommended for this command value. Valid value range is 136ms to 65.52 seconds. The LTC3882-1 uses a resolution of 16ms for this command and will not produce delays outside of this range.

This command has two data bytes in Linear_5s_11s format.

TON_DELAY

The TON_DELAY command sets the delay, in milliseconds, between a start condition and the beginning of the output voltage rise. Values from 0ms to 83 seconds are considered valid, and the LTC3882-1 will not produce delays outside of this range.

This command has two data bytes in Linear_5s_11s format.

TON_RISE

The TON_RISE command sets the desired time, in milliseconds, from the point the output starts to rise until it enters the regulation band. Values from 0 seconds to 1.3 seconds are considered valid, and the LTC3882-1 will not produce rise times outside of this range. Values of TON_RISE less than 0.25ms or resulting slopes greater than 4V/ms will result in an output step to the commanded voltage limited only by PWM analog loop response.

This command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS (Output Timing, Delays and Ramping)

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the maximum time, in milliseconds, the unit is allowed from the beginning of TON_RISE to power up the output without passing VOUT_UV_FAULT_LIMIT. A value of 0ms means there is no limit and the unit can attempt to bring up the output voltage indefinitely. The maximum allowed TON_MAX is 8 seconds.

This command has two data bytes in Linear_5s_11s format.

VOUT_TRANSITION_RATE

The VOUT_TRANSITION_RATE command sets the rate at which the output voltage changes, in volts per millisecond (or mV/µs), in response to a VOUT_COMMAND or OPERATION (margin) command. This rate of change does not apply to operations that fully turn the PWM channel on or off. Values from 1mV/ms to 4V/ms are considered valid. The LTC3882-1 will not produce V_{OUT} transitions slower than 1mV/ms, and values exceeding 4V/ms cause the device to transition the output as quickly as possible, limited only by PWM analog loop response.

This command has two data bytes in Linear_5s_11s format.

TOFF_DELAY

The TOFF_DELAY command sets the delay, in milliseconds, between a stop condition and the beginning of the output voltage fall. Values from 0s to 16s are considered valid.

This command has two data bytes in Linear_5s_11s format.

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of TOFF_DELAY until the output voltage is commanded fully to zero. The part attempts to linearly reduce the commanded output voltage to zero during TOFF_FALL. At the end of this period, the PWM output is disabled.

The part will maintain its programmed PWM operating mode during TOFF_FALL. Using continuous conduction mode will produce a well defined V_{OUT} ramp off but may result in negative output current. The minimum supported fall time is 0.25ms, or any value that results in a rate of fall exceeding 4V/ms. Programmed values less than this will result in a commanded 0.25ms ramp, possibly limited by PWM analog loop response. Maximum fall time is 1.3 seconds.

In discontinuous conduction mode, the controller will not be able to draw current from the load and fall time will be set by output capacitance and load current.

This command has two data bytes in Linear_5s_11s format.

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the time, in milliseconds, the unit is allotted to have the output off after TOFF_FALL completes before a warning is issued. The output is considered off when V_{OUT} is less than 12.5% of the VOUT_COMMAND value.

A data value of 0ms means there is no limit and the unit can attempt to turn the output off indefinitely. There is also no limit enforced if bit 0 of MFR_CHAN_CONFIG_LTC3882-1 is set.

This command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS (External Temperature and Limits)

EXTERNAL TEMPERATURE AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_TEMP_1_GAIN	0xF8	Set slope for external temperature calculations.	R/W Word	Y	CF		●	1.0 0x4000
MFR_TEMP_1_OFFSET	0xF9	Offset addend for external temperature calculations.	R/W Word	Y	L11	°C or V	●	0.0 0x8000
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	°C	●	100.0°C 0xEB20
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	°C	●	85.0°C 0xEAA8
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	°C	●	–40.0°C 0xE580

Related commands: STATUS_TEMPERATURE, SMBALERT_MASK, MFR_TEMPERATURE1_PEAK, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE, STATUS_MFR_SPECIFIC, READ_TEMPERATURE_2, MFR_OT_FAULT_RESPONSE, MFR_PWM_MODE_LTC3882-1

MFR_TEMP_1_GAIN

The MFR_TEMP_1_GAIN command sets the slope used in the calculation of external temperature to account for non-idealities in the element and remote sensing errors, if any. Refer to the MFR_PWM_MODE_LTC3882-1 command for equation details.

This command has two data bytes representing a 2's complement integer.

MFR_TEMP_1_OFFSET

The MFR_TEMP_1_OFFSET command sets the offset used in the calculation of external temperature to account for non-idealities in the element and remote sensing errors, if any. The unit of measure for MFR_TEMP1_OFFSET depends on bit 5 of MFR_PWM_MODE. MFR_TEMP1_ OFFSET is expressed volts if this bit is set and in °C otherwise. Refer to the MFR_PWM_MODE_ LTC3882-1 command for equation details.

This command has two data bytes in Linear_5s_11s format.

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of sensed external temperature, in degrees Celsius, which causes an overtemperature fault.

This command has two data bytes in Linear_5s_11s format.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of sensed external temperature, in degrees Celsius, which causes an overtemperature warning. If the OT_WARN_LIMIT is exceeded, the device:

- Sets the TEMPERATURE Bit in the STATUS_BYTE
- Sets the Overtemperature Warning Bit in the STATUS_TEMPERATURE Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS (External Temperature Limits)

UT_FAULT_LIMIT

The UT_FAULT_LIMIT command sets the value of sensed external temperature, in degrees Celsius, which causes an undertemperature fault.

This command has two data bytes in Linear_5s_11s format.

STATUS REPORTING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
STATUS_BYTE	0x78	One-byte channel status summary.	R/W Byte	Y	Reg			
STATUS_WORD	0x79	Two-byte channel status summary.	R/W Word	Y	Reg			
STATUS_VOUT	0x7A	V_{OUT} fault and warning status.	R/W Byte	Y	Reg			
STATUS_IOUT	0x7B	I_{OUT} fault and warning status.	R/W Byte	Y	Reg			
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status.	R/W Byte	Y	Reg			
STATUS_CML	0x7E	Communication, memory and logic fault and warning status.	R/W Byte	N	Reg			
STATUS_MFR_SPECIFIC	0x80	LTC3882-1-specific status.	R/W Byte	Y	Reg			
MFR_PADS_LTC3882-1	0xE5	State of selected LTC3882-1 pads.	R Word	N	Reg			
MFR_COMMON	0xEF	LTC-generic device status reporting.	R Byte	N	Reg			
CLEAR_FAULTS	0x03	Clear all set fault bits.	Send Byte	N				
MFR_INFO	0xB6	Manufacturer Specific Information	R Word	N	Reg			

Refer to Figure 2 for a graphical depiction of these register contents and their relationships.

STATUS_BYTE

The STATUS_BYTE command returns a one-byte summary of the most critical faults.

STATUS_BYTE Message Contents:

BIT	STATUS BIT NAME	MEANING
7*	BUSY	A fault was declared because the LTC3882-1 was unable to respond.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	VIN_UV	Not supported (LTC3882-1 returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0*	NONE OF THE ABOVE	A fault Not listed in bits[7:1] has occurred.

*$\overline{\text{ALERT}}$ can be asserted if either of these bits is set. They may be cleared by writing a 1 to their bit position in the STATUS_BYTE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

PMBus COMMAND DETAILS (Status Reporting)

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

STATUS_WORD High Byte Message Contents:

BIT	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current fault or warning has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LTC3882-1 has occurred.
11	POWER_GOOD#	The POWER_GOOD state is false if this bit is set.
10	FANS	Not supported (LTC3882-1 returns 0).
9	OTHER	Not supported (LTC3882-1 returns 0).
8	UNKNOWN	Not supported (LTC3882-1 returns 0).

This command has two data bytes.

STATUS_VOUT

The STATUS_VOUT command returns one byte of V_{OUT} status information.

STATUS_VOUT Message Contents:

BIT	MEANING
7	V_{OUT} overvoltage fault.
6	V_{OUT} overvoltage warning.
5	V_{OUT} undervoltage warning.
4	V_{OUT} undervoltage fault.
3	VOUT_MAX warning.
2	TON_MAX fault.
1	TOFF_MAX warning.
0	Not supported by the LTC3882-1 (returns 0).

$\overline{\text{ALERT}}$ can be asserted if any of bits[7:1] are set. These may be cleared by writing a 1 to their bit position in STATUS_VOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT command returns one byte of I_{OUT} status information.

STATUS_IOUT Message Contents:

BIT	MEANING
7	I_{OUT} overcurrent fault.
6	Not supported (LTC3882-1 returns 0).
5	I_{OUT} overcurrent warning.
4:0	Not supported (LTC3882-1 returns 0).

$\overline{\text{ALERT}}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_IOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

PMBus COMMAND DETAILS (Status Reporting)

STATUS_INPUT

The STATUS_INPUT command returns one byte of V_{IN} (VINSNS) status information.

STATUS_INPUT Message Contents:

BIT	MEANING
7	V_{IN} overvoltage fault.
6	Not supported (LTC3882-1 returns 0).
5	V_{IN} undervoltage warning.
4	Not supported (LTC3882-1 returns 0).
3	Unit off for insufficient V_{IN}.
2:0	Not supported (LTC3882-1 returns 0).

$\overline{ALERT}$ can be asserted if bit 7 is set. Bit 7 may be cleared by writing it to a 1, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one byte of sensed external temperature status information.

STATUS_TEMPERATURE Message Contents:

BIT	MEANING
7	External overtemperature fault.
6	External overtemperature warning.
5	Not supported (LTC3882-1 returns 0).
4	External undertemperature fault.
3:0	Not supported (LTC3882-1 returns 0).

$\overline{ALERT}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_TEMPERATURE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_CML

The STATUS_CML command returns one byte of status information on received commands, internal memory and logic.

STATUS_CML Message Contents:

BIT	MEANING
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	Packet error check failed.
4	Memory fault detected.
3	Processor fault detected.
2	Reserved (LTC3882-1 returns 0).
1	Other communication fault.
0	Other memory or logic fault.

$\overline{ALERT}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_CML, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

PMBus COMMAND DETAILS (Status Reporting)

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns one byte with LTC3882-1-specific status information.

STATUS_MFR_SPECIFIC Message Contents:

BIT	MEANING
7	Internal temperature fault (>160°C).
6	Internal temperature warning (>130°C).
5	EEPROM CRC error.
4	Internal PLL unlocked.
3	Fault log present.
2	Not supported (LTC3882-1 returns 0).
1	Output short cycled.
0	$\overline{\text{FAULT}}$ low.

If any supported bits are set, the MFR bit in the STATUS_WORD will be set and $\overline{\text{ALERT}}$ may be asserted. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_MFR_SPECIFIC, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

MFR_PADS_LTC3882-1

The MFR_PADS_LTC3882-1 command provides status of the LTC3882-1 digital I/O and control pins, in addition to general output voltage conditions.

MFR_PADS_LTC3882-1 Message Contents:

BIT	MEANING
15	Channel 1 is a slave.
14	Channel 0 is a slave.
13:12	Not supported (LTC3882-1 returns 0).
11	ADC results for I_{OUT} may be invalid.
10	SYNC output disabled externally.
9	Channel 1 POWER_GOOD (normally returns 1 if slave).
8	Channel 0 POWER_GOOD (normally returns 1 if slave).
7	LTC3882-1 forcing RUN1 low.
6	LTC3882-1 forcing RUN0 low.
5	RUN1 pin state.
4	RUN0 pin state.
3	LTC3882-1 forcing $\overline{\text{FAULT1}}$ low.
2	LTC3882-1 forcing $\overline{\text{FAULT0}}$ low.
1	$\overline{\text{FAULT1}}$ pin state.
0	$\overline{\text{FAULT0}}$ pin state.

This read-only command has two data bytes.

PMBus COMMAND DETAILS (Status Reporting)

MFR_COMMON

The MFR_COMMON command contains status bits that are common to multiple LTC PMBus products.

MFR_COMMON Message Contents:

BIT	MEANING
7	LTC3882-1 not forcing $\overline{\text{ALERT}}$ low.
6	LTC3882-1 not BUSY.
5	LTC3882-1 calculations not pending.
4	LTC3882-1 output not in transition.
3	LTC3882-1 EEPROM initialized.
2	Not supported (LTC3882-1 returns 0).
1	SHARE_CLK timeout.
0	Not supported (LTC3882-1 returns 0).

This read-only command has one data byte.

MFR_INFO

The MFR_INFO command contains additional status bits that are LTC3882-1-specific and may be common to multiple LTC PSM products.

MFR_INFO Data Contents:

BIT	MEANING
15:6	Reserved.
5	EEPROM ECC status. 0: Corrections have been made in the EEPROM user space. 1: No corrections have been made in the EEPROM user space.
4:0	Reserved

EEPROM ECC status is updated after each RESTORE_USER_ALL or RESET command, a power-on reset or an EEPROM bulk read operation. This read-only command has two data bytes.

CLEAR_FAULTS

The CLEAR_FAULTS command clears any fault bits that have been set and deasserts (releases) the $\overline{\text{ALERT}}$ pin. This command clears all bits in all status commands simultaneously.

CLEAR_FAULTS does not cause a channel that has latched off for a fault condition to restart. Channels that are latched off for a fault condition are restarted when the output is commanded to turn off and then on through the OPERATION command or RUN pins, or IC supply power is cycled.

If a fault is still present when CLEAR_FAULTS is commanded, that fault bit will immediately be set and $\overline{\text{ALERT}}$ again asserted low.

This write-only command has no data bytes.

PMBus COMMAND DETAILS (Status Reporting)

TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
READ_VIN	0x88	Measured V_{IN}.	R Word	N	L11	V		
MFR_VIN_PEAK	0xDE	Maximum V_{IN} measurement since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		
READ_VOUT	0x8B	Measured V_{OUT}.	R Word	Y	L16	V		
MFR_VOUT_PEAK	0xDD	Maximum V_{OUT} measurement since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		
READ_IOUT	0x8C	Measured I_{OUT}.	R Word	Y	L11	A		
MFR_IOUT_PEAK	0xD7	Maximum I_{OUT} measurement since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		
READ_TEMPERATURE_1	0x8D	Measured external temperature.	R Word	Y	L11	°C		
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum external temperature measurement since last MFR_CLEAR_PEAKS.	R Word	Y	L11	°C		
READ_TEMPERATURE_2	0x8E	Measured internal temperature.	R Word	N	L11	°C		
MFR_TEMPERATURE_2_PEAK	0xF4	Maximum internal temperature measurement since last MFR_CLEAR_PEAKS.	R Word	N	L11	°C		
READ_DUTY_CYCLE	0x94	Measured commanded PWM duty cycle.	R Word	Y	L11	%		
READ_FREQUENCY	0x95	Measured PWM input clock frequency.	R Word	Y	L11	kHz		
MFR_CLEAR_PEAKS	0xE3	Clear all peak values.	Send Byte	N				

Related commands: IOUT_CAL_GAIN, MFR_IOUT_CAL_GAIN_TC, MFR_PWM_MODE_LTC3882-1

READ_VIN

The READ_VIN command returns the input voltage measured between VINSNS and GND in volts.

This read-only command has two data bytes in Linear_5s_11s format.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, measured for READ_VIN. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

READ_VOUT

The READ_VOUT command returns the output voltage measured at the $V_{SENSE}^{\pm}$ pins in volts.

This read-only command has two data bytes in Linear_16u format.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, measured for READ_VOUT. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_16u format.

PMBus COMMAND DETAILS (Telemetry)

READ_IOUT

The READ_IOUT command returns the output current in amperes. This value is computed from:

- The differential voltage measured across the $I_{SENSE}^{\pm}$ pins
- The IOUT_CAL_GAIN value
- The MFR_IOUT_CAL_GAIN_TC value
- The READ_TEMPERATURE_1 value
- The MFR_TEMP_1_GAIN value
- The MFR_TEMP_1_OFFSET value

This read-only command has two data bytes in Linear_5s_11s format.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, calculated for READ_IOUT. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

READ_POUT

The READ_POUT command reports the output power in watts. The value is calculated from the product of the most recent correlated output voltage and current readings.

This read-only command has two data bytes in Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the external sense element.

This read-only command has two data bytes in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, calculated for READ_TEMPERATURE_1. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the LTC3882-1 internal temperature in degrees Celsius.

This read-only command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS (Telemetry)

MFR_TEMPERATURE_2_PEAK

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, calculated for READ_TEMPERATURE_2. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

READ_DUTY_CYCLE

The READ_DUTY_CYCLE command returns the duty cycle of the PWM control in percent. This will not be the exact duty cycle of the PWM switch node due to efficiency losses in the power stage and current consumption of the LTC3882-1 itself.

This read-only command has two data bytes in Linear_5s_11s format.

READ_FREQUENCY

The READ_FREQUENCY command returns the switching frequency supplied to the internal PLL in kilohertz, whether derived internally or provided by external clock on the SYNC pin. This may not be the actual PWM output switching frequency during certain exception processing, such as an output overcurrent condition.

This read-only command has two data bytes in Linear_5s_11s format.

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command resets all stored _PEAK values. The LTC3882-1 determines new peak values after this command is received.

This write-only command has no data bytes.

PMBus COMMAND DETAILS (Fault Response and Communication)

FAULT RESPONSE AND COMMUNICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_RESPONSE	0x56	V_{IN} overvoltage fault response.	R/W Byte	Y	Reg		●	0x80
VOUT_OV_FAULT_RESPONSE	0x41	V_{OUT} overvoltage fault response.	R/W Byte	Y	Reg		●	0xB8
VOUT_UV_FAULT_RESPONSE	0x45	V_{OUT} undervoltage fault response.	R/W Byte	Y	Reg		●	0xB8
IOUT_OC_FAULT_RESPONSE	0x47	Output overcurrent fault response.	R/W Byte	Y	Reg		●	0x00
OT_FAULT_RESPONSE	0x50	External overtemperature fault response.	R/W Byte	Y	Reg		●	0xB8
UT_FAULT_RESPONSE	0x54	External undertemperature fault response.	R/W Byte	Y	Reg		●	0xB8
MFR_OT_FAULT_RESPONSE	0xD6	Internal overtemperature fault response.	R Byte	N	Reg		●	0xC0
TON_MAX_FAULT_RESPONSE	0x63	Fault response when TON_MAX_FAULT_LIMIT is exceeded.	R/W Byte	Y	Reg		●	0xB8
MFR_RETRY_DELAY	0xDB	Minimum time before retry after a fault.	R/W Word	N	L11	ms	●	350ms 0xFABC
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ Activity.	Block R/W	Y	Reg		●	See CMD Details
MFR_FAULT_PROPAGATE_ LTC3882-1	0xD2	Configure status propagation via $\overline{\text{FAULT}}n$ pins.	R/W Word	Y	Reg		●	0x6993
MFR_FAULT_RESPONSE	0xD5	PWM response when $\overline{\text{FAULT}}n$ pin is low.	R/W Byte	Y	Reg		●	0xC0
MFR_FAULT_LOG	0xEE	Read fault log data.	R Block	N	Reg			
MFR_FAULT_LOG_CLEAR	0xEC	Clear existing EEPROM fault log.	Send Byte	N				

Related commands: STATUS_BYTE, STATUS_WORD, MFR_PADS_LTC3882-1, MFR_RESTART_DELAY, MFR_CHAN_CONFIG_LTC3882-1, MFR_FAULT_LOG_STORE, CLEAR_FAULTS

These commands detail programmable device responses for detected faults beyond the hardware-level actions described in the Operations section. LTC3882-1 hardware-level fault responses cannot be modified. Refer to Table 1 to Table 4 for details of fault log contents. PMBus warning event responses are listed under _WARN_LIMIT command details.

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The format for this command is given in Table 13. The device also:

- Sets the INPUT Bit in the STATUS_WORD
- Sets the V_{IN} Overvoltage Fault Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

PMBus COMMAND DETAILS (Fault Response and Communication)

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. The format for this command is given in Table 12. The device also:

- Sets the VOUT_OV Bit in the STATUS_BYTE
- Sets the VOUT Bit in the STATUS_WORD
- Sets the V_{OUT} Overvoltage Fault Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The format for this command is given in Table 12. The device also:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the V_{OUT} Undervoltage Fault Bit in the STATUS_VOUT Command,
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

Table 12. Data Byte Contents for VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
[7:6]	For all values of bits [7:6], the LTC3882-1: • Sets the corresponding fault bits in the status commands. • Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked. The fault, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The corresponding STATUS_VOUT bit is written to a one. • The output is commanded off, then on, by the RUN pin or OPERATION command. • The device receives a RESTORE_USER_ALL command. • The device receives an MFR_RESET command. • IC supply power is cycled.	00	The LTC3882-1 continues to operate indefinitely with the normal hardware response described in the Operation section.
		01	The LTC3882-1 continues operating with the normal hardware response for the delay time specified by bits [2:0]. If the fault is continuously present for the entire delay, the unit then disables the output and does attempt to restart.
		10	The LTC3882-1 immediately disables the output and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
[5:3]	Retry setting.	000-110	The LTC3882-1 does not attempt to restart. The output remains disabled until the fault is cleared, the device is commanded off and then on, or bias power (LTC3882-1 power supply input) is cycled.
		111	The LTC3882-1 attempts to restart continuously without limitation with an interval set by MFR_RETRY_DELAY. This response persists until the unit is commanded off, or bias power is removed, or another fault response forces shutdown without retry.
[2:0]	Delay time.	xxx	Response delay time in 10µs increments. This delay time determines how long the fault may have to persist before the controller is disabled, depending on bits [7:6]. Hardware-level response, if any, will occur during this delay. These bits always return zero if bits [7:6] are not set to 0x2.

PMBus COMMAND DETAILS (Fault Response and Communication)

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The device also:

- Sets the IOUT_OC Bit in the STATUS_BYTE
- Sets the IOUT Bit in the STATUS_WORD
- Sets the I_{OUT} Overcurrent Fault Bit in the STATUS_IOUT Command
- Notifies the Host by Asserting $\overline{ALERT}$

Output overcurrent faults are ignored during TON_RISE and TOFF_FALL output sequencing.

Data Byte Contents for IOUT_OC_FAULT_RESPONSE:

BITS	DESCRIPTION	VALUE	MEANING
[7:6]	For all values of bits [7:6], the LTC3882-1: • Sets the corresponding fault bits in the status commands. • Notifies the host by asserting $\overline{ALERT}$, unless masked. The fault, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The corresponding STATUS_IOUT bit is written to a one. • The output is commanded off, then on, by the RUN pin or OPERATION command. • The device receives a RESTORE_USER_ALL command. • The device receives an MFR_RESET command. • IC supply power is cycled.	0x	The LTC3882-1 continues to operate indefinitely with the normal hardware response described in the Operation section.
		10	The LTC3882-1 continues operating with the normal hardware response for the delay time specified by bits [2:0]. If the fault is continuously present for the entire delay, the unit then disables the output and does not attempt to restart.
		11	The LTC3882-1 shuts down (disables the output) and responds according to the retry setting in bits [5:3].
[5:3]	Retry setting.	000-110	The LTC3882-1 does not attempt to restart. The output remains disabled until the fault is cleared, the device is commanded off and then on, or bias power is cycled.
		111	The LTC3882-1 attempts to restart continuously without limitation with an interval set by MFR_RETRY_DELAY. This response persists until the unit is commanded off, bias power is removed, or another fault response forces shutdown without retry.
[2:0]	Delay time.	xxx	Response delay time in 16ms increments. This delay time determines how long the fault may have to persist before the controller is disabled, depending on bits [7:6]. These bits always return zero if bits [7:6] are not set to 0x2.

Programming an unsupported IOUT_OC_FAULT_RESPONSE value will generate a CML fault and the command will be ignored.

This command has one data byte.

PMBus COMMAND DETAILS (Fault Response and Communication)

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an overtemperature fault. The format for this command is given in Table 13. The device also:

- Sets the TEMPERATURE Bit in the STATUS_BYTE
- Sets the Overtemperature Fault Bit in the STATUS_TEMPERATURE Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

UT_FAULT_RESPONSE

The UT_FAULT_RESPONSE command instructs the device on what action to take in response to an undertemperature fault. The format for this command is given in Table 13. The device also:

- Sets the TEMPERATURE Bit in the STATUS_BYTE
- Sets the Undertemperature Fault Bit in the STATUS_TEMPERATURE Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

MFR_OT_FAULT_RESPONSE

The MFR_OT_FAULT_RESPONSE command instructs the device on what action to take in response to an internal overtemperature fault (150°C to 160°C). The device also:

- Sets the MFR Bit in the STATUS_WORD
- Sets the Overtemperature Fault Bit in the STATUS_MFR_SPECIFIC Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

Supported Values:

VALUE	MEANING
0xC0	The LTC3882-1 disables when the die temperature exceeds 160°C and restarts when the die temperature drops below 150°C.
0x80	

This command is read only.

This command has one data byte.

PMBus COMMAND DETAILS (Fault Response and Communication)

TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The format for this command is given in Table 13. The device also:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the TON_MAX_FAULT Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

Table 13. Data Byte Contents for the Following _FAULT_RESPONSE Commands: VIN_OV, OT, UT and TON_MAX

BITS	DESCRIPTION	VALUE	MEANING
[7:6]	For all values of bits [7:6], the LTC3882-1: • Sets the corresponding fault bits in the status commands. • Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked. The fault, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The corresponding fault bit is written to a one. • The output is commanded off, then on, by the RUN pin or OPERATION command. • The device receives a RESTORE_USER_ALL command. • The device receives an MFR_RESET command. • IC supply power is cycled.	00	The LTC3882-1 continues operating without interruption.
		01	Not supported. Writing this value will generate a CML fault.
		10	The LTC3882-1 shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
[5:3]	Retry setting.	000-110	The LTC3882-1 does not attempt to restart. The output remains disabled until the fault is cleared, the device is commanded off and then on, or bias power is cycled.
		111	The LTC3882-1 attempts to restart continuously without limitation with an interval set by MFR_RETRY_DELAY. This response persists until the unit is commanded off, bias power is removed, or another fault response forces shutdown without retry.
[2:0]	Delay time.	xxx	Not supported. Values ignored.

MFR_RETRY_DELAY

The MFR_RETRY_DELAY command sets the time in milliseconds between restart attempts for all retry fault responses. The actual retry delay may be the longer of MFR_RETRY_DELAY or the time required for the output voltage to decay below 12.5% of its programmed value. Decay qualification can be disabled using the MFR_CHAN_CONFIG_LTC3882-1 command. Retry delay starts once the fault is no longer detected by the LTC3882-1 or its $\overline{\text{FAULT}}$ pin is externally released. Legal values run from 120ms to 32.7 seconds.

This command has two data bytes in Linear_5s_11s format.

SMBALERT_MASK

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from asserting $\overline{\text{ALERT}}$ as they are asserted.

PMBus COMMAND DETAILS (Fault Response and Communication)

Figure 51 shows an example of the Write Word format used to set an $\overline{\text{ALERT}}$ mask, in this case without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ if set.

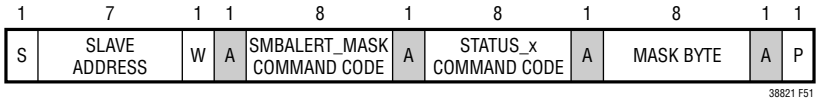


Figure 51. Example of Setting SMBALERT_MASK

Figure 52 shows an example of the Block Write – Block Read Process Call protocol used to read back the present state of any supported status register, again without PEC.

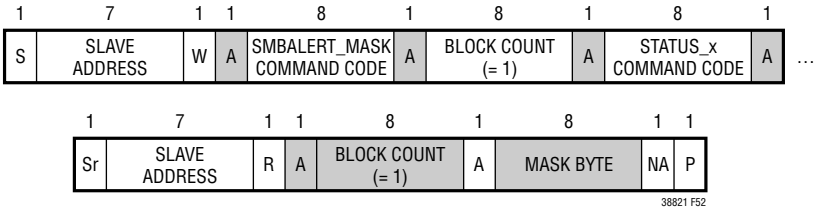


Figure 52. Example of Reading SMBALERT_MASK

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON or MFR_PADS_LTC3882-1. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

SMBALERT_MASK Default Setting: (Refer Also to Figure 2)

STATUS RESISTER	ALERT Mask Value	MASKED BITS
STATUS_VOUT	0x00	None
STATUS_IOUT	0x00	None
STATUS_TEMPERATURE	0x00	None
STATUS_CML	0x00	None
STATUS_INPUT	0x00	None
STATUS_MFR_SPECIFIC	0x11	Bit 4 (internal PLL unlocked), bit 0 ($\overline{\text{FAULT}}$ low)

MFR_FAULT_PROPAGATE_LTC3882-1

The MFR_FAULT_PROPAGATE_LTC3882-1 command determines events that cause $\overline{\text{FAULT}}$ to be asserted. Setting a bit in this register to a one allows the specified condition to assert the $\overline{\text{FAULT}}$ output for that channel. $\overline{\text{FAULT}}$ is not asserted by a fault, even if set to propagate, if that FAULT_RESPONSE is set to Ignore. The state of SMBLALERT_MASK does not affect $\overline{\text{FAULT}}$ propagation.

PMBus COMMAND DETAILS (Fault Response and Communication)

Supported Values:

BIT	PROPAGATED CONDITION
15	Waiting for V_{OUT} decay before restart.
14	V_{OUT} short cycled (automatically deasserted 120ms after V_{OUT} is fully OFF).
13	TON_MAX_FAULT_LIMIT exceeded.
12	(Reserved, must be set to 0).
11	MFR_OT_FAULT_LIMIT exceeded.
10	(Reserved, must be set to 0).
9	(Reserved, must be set to 0).
8	UT_FAULT_LIMIT exceeded.
7	OT_FAULT_LIMIT exceeded.
6	(Reserved).
5	(Reserved).
4	VIN_OV_FAULT_LIMIT exceeded.
3	(Reserved).
2	IOUT_OC_FAULT_LIMIT exceeded.
1	VOUT_UV_FAULT_LIMIT exceeded.
0	VOUT_OV_FAULT_LIMIT exceeded.

This command has two data bytes.

MFR_FAULT_RESPONSE

The MFR_FAULT_RESPONSE command instructs the device on what action to take in response to a $\overline{\text{FAULT}}$ pin being pulled low by anything other than an internal fault.

Supported Values:

VALUE	MEANING
0xC0	Related PWM output is immediately disabled.
0x00	Input ignored, PWM operation continues without interruption.

When a FAULT pin is low, the device also:

- Sets the MFR_SPECIFIC Bit in the STATUS_WORD
- Sets Bit 0 in the STATUS_MFR_SPECIFIC Command to Indicate $\overline{\text{FAULT}}$ Is or Has Been Low
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

PMBus COMMAND DETAILS (Fault Response and Communication)

MFR_FAULT_LOG

The MFR_FAULT_LOG command allows the contents of the fault log to be read. This log is created with a MFR_FAULT_LOG_STORE command or at the first fault occurrence after a CLEAR_FAULTS or MFR_FAULT_LOG_CLEAR command. If a fault occurs within the first second after applying power, some earlier pages in the log may not contain valid data.

This read-only command uses block protocol with 147 bytes of data requiring an estimated data transfer time of 3.4ms at 400kHz. The $t_{TIMEOUT}$ parameter is extended when this command is executed and a fault log is present.

Fault Log Operation

A conceptual diagram of the fault log is shown in Figure 53. The fault log provides telemetry recording capability to the LTC3882-1. During normal operation the contents of the status registers, the output voltage readings, temperature readings as well as peak values of these quantities are stored in a continuously updated buffer in RAM. The operation is similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for nonvolatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced. When reading the fault log from RAM all 6 events of cyclical data remain. However, when the fault log is read from EEPROM (after a reset), the last 2 events are lost. The read length of 147 bytes remains the same, but the fifth and sixth events are a repeat of the fourth event.

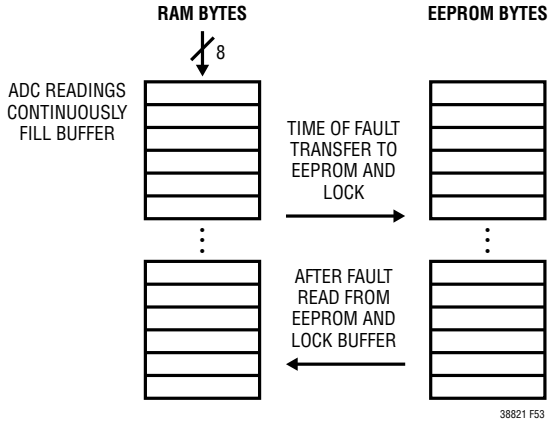


Figure 53. Fault Log Conceptual Diagram

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command erases all stored fault log values. After a clear is issued, up to 8ms may be required to clear related bit 3 in STATUS_MFR_SPECIFIC.

This write-only command has no data bytes.

PMBus COMMAND DETAILS (EEPROM User Access)

EEPROM USER ACCESS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
STORE_USER_ALL	0x15	Store entire operating memory in EEPROM.	Send Byte	N				NA
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA
MFR_COMPARE_USER_ALL	0xF0	Compare operating memory with EEPROM contents.	Send Byte	N				
MFR_FAULT_LOG_STORE	0xEA	Force transfer of fault log from operating memory to EEPROM.	Send Byte	N				
MFR_EE_UNLOCK	0xBD	(contact the factory)						
MFR_EE_ERASE	0xBE	(contact the factory)						
MFR_EE_DATA	0xBF	(contact the factory)						
USER_DATA_00	0xB0	EEPROM word reserved for LTpowerPlay.	R/W Word	N	Reg		●	
USER_DATA_01	0xB1	EEPROM word reserved for LTpowerPlay.	R/W Word	Y	Reg		●	
USER_DATA_02	0xB2	EEPROM word reserved for OEM use.	R/W Word	N	Reg		●	
USER_DATA_03	0xB3	EEPROM word available for general data storage.	R/W Word	Y	Reg		●	0x0000
USER_DATA_04	0xB4	EEPROM word available for general data storage.	R/W Word	N	Reg		●	0x0000

Related commands: MFR_CONFIG_ALL_LTC3882-1

Note that if the LTC3882-1 die temperature exceeds 130°C, execution of any command in the above table except RESTORE_USER_ALL and MFR_FAULT_LOG_STORE will be disabled until the IC temperature drops below 125°C. RESTORE_USER_ALL is executed immediately, and MFR_FAULT_LOG_STORE is executed after the IC temperature drops below 125°C. Refer to Table 4 for details of fault log contents. *Using any command that writes data to the EEPROM is strongly discouraged if bit 6 of STATUS_MFR_ SPECIFIC is set, indicating the internal die temperature is above 85°C. Data retention of 10 years is not guaranteed if the EEPROM is written above a junction temperature of 85°C.*

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the operating memory to internal EEPROM PMBus configuration space.

This write-only command has no data bytes.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the internal EEPROM to matching locations in operating memory. The values in operating memory are overwritten by the values retrieved from EEPROM. Both channels should be turned off prior to issuing this command. The LTC3882-1 ensures both PWM channels are off, loads the operating memory from internal EEPROM, clears all faults, reads the resistor configuration pins, and then performs a soft-start of both PWM channels, if enabled

This write-only command has no data bytes.

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the LTC3882-1 to compare current operating memory (PMBus command values in RAM) with the contents of the internal EEPROM. If the compared memories differ, a CML fault is generated.

This write-only command has no data bytes.

PMBus COMMAND DETAILS (EEPROM User Access)

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces a data log to be written to internal EEPROM as if a fault event had occurred. This command will generate a CML fault if the Enable Fault Logging bit is cleared in MFR_CONFIG_ALL_LTC3882-1.

This write-only command has no data bytes.

MFR_EE_xxxx

The MFR_EE_xxxx commands facilitate bulk programming of the LTC3882-1 internal EEPROM. Contact the factory for details.

USER_DATA_0x

The USER_DATA_0x commands provide uncommitted EEPROM locations that may be applied as system scratchpad space. USER_DATA_00 and USER_DATA_01 should not be modified when using the LTpowerPlay GUI. Some contract manufacturers also reserve use of USER_DATA_02 for their own inventory control.

PMBus COMMAND DETAILS (Unit Identification)

UNIT IDENTIFICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_ID	0x99	Manufacturer identification.	R String	N	ASC			LTC
MFR_MODEL	0x9A	LTC model number.	R String	N	ASC			LTC3882-1 LTC3882-2
MFR_SERIAL	0x9E	Device serial number.	R Block	N	Reg			
IC_DEV_ID (LTC3882-2 only)	0xAD	LTC3882-2 model number	R String	N	ASC			LTC3882-2
IC_DEVICE_REV (LTC3882-2 only)	0xAE	LTC3882-2 device revision code	R String	N	ASC			A4802
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC3882-1	R Word	N	Reg			0x424X(-1) 0x452X(-2)

MFR_ID

The MFR_ID command returns the manufacturer ID of the LTC3882-1 using 8-bit ASCII characters.

This read-only command is in block format.

MFR_MODEL

The MFR_MODEL command returns the LTC part number using 8-bit ASCII characters.

This read-only command is in block format.

MFR_SERIAL

The MFR_SERIAL command returns the serial number of this specific device using a maximum of fourteen 8-bit ASCII characters.

This read-only command is in block format.

PMBus COMMAND DETAILS (Unit Identification)

IC_DEVICE_ID

The IC_DEVICE_ID command returns the ADI IC part number using 8 bit ASCII characters.

This read-only command is in block format.

IC_DEVICE_REV

The IC_DEVICE_REV command returns the device revision code using 8 bit ASCII characters.

This read-only command is in block format.

MFR_SPECIAL_ID

The MFR_SPECIAL_ID command returns a 16-bit word representing the part name. 0x424x(LTC3882-1), 0x452x(LTC3882-2) denotes the part is a LTC3882-1, LTC3882-2. X is adjustable by the manufacturer. This read-only command has 2 data bytes.

TYPICAL APPLICATIONS

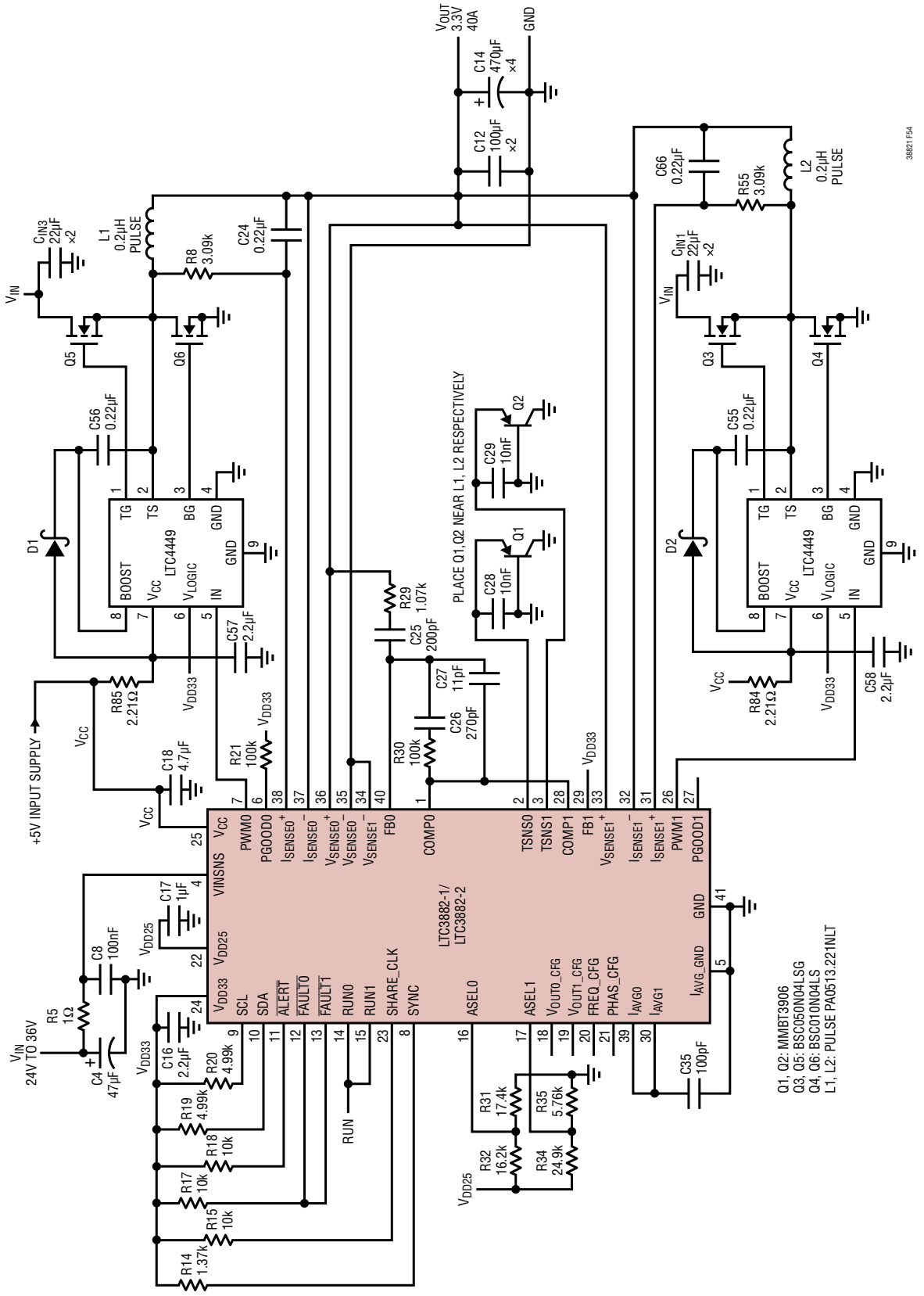


Figure 54. 36V Input 3.3V/40A 1.0MHz Converter with Discrete Gate Drivers

TYPICAL APPLICATIONS

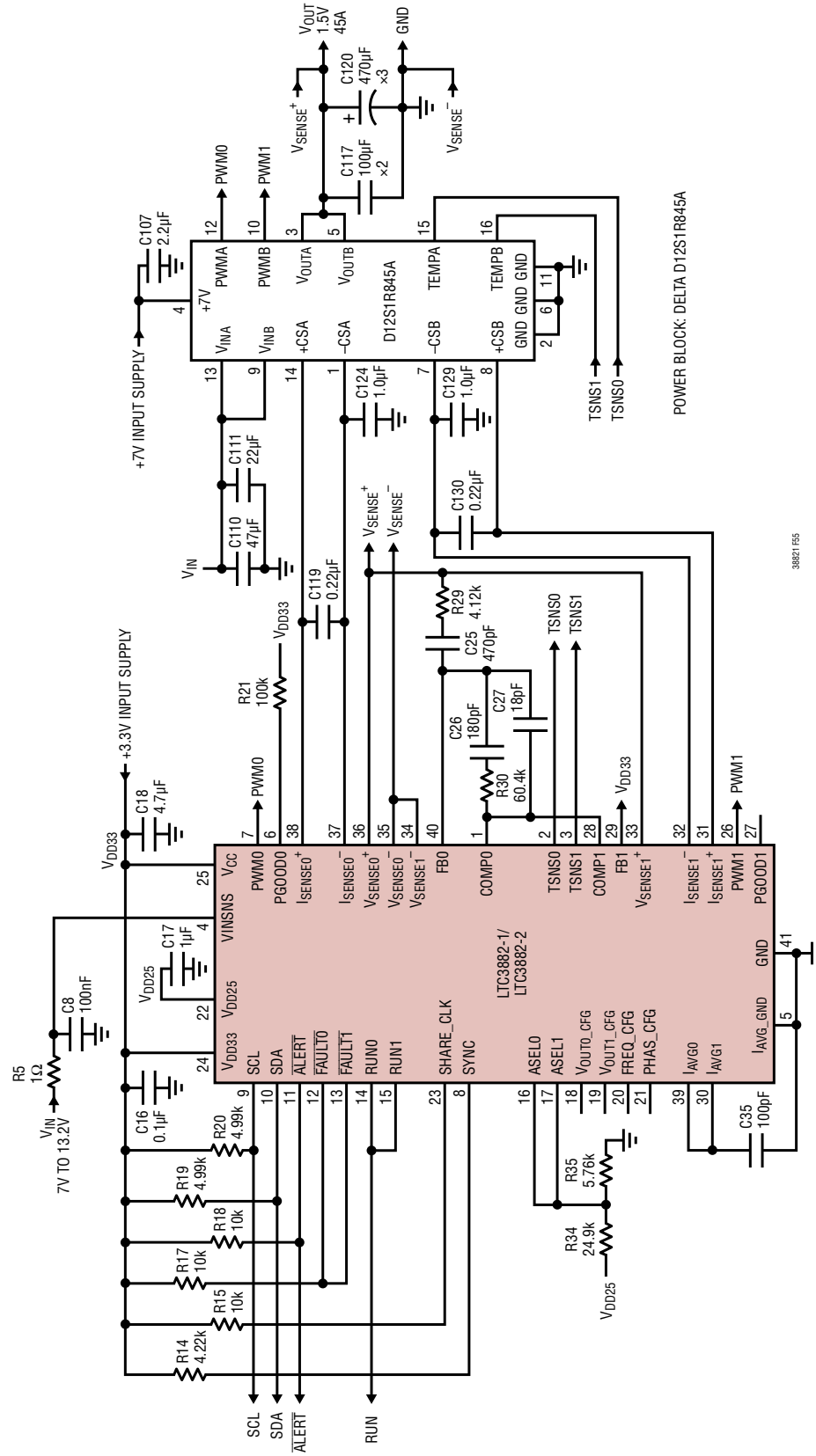
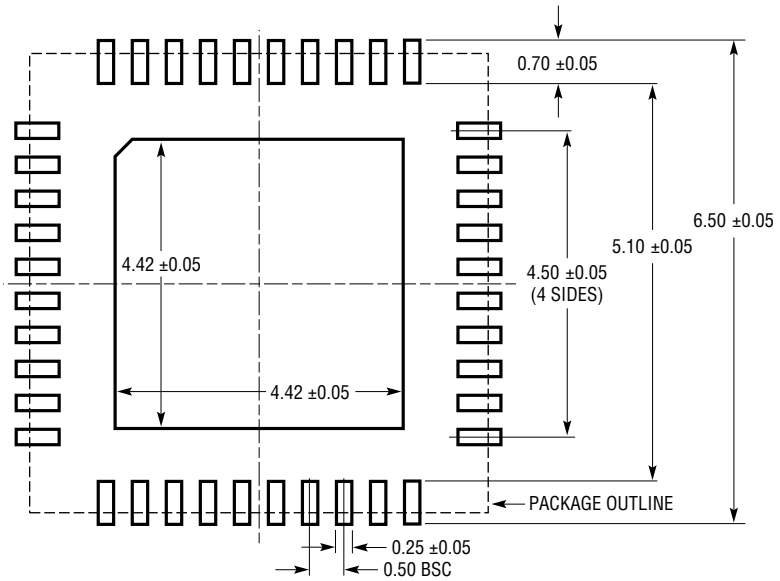


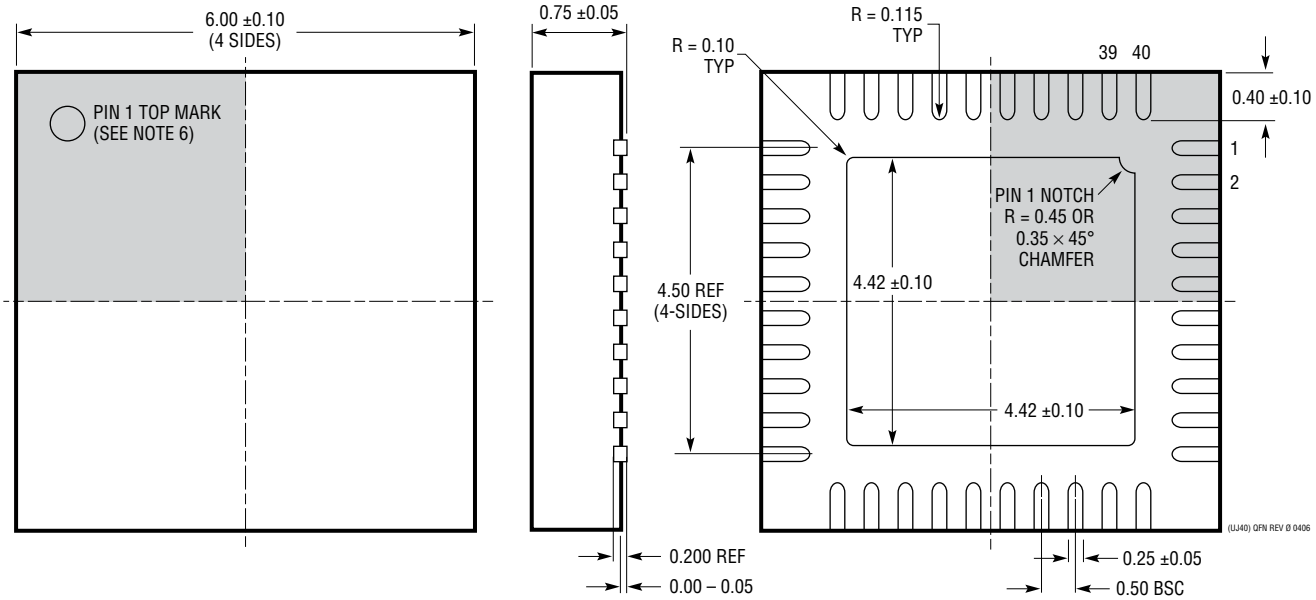
Figure 55. High Density 1.5V/45A 650kHz Converter Using Dual Power Block

PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/18	Added ECC. Reduced initialization time. Reduced conversion time.	1, 17, 24 5, 19 6
B	09/19	Added AEC-Q100 Qualified for Automotive Applications and orderable part numbers.	1, 4
C	07/22	Added LTC3882-2 Part Number and Related Specifications.	All
D	07/25	Added a note indicating that Analog Devices does not recommend the use of the following PWM frequencies in new designs: 600kHz, 750kHz, 900kHz, and 1MHz. Changes to Table 7 PMBus Command Summary. Change to text to include link to AN-152: Power System Management Addressing. Change to General Device Configuration Change to PMBus Command Details: Output Voltage and Limits	1, 63, 77 40, 42 65 74 82

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TYPICAL APPLICATION

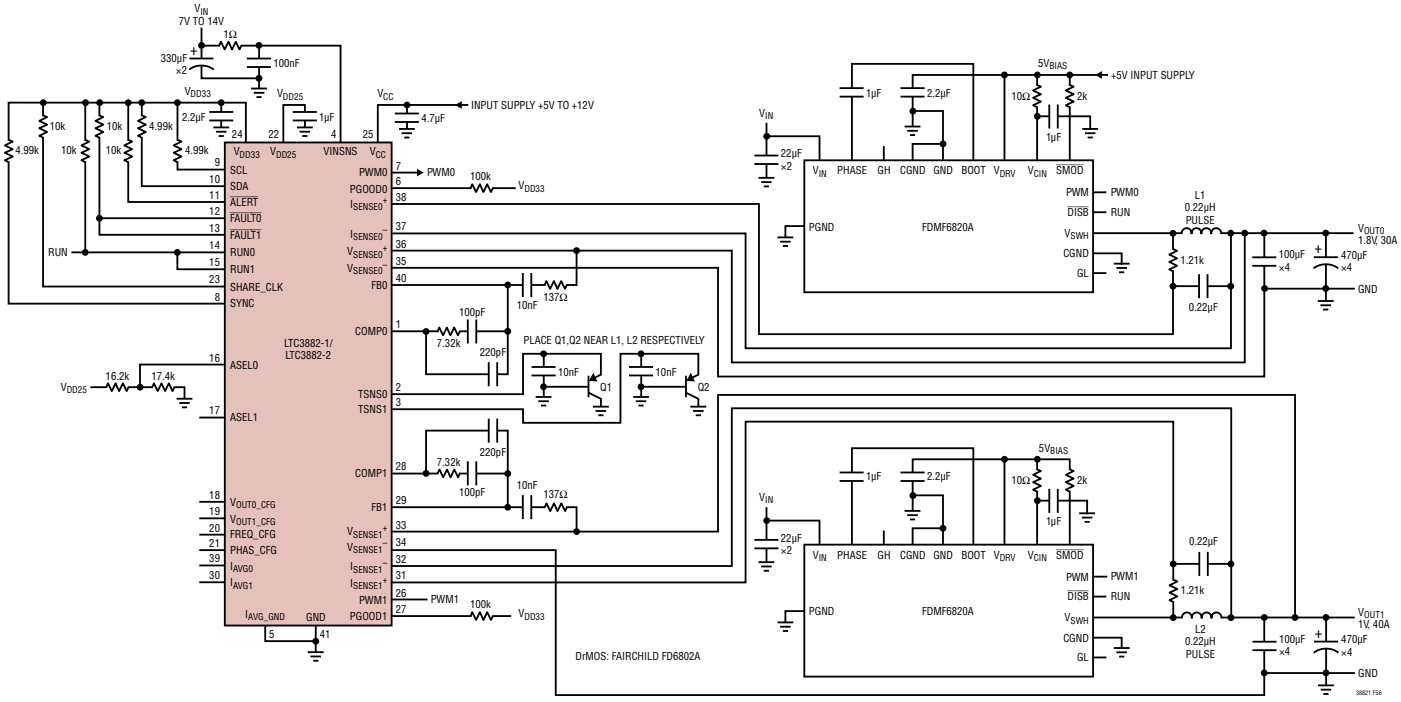


Figure 56. 1V/40A and 1.8V/30A 500kHz Converter with DrMOS Power Stage

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4676A	Dual 13A or Single 26A Step-Down DC/DC µModule Regulator with Digital Power Management	V_{IN} Up to 26.5V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.4V, ±2% I_{OUT} ADC Accuracy, Fault Logging, I^2C/PMBus Interface, 16mm × 16mm × 5mm, BGA Package
LTC3887/ LTC3887-1	Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ $V_{OUT0,1}$ ≤ 5.5V, I^2C/PMBus Interface, with EEPROM and 16-Bit ADC. –1 Version Operates with DrMOS and Power Blocks
LTC3886	60V Dual Output Step-Down Controller with Digital Power System Management	V_{IN} Up to 60V, 0.5V ≤ V_{OUT} ≤ 13.8V, Analog Control Loop, I^2C/PMBus Interface with EEPROM and 16-Bit ADC, Programmable Loop Compensation
LTC3880/ LTC3880-1	Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Analog Control Loop, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3883/ LTC3883-1	Single Phase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Input Current Sense Amplifier, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC2977	8-Channel PMBus Power System Manager Featuring Accurate Output Voltage Measurement	Fault Logging to Internal EEPROM Monitors Eight Output Voltages, Input Voltage and Die Temperature
LTC2974	Quad Digital Power Supply Manager with EEPROM	Controls and Monitors Four Outputs, 16-Bit ADC, Differential Inputs, with Fault Logging
LTC3774	Dual, Multiphase Current Mode Synchronous Controller for Sub-Milliohm DCR Sensing, with Remote Sense	Operates with Power Blocks, DrMOS Devices or External MOSFETs 4.5V ≤ V_{IN} ≤ 38V
LTC3861	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Accurate Current Share	Operates with Power Blocks, DrMOS Devices or External MOSFETs 3V≤ V_{IN} ≤ 24V
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	V_{IN} Up to 38V, 4V ≤ V_{CC} ≤ 6.5V, Adaptive Shoot-Through Protection, 2mm × 3mm DFN-8 Package
LTC7050/ LTC7051	Silent MOS Smart Power Stages with Accurate Current Monitoring	V_{IN} up to 14V, Integrated Silent MOS Power Stages with Integrated Boost Supplies and Fault Detection and Support

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