MAX14001/MAX14002

Configurable, Isolated 10-bit ADCs for Multi-Range Binary Inputs

General Description

The MAX14001/MAX14002 are isolated, single-channel analog-to-digital converters (ADCs) with programmable voltage comparators and inrush current control optimized for configurable binary input applications. 3.75kV$_{RMS}$ of integrated isolation is provided between the binary input side (field-side) and the comparator output/SPI-side (logic-side) of the MAX14001/MAX14002. An integrated, isolated, DC-DC converter powers all field-side circuitry, and this allows running field-side diagnostics even when no input signal is present. The 20-pin SSOP package provides 5.5mm of creepage and clearance with group II CTI rating.

These devices continually digitize the input voltage on the field-side of an isolation barrier and transmit the data across the isolation barrier to the logic-side of the device where the magnitude of the input voltage is compared to programmable thresholds. The binary comparator output pin is high when the input voltage is above the upper threshold and low when it is below the lower threshold. Response time of the comparator to an input change is less than 150µs with filtering disabled. With filtering enabled, the comparator uses the moving average of the last 2, 4, or 8 ADC readings. Both filtered and unfiltered ADC readings are available through the 5MHz SPI port, which is also used to set comparator thresholds and other device configuration.

The MAX14001/MAX14002 control the current of a binary input through an external, high-voltage FET. This current cleans relay contacts and attenuates input noise. An inrush comparator monitoring the ADC readings triggers the inrush current, or wetting pulse. The inrush trigger threshold, current magnitude, and current duration are all programmable in the MAX14001 but are fixed in the MAX14002. When the high-voltage FET is not providing inrush current, it switches to bias mode. Bias mode places a small current load on the binary input to attenuate capacitively coupled noise. The level of bias current is programmable between 50µA and 3.75mA in both the MAX14001 and MAX14002. This allows optimization of the tradeoff between noise attenuation and power dissipation.

Benefits and Features

- Enables Robust Detection of Binary Inputs
  - Programmable Input Bias Current Rejects Line Noise
  - 3.75kV$_{RMS}$ of Isolation for 60 Seconds
  - 5.5mm of Creepage and Clearance
  - Group II CTI Package Material
- Reduces BOM and Board Space Through High Integration
  - 10-bit, 10ksps ADC
  - Binary Threshold Comparators
  - Control Circuit for Driving a Depletion Mode FET
  - Isolation for Both Data and DC-DC Supply
  - 20-SSOP Package
- Increases Equipment “Up Time” and Simplifies System Maintenance
  - Enables Field-Side Diagnostics
  - Automatic Self-Diagnostics
- Provides Unparalleled Flexibility
  - Programmable Upper and Lower Input Thresholds
  - Programmable Inrush Current Activation Threshold, Magnitude, and Duration
  - Daisy-Chainable SPI Interface

Applications

- High-Voltage Binary Input (12V–300V)
- Distribution Automation
- Substation Automation
- Industrial Control, Multi-Range, Digital Input Modules with Individually Isolated Inputs

Safety Regulatory Approvals

- UL According to UL1577

Ordering Information ***appears at end of data sheet.***

19-8514; Rev 1; 8/17

maxim integrated™

Absolute Maximum Ratings

V_{DDL} to GNDL.....-0.3V to +6V
V_{DD} to GNDL .....-0.3V to +6V
Logic-Side Inputs ($\overline{CS}$, SCLK, SDI, $\overline{FAULT}$) to GNDL
.....-0.3V to +6V
Logic-Side Outputs (SDO, COUT)
to GNDL..... -0.3V to (V_{DDL} + 0.3V)
V_{REFIN}, V_{AIN} to AGND .....-0.3V to +2V
AGND to GNDF.....-0.3V to +0.3V
GATE to GNDF.....-0.3V to +4V
IFET to GNDF .....-0.3V to +12V
ISET to GNDF .....-0.3V to +2V
V_{DDF} to GNDF .....-0.3V to +6V
Short-Circuit Duration
($\overline{FAULT}$, COUT, SDO to GNDL or V_{DD}).....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-pin SSOP.....952.4mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

20-pin SSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....84°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....32°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DDL} - V_{GNDL} = 1.71V to 5.5V, V_{DD} - V_{GNDL} = 3.0V to 3.6V, R_{ISET} = 120kΩ, T_A = -40°C to +125°C, V_{GNDF} = V_{GNDL}. Typical values are at T_A = +25°C with V_{DDL} = V_{DD} = +3.3V, R_{ISET} = 120kΩ, V_{GNDF} = V_{GNDL}.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Logic Power Supply	V_{DDL}		1.71		5.5	V
Logic Supply Current	I_{DDL}	V_{DDL} = 3.3V, no load, $\overline{CS}$ = high		0.7	1.5	mA
Isolated DC-DC Power Supply Input Voltage	V_{DD}		3.0	3.3	3.6	V
Isolated DC-DC Supply Input Current	I_{DD}	V_{DD} = 3.3V		4.8	8	mA
Logic Power-Up Delay					0.2	ms
Field Power-Up Delay		C_{VDDF} = 0.1µF			1	ms
Field Power Supply	V_{DDF}	C_{VDDF} = 0.1µF, unregulated output voltage	2.5	3.0	3.5	V
Gate Charge Pump Voltage	V_{GATE}	1µA pull-down	3	3.6	4	V
Logic-Side Undervoltage Lockout Threshold	V_{UVLOL}	V_{DD} ≥ 3V	1.5	1.6	1.66	V
	V_{UVLOD}	V_{DDL} ≥ 1.71V	2.69	2.82	2.95	V
Logic-Side Undervoltage Lockout Threshold Hysteresis	$V_{UVLHYST}$			50		mV
	$V_{UVDHYST}$			100		mV
Field-Side Undervoltage Lockout Threshold	V_{UVLOF}	(Note 4)	1.95	2.1	2.25	V

Electrical Characteristics (continued)

(V_{DDL} - V_{GNDL} = 1.71V to 5.5V, V_{DD} - V_{GNDL} = 3.0V to 3.6V, R_{ISET} = 120kΩ, T_A = -40°C to +125°C, V_{GNDF} = V_{GNDL}. Typical values are at T_A = +25°C with V_{DDL} = V_{DD} = +3.3V, R_{ISET} = 120kΩ, V_{GNDF} = V_{GNDL}.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Field-Side Undervoltage Lockout Threshold Hysteresis	$V_{UVFHYST}$			100		mV
PROTECTION						
ESD		Any pin to GNDL or GNDF inclusive		±2		kV
EFT (Burst)		System-level requirement IEC 61000-4-4 common mode (Note 5)		3		kV
DYNAMIC						
Common-Mode Transient Immunity	CMTI	(Note 6)		50		kV/µs
ADC AND COMPARATOR						
Input Voltage Range	V_{AIN}	Nominal measurement range	0		V_{REFIN} (1.25)	V
Reference Input Range	V_{REFIN}		1.15	1.25	1.35	V
ADC Resolution			10			Bits
Gain Error	GE	V_{IN} = 98% V_{REF}, excluding offset error and reference errors	-0.55		+0.55	%
Offset Error	OE	V_{IN} = 2% V_{REF}, offset calculated	-0.2		+0.2	%FS
Differential Nonlinearity	DNL				±1	LSB
Integral Nonlinearity	INL	Included in the gain + offset window			±1	LSB
Input Leakage Current	IILR	V_{AIN} = 1.25V	-200		+200	nA
Throughput			8	10	12	ksps
Latency (No Filtering)		AIN step input to COUT transition (Notes 4, 7)	12		150	µs
Latency (2 Readings)		AIN step input to COUT transition (Notes 4, 7)	92		270	µs
Latency (4 Readings)		AIN step input to COUT transition (Notes 4, 7)	180		510	µs
Latency (8 Readings)		AIN step input to COUT transition (Notes 4, 7)	340		990	µs
INTERNAL VOLTAGE REFERENCE						
Nominal Output Voltage				1.25		V
Output Voltage Accuracy		Over the entire temperature range	-5		+5	%
Output Voltage Temperature Drift	T_{CVOUT}			50		ppm/°C
EXTERNAL VOLTAGE REFERENCE						
Reference Voltage			1.15	1.25	1.35	V
Available Bias Current		When powered from V_{DDF} (series) or REFIN (shunt)	70			µA

Electrical Characteristics (continued)

(V_{DDL} - V_{GNDL} = 1.71V to 5.5V, V_{DD} - V_{GNDL} = 3.0V to 3.6V, R_{ISET} = 120kΩ, T_A = -40°C to +125°C, V_{GNDF} = V_{GNDL}. Typical values are at T_A = +25°C with V_{DDL} = V_{DD} = +3.3V, R_{ISET} = 120kΩ, V_{GNDF} = V_{GNDL}.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS CURRENT DAC						
Full-Scale Current		Excludes R_{ISET} errors	3.375	3.75	4.125	mA
Resolution				0.25		mA
Offset Error		IBIAS[3:0] = 0 (see CFG register)		50	100	µA
Integral Nonlinearity	INL			0.25		LSB
INRUSH CURRENT DAC						
Full-Scale Current		Excludes R_{ISET} errors	94.5	105	115.5	mA
Resolution				7		mA
Offset		IINR[3:0] = 0 (see INRP register)		50	100	µA
Integral Nonlinearity	INL			0.25		LSB
Inrush Current		MAX14002 only. Excludes R_{ISET} errors	44.1	49	53.9	mA
INRUSH TIMER						
Range		Nominal	0		120	ms
Resolution		Programmed by TINR[3:0] (see INRP register)		8		ms
Error			-20		+20	%
Maximum Duty Cycle		DU1 = 0, DU0 = 1 (see INRP register)		1.6		%
		DU1 = 1, DU0 = 0 (see INRP register)		3.1		
		DU1 = 1, DU0 = 1 (see INRP register)		6.3		
Inrush Duration		MAX14002 only	38.4	48	57.6	ms
INRUSH COMPARATOR						
Range			0		ADC FS	V
Resolution			10			Bits
Latency (No Filtering)		From input voltage = INRT until IINR = 50% of set value (Notes 4, 7)	22		160	µs
Latency (2 Readings)		From input voltage = INRT until IINR = 50% of set value (Notes 4, 7)	102		280	µs
Latency (4 Readings)		From input voltage = INRT until IINR = 50% of set value (Notes 4, 7)	192		520	µs
Latency (8 Readings)		From input voltage = INRT until IINR = 50% of set value (Notes 4, 7)	356		1000	µs
LOGIC I/O LEVELS						
Input High Voltage	V_{IH}	SCLK, SDI, $\overline{CS}$	0.7 x V_{DDL}			V
Input Low Voltage	V_{IL}	SCLK, SDI, $\overline{CS}$			0.3 x V_{DDL}	V
Input Hysteresis	V_{HYST}	SCLK, SDI, $\overline{CS}$		0.05 x V_{DDL}		V

Electrical Characteristics (continued)

(V_{DDL} - V_{GNDL} = 1.71V to 5.5V, V_{DD} - V_{GNDL} = 3.0V to 3.6V, R_{ISET} = 120kΩ, T_A = -40°C to +125°C, V_{GNDF} = V_{GNDL}. Typical values are at T_A = +25°C with V_{DDL} = V_{DD} = +3.3V, R_{ISET} = 120kΩ, V_{GNDF} = V_{GNDL}.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	SDO, COUT, sourcing 4mA	V_{DDL}- 0.4			V
Output Low Voltage	V_{OL}	SDO, COUT, $\overline{FAULT}$, sinking 4mA			0.4	V
Output High-Impedance Leakage Current	I_{OL}	SDO, $\overline{FAULT}$	-1		+1	µA
Input Leakage Current	I_{IL}	SCLK, SDI, $\overline{CS}$	-1		+1	µA
Input Capacitance	C_{IN}	SCLK, SDI, $\overline{CS}$, f = 1MHz		2		pF
SPI TIMING CHARACTERISTICS						
SCLK Clock Frequency	f_{SCLK}	Single device			5	MHz
SCLK Clock Period	t_{SCLK}	Single device	200			ns
SCLK Pulse-Width High	t_{SCLKH}	Single device	80			ns
SCLK Pulse-Width Low	t_{SCLKL}	Single device	80			ns
$\overline{CS}$ Fall-to-SCLK Rise Time	$t_{CS(lead)}$		80			ns
SCLK Fall-to-$\overline{CS}$ Rise Time	$t_{CS(lag)}$		80			ns
SDI Hold Time	t_{DINH}		40			ns
SDI Setup Time	t_{DINSU}		40			ns
SDO Enable Time ($\overline{CS}$ Falling to SDO Valid)	$t_{DOUT(en)}$	C_L = 50pF	40			ns
SDO Disable Time ($\overline{CS}$ Rising to SDO Three-State)	$t_{DOUT(dis)}$	C_L = 50pF	40			ns
Output Data Propagation Delay	t_{DO}	C_L = 50pF. SCLK falling-edge to SDO valid			50	ns
Write-Command to Field Implementation Delay	t_{FID}	From $\overline{CS}$ de-assertion until field-side registers are loaded			165	ns
Inter-Access Gap	t_{IAG}	Minimum time $\overline{CS}$ must be de-asserted between commands	920			ns

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications for all temperature limits are guaranteed by design.

Note 3: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to their respective ground (GNDL or GNDF), unless otherwise noted.

Note 4: Guaranteed by characterization; not production tested.

Note 5: EFT voltage according to IEC 61004-4 is tested through direct coupling to the generator.

Note 6: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDF and GNDL (V_{CM} = 1000V).

Note 7: Latency numbers are based on the following condition: a full-scale step is applied at the ADC input and THU is set to mid-scale value (0x1ff). Latency is the delay from the step at the ADC input to the digital comparator output.

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1050	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 8)	560	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 8)	400	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	6300	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	t = 60s, f = 60Hz (Notes 8, 9)	3.75	kV_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic Insulation, 1.2/50µs surge pulse per IEC 61000-4-5	7.5	kV
Insulation Resistance Logic-to-Field	R_S	T_A = +125°C, V_{IO} = 500V	$>10^9$	Ω
Barrier Capacitance Logic-to-Field	CIO	f = 1MHz (Note 10)	10	pF
Minimum Creepage Distance	CPG	SSOP	5.5	mm
Minimum Clearance Distance	CLR	SSOP	5.5	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Resistance Index	CTI	Material Group II (IEC 60112)	>400	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 8: V_{ISO}, V_{IOWM} and V_{IORM} are defined by the IEC 60747-5-5 standard.
Note 9: Product is qualified V_{ISO} for 60 seconds. 100% production tested at 120% of V_{ISO} for 1s.
Note 10: Capacitance is measured with all pins on field-side and logic-side tied together.

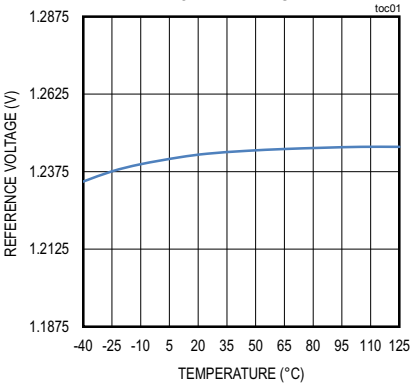
Safety Regulatory Approvals

UL
The MAX14001/MAX14002 are certified under UL1577. For more details, refer to File E351759.
Rated up to $3750V_{RMS}$ isolation voltage for basic insulation.

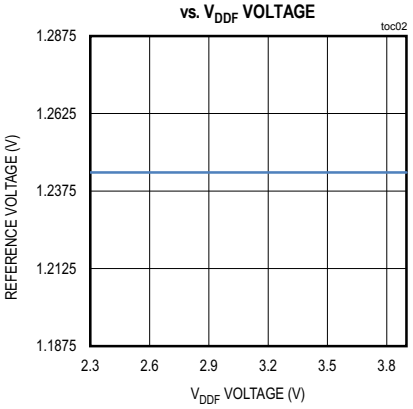
Typical Operating Characteristics

(V_{DDL} = V_{DD} = +3.3V, R_{ISET} = 120kΩ, isolated GNDF and GNDL, high-voltage FET is IXTY08N100D2, with T_A = +25°C unless otherwise noted.)

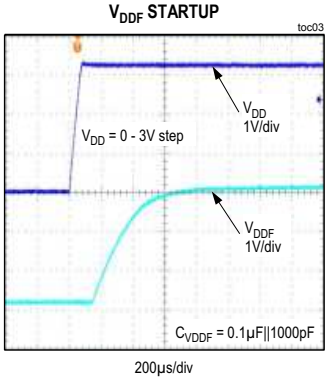
INTERNAL VOLTAGE REFERENCE vs. TEMPERATURE



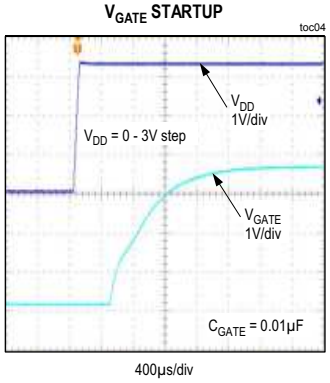
INTERNAL VOLTAGE REFERENCE vs. V_{DDF} VOLTAGE



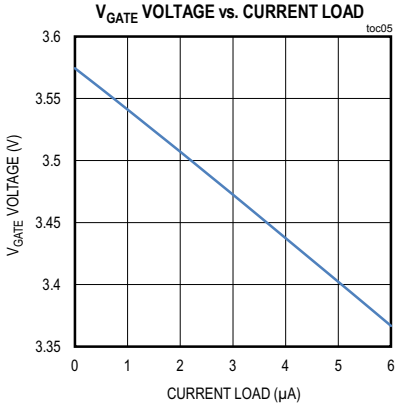
V_{DDF} STARTUP



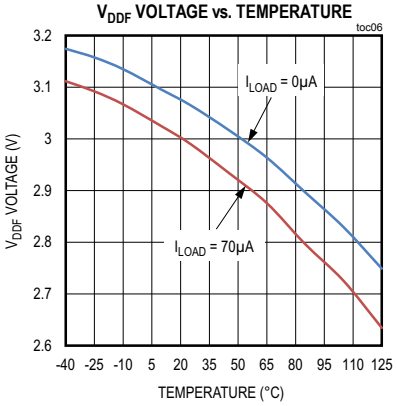
V_{GATE} STARTUP



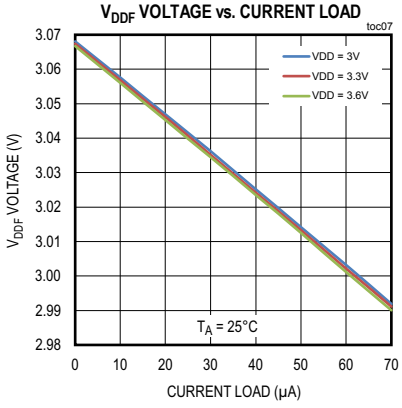
V_{GATE} VOLTAGE vs. CURRENT LOAD



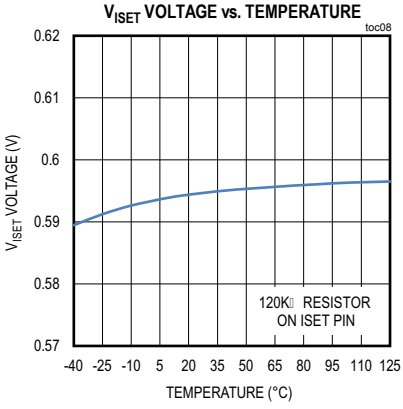
V_{DDF} VOLTAGE vs. TEMPERATURE



V_{DDF} VOLTAGE vs. CURRENT LOAD



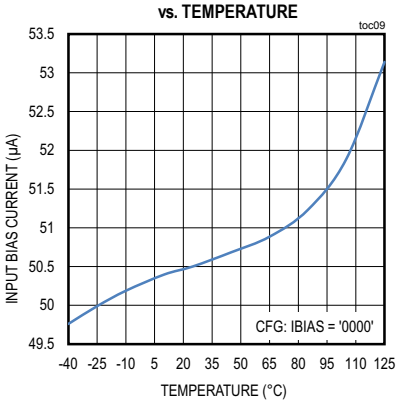
V_{ISET} VOLTAGE vs. TEMPERATURE



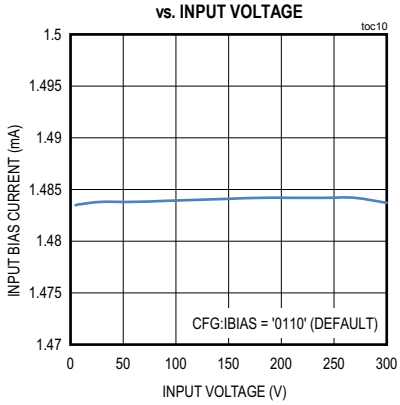
Typical Operating Characteristics (continued)

(V_{DDL} = V_{DD} = +3.3V, R_{ISET} = 120kΩ, isolated GNDF and GNDL, high-voltage FET is IXTY08N100D2, with T_A = +25°C unless otherwise noted.)

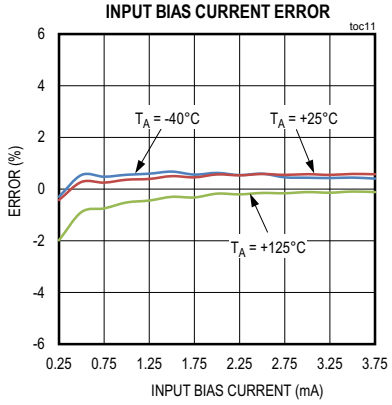
INPUT BIAS CURRENT vs. TEMPERATURE



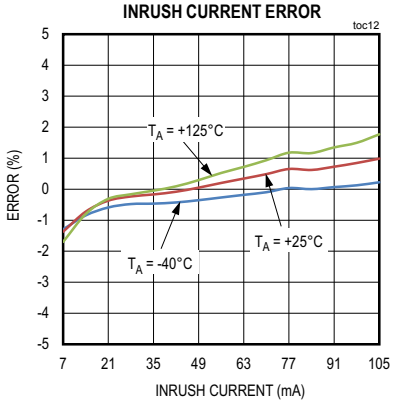
INPUT BIAS CURRENT vs. INPUT VOLTAGE



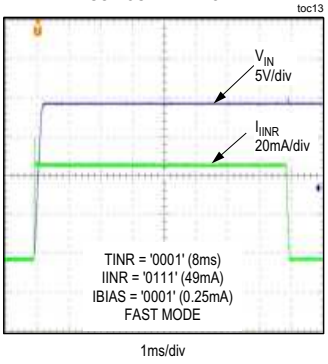
INPUT BIAS CURRENT ERROR



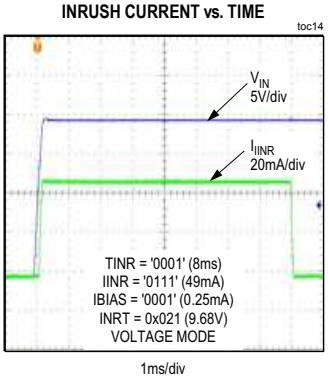
INRUSH CURRENT ERROR



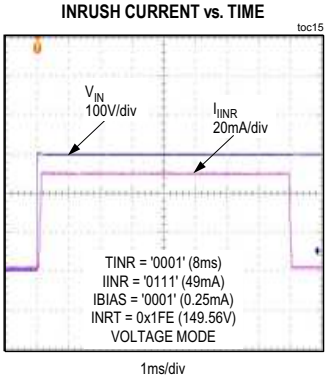
INRUSH CURRENT vs. TIME



INRUSH CURRENT vs. TIME



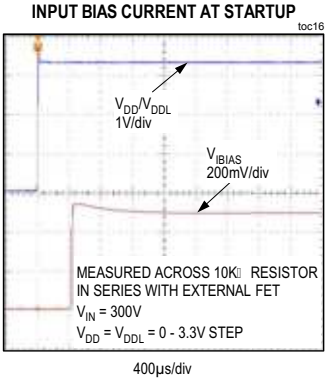
INRUSH CURRENT vs. TIME



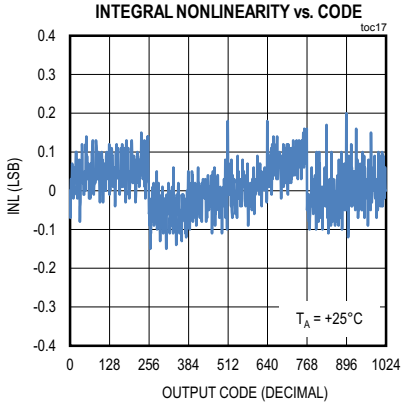
Typical Operating Characteristics (continued)

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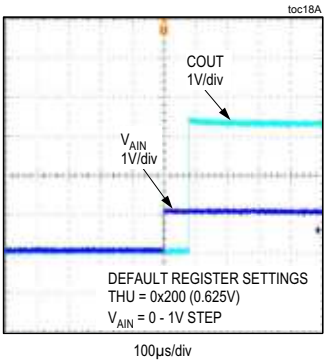
INPUT BIAS CURRENT AT STARTUP



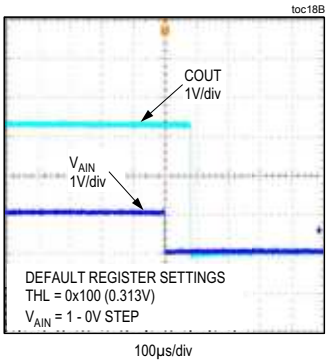
INTEGRAL NONLINEARITY vs. CODE



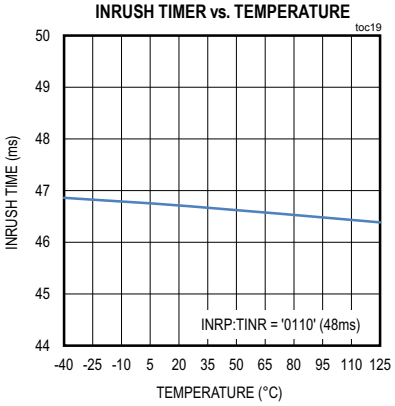
COUT CHANGE ON RISING EDGE



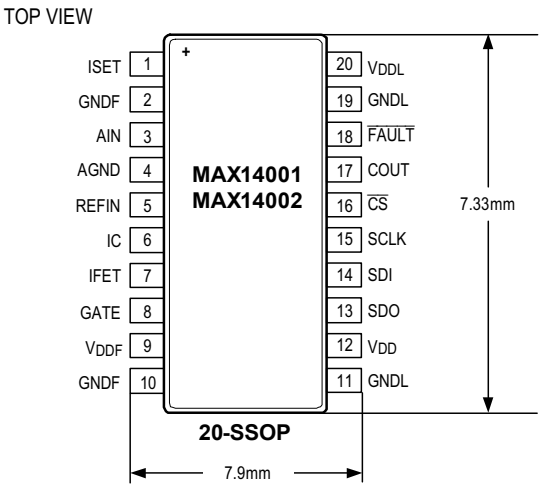
COUT CHANGE ON FALLING EDGE



INRUSH TIMER vs. TEMPERATURE



Pin Configuration



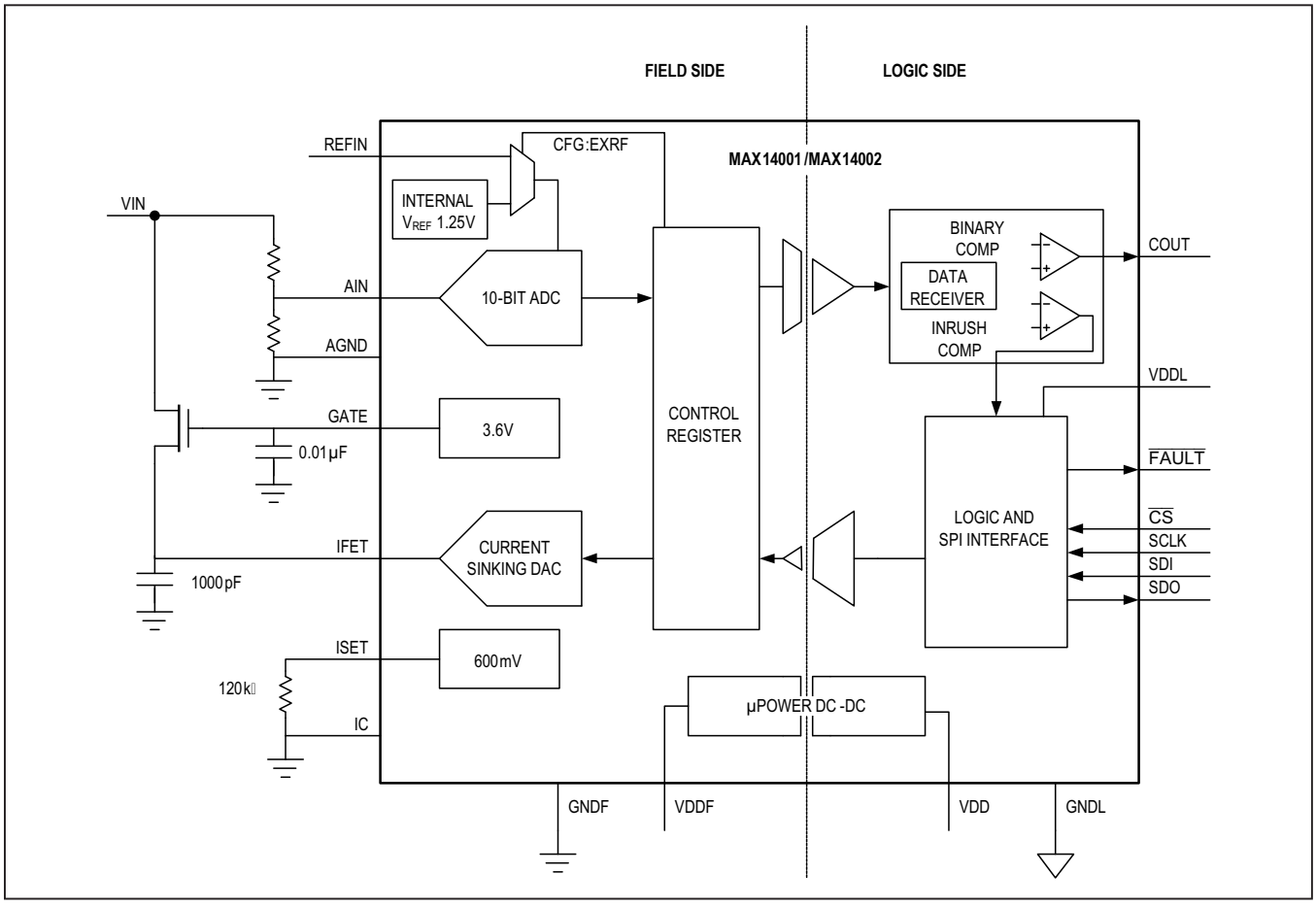
Pin Description

PIN	NAME	REFERENCE	FUNCTION
POWER SUPPLY			
20	V_{DDL}	GNDL	Power Input for the Logic-Side of the MAX14001/MAX14002. Bypass with 10µF||1000pF capacitors to GNDL.
12	V_{DD}	GNDL	Power Input for the Isolated DC-DC Converter. The DC-DC converter powers the field-side of the MAX14001/MAX14002. Bypass with 10µF||1000pF capacitors to GNDL.
11, 19	GNDL	—	Power and Signal Ground for All Logic-Side Pins.
9	V_{DDF}	GNDF	Unregulated Output of the DC-DC Converter. Bypass to GNDF with 0.1µF||1000pF capacitors. The 1000pF capacitor should be placed as close to the pin as possible.
8	GATE	GNDF	Bias Voltage for the Gate of the External Depletion Mode FET. Connect a 0.01µF capacitor from GATE to GNDF.
2, 10	GNDF	—	Field-side ground for everything except the ADC front-end and voltage reference.
ANALOG			
1	ISET	GNDF	Connect a 120kΩ Resistor From ISET to GNDF. This generates a reference current used to establish the correct bias and inrush currents. Parasitic capacitance on this pin should not exceed 10pF.
7	IFET	GNDF	Current Sink Input for Inrush and Bias Current. This pin is buffered from high voltage by connecting it to the source of the external high-voltage FET. Connect a 1000pF capacitor from IFET to GNDF.
3	AIN	AGND	Analog Input. The ADC measures the voltage on this pin with respect to AGND.
4	AGND	—	Analog Ground Reference for AIN and REFIN
5	REFIN	AGND	Optional External Voltage Reference Input (Nominally 1.25V). When an external reference is used, connect a 0.1µF bypass capacitor from REFIN to AGND. When an internal reference is used, connect REFIN directly to AGND.
6	IC	GNDF	Internally Connected. Connect to GNDF.

Pin Description (continued)

PIN	NAME	REFERENCE	FUNCTION
DIGITAL			
18	$\overline{\text{FAULT}}$	GNDL	Open-Drain Output That Asserts Low During a Number of Different Error Conditions. The cause of the error is latched in the FLAGS register. See *Diagnostic and Fault Reporting Features* for details on clearing $\overline{\text{FAULT}}$.
17	COUT	GNDL	Digital Comparator Output. COUT is high when AIN is above the upper threshold (THU) and low when AIN is below the lower threshold (THL).
16	$\overline{\text{CS}}$	GNDL	Chip Select for SPI Interface. Assert low to enable SPI functions and SDO. SDO is high impedance when $\overline{\text{CS}}$ is high.
15	SCLK	GNDL	Serial Clock for SPI Interface
14	SDI	GNDL	Serial Data Input for SPI Interface (MOSI)
13	SDO	GNDL	Serial Data Out for SPI Interface (MISO)

Functional Diagram



Detailed Description

The MAX14001/MAX14002 are 10-bit ADCs with a 3.75kV$_{RMS}$ isolated SPI interface. Additional features include a programmable magnitude comparator, programmable inrush current for cleaning relay contacts, and programmable input bias current to optimize power dissipation while reducing capacitively coupled input noise. The ADC and all field-side circuits are powered by an integrated, isolated, DC-DC converter that allows field-side functionality to be verified even when there is no input signal or other field-side supply. This makes the MAX14001/MAX14002 ideally suited for high density, multi-range, individually isolated, binary input modules.

ADC

The devices' ADC employs a 10-bit SAR architecture with a nominal sampling rate of 10ksps, and has an input voltage range of 0V to +1.25V with respect to AGND. After power-up, the ADC runs continually at the nominal sampling rate. The 10-bit unfiltered ADC reading and filtered ADC reading are both available via the SPI interface. Filtering averages the most recent 2, 4, or 8 readings depending on the value of the FT[1:0] bits in the CFG register. A binary comparator responds within 150µs to changes in input voltage by continually comparing the latest ADC reading to the programmed thresholds (refer to the EC table for response times when using the ADC filter). When the latest ADC reading is higher than the upper threshold (THU), the comparator's output pin (COUT) is high and when it is lower than the lower threshold (THL), the comparator's output pin (COUT) is low.

Internal/External Voltage Reference Configuration

The MAX14001/MAX14002 feature both internal and external voltage reference capability. The 1.25V internal reference has a maximum error of ±5% over the entire operating temperature range. If higher accuracy is required, an external reference may be used. The external reference may be either series or shunt, but must not draw more than 70µA of supply current. Series references must be powered from V_{DDF} while shunt references are powered from an internal 70µA current source that is connected to the REFIN pin. Internal/external voltage reference mode is selected using the SPI interface to program the CFG register. Refer to Table 1 for the CFG register configuration, Figure 1 for shunt reference hardware connection, and Figure 2 for series reference hardware connection.

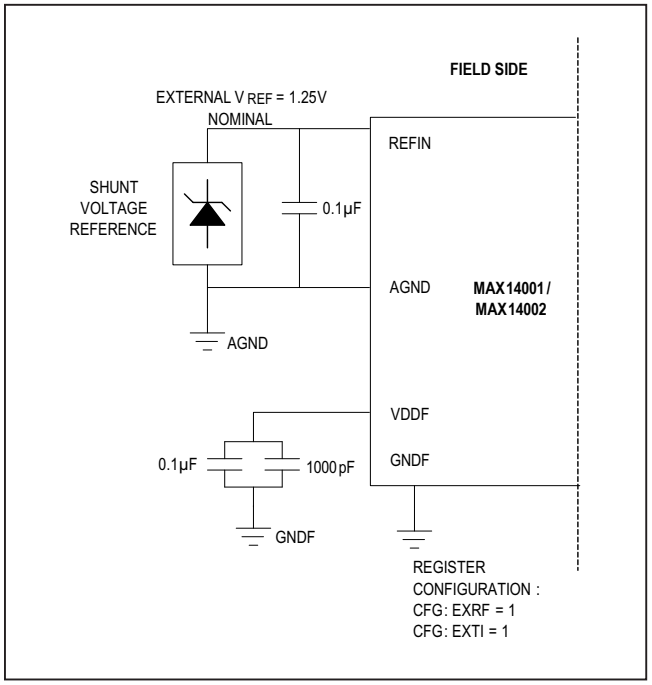


Figure 1. Shunt Voltage Reference Connection

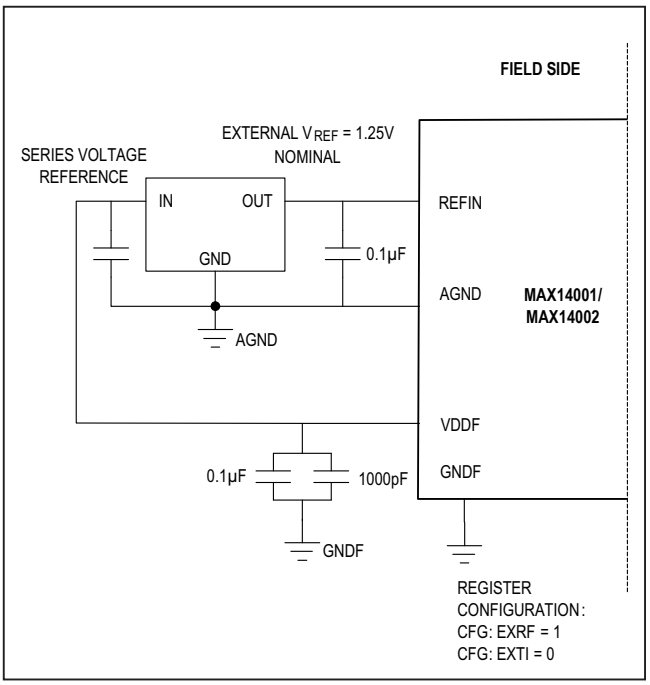


Figure 2. Series Voltage Reference Connection

Table 1. Voltage Reference Register Configuration

REFERENCE CONFIGURATION	CFG:EXRF	CFG:EXTI	CONNECTION
Internal Reference	0	0	Connect REFIN directly to AGND.
External Series Reference	1	0	Series reference is supplied by V_{DDF}. Output is connected to the REFIN pin. Bypass REFIN to AGND with a 0.1µF capacitor.
External Shunt Reference	1	1	Internal current source is turned on. Shunt reference is connected between REFIN and AGND. Bypass REFIN to AGND with a 0.1µF capacitor.

ADC Error

The uncalibrated error of the ADC lies within the window shown in the Figure 3 ADC Error Window. The boundaries of the box are defined by the offset and gain error from the EC table and include INL errors as well as drift over temperature. The upper-boundary is set by the most positive offset combined with the most positive gain error. Conversely, the lower-boundary is set by the most negative offset combined with the most negative gain error.

$$ERROR_{MAX} = OE \times FS + V_{IN} \times GE$$

Where OE is the offset error in %FS, FS is the full scale voltage, V_{IN} is the input voltage being measured, and GE is the gain error in %.

If a resistor-divider is used in front of the ADC, FS and V_{IN} can be the voltages at the input of the divider. For total system error, the resistive-divider error and the error of the voltage reference in percent are added to the gain error of the ADC.

$$SYSTEM\ ERROR_{MAX} = OE \times FS + V_{IN} \times (GE + ERROR_R + ERROR_{VREF})$$

Where OE is the offset error in %FS, FS is the full scale voltage, V_{IN} is the input voltage being measured, GE is the gain error in %, $ERROR_R$ is the resistive-divider error in %, and $ERROR_{VREF}$ is the voltage reference error in %.

For example, assume:

- All errors specs are symmetrical.
  - |Maximum Positive Error| = |Maximum Negative Error|
- The input resistive-divider is made of 1% resistors and divides the binary voltage by a nominal factor of 240.
  - Maximum resistive-divider error $ERROR_R$ = 2%

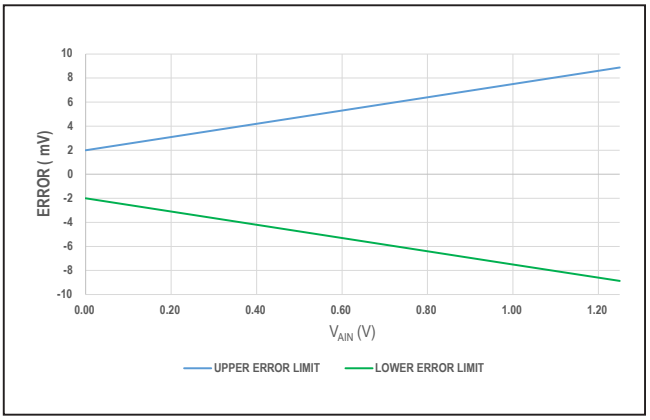


Figure 3. ADC Error Window (Excludes V_{REF} Error)

- A nominal 1.25V reference with an error of 5%
  - Full-scale input voltage F_S = 1.25V x 240 = 300
  - $ERROR_{VREF}$ = 5%
- ADC offset error OE = 0.3%
- ADC gain error GE = 0.3%
- Input voltage V_{IN} = 200V

$$SYSTEM\ ERROR_{MAX} = 0.3\% \times 300V + V_{IN} \times (0.3\%+2\%+5\%)$$

When V_{IN} = 200V, the maximum error is 15.5V.

If the comparator threshold is set at 200V (ADC reading of decimal 682), the comparator could trip with a voltage as low as 184.5V or as high as 215.5V. Conversely, if the ADC is to read 682, the nominal input voltage would be 200V, but the actual voltage could be as high a 215.5V or as low as 184.5V.

High-Voltage FET Current Control

The devices control a high-voltage depletion mode FET that can be used to sink inrush current for cleaning relay contacts while contacts are closing, or a smaller bias current for input noise suppression while contacts are open. When the inrush pulse is finished, the FET current is reduced to the bias level, lowering power dissipation in the FET while still providing an input load. Inrush current is fixed in the MAX14002 (49mA for 48ms) but is configurable in the MAX14001. The MAX14001's inrush current magnitude and duration are both programmable: the magnitude ranges from 50µA to 105mA in 7mA increments, and the duration ranges from 0ms to 120ms in 8ms increments. Bias current is adjustable in both the MAX14001 and MAX14002, and ranges from 50uA to 3.75mA in 0.25mA increments.

The MAX14001's inrush pulse can be initiated in one of two ways: voltage triggered inrush mode based on the ADC reading or FAST inrush mode based on the high-voltage FET current level. In voltage triggered inrush mode (FAST bit in the CFG register = 0), the pulse is initiated when the ADC reading equals or exceeds the programmed trigger threshold in the INRT register. Once an inrush pulse has been triggered, the ADC reading must drop below the re-arm threshold in the INRR register before another inrush pulse can be triggered. In FAST mode (FAST bit in the CFG register = 1), the inrush pulse starts as soon as the input signal is able to supply the inrush current. Re-arming occurs when the input no longer supplies enough current to the high-voltage FET (either inrush or bias current depending on the present mode). The MAX14002 operates in FAST mode only.

Figure 4 and Figure 5 illustrate the two methods for triggering a pulse of inrush current.

Voltage Mode

A) The high-voltage FET is trying to sink bias current, but cannot because the input signal is not supplying enough current.

B) When the input voltage increases to the inrush trigger threshold (INRT), the FET current is increased to the inrush level and the inrush timer is started.

C) Contact bounce causes the input voltage to drop below the inrush reset threshold (INRR). The FET current is reduced to the bias level and the inrush timer is reset.

D) The input voltage again rises to the inrush trigger threshold. The FET current is increased to the inrush level and the inrush timer is started.

E) The inrush timer expires and the FET current is reduced to the bias level.

F) The input voltage drops below the inrush re-arm threshold (INRR). The inrush timer is reset and prepared to deliver the next inrush pulse. The FET current remains at the bias level.

G) The noise pulse is fully clamped at the turn-on voltage of the FET circuit.

H) Higher energy noise pulse that is partially clamped by the bias current. Noise current exceeds the bias current so the voltage rises above the turn-on voltage of the FET circuit.

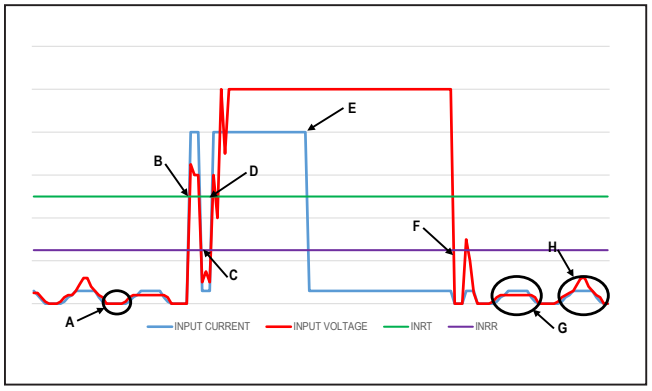


Figure 4. Voltage Triggered Inrush Mode

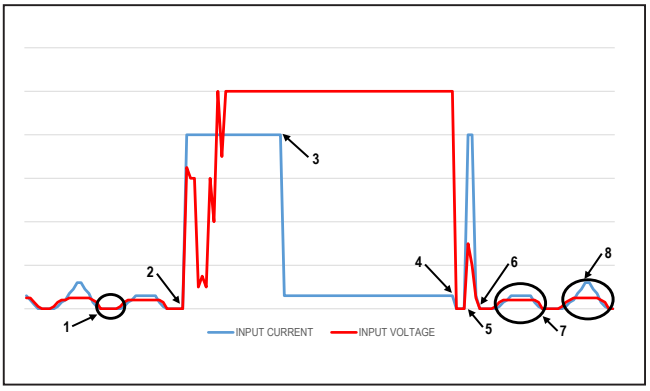


Figure 5. FAST Inrush Mode

FAST Mode

1) The high-voltage FET is trying to sink the inrush current, but cannot because the input signal is not supplying enough current. Since the current level cannot be met, the FET current is set to the inrush level, and the inrush timer is reset.
2) The input voltage increases and supplies enough current for the inrush pulse. The inrush timer is started.
3) The inrush timer expires and the FET current is reduced to the bias level.
4) The input voltage drops and can no longer supply the bias current. The inrush timer is reset and the FET current is set to the inrush level.
5) Contact bounce raises the input voltage and supplies enough current for an inrush pulse. The inrush timer is started.
6) The input voltage drops and can no longer supply the inrush current. The inrush timer is reset and the FET current remains the inrush level.
7) The noise pulse is fully clamped at the turn-on voltage of the FET circuit.
8) Higher energy noise pulse is fully clamped by the inrush current. Noise current exceeds the bias current, but since the FET is trying to sink the larger input current, the input current rises and the voltage remains clamped at the turn-on voltage of the FET circuit.

Repetitive Inrush Pulse Limiting (MAX14001 Only)

The MAX14001 can limit repetitive inrush pulses to prevent overheating from abnormal input signals that would otherwise trigger a continuous stream of inrush pulses. When the pulse limiting function is enabled, the MAX14001 monitors the percentage of time that the inrush current is flowing. When it exceeds the duty cycle threshold over the last 10 seconds, additional inrush pulses are disabled for the next 10 seconds. When the pulse limiting is triggered, the INRD bit in the FLAGS register is set and $\overline{\text{FAULT}}$ is asserted if the EINRD bit in the FLTEN register is set. The pulse limiting function can be turned off or the pulse duty cycle can be set to 1.6%, 3.1%, or 6.3% using the DU[1:0] bits in the INRP register. The MAX14002 does not provide a repetitive inrush pulse limiting feature.

Diagnostic and Fault Reporting Features

The MAX14001/MAX14002 continuously monitor seven possible fault conditions, and a hardware alert is provided via the open drain $\overline{\text{FAULT}}$ pin, which asserts low when an enabled fault is detected. The possible faults are: ADC functionality error, repetitive inrush pulses being triggered, SPI framing error, loss of internal isolated data stream, CRC errors from internal communication, high-voltage FET failure, and corrupted memory error.

The bits in the FLTEN register determine how the $\overline{\text{FAULT}}$ output responds to the seven error conditions, and the $\overline{\text{FAULT}}$ output is asserted if the corresponding bit is enabled in the FLTEN register. If the FLTEN register bit DYEN = 0, $\overline{\text{FAULT}}$ operates as a latched output and remains asserted until the FLAGS register is cleared but if the bit DYEN = 1, $\overline{\text{FAULT}}$ operates as a dynamic output and de-asserts when the faults are no longer detected even though bits in the FLAGS register remain set.

If the corresponding bit in the FLTEN register is not set, when an error is flagged, $\overline{\text{FAULT}}$ will not be asserted, but the bit in the FLAGS register will still be latched and remain set until the register is read, which automatically clears all bits in the FLAGS register. *Note that if a fault condition still exists when the register is read, the cleared fault bit will immediately be set again*.

In a typical application, $\overline{\text{FAULT}}$ triggers an interrupt routine in the microcontroller or FPGA, which will read the FLAGS register to determine the cause of the interrupt.

Diagnostic Conditions

The diagnostic features implemented on the MAX14001/MAX14002 can be summarized as follows:

1) **ADC Functionality Error:** ADC functionality is checked by looking for changes in the ADC output. To ensure that a change should have occurred, a special test measurement is made while injecting a small current at the input of the ADC. This special measurement used for ADC functionality verification is interleaved between normal measurements and does not affect the ADC sampling time. If the ADC reading does not change, an ADC functional failure is declared and bit ADC (bit 1) in the FLAGS register is set.
2) **Repetitive Inrush Pulses:** If the repetitive inrush pulse limiting feature of the MAX14001 is turned on, and pulse limiting is triggered, bit INRD (bit 2) in the FLAGS register is set. See *Repetitive Inrush Pulse Limiting (MAX14001 Only)* for details on inrush pulse limiting.
3) **SPI Framing Error:** After $\overline{\text{CS}}$ transitions from low to high, if the number of bits clocked in while $\overline{\text{CS}}$ was low is not an integer multiple of 16, an SPI framing error is declared and bit SPI (bit 3) in the FLAGS register is set. The instruction in the SPI shift register is not decoded and no register value is changed.
4) **Loss of Data Stream:** The field-side sends ADC

data across the isolation barrier to the logic-side every 100µs, except for the startup period. If the periodic field-side data is not received, a loss of data stream fault is declared and bit COM (bit 4) in the FLAGS register is set. It is possible to recover from a loss of data stream fault by asserting a hard reset through the ACT register, which will return all of the registers to their default state, thus requiring the MAX14001/MAX14002 to go through the startup configuration process.

5) **CRC Errors From Internal Communication:** Internal communication across the isolation barrier includes a CRC code to ensure that corrupt data does not cause system problems. If the CRC indicates an error, the received data is discarded. If six consecutive CRCs fail, a CRC fault is declared and bit CRCL (bit 5) or CRCF (bit 6) in the FLAGS register is set.

6) **High-Voltage FET Failure:** If the ADC reading is greater than the inrush re-arm threshold (INRR), and IFET is not able to sink the programmed current, a FET fault is declared and bit FET (bit 7) in the FLAGS register is set. INRR is permanently set to 0x0C0 in MAX14002.

7) **Memory Error:** The devices continually compare the bits of each verification register to the bits of their corresponding configuration register. If any of the bits do not match, a memory fault is declared and bit MV (bit 8) in the FLAGS register is set. No information on which register failed is provided. *Note that the default value for each verification register is the 1's complement of its corresponding configuration register (each verification register value is bitwise inverting of the corresponding configuration register value.), which guarantees an MV fault any time power is lost and restored*.

$\overline{\text{FAULT}}$ at Power-On

The devices' internal memory is volatile and must be reprogrammed after power cycling. To protect against undetected power glitches and the remote possibility that a memory bit would be lost during years of static operation, the devices monitor their configuration registers and assert bit MV (bit 8) in the FLAGS register any time the memory is corrupted. Verification registers have the 1's complement of the POR values compared to the configuration registers and, therefore, the MAX14001/MAX14002 start with a memory fault condition and assert the $\overline{\text{FAULT}}$ pin at startup.

Isolated Power and Data Transfer

A simplified view of the isolated power and data transfer sections is shown in the *Functional Diagram*. The logic-side supply V_{DD} powers an integrated, inductively coupled, DC-DC converter that generates a nominal 3V with just enough output current to power the field-side of the MAX14001/MAX14002 and an external circuit that consumes less than 70µA, such as an external series reference (Figure 2).

Serial data is transferred by capacitively-isolated differential transceivers. To verify reliable communication through the isolation barrier, a cyclic redundancy check (8-bit CRC) is embedded in the transmitted serial data streams. If a CRC fails, the data is discarded and no action is taken. If six consecutive CRCs fail, the CRC bit in the FLAGS register is set and $\overline{\text{FAULT}}$ is asserted if the CRC fault enable bit is set in the FLTEN register.

Configuration and Monitoring

An SPI interface is used for transferring configuration, control and diagnostic data as well as ADC readings between a master (FPGA or microcontroller) and single/multiple MAX14001/MAX14002(s). The interface can support daisy-chain configuration and consists of four ports: SCLK, $\overline{\text{CS}}$, SDI and SDO.

SPI Interface

SPI communication includes the following features:

- Support for daisy-chain operation
- Able to verify the previous command was correctly received by reading SDO on the next instruction cycle
- Able to read/verify all written registers (except ACT register)
- Identify when commands are not a multiple of 16-bits and set the SPI fault flag
- Commands of all 0s or all 1s do not change any writable registers
- A single command cannot program both the configuration and verification register
- Serial clock up to 5MHz

The command is 16-bits in length and the structure of the 16-bit data is shown in the Table 2.

Table 2. SPI Command

ADDRESS	CONTROL	DATA
5-bits A[4:0], MSB to LSB	W/$\overline{\text{R}}$ bit, Read = 0, Write = 1	10-bits D[9:0], MSB to LSB

The first bit clocked into the SDI port is D[0], the data LSB (*note: many SPI products clock MSB first so the microcontroller or FPGA needs to reverse data prior to outputting it to the MAX14001/MAX14002 SDI pin*). As long as $\overline{CS}$ is in a logic-low state, the SPI interface is working as a simple shift register, and SDI data is shifted on the rising edge of SCLK without decoding the commands. When $\overline{CS}$ goes back to logic-high state, the bits in the shift register are decoded. If the command is a write, the data portion of the SPI shift register is copied to the specified register and the shift register is unchanged. If the command is a read, the content of the specified register is copied to the data portion of the SPI shift register, while the address bits A[4:0] and control bit W/$\overline{R}$ are unchanged. The read action is completed during the next instruction cycle when $\overline{CS}$ again goes to logic-low state and the contents of the shift register are clocked out of SDO on the falling edge of SCLK.

The functionality of each SPI pin can be summarized as follows.

Serial Clock (SCLK): Input for the master serial clock signal. The clock signal determines the speed of the data transfer (5MHz maximum) and all data transfers are synchronous to this clock. SCLK must remain low when $\overline{CS}$ transitions are from high to low and from low to high. The number of SCLK rising edges that are received during $\overline{CS}$ logic-low state must be a multiple of 16. Otherwise, the received command will be ignored.

Chip Select ($\overline{CS}$): The $\overline{CS}$ input enables the SPI interface. During a logic-low state, data is transferred on the edges of SCLK. A logic-high state on $\overline{CS}$ forces SDO to high impedance mode and any SCLK transitions are ignored.

During a write cycle, the content of the shift register is transferred to the addressed internal register on the *rising edge* of $\overline{CS}$. During a read cycle, the content of the internal register that was addressed is transferred to the shift register on the *rising edge* of $\overline{CS}$ and the data will be clocked out of the SDO pin during the next SPI cycle.

Serial Input (SDI): SDI or MOSI is the serial input port of the SPI shift register and data is clocked LSB first into the shift register on the *rising edge* of SCLK. On the rising edge of $\overline{CS}$, the input data is latched into the internal registers.

Serial Output (SDO): SDO or MISO is the serial output port of the SPI shift register, and is in a high impedance state until the $\overline{CS}$ pin goes to logic-low state. Data is clocked LSB first out of the shift register on the *falling edge* of SCLK.

The SPI interface Read and Write Timing Diagrams are shown in Figure 6, Figure 7, and Figure 8.

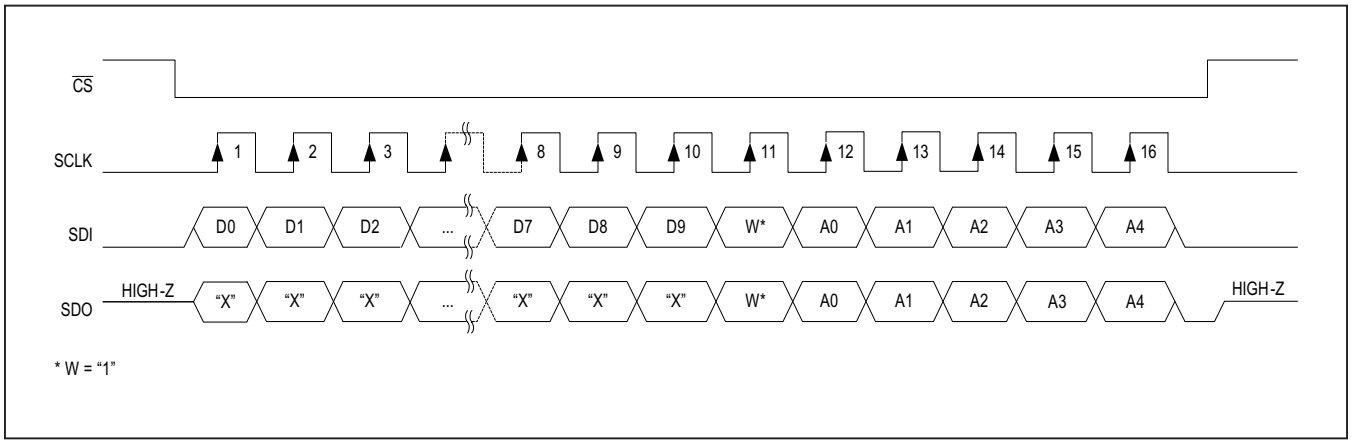


Figure 6. SPI Write

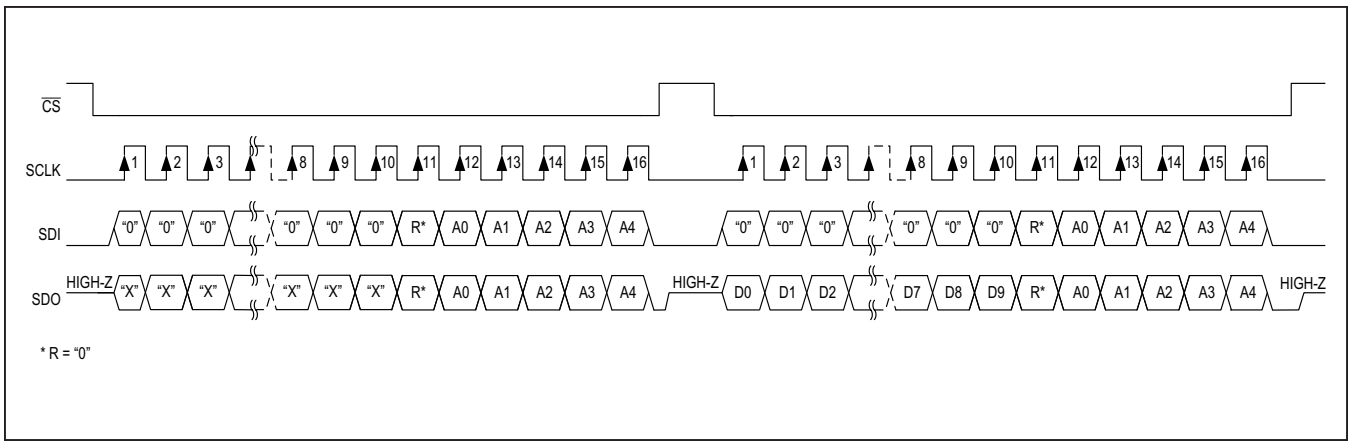


Figure 7. SPI Read

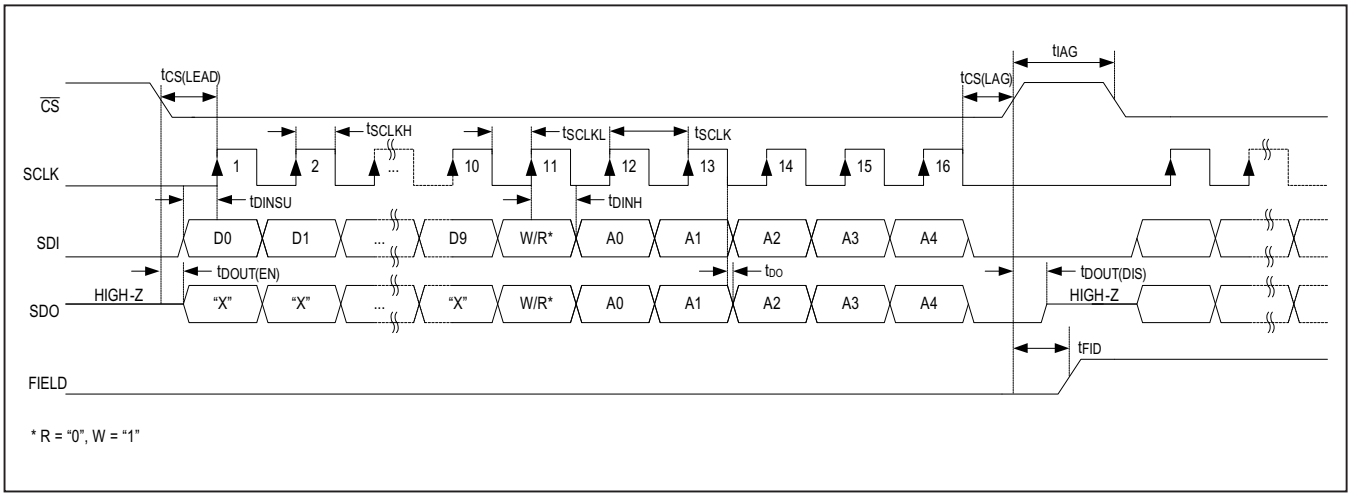


Figure 8. SPI Timing Diagram

Daisy-Chain SPI Operation

The device supports daisy-chain operation, allowing control/monitoring of multiple MAX14001/MAX14002 devices from a single serial interface host with common $\overline{CS}$ and SCLK signals as illustrated in Figure 9. The data that is clocked into SDI is clocked out of SDO with a 16-SCLK-cycle delay for each device in the daisy-chain, which is illustrated in Figure 10 and Figure 11.

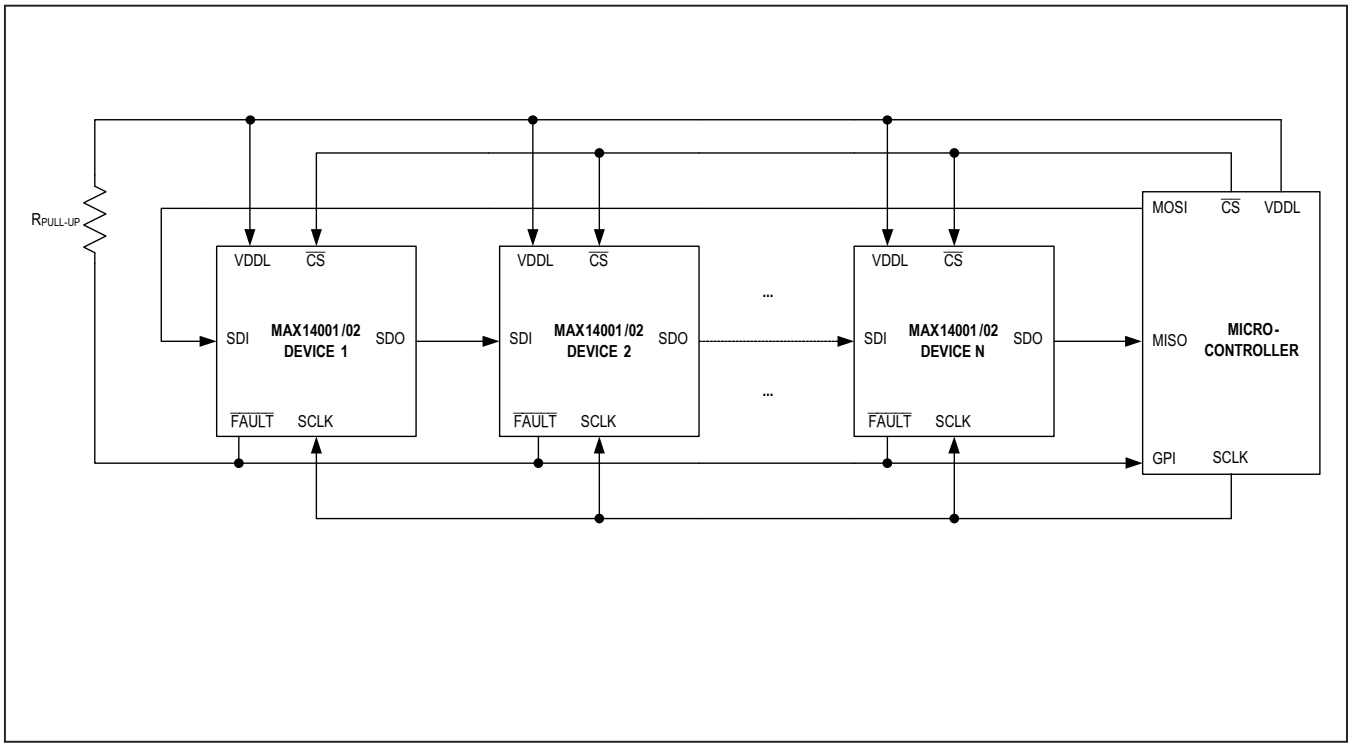


Figure 9. Daisy-Chain Connection

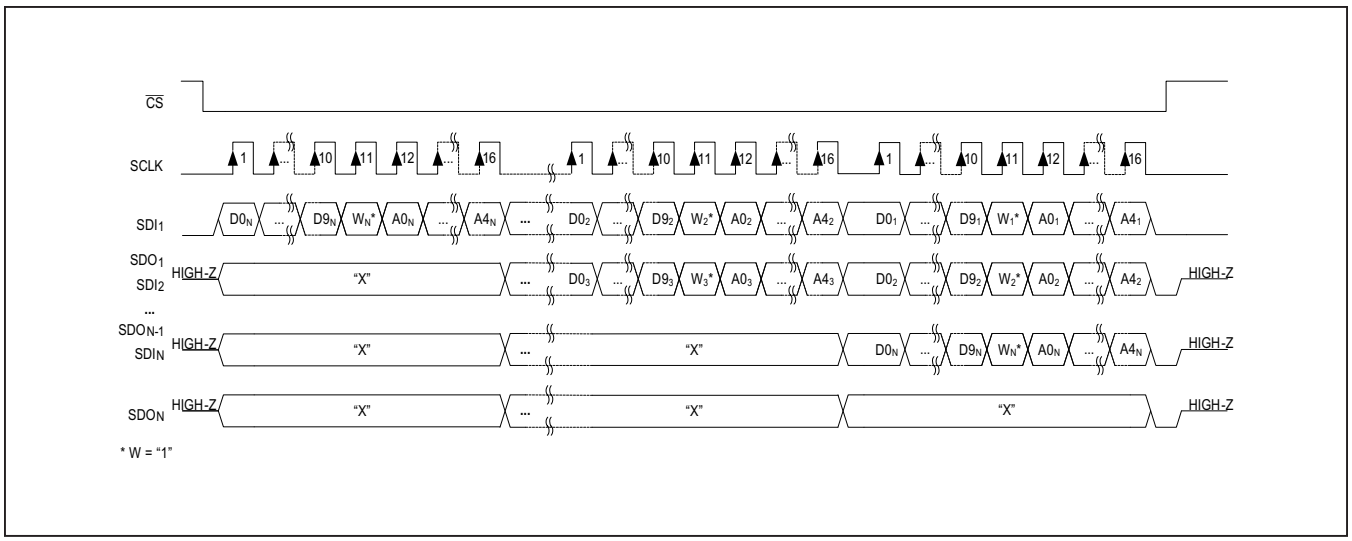


Figure 10. SPI Daisy-Chain Write

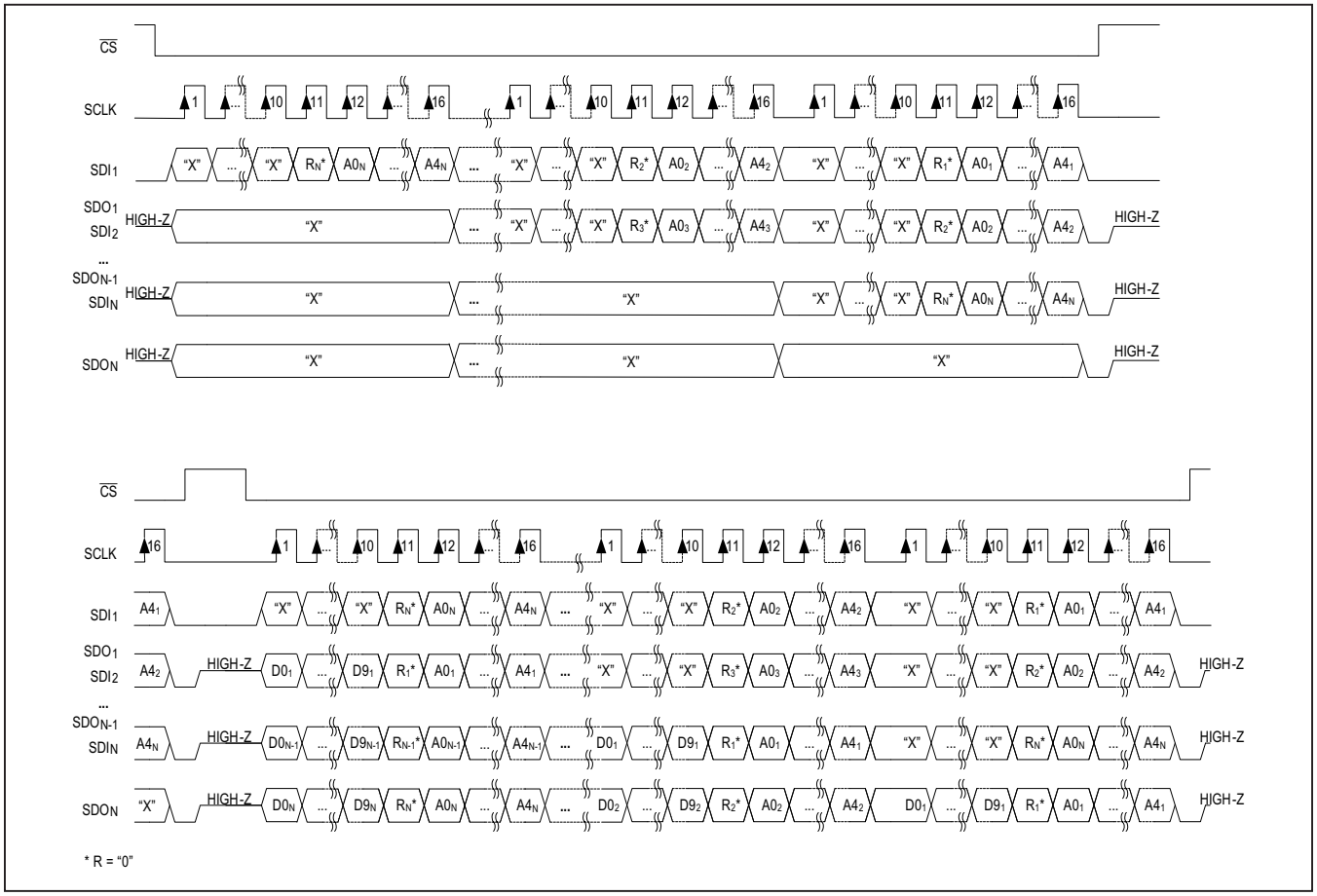


Figure 11. SPI Daisy-Chain Read

Register Map

The MAX14001/MAX14002 registers and their default Power-On-Reset (POR) values are shown in Table 3:

Table 3. Register Map

ADDR	NAME	TYPE	PURPOSE	9	8	7	6	5	4	3	2	1	0	DEFAULT
0x00	ADC	R	Unfiltered ADC reading	ADC[9:0]										
0x01	FADC	R	Filtered ADC reading	FADC[9:0]										
0x02	FLAGS	COR	Error Flags	x(6)	MV	FET	CRCF	CRCL	COM	SPI	INRD	ADC	x	0x100
0x03	FLTEN	RW	FAULT Enable	x	EMV	EFET	ECRCF	ECRCL	ECOM	ESPI	EINRD	EADC	DYEN	0x1FF
0x04	THL	RW	Lower Comparator Threshold	THL[9:0]										0x100
0x05	THU	RW	Upper Comparator Threshold	THU[9:0]										0x200
0x06	INRR	RW*	Inrush Re-arm Threshold(1)	INRR[9:0]										0x0C0
0x07	INRT	RW*	Inrush Trigger Threshold(2)	INRT[9:0]										0x180
0x08	INRP	RW*	Inrush Pulse(3)	IINR[3:0](4)				TINR[3:0]				DU[1:0]		0x1D8
0x09	CFG	RW	Configuration	IBIAS[3:0](5)				EXRF	EXTI	FT[1:0]		FAST	IRAW	0x183
0x0A	ENBL	RW	Enable	x	x	x	x	x	ENA	x	x	x	x	0x000
0x0B	ACT	WC	Action	INPLS	x	RSET	SRES	x	x	x	x	x	x	0x000
0x0C	WEN	RW	Write Enable	WEN[9:0]										0x000
0x0D-0x12			Reserved	Reserved. Do not use										
0x13	FLTV	RW	FLTEN Verification	FLTV[9:0]										0x000
0x14	THLV	RW	THL Verification	THLV[9:0]										0x2FF
0x15	THUV	RW	THU Verification	THUV[9:0]										0x1FF
0x16	INRRV	RW*	INRR Verification(1)	INRRV[9:0]										0x33F
0x17	INRTV	RW*	INRT Verification(2)	INRTV[9:0]										0x27F
0x18	INRPV	RW*	INRP Verification(3)	INRPV[9:0]										0x227
0x19	CFGV	RW	CFG Verification	CFGV[9:0]										0x27C
0x1A	ENBLV	RW	Enable Verification	ENBLV[9:0]										0x3FF
0x1B-0x1F			Reserved	Reserved. Do not use										

** Register is read only for the MAX14002*

Notes:

1: INRR = INRRV = 0x0C0 for MAX14002

2: INRT = INRTV = 0x180 for MAX14002

3: INRP = INRPV = 0x1D8 for MAX14002

4: Setting IINR = 0 forces IFET = 50µA

5: Setting IBIAS = 0 forces IFET = 50µA

6. "x" is unused.

Register Type Legend:

R - Read only

RW - Read and write

COR - Latched read only, clear on read

WC - Write and clear (Write only, executes and clears immediately)

Register Detailed Description

ADC (Read)

Address = 0x00

BIT	FIELD NAME	DESCRIPTION
9:0	ADC[9:0]	Contains the latest ADC reading (straight binary)

FADC (Read)

Address = 0x01

BIT	FIELD NAME	DESCRIPTION
9:0	FADC[9:0]	Contains the latest filtered ADC reading as set by bits FT[1:0] in the CFG register (straight binary)

FLAGS (Latched, Clear On Read)

Address = 0x02

Default = 0x100

Latched flags indicate errors and why the $\overline{FAULT}$ pin was asserted if the fault is enabled in the FLTEN register. Reading the register clears all flags.

Note: Faults conditions are latched and the relevant bits are set; reading the value of this register will reset the fault flags that are not active anymore. However, if the fault is still valid, reading the FLAGS register will not be able to clear the specific bit.

BIT	FIELD NAME	DESCRIPTION
0	FLAG0	Unused
1	ADC	ADC reading stuck at one value
2	INRD	Exceeding specified duty-cycle for the inrush current
3	SPI	Number of bits clocked in while $\overline{CS}$ was asserted is not an integer multiple of 16
4	COM	Field-side communication failure
5	CRCL	Field-to-logic-side transmission had 6 consecutive CRC errors reported
6	CRCF	Logic-to-field-side transmission had 6 consecutive CRC errors reported
7	FET	Input voltage detected without input current
8	MV	Failed memory validation
9	FLAG9	Unused

FLTEN (Read/Write)

Address = 0x03

Default = 0x1FF

Enables fault conditions to assert the $\overline{\text{FAULT}}$ signal.

Note: Fault enable bits only effect fault reporting through the $\overline{FAULT}$ pin. Bits in the FLAGS register will be set regardless whether fault is enabled or disabled by the FLTEN register.

BIT	FIELD NAME	DESCRIPTION
0	DYEN	0: $\overline{\text{FAULT}}$ is latched; it is cleared after the FLAGS register is read. 1: $\overline{\text{FAULT}}$ is dynamic; it is cleared as soon as the fault condition disappears. (Default)
1	EADC	0: Prevents ADC error from asserting $\overline{\text{FAULT}}$ 1: Allows ADC error to assert $\overline{\text{FAULT}}$ (Default)
2	EINRD	0: Prevents INRD error from asserting $\overline{\text{FAULT}}$ 1: Allows INRD error to assert $\overline{\text{FAULT}}$ (Default)
3	ESPI	0: Prevents SPI error from asserting $\overline{\text{FAULT}}$ 1: Allows SPI error to assert $\overline{\text{FAULT}}$ (Default)
4	ECOM	0: Prevents COM error from asserting $\overline{\text{FAULT}}$ 1: Allows COM error to assert $\overline{\text{FAULT}}$ (Default)
5	ECRCL	0: Prevents CRCL error from asserting $\overline{\text{FAULT}}$ 1: Allows CRCL error to assert $\overline{\text{FAULT}}$ (Default)
6	ECRCF	0: Prevents CRCF error from asserting $\overline{\text{FAULT}}$ 1: Allows CRCF error to assert $\overline{\text{FAULT}}$ (Default)
7	EFET	0: Prevents FET error from asserting $\overline{\text{FAULT}}$ 1: Allows FET error to assert $\overline{\text{FAULT}}$ (Default)
8	EMV	0: Prevents MV error from asserting $\overline{\text{FAULT}}$ 1: Allows MV error to assert $\overline{\text{FAULT}}$ (Default)
9	FLTEN9	Unused

THL (Read/Write)

Address = 0x04

Default = 0x100

User-programmed lower comparator threshold. When the output of the comparator is high, this value is compared to ADC (or FADC as set by IRAW, FT0 and FT1). If ADC ≤ THL, the comparator output COUT is set low. To prevent oscillation, the value of THL should be smaller than THU.

BIT	FIELD NAME	DESCRIPTION
9:0	THL[9:0]	Lower comparator threshold (straight binary)

THU (Read/Write)

Address = 0x05

Default = 0x200

User-programmed upper comparator threshold. When the output of the comparator is low, this value is compared to ADC (or FADC as set by IRAW, FT0, and FT1). If ADC ≥ THU, the comparator output COUT is set high. To prevent oscillation, the value of THU should be larger than THL.

BIT	FIELD NAME	DESCRIPTION
9:0	THU[9:0]	Upper comparator threshold (straight binary)

INRR (Read/Write) (Read only for MAX14002)

Address = 0x06

Default = 0x0C0

User-programmed inrush timer re-arm threshold. ADC reading must drop below this value before another inrush pulse will occur when the input voltage exceeds INRT. This register is not used in the MAX14002, which always uses FAST mode (see bit 1 of the CFG register).

BIT	FIELD NAME	DESCRIPTION
9:0	INRR[9:0]	Inrush re-arm threshold (straight binary)

INRT (Read/Write) (Ready only for MAX14002)

Address = 0x07

Default = 0x180

User-programmed inrush current trigger threshold. When the inrush timer is armed, an inrush pulse is initiated when the ADC reading equals or exceeds this value. This register is not used in the MAX14002, which always uses FAST mode (see bit 1 of the CFG register).

BIT	FIELD NAME	DESCRIPTION
9:0	INRT[9:0]	Inrush trigger threshold (straight binary)

INRP (Read/Write) (Read only for MAX14002)

Address = 0x08

Default = 0x1D8

Contains user-programmed values for the inrush current pulse magnitude, inrush pulse duration, and inrush pulse duty cycle.

IT	FIELD NAME	DESCRIPTION
1:0	DU[1:0]	DU1 and DU0 set the maximum duty cycle for inrush current over the last 10 seconds. DU[1:0] = 00 Duty Cycle limiting function off (Default) DU[1:0] = 01 Duty Cycle = 1.6% DU[1:0] = 10 Duty Cycle = 3.1% DU[1:0] = 11 Duty Cycle = 6.3%
5:2	TINR[3:0]	4-bit inrush time, 0 to 120ms in 8ms steps, straight binary TINR[3:0] = 0000 = 0ms TINR[3:0] = 0001 = 8ms ..... TINR[3:0] = 0110 = 48ms (Default) ……. TINR[3:0] = 1110 = 112ms TINR[3:0] = 1111 = 120ms
9:6	IINR[3:0]	4-bit inrush current, 50µA to 105mA in 7mA steps, straight binary IINR[3:0] = 0000 = 50µA IINR[3:0] = 0001 = 7mA ..... IINR[3:0] = 0111 = 49mA (Default) ……. IINR[3:0] = 1110 = 98mA IINR[3:0] = 1111 = 105mA

CFG (Read/Write)

Address = 0x09

Default = 0x183

Configuration register controls functions within the MAX14001/MAX14002.

BIT	FIELD NAME	DESCRIPTION
0	IRAW	Selects Inrush comparator input multiplexer 0: Inrush comparator input is connected to filtered data in the FADC register 1: Inrush comparator input is connected to 'raw' data in the ADC register (default)
1	FAST	Selects FAST Inrush Mode. ADC is not used to trigger inrush. Inrush starts as soon as sufficient voltage is present at high-voltage FET to provide the current. Inrush timer is reset when there is not sufficient voltage to sustain the bias/inrush current. *Note: MAX14002 only works in FAST inrush mode*. 0: ADC controlled (unused in MAX14002) 1: FAST inrush mode (default)
3:2	FT[1:0]	FT1 and FT0 control the number of readings that are averaged in the ADC filter FT[1:0] = 00 Filtering off (default) FT[1:0] = 01 Average 2 readings FT[1:0] = 10 Average 4 readings FT[1:0] = 11 Average 8 readings
4	EXTI	Connects the 70µA current source to the REFIN pin. This current powers an external shunt voltage reference. 0: Current source off (default) 1: Current source on and connected to the REFIN pin (external shunt reference)
5	EXRF	Selects the voltage reference source for the ADC. 0: Internal voltage reference enabled (default) 1: External voltage reference enabled
9:6	IBIAS[3:0]	4-bit bias current, 50µA to 3.75mA in 0.25mA steps. This current flows through the high-voltage FET when not in inrush mode. IBIAS[3:0] = 0000 = 50µA IBIAS[3:0] = 0001 = 0.25mA ..... IBIAS[3;0] = 0110 = 1.5mA (Default) ……. IBIAS[3:0] = 1110 = 3.5mA IBIAS[3:0] = 1111 = 3.75mA

ENBL (Read/Write)

Address = 0x0A

Default = 0x000

The ENA bit in the ENBL register enables the inrush and bias current. At POR, ENA is set to “0”. After programming all the configuration registers, the user sets ENA to “1”, which enables the IFET current sink. This procedure prevents unintentional currents from flowing during the configuration process. It is recommended to set this bit at the very end of the configuration procedure.

BIT	FIELD NAME	DESCRIPTION
3:0	ENBL[3:0]	Unused
4	ENA	0: Prevents the field-side current sink (default) 1: Enables the field-side current sink
9:5	ENBL[9:5]	Unused

ACT (Write and Clear)

Address = 0x0B

Default = 0x000

Immediate action register. When a bit is written to this register, action is taken immediately and the bit is then cleared.

Note: The SRES bit (bit 6) resets only the SPI registers while the RSET bit (bit 7) is acting as the global POR, the DC-DC converter will turn off and field-side will be reset as well as the logic-side (SPI interface).

BIT	FIELD NAME	DESCRIPTION
5:0	ACT[5:0]	Unused
6	SRES	Software reset. Restores all registers to their POR value. 0: Normal operation (default) 1: Software reset
7	RSET	Reset. Has the same effect as a power on reset. 0: Normal operation (default) 1: Reset
8	ACT8	Unused
9	INPLS	Trigger an inrush current pulse. Has no effect when ENA = 0 (in the ENBL Register) 0: Normal operation (default) 1: Trigger an inrush current

WEN (Read/Write)

Address = 0x0C

Default = 0x000

Write enable register. A value of 0x294 in this register enables writing to the SPI registers. Set to 0x294 prior to writing to any configuration or verification registers. Set to 0x000 after configuring all registers. Its purpose is to make it highly unlikely that any settings will be unintentionally changed by noise on the SPI bus.

Note: This register should be reset to 0x000 after configuring the device prior to normal operation.

BIT	FIELD NAME	DESCRIPTION
9:0	WEN[9:0]	This register must be set to 0x294 prior to writing to any SPI registers.

FLTV (Read/Write)

Address = 0x13

Default = 0x000

FLTEN verification register. Bits are continually compared to the FLTEN register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of FLTEN register POR value.

BIT	FIELD NAME	DESCRIPTION
9:0	FLTV[9:0]	FLTEN verification register. Bits are continually compared to the FLTEN register.

THLV (Read/Write)

Address = 0x14

Default = 0x2FF

THL verification register. Bits are continually compared to the THL register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of THL register POR value.

BIT	FIELD NAME	DESCRIPTION
9:0	THLV[9:0]	THL verification register. Bits are continually compared to the THL register.

THUV (Read/Write)

Address = 0x15

Default = 0x1FF

THU verification register. Bits are continually compared to the THU register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of THU register POR value.

BIT	FIELD NAME	DESCRIPTION
9:0	THUV[9:0]	THU verification register. Bits are continually compared to the THU register.

INRRV (Read/Write) (Read only for MAX14002)

Address = 0x16

Default = 0x33F (0x0C0 for MAX14002)

INRR verification register. Bits are continually compared to the INRR register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of INRR register POR value.

Note: this register is not used in MAX14002. Default value is fixed at 0x0C0.

BIT	FIELD NAME	DESCRIPTION
9:0	INRRV[9:0]	INRR verification register. Bits are continually compared to the INRR register.

INRTV (Read/Write) (Read only for MAX14002)

Address = 0x17

Default = 0x27F (0x180 for MAX14002)

INRT verification register. Bits are continually compared to the INRT register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of INRT register POR value.

Note: this register is not used in MAX14002. Default value is fixed at 0x180.

BIT	FIELD NAME	DESCRIPTION
9:0	INRTV[9:0]	INRT verification register. Bits are continually compared to the INRT register.

INRPV (Read/Write) (Read only for MAX14002)

Address = 0x18

Default = 0x227 (0x1D8 for MAX14002)

INRP verification register. Bits are continually compared to the INRP register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of INRP register POR value.

Note: this register is not used in MAX14002. Default value is fixed at 0x1D8.

BIT	FIELD NAME	DESCRIPTION
9:0	INRPV[9:0]	INRP verification register. Bits are continually compared to the INRP register.

CFGV (Read/Write)

Address = 0x19

Default = 0x27C

CFG verification register. Bits are continually compared to the CFG register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of CFG register POR value.

BIT	FIELD NAME	DESCRIPTION
9:0	CFGV[9:0]	CFG verification register. Bits are continually compared to the CFG register.

ENBLV (Read/Write)

Address = 0x1A

Default = 0x3FF

ENBL verification register. Bits are continually compared to the ENBL register. If any bits do not match, the MV bit in the FLAGS register is set and $\overline{FAULT}$ is asserted if the EMV bit in the FLTEN register is set. POR value is 1's complement of ENBL register POR value.

BIT	FIELD NAME	DESCRIPTION
9:0	ENBLV[9:0]	ENBL verification register. Bits are continually compared to the ENBL register.

Configuration Flowchart

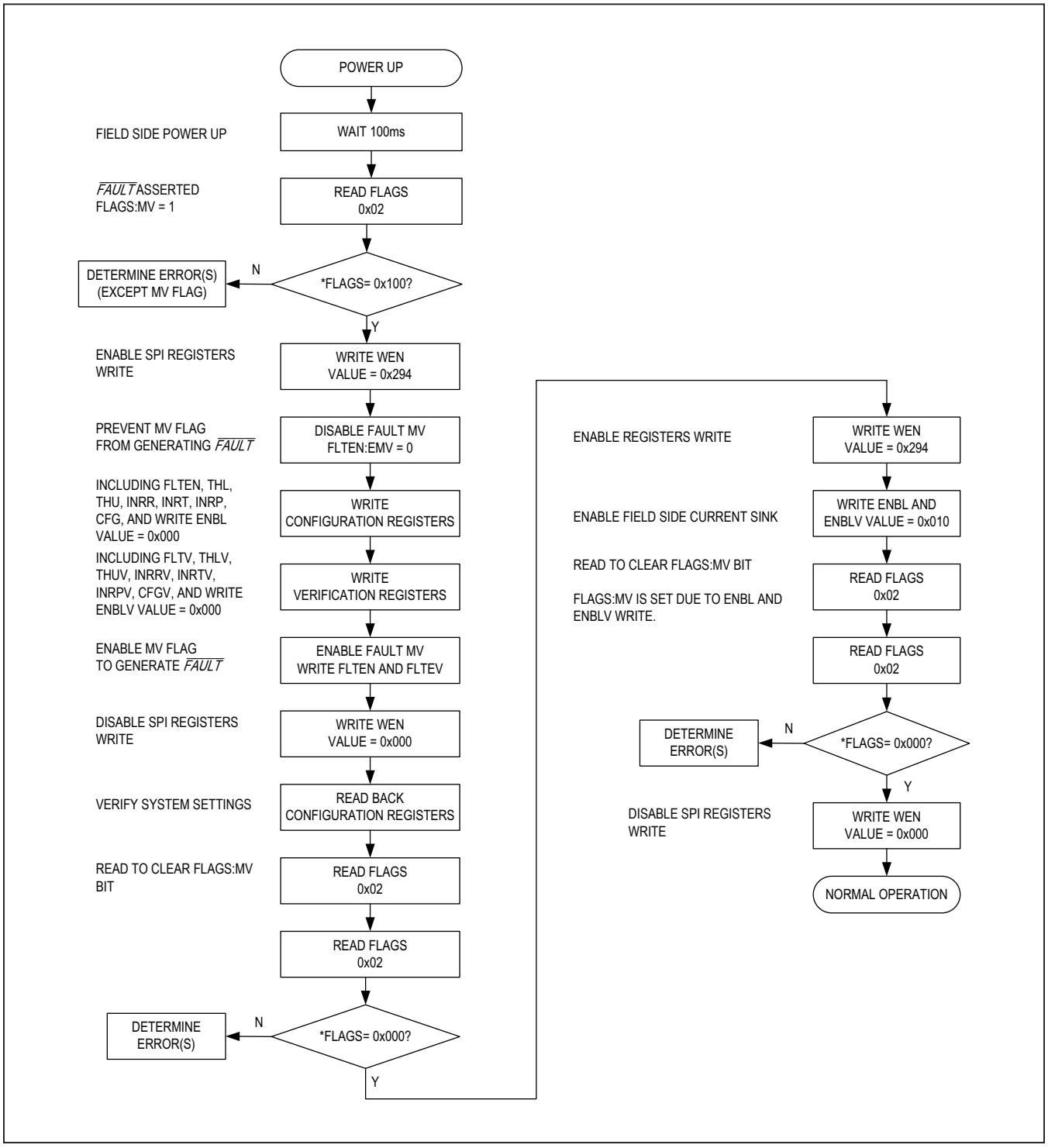


Figure 12. Register Programming for Configuration of MAX14001/MAX14002 After Power-On-Reset

MAX14002 vs. MAX14001

The MAX14002 is a reduced functionality version of the MAX14001. The MAX14002 only works in FAST mode and does not limit the number of inrush pulses. In the MAX14002, write access is permanently disabled to three registers: INRR, INRT, and INRP. In addition to disabling write access to these registers, the three corresponding verification registers INRRV, INRTV, and INRPV will default to the same value as the configuration registers, and an MV fault in the FLAGS register related to these registers is not generated during startup unless the memory is corrupted.

All other functions are the same as the MAX14001.

Applications Information

Typical Application Circuit

The MAX14001/MAX14002 are designed for industrial configurable binary input applications. The input voltage on the field-side is continuously measured by the integrated ADC, and results are transmitted across the isolation barrier and compared to the programmable high and low thresholds on the logic-side. The COUT pin presents the real-time result of the comparison and notifies the system if the binary input is a logic-high/logic-low voltage level.

The MAX14001/MAX14002 also provide current control through a high-voltage depletion mode FET. While the drain of the high-voltage FET is connected to the binary module input, the gate voltage of the FET is set at a nominal 3.6V by the MAX14001/MAX14002's GATE pin. The IFET pin is connected to the source of the FET to sink a programmable inrush or bias current. When the binary module input voltage is higher than the trigger threshold, typically in the case of an external relay closing, an inrush current is triggered to clean the relay contacts. Control of the inrush current allows the binary input module to be used in different pulse counting and relay monitoring applications. See the *Typical Application Circuit* for connection between the devices and the high-voltage FET.

These devices are configured and monitored through an SPI interface. The $\overline{FAULT}$ output can be configured to generate an interrupt when certain errors are detected by the embedded self-diagnostic circuit. $\overline{FAULT}$ is an open-drain digital output so an external pullup resistor is needed, typically 4.7kΩ.

Layout, Grounding and Bypassing

Power Supply Recommendations

It is recommended to decouple both the V_{DD} and V_{DDL} supplies with 10µF capacitors in parallel with 1000pF capacitors to GNDL. Place the 1000pF capacitors as close to V_{DD} and V_{DDL} as possible. It is preferred to decouple the V_{DD} pin through the GNDL pin 11, and the V_{DDL} pin through the GNDL pin 19. The V_{DDF} pin is the integrated DC-DC converter output and it is recommended to decouple it with low-ESR capacitors of 0.1µF in parallel with 1000pF to GNDF (pin 10). Place the 1000pF capacitor as close to V_{DDF} as possible.

For best performance, bypass the GATE pin to the GNDF plane with a low-ESR capacitor of 0.01µF and bypass the IFET pin to the GNDF plane with a low-ESR capacitor of 1000pF. REFIN is the optional external voltage reference input, and, for best performance, bypass REFIN to AGND with a 0.1µF ceramic capacitor when an external voltage reference is used. Refer to the *Typical Application Circuit* for a connection example.

Layout Considerations

It is recommended to design an isolation or keep-out channel underneath the MAX14001/MAX14002 that is free from ground and signal planes. Any galvanic or metallic connection between the field-side and the logic-side defeats the isolation.

Ensure that the decoupling capacitors between V_{DDL}, V_{DD} and GNDL and between V_{DDF} and GNDF are located as close as possible to the IC to minimize inductance.

Route important signal lines close to the ground plane to minimize possible external influences. On the field-side, it is good practice to separate the ADC input and voltage reference ground AGND from the GATE and IFET reference ground GNDF.

High-Voltage FET

The MAX14001/MAX14002 are designed to use a low cost, readily available high-voltage depletion mode FET as the external high-voltage power device. The high voltage binary input is connected to the FET's drain while the gate and source are at low voltages compatible with the MAX14001/MAX14002. The FET is driven in a cascade fashion with its gate held at a constant voltage by the GATE pin. The IFET pin sinks the specified inrush or bias current from the FET's source and in the process modulates the FET's source voltage. Refer to the *Typical Application Circuit* for a connection example.

The MAX14001/MAX14002 need at least 1V on the IFET pin under worst-case conditions. With a typical voltage of 3.6V, the GATE pin provides a maximum V_{GS} of 2.6V to the FET. The required maximum FET on resistance R_{ON} can be calculated as:

$$R_{ON} \leq (V_{DRAIN} - V_{IFET})/I_{INRUSH}$$

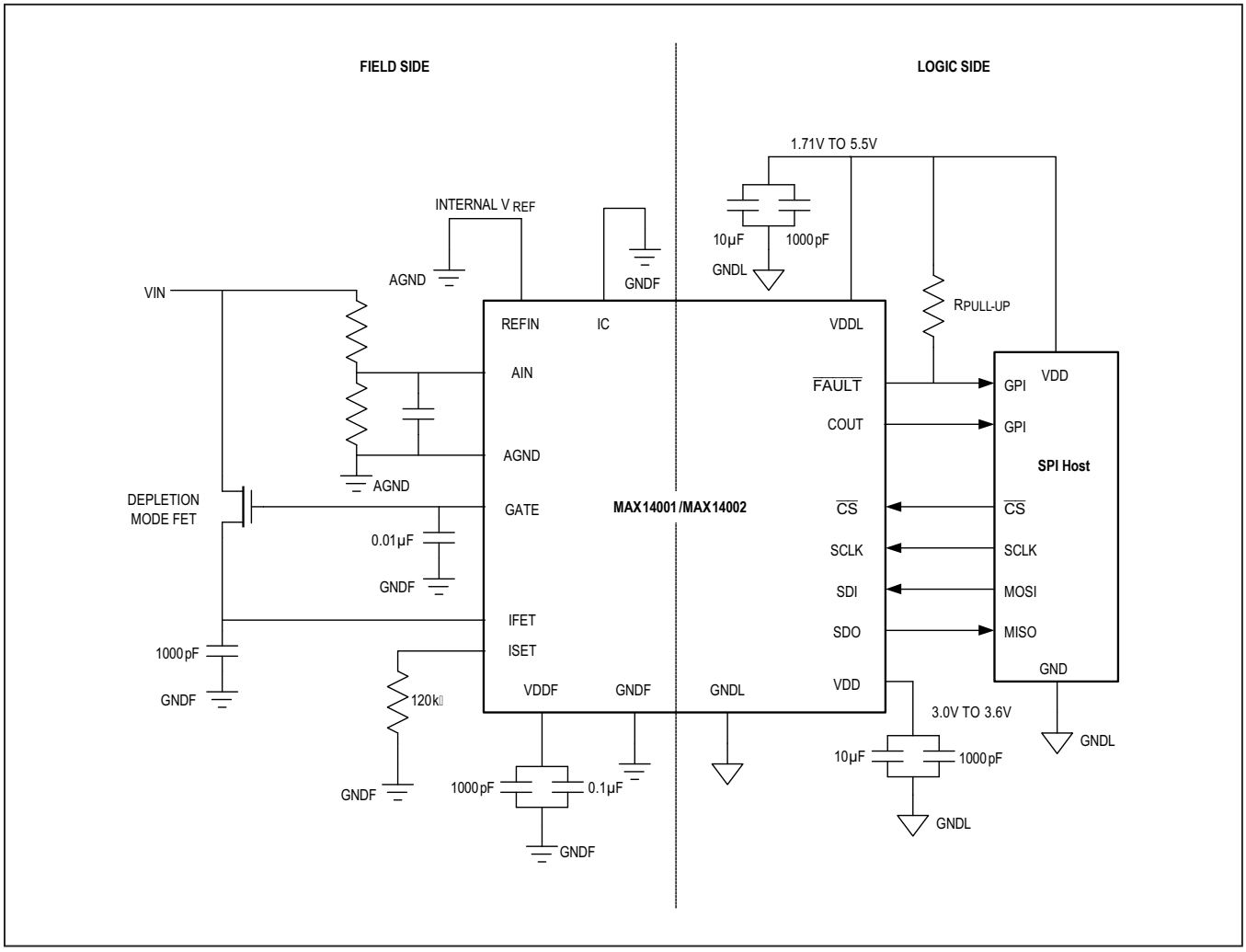
Where I_{INRUSH} can be configured to 105mA maximum and V_{IFET} = 1V. For example, if the FET V_{DRAIN} = 24V, the maximum R_{ON} is calculated to be 219Ω at V_{GS} = 2.6V.

When selecting the FET, temperature tolerance should also be taken into consideration.

For applications where the peak input voltage does not exceed 600V, it is recommended to use the following devices:

- Infineon BSP135
- IXYS IXTY08N100D2

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14001AAP+	-40°C to 125°C	20-SSOP
MAX14002AAP+	-40°C to 125°C	20-SSOP

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
SSOP-20	A20MS-6	21-0056	90-0094

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/16	Initial release	—
1	8/17	Added UL certification and general data sheet updates	1, 16, 21, 22, 30

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