Click here to ask an associate for production status of specific part numbers.

MAX16712

Dual-Output, 6A, 2MHz, 2.7V to 16V Step-Down Switching Regulator

General Description

The MAX16712 is a dual-output, fully integrated, highly efficient, step-down DC-DC switching regulator. The device operates from 2.7V to 16V input supplies, and each output can be regulated from 0.5V to 5.8V. The IC delivers up to 6A of load current per output. The two outputs can be connected in parallel as a single-output, dual-phase regulator that supports up to 12A load current.

The switching frequency of the device can be configured from 500kHz to 2.0MHz and provides the capability of optimizing the design in terms of solution size and performance.

The MAX16712 utilizes fixed-frequency, current-mode control with internal compensation. The dual-switching regulators operate 180° out-of-phase. The IC features an advanced modulation scheme (AMS) and selectable discontinuous current mode (DCM) operation to provide improved performance. Operation settings and configurable features can also be selected by connecting a pin-strap resistor from PGM0 pin to ground.

The MAX16712 has an internal 1.8V LDO output to power the gate drives (V_{CC}) and internal circuitry (AVDD).

The MAX16712 integrates multiple protections including positive and negative overcurrent protection, output overvoltage protection and overtemperature protection to ensure robust design.

The device is available in a compact 2.2mm x 3.5mm wafer-level package (WLP). It supports -40°C to +125°C junction temperature operation.

Applications

- Communications Equipment
- Networking Equipment
- Servers and Storage Equipment
- Point-of-Load (POL) Voltage Regulators
- µP Chipsets
- Memory V_{DDQ}
- I/O Pins of an FPGA/DSP/MCU

Ordering Information **appears at end of data sheet.**

Benefits and Features

- High Power Density with Low Component Count
  - Dual-Output or Dual-Phase Operation
  - Single-Supply Operation with Integrated LDO for Bias Generation
  - Compact 2.2mm x 3.5mm, 28-Bump WLP
  - Internal Compensation
- Wide Operating Range
  - 2.7V to 16V Input Voltage Range
  - 0.5V to 5.8V Output Voltage Range
  - 500kHz to 2MHz Configurable Switching Frequency
  - -40°C to +125°C Junction Temperature Range
  - Three Programming Pins to Select Different Configurations
  - Independent Enable and Power Good for Each Output
- Optimized Performance and Efficiency
  - 90.5% Peak Efficiency with V_{DDH} = 12V, V_{OUT} = 1.8V, and f_{SW} = 1MHz
  - Interleaved 180° Out-of-Phase Operation
  - AMS to Improve Load Transient
  - Selectable DCM to Improve Light Load Efficiency
  - Active Current Balancing for Dual-Phase Operation

DESCRIPTION	CURRENT RATING* (DUAL-PHASE) (A)	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)
Electrical Rating	12	2.7 to 16	0.5 to 5.8
Thermal Rating T_A = +55°C, 200LFM Airflow	12	12	3.3
Thermal Rating T_A = +85°C, No Airflow	10	12	0.8

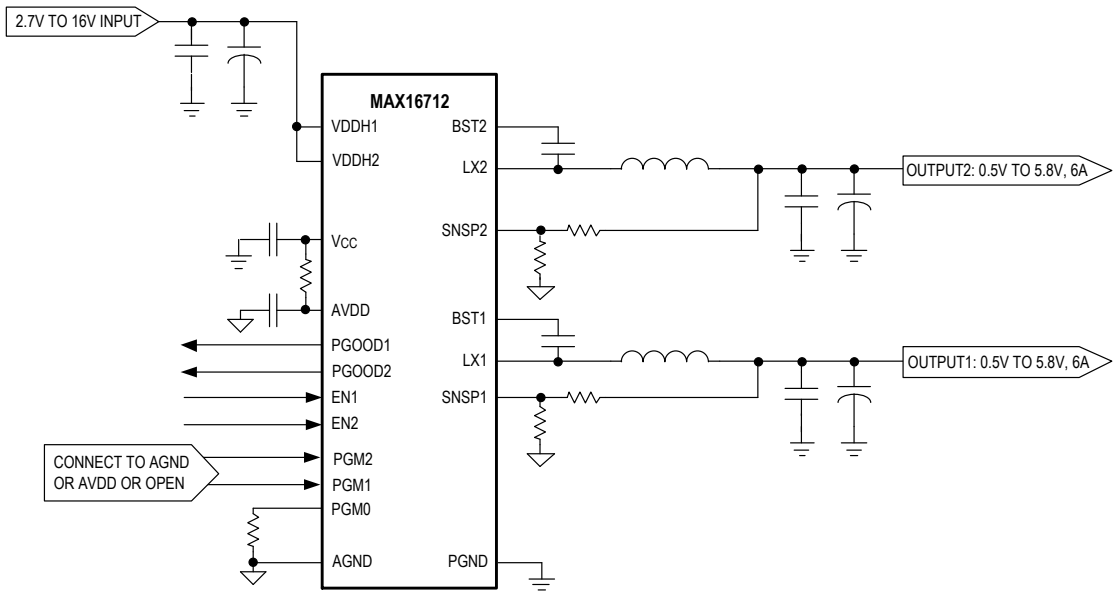
**Maximum T_J = +125°C. For specific operating conditions, see the Safe Operating Area (SOA) curves in the Typical Operating Characteristics section.*

19-101017; Rev 1; 2/22

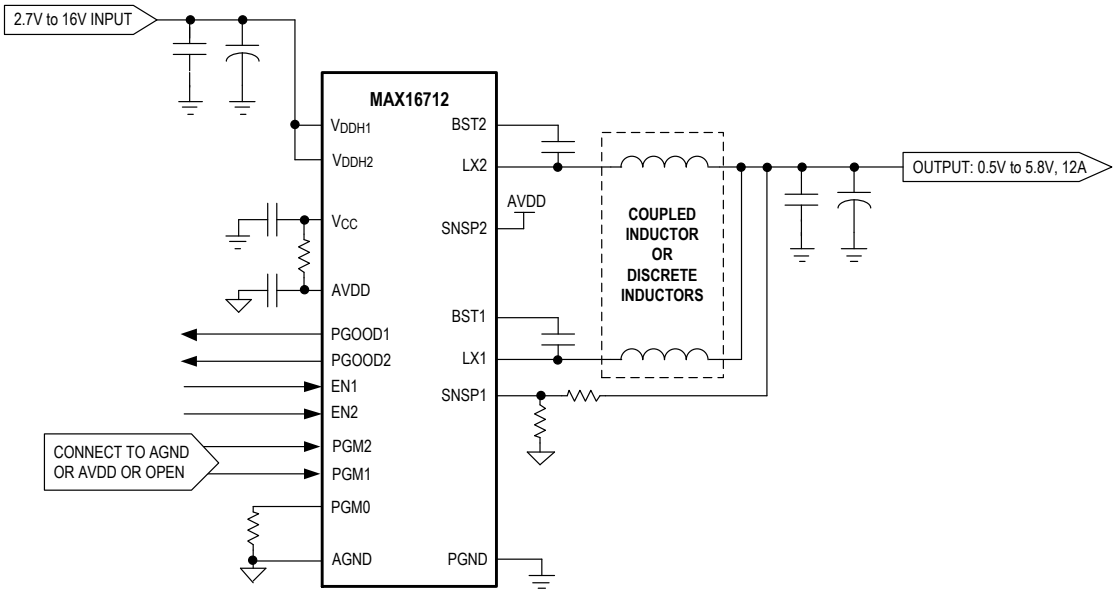
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Simplified Block Diagram

DUAL-OUTPUT APPLICATION CIRCUIT



SINGLE-OUTPUT, DUAL-PHASE APPLICATION CIRCUIT



Absolute Maximum Ratings

V_{DDH1}, V_{DDH2} to PGND (Note 1) ..... -0.3V to +19V
LX1, LX2 to PGND (DC) ..... -0.3V to +19V
LX1, LX2 to PGND (AC) (Note 2) ..... -10V to +23V
V_{DDH1} to LX1 (DC) (Note 1) ..... -0.3V to +19V
V_{DDH1} to LX1 (AC) (Note 2) ..... -10V to +23V
V_{DDH2} to LX2 (DC) (Note 1) ..... -0.3V to +19V
V_{DDH2} to LX2 (AC) (Note 2) ..... -10V to +23V
BST1, BST2 to PGND (DC) ..... -0.3V to +21.5V
BST1, BST2 to PGND (AC) (Note 2) ..... -7V to +25.5V
BST1 to LX1 ..... -0.3V to +2.5V
BST2 to LX2 ..... -0.3V to +2.5V

PGND to AGND ..... -0.3V to +0.3V
V_{CC} to PGND ..... -0.3V to +2.5V
AVDD to AGND ..... -0.3V to +2.5V
EN1, EN2 to AGND ..... -0.3V to +4V
PGOOD1, PGOOD2 to AGND ..... -0.3V to +4V
SNSP1, SNSP2 to AGND ..... -0.3V to AVDD + 0.3V
PGM0, PGM1, PGM2 to AGND ..... -0.3V to AVDD + 0.3V
Peak LX_ Current ..... -12A to +19A
Junction Temperature (T_J) (Note 3) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Peak Reflow Temperature Lead-Free ..... +260°C

Note 1: Input HF capacitors placed not more than 40 mils away from the V_{DDH} pin required to keep inductive voltage spikes within Absolute Maximum limits.

Note 2: AC is limited to 25ns.

Note 3: Recommended operating junction temperature from -40°C to +125°C. The device guarantees 90k hours of continuous operation with 6A output current per output/phase at +85°C junction temperature, or 40k hours of continuous operation with 4.8A output current per output/phase at +105°C junction temperature, for a typical application with 12V input, 1.2V output.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28 WLP

Package Code	W282D3Z+1
Outline Number	*21-100392*
Land Pattern Number	Refer to *Application Note 1891*
Junction-to-Ambient Thermal Resistance (θ_{JA}) JEDEC	42.26°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) on MAX16712EVKIT# (no heat sink, no airflow)	27.3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(See the Typical Application Circuits V_{DDH} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{DDH}		2.7		16	V
Input Supply Current	I_{VDDH}	EN_ = AGND		2.2		mA
Internal LDO Regulated Output	V_{CC}		1.71		1.95	V
Linear Regulator Current Limit			80			mA
		V_{CC} < 1.6V		20		
AVDD Undervoltage Lockout	$AVDD_{UVLO}$	Rising	1.65	1.67	1.70	V
AVDD Undervoltage Lockout Hysteresis				55		mV
$V_{DDH_}$ Undervoltage Lockout	V_{DDH_UVLO}	Rising	2.4	2.5	2.6	V
$V_{DDH_}$ Undervoltage Lockout Hysteresis				100		mV
$V_{DDH_}$ Overvoltage Lockout	V_{DDH_OVLO}	Rising	17.3	17.8	18.3	V
$V_{DDH_}$ Overvoltage Lockout Hysteresis				500		mV
OUTPUT VOLTAGE RANGE AND ACCURACY						
Internal Reference Voltage			0.495	0.500	0.505	V
		T_A = T_J = 0°C to +85°C	0.497	0.500	0.503	
Voltage Sense Leakage Current	$I_{SNSP_}$	T_A = T_J = +25°C			1	µA
SWITCHING FREQUENCY						
Switching Frequency	$f_{SW_}$			500		kHz
				600		
				750		
				1000		
				1200		
				1500		
				2000		
Switching Frequency Accuracy			-10		+10	%
Phase Shift Between Two Outputs/Phases				180		degrees
Minimum Controllable On-Time		I_{OUT} = 0A (Note 4)			50	ns
Minimum Controllable Off-Time		I_{OUT} = 0A (Note 4)			110	ns
ENABLE AND STARTUP						
Initialization Time	t_{INIT}			800		µs
EN_ Threshold		Rising	0.9			V
		Falling			0.6	

(See the Typical Application Circuits V_{DDH} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN_ Filtering Delay	$t_{EN_RISING_DELAY}$	Rising		200		µs
	$t_{EN_FALLING_DELAY}$	Falling		2		
Soft-Start Time	t_{SS}			3		ms
POWER-GOOD AND FAULT PROTECTIONS						
PGOOD_ Output Low		$I_{PGOOD_}$ = 4mA			0.4	V
Output Undervoltage (UV) Threshold			-16	-13	-10	%
Output UV Deglitch Delay				2		µs
Output Overvoltage Protection (OVP) Threshold			10	13	16	%
Output OVP Deglitch Delay				2		µs
Positive Overcurrent Protection (POCP) Threshold	POCP	Inductor Peak Current, POCP = 9A	8.1	9.0	9.9	A
		Inductor Peak Current, POCP = 6A	5.4	6.0	6.6	
		Inductor Peak Current, POCP = 4.5A	4.05	4.50	4.95	
POCP Deglitch Delay				36		ns
Fast Positive Overcurrent Protection (FPOCP) Threshold	FPOCP		12.5	14.5	16.5	A
Negative Overcurrent Protection (NOCP) Threshold to POCP Threshold Ratio	NOCP	With respect to POCP threshold (typ)		-83		%
NOCP Accuracy			-20		+20	%
BST UVLO Threshold	V_{BST}	Rising	1.47	1.57	1.62	V
BST UVLO Threshold Hysteresis				60		mV
Overtemperature Protection (OTP) Rising Threshold	OTP			155		°C
OTP Accuracy				6		%
OTP Hysteresis				20		°C
Hiccup Protection Time	t_{HICCUP}	OVP, POCP, or NOCP		20		ms
DCM OPERATION MODE						
DCM Comparator Threshold to Enter DCM		POCP = 9A, Inductor Valley Current		-440		mA
		POCP = 6A, Inductor Valley Current		-310		
		POCP = 4.5A, Inductor Valley Current		-220		
DCM Comparator Threshold to Exit DCM		Inductor Valley Current		100		mA
PROGRAMMING PINS						
PGM0 Pin Resistor Range			0.095		115	kΩ

(See the Typical Application Circuits V_{DDH} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

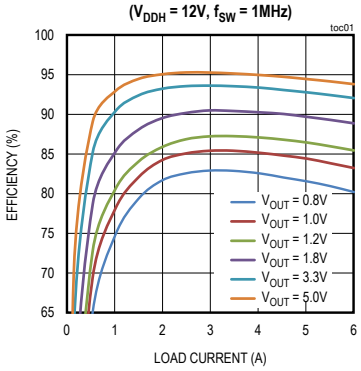
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGM0 Resistor Accuracy			-1		+1	%
PGM1/PGM2 3-Level Detection Thresholds		PGM_ Pin Connected to AVDD	AVDD - 0.23			V
		PGM_ Pin OPEN		0.9		
		PGM_ Pin Connected to AGND or PGM0			0.24 × AVDD	
PGM1/PGM2 Input Current		PGM_ Pin Connected to AVDD		140		µA
		PGM_ Pin Connected to AGND or PGM0		-125		

Note 4: Guaranteed by design.

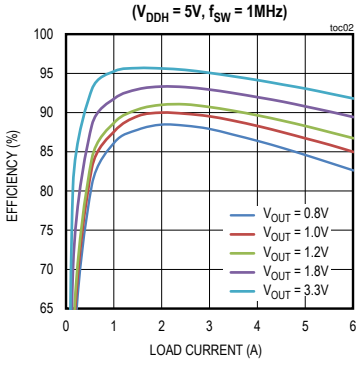
Typical Operating Characteristics

(V_{DDH} = 12V, tested on MAX16712EVKIT#, T_A = +25°C, unless otherwise noted.)

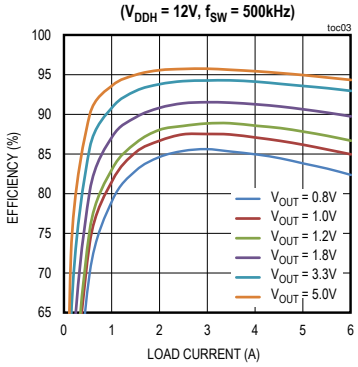
EFFICIENCY (MAX16712)
(SINGLE-PHASE, L = PA5003.XXXNLT)
(V_{DDH} = 12V, f_{SW} = 1MHz)



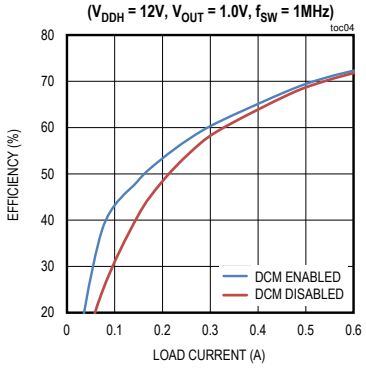
EFFICIENCY (MAX16712)
(SINGLE-PHASE, L = PA5003.XXXNLT)
(V_{DDH} = 5V, f_{SW} = 1MHz)



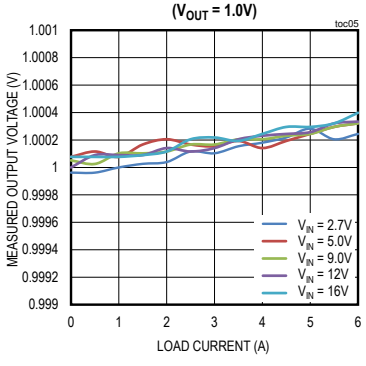
EFFICIENCY (MAX16712)
(SINGLE-PHASE, L = PA5005.XXXNLT)
(V_{DDH} = 12V, f_{SW} = 500kHz)



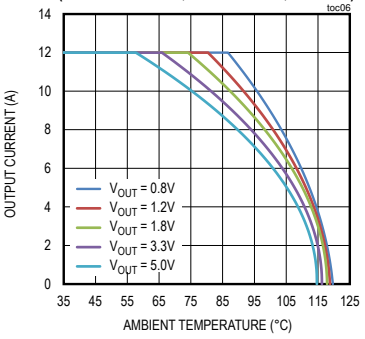
EFFICIENCY
(MAX16712, DCM vs CCM)
(V_{DDH} = 12V, V_{OUT} = 1.0V, f_{SW} = 1MHz)



LOAD AND LINE REGULATIONS
(SINGLE-PHASE OPERATION)
(V_{OUT} = 1.0V)

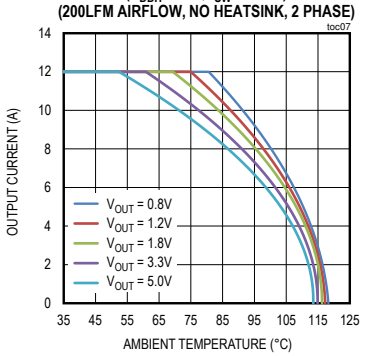


SAFE OPERATING AREA (MAX16712)
(V_{DDH} = 12V, f_{SW} = 1MHz)
(400LFM AIRFLOW, NO HEATSINK, 2 PHASE)

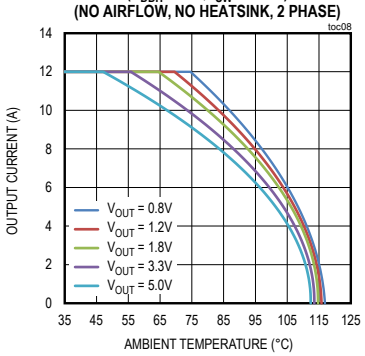


(V_{DDH} = 12V, tested on MAX16712EVKIT#, T_A = +25°C, unless otherwise noted.)

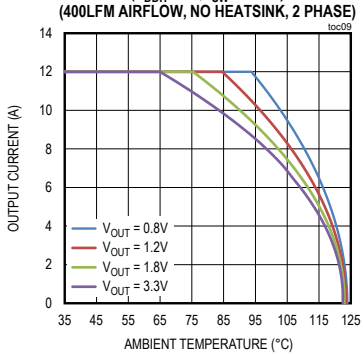
SAFE OPERATING AREA (MAX16712)
(V_{DDH} = 12V, f_{SW} = 1MHz)
(200LFM AIRFLOW, NO HEATSINK, 2 PHASE)



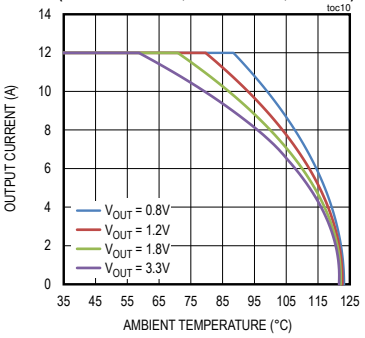
SAFE OPERATING AREA (MAX16712)
(V_{DDH} = 12V, f_{SW} = 1MHz)
(NO AIRFLOW, NO HEATSINK, 2 PHASE)



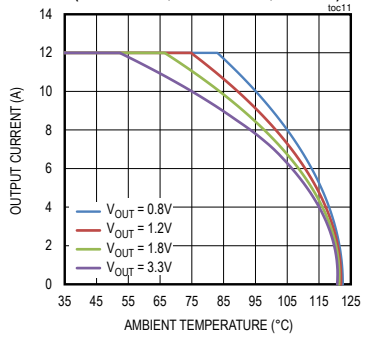
SAFE OPERATING AREA (MAX16712)
(V_{DDH} = 5V, f_{SW} = 1MHz)
(400LFM AIRFLOW, NO HEATSINK, 2 PHASE)



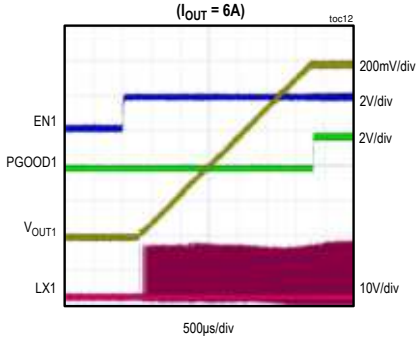
SAFE OPERATING AREA (MAX16712)
(V_{DDH} = 5V, f_{SW} = 1MHz)
(200LFM AIRFLOW, NO HEATSINK, 2 PHASE)



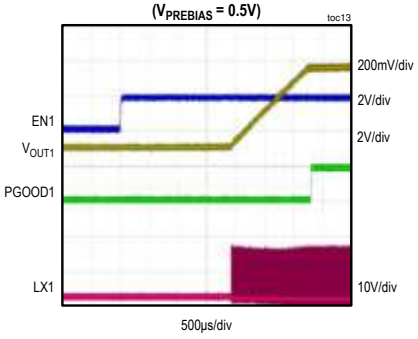
SAFE OPERATING AREA (MAX16712)
(V_{DDH} = 5V, f_{SW} = 1MHz)
(NO AIRFLOW, NO HEATSINK, 2 PHASE)



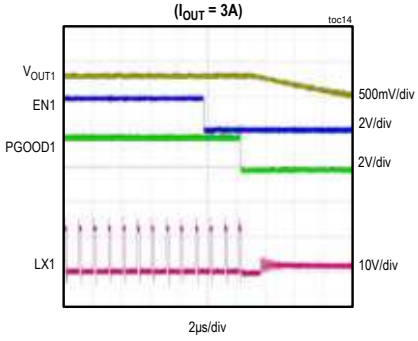
STARTUP
(SINGLE-PHASE OPERATION)
(I_{OUT} = 6A)



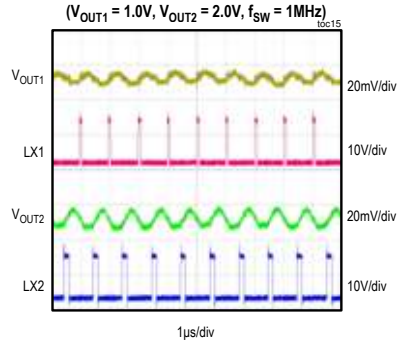
PRE-BIASED STARTUP
(SINGLE-PHASE OPERATION)
($V_{PREBIAS}$ = 0.5V)



SHUTDOWN
(SINGLE-PHASE OPERATION)
(I_{OUT} = 3A)

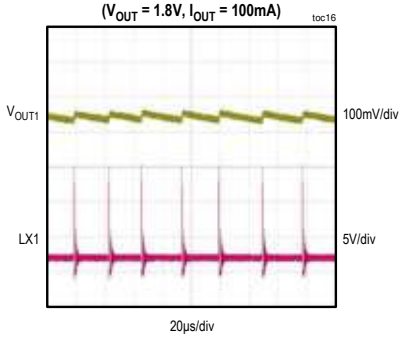


OUTPUT-VOLTAGE RIPPLE
(SINGLE-PHASE OPERATION)
(V_{OUT1} = 1.0V, V_{OUT2} = 2.0V, f_{SW} = 1MHz)

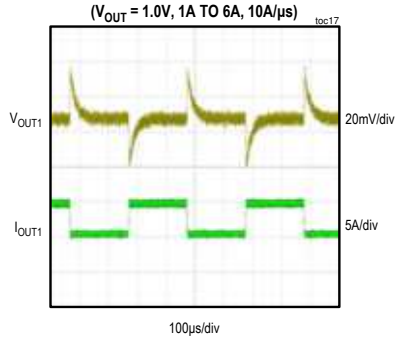


(V_{DDH} = 12V, tested on MAX16712EVKIT#, T_A = +25°C, unless otherwise noted.)

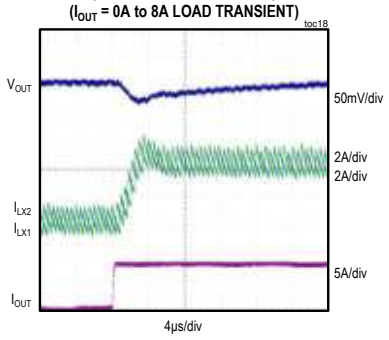
OUTPUT-VOLTAGE RIPPLE (DCM OPERATION) (V_{OUT} = 1.8V, I_{OUT} = 100mA)



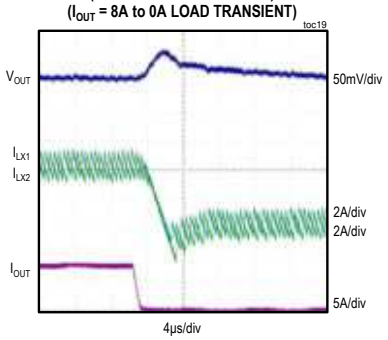
LOAD-TRANSIENT RESPONSE (SINGLE-PHASE OPERATION) (V_{OUT} = 1.0V, 1A TO 6A, 10A/µs)



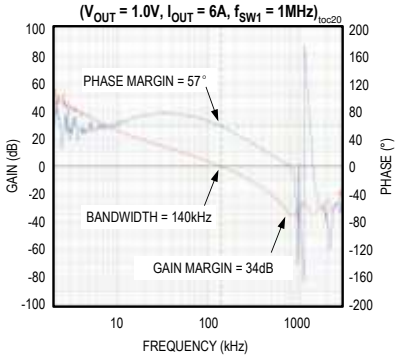
CURRENT BALANCE (DUAL-PHASE OPERATION) (I_{OUT} = 0A to 8A LOAD TRANSIENT)



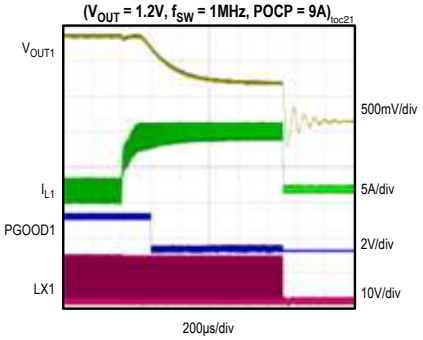
CURRENT BALANCE (DUAL-PHASE OPERATION) (I_{OUT} = 8A to 0A LOAD TRANSIENT)



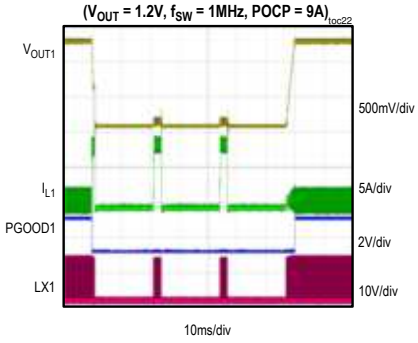
BODE PLOT (SINGLE-PHASE OPERATION) (V_{OUT} = 1.0V, I_{OUT} = 6A, f_{SW1} = 1MHz)



POSITIVE OVERCURRENT PROTECTION (SINGLE-PHASE OPERATION) (V_{OUT} = 1.2V, f_{SW} = 1MHz, POCP = 9A)

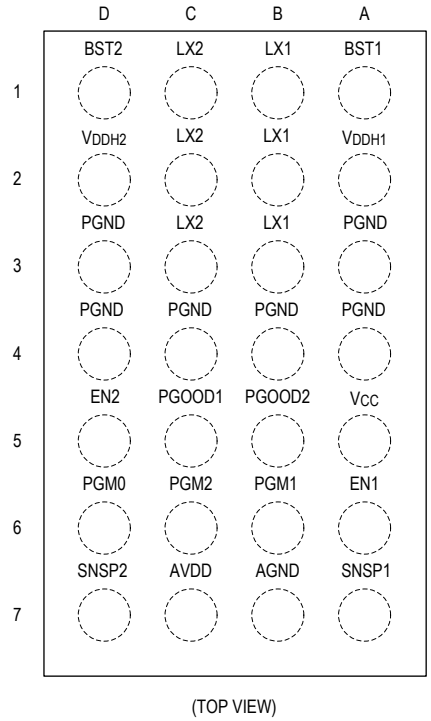


POCP HICCUP AND AUTORETRY (SINGLE-PHASE OPERATION) (V_{OUT} = 1.2V, f_{SW} = 1MHz, POCP = 9A)



Pin Configuration

28-Bump WLP



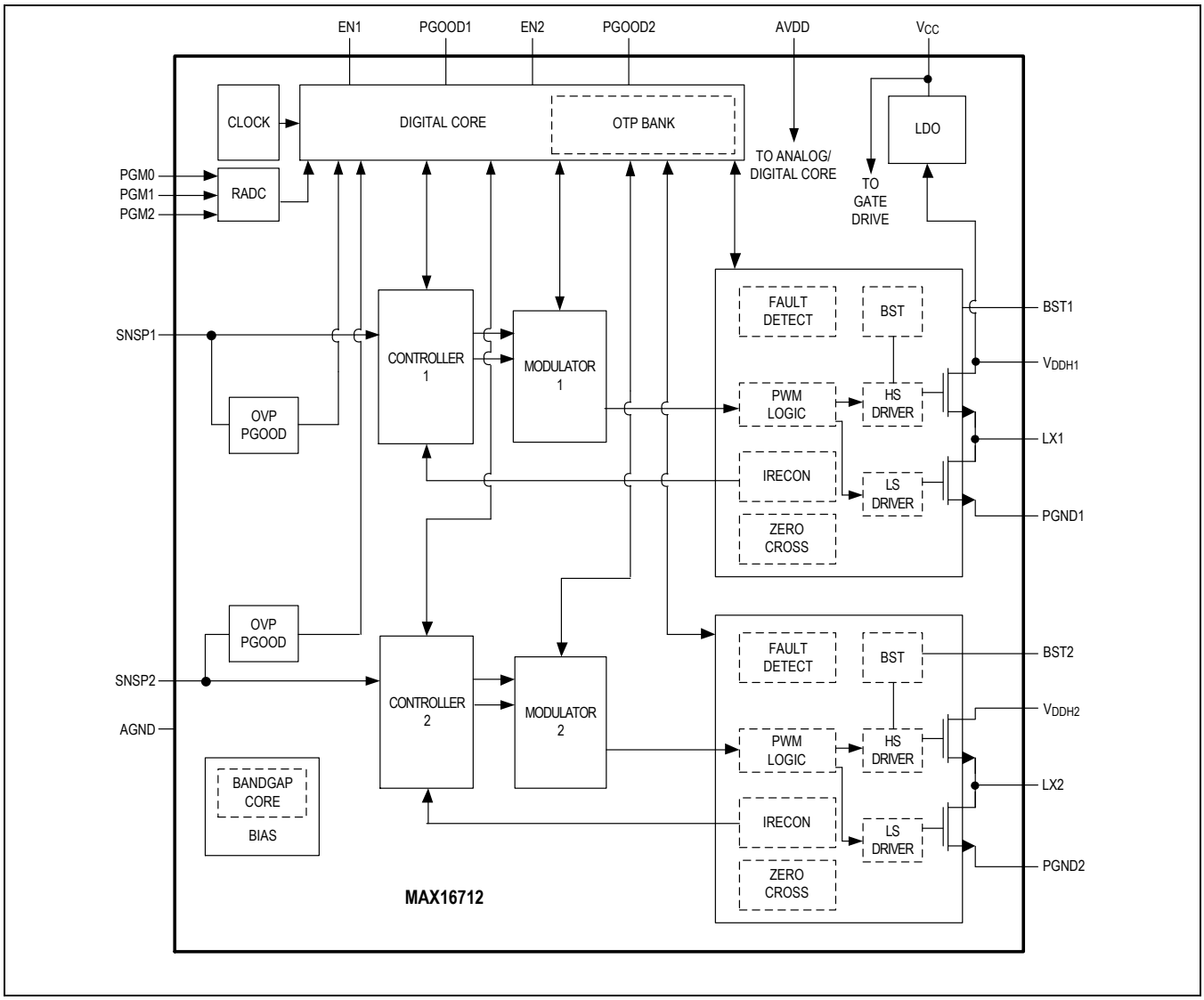
(TOP VIEW)

Pin Descriptions

PIN	NAME	FUNCTION
A1	BST1	Bootstrap Pin for Output 1. Connect 0.22µF ceramic capacitor from BST1 to LX1.
A2	V_{DDH1}	Regulator Input Supply for Output 1. V_{DDH1} and V_{DDH2} should be connected on PCB.
A3, A4, B4, C4, D3, D4	PGND	Power Ground.
A5	V_{CC}	Internal 1.8V LDO Output. Connect a 2.2µF or greater ceramic capacitor from V_{CC} to PGND.
A6	EN1	Output Enable for Output 1.
A7	SNSP1	Output 1 Voltage Sense Feedback Pin. Connect SNSP1 to V_{OUT1} at the load. A resistive voltage divider can be inserted between the output and SNSP1 to regulate the output above the 0.5V fixed reference voltage.
B1, B2, B3	LX1	Switching Node of Output 1. Connect LX1 directly to the output inductor.
B5	PGOOD2	Open-Drain Power-Good Output for Output 2.
B6	PGM1	Program Input. Connect this pin to AGND or AVDD or leave it unconnected.
B7	AGND	Analog Ground.
C1, C2, C3	LX2	Switching Node of Output 2. Connect LX2 directly to the output inductor.
C5	PGOOD1	Open-Drain Power-Good Output for Output 1.
C6	PGM2	Program Input. Connect this pin to AGND or AVDD or leave it unconnected.
C7	AVDD	1.8V Supply for Analog Circuitry. Connect a 2.2Ω to 4.7Ω resistor from AVDD to V_{CC}. Connect a 1µF or greater ceramic capacitor from AVDD to AGND.

D1	BST2	Bootstrap Pin for Output 2. Connect 0.22µF ceramic capacitor from BST2 to LX2.
D2	V_{DDH2}	Regulator Input Supply for Output 2. V_{DDH1} and V_{DDH2} should be connected on PCB.
D5	EN2	Output Enable for Output 2.
D6	PGM0	Program Input. Connect this pin to ground though a programming resistor.
D7	SNSP2	Output 2 Voltage Sense Feedback Pin. Connect SNSP2 to V_{OUT2} at the load. A resistive voltage divider can be inserted between the output and SNSP2 to regulate the output above the 0.5V fixed reference voltage. Connect SNSP2 to AVDD to select dual-phase operation.

Block Diagram



Detailed Description

Dual-Output or Dual-Phase Operation

The MAX16712, by default, is configured as a dual-output step-down regulator. It supports a single-input supply from 2.7V to 16V and two independent output rails of up to 6A load. The selection of DCM operation applies to both outputs. The device has two independent control loops for the two outputs and the loop parameters can be selected by predefined scenarios (see *Pin-Strap Programmability*).

The device can also be configured as a single-output, dual-phase 12A converter by connecting the SNSP2 pin to AVDD. When configured to dual-phase operation, only the control loop for OUTPUT1 will work and the control loop for OUTPUT2 is bypassed. EN1 and PGOOD1 are used in dual-phase operation mode to enable the device and indicate power-good status. EN2 and PGOOD2 can be disconnected.

Control Architecture

Fixed-Frequency Peak Current Mode Control Loop

The MAX16712 control loop is based on fixed-frequency peak current-mode control architecture. A simplified control architecture is shown in *Figure 1*. The loop contains an error amplifier stage, internal voltage loop compensation network, current sense, internal slope compensation, and a PWM modulator that generates the PWM signals to drive high-side and low-side MOSFETs. The device has a fixed 0.5V reference voltage (V_{REF}). The difference of V_{REF} and the sensed output voltage is amplified by the first error amplifier. Its output voltage ($V_{ERR_}$) is used as the input of the voltage loop compensation network. The output of the compensation network ($V_{COMP_}$) is fed to a PWM comparator with current-sense signal ($V_{ISENSE_}$) and the slope compensation ($V_{RAMP_}$). The output of the PWM comparator is the input of the PWM modulator. The turning on of the high-side MOSFET is aligned with an internal clock. It is a fixed-frequency phase shifted clock generated by the advanced modulation scheme (AMS) block.

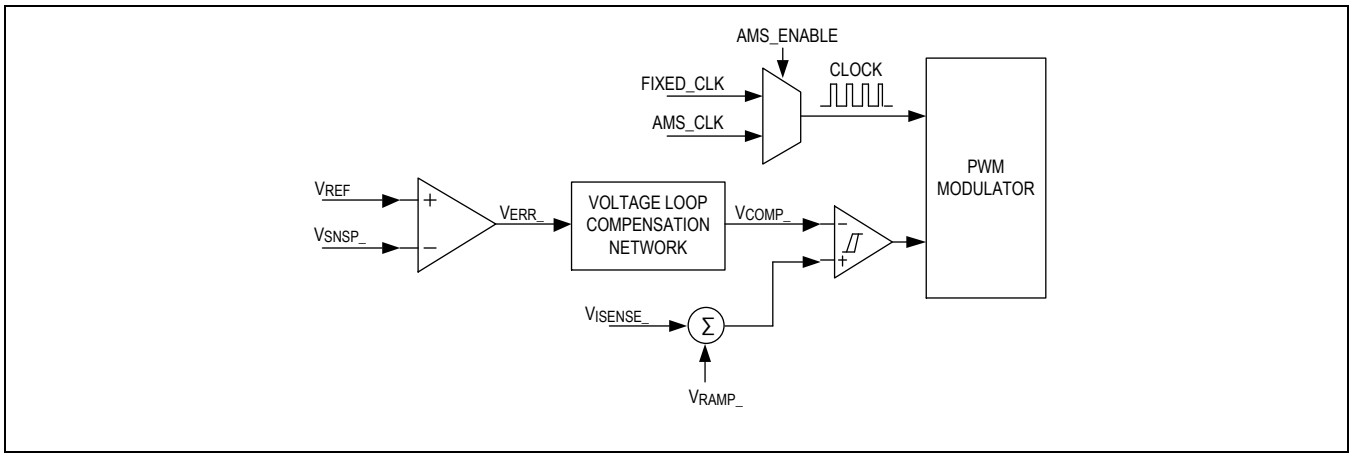


Figure 1. Simplified Control Architecture

Advanced Modulation Scheme (AMS)

The device offers an advanced modulation scheme (AMS) to provide improved transient response. AMS provides a significant advantage over conventional fixed-frequency PWM schemes. The AMS feature allows for modulation at both leading and trailing edges, which result a temporary increase or decrease of the switching frequency during large load transients. *Figure 2* shows the scheme to include leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows the turn on and off with minimal delay. Since the total inductor current increases very quickly, thus satisfying the load demand, the current drawn from output capacitors is reduced. With AMS enabled, the system closed-loop bandwidth can be extended without phase-margin penalty. As a result, the output capacitance can be minimized.

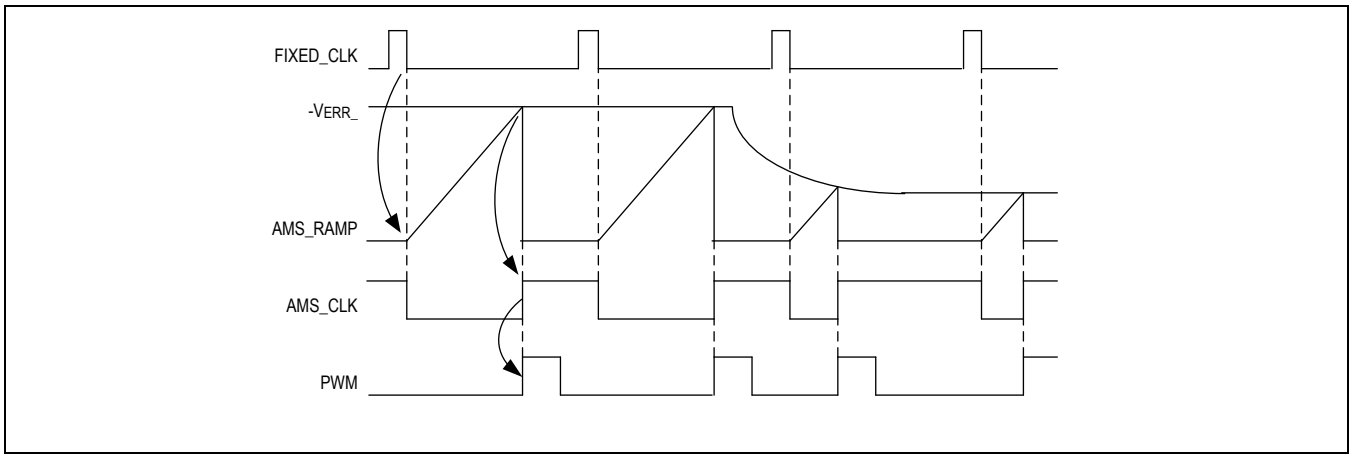


Figure 2. AMS Operation

Discontinuous Current Mode (DCM) Operation

Discontinuous current mode (DCM) operation can be enabled to improve light-load efficiency. It is required that V_{DDH} is at least 2V higher than desired V_{OUT} for the device to operate in DCM. The device has a DCM current-detection comparator to monitor the inductor valley current while operating in CCM. At light load, if the inductor valley current is below the DCM comparator threshold for 48 consecutive cycles, the device transition seamlessly to DCM. Once in DCM, the switching frequency decreases as load decreases. The MAX16712 transitions back to CCM operation as soon as the inductor valley current is higher than 100mA.

Active Current Balancing

When configured to dual-phase operation, the MAX16712 implements active current balancing for enhanced dynamic-current sharing or balancing between two phase currents. This feature maintains current balance during load transients, even at a load-step frequency close to switching frequency or its harmonics. In the device, the active current balancing circuit adjusts the individual phase-current control signal in order to minimize the phase-current imbalance.

Internal Linear Regulator

The MAX16712 contains an internal 1.8V linear regulator (LDO). The 1.8V LDO output voltage on V_{CC} is derived from V_{DDH1} pin. The 1.8V voltage on the V_{CC} pin supplies the current to the MOSFET drivers of both outputs. A decoupling capacitor of at least 2.2µF must be connected between V_{CC} and PGND. The AVDD pin of the MAX16712 also requires a 1.8V supply to power the device's internal analog circuitry. A 2.2Ω to 4.7Ω resistor must be connected between AVDD and V_{CC}. A 1µF or greater decoupling capacitor must be used between AVDD and AGND.

Startup and Shutdown

The startup and shutdown timing is shown in *Figure 3*. When the AVDD pin voltage is above its rising UVLO threshold, the device goes through an initialization procedure. The dual-output or dual-phase operation is detected. Configuration settings on the PGM_ pins are read. Once initialization is complete, the device detects V_{DDH} UVLO and EN_ status. When both are above their rising thresholds, the soft-start begins and switching is enabled. The output voltage of the enabled output starts to ramp up. The soft-start ramp time is 3ms. If there are no faults, the open-drain PGOOD_ pin is released from being held low after the soft-start ramp is complete. The device supports smooth startup with the output pre-biased.

During operation, if either V_{DDH} UVLO or EN_ falls below its threshold, switching is stopped immediately. The PGOOD_ pin is driven low. The output voltage is discharged by load current.

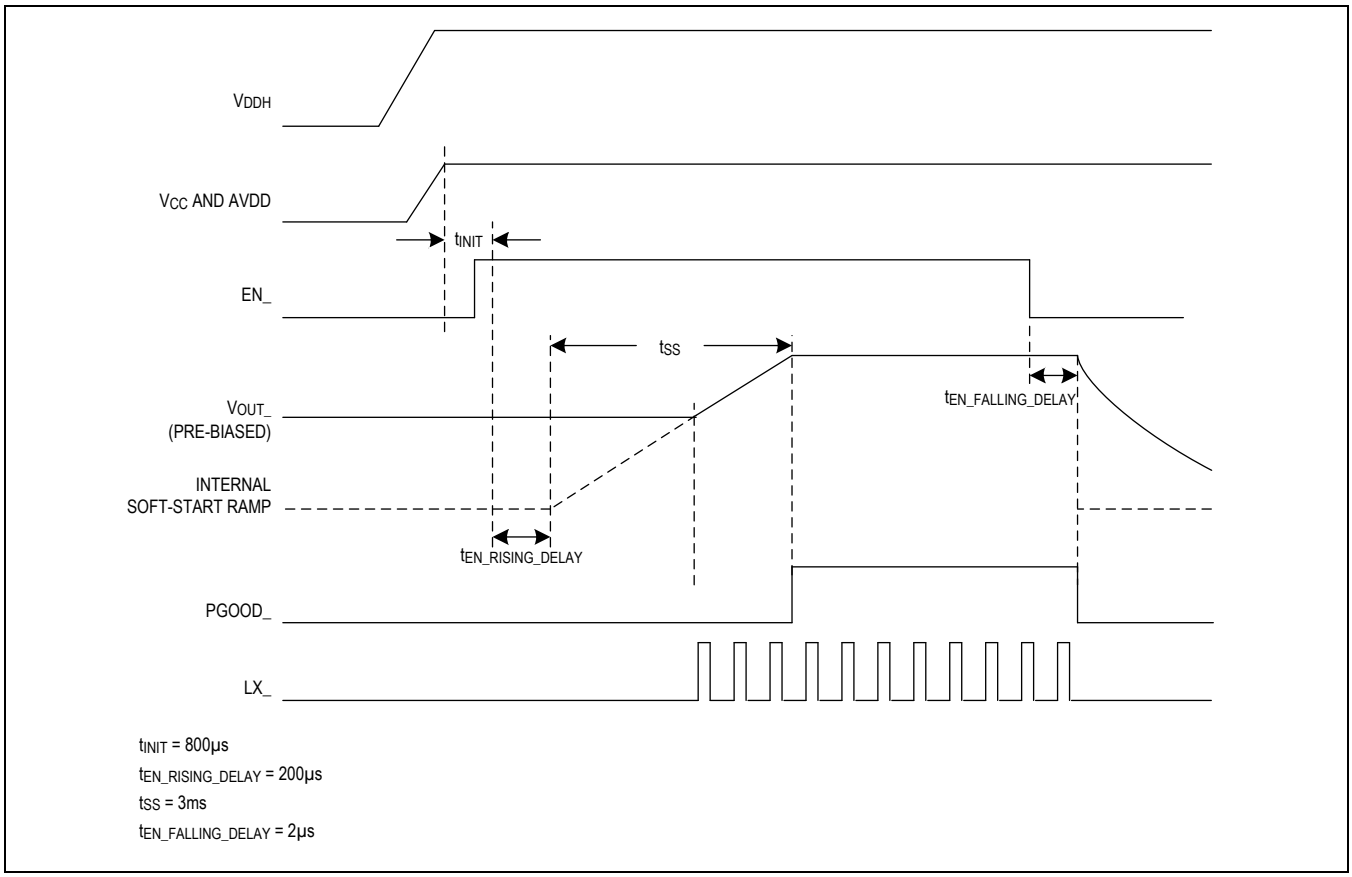


Figure 3. Startup and Shutdown Timing

Fault Handling

Input Undervoltage and Overvoltage Lockout (V_{DDH} UVLO, V_{DDH} OVLO)

The MAX16712 internally monitors the V_{DDH} voltage level. When the input supply voltage is below the UVLO threshold or above the OVLO threshold, the device stops switching and drives the PGOOD_ pin low. The device restarts after 20ms if the V_{DDH} UVLO or OVLO status is cleared. See *Startup and Shutdown* for the startup sequence.

Output Overvoltage Protection (OVP)

The feedback voltage on SNSP_ is monitored for output overvoltage once the soft-start ramp is complete. If the feedback voltage is above the OVP threshold beyond the OVP deglitch filtering delay, the device stops switching and drives the PGOOD_ pin low. The OVP is a hiccup protection, and the device restarts after 20ms if the OVP status is cleared. When configured to dual-output operation, the OVP of one output does not affect the operation of the other output.

Positive Overcurrent Protection (POCP)

The device's peak current mode control architecture provides inherent current limiting and short-circuit protection. The inductor current is continuously monitored while switching. The inductor peak current is limited on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the POCP threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by output voltage. An up-down counter is used to accumulate the number of consecutive POCP events each switching cycle. If the counter exceeds 1024, the device stops switching and drives the PGOOD_ pin low. The POCP is a hiccup protection, and the device restarts after 20ms. When configured to dual-output operation, the POCP of one output does not affect the operation of the other output.

The MAX16712 offers three POCP thresholds (9A, 6A, and 4.5A) for each output, which can be selected by the PGM1 and PGM2 pins (see *Pin-Strap Programmability*). Due to POCP deglitch delay, for a specific application use case, the actual POCP threshold should be higher (see *Output Inductor Selection*).

Negative Overcurrent Protection (NOCP)

The device also has negative overcurrent protection against inductor valley current. The NOCP threshold is -83% of the POCP threshold. In each switching cycle, once the sensed inductor current exceeds the NOCP threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 100ns time to allow the inductor current to be charged by input voltage. Same as POCP, an up-down counter is used to accumulate the number of consecutive NOCP events. If the counter exceeds 1024, the device stops switching and drives PGOOD_ pin low. The device restarts after 20ms. When configured to dual-output operation, NOCP of one output does not affect the operation of the other output.

Overtemperature Protection (OTP)

The overtemperature protection threshold is +155°C with 20°C hysteresis. If the junction temperature reaches the OTP threshold during operation, the device stops switching and drives the PGOOD_ pin low. The device restarts if the OTP status is cleared.

Pin-Strap Programmability

The MAX16712 has three program pins (PGM0, PGM1, and PGM2) to set some of the key configurations of the device. The PGM values are read during startup initialization. PGM0 has 32 detection levels. A pin-strap resistor is connected from PGM0 pin to AGND to select one of the 32 PGM0 codes. PGM0 is used to select the switching frequency and a predefined scenario, which is defined in *Table 4*. PGM1 and PGM2 each have three levels. PGM1 or PGM2 can be connected to AVDD or AGND (PGM0) or left OPEN to select the POCP level of each output. When the device is configured to dual-phase operation, the POCP level of each phase is only selected by PGM1. PGM2 code is ignored in the IC.

Table 1. PGM0 Switching Frequency and Scenario Selections

PGM0 CODES	R (Ω)	SWITCHING FREQUENCY (kHz)	SCENARIO #
0	95.3	500	A
1	200		B
2	309		C
3	422		D
4	536		E
5	649	600	A
6	768		B
7	909		C
8	1050		D
9	1210		E
10	1400	750	A
11	1620		B
12	1870		C
13	2150		D
14	2490		E
15	2870	1000	A
16	3740		B
17	8060		C
18	12400		D
19	16900		E
20	21500	1200	A
21	26100		B
22	30900		C
23	36500		D
24	42200		E
25	48700	1500	A
26	56200		B
27	64900		C

28	75000		D
29	86600		E
30	100000	2000	A
31	115000		B

Table 2. PGM1 POCP Selection for Output 1

PGM1 CODES	PGM1 CONNECTION	POCP1 (A)
0	AVDD	9
1	AGND or PGM0	6
2	OPEN	4.5

Table 3. PGM2 POCP Selection for Output 2

PGM2 CODES	PGM2 CONNECTION	POCP2 (A)
0	AVDD	9
1	AGND or PGM0	6
2	OPEN	4.5

The MAX16712 has five predefined scenarios for each selectable switching frequency, where the control loop is optimized to cover the most commonly used applications, which are summarized in *Table 4*. See *Voltage Loop Gain* for information about how to select the voltage loop gain resistance (R_{VGA}) for optimized control loop performance. The scenario is selected by a pin-strap resistor connected from the PGM0 pin to AGND.

Table 4. Predefined Scenarios

SCENARIO #	R_{VGA} (kΩ)	DCM OPTION
A	74.5	Disabled
B	52.2	Disabled
C	37.3	Disabled
D	52.2	Enabled
E	37.3	Enabled

Reference Design Procedure

Output Voltage Sensing

The MAX16712 has an internal 0.5V reference voltage. When the desired output voltage is higher than 0.5V, it is required to use resistor-dividers R_{FB1} and R_{FB2} to sense the output voltage (see *Typical Application Circuits*). It is recommended that the value of R_{FB2} does not exceed 5kΩ. The resistor-divider ratio is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where:

V_{OUT} = Output voltage

V_{REF} = 0.5V fixed reference voltage

R_{FB1} = Top resistor-divider

R_{FB2} = Bottom resistor-divider

Switching Frequency Selection

The MAX16712 offers a wide range of selectable switching frequencies from 500kHz to 2MHz. Switching frequency selection can be optimized for different applications. Higher switching frequencies are recommended for applications prioritizing solution size, so that the value and size of output LC filter can be reduced. Lower switching frequencies are recommended for applications prioritizing efficiency and thermal dissipation, due to reduced switching losses. The frequency must be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by the following equation:

$$f_{SWMAX} = MIN\left\{\frac{V_{OUT}}{t_{ONMIN} \times V_{DDHMAX}}, \frac{V_{DDHMIN} - V_{OUT}}{t_{OFFMIN} \times V_{DDHMIN}}\right\}$$

where:

f_{SWMAX} = Maximum selectable switching frequency

V_{DDHMAX} = Maximum input voltage

V_{DDHMIN} = Minimum input voltage

t_{ONMIN} = Minimum controllable on-time

t_{OFFMIN} = Minimum controllable off-time

The MAX16712 internally has a slope compensation applied to the current loop during on-time to guarantee stability and improve noise immunity. To avoid the slope compensation saturating the current loop, it is required that the maximum on-time be limited by:

$$t_{ONMAX} = \frac{5pF\left[800mV - \left(\frac{I_{OUTMAX}}{N} + \frac{I_{RIPPLE}}{2}\right) \times \frac{1.6\Omega}{25}\right]}{3.7uA}$$

where:

t_{ONMAX} = Maximum on-time of the high-side MOSFET

I_{OUTMAX} = Maximum load current

N = Number of phases

I_{RIPPLE} = Inductor current ripple peak-to-peak value

The minimum recommended switching frequency is calculated by the following equation:

$$f_{SWMIN} = \frac{V_{OUT}}{t_{ONMAX} \times V_{DDHMIN}}$$

where:

f_{SWMIN} = Minimum selectable switching frequency

Due to system noise injection, even at steady-state operation, typically the LX rising and falling edges would have some random jittering noise. The selection of the switching frequency (f_{SW}) should take into consideration the jittering, be higher than f_{SWMIN}, and be lower than f_{SWMAX}. To improve the LX jittering, it is recommended to use smaller inductor values and lower voltage loop gain to minimize the noise sensitivity.

Output Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitance needed to maintain transient tolerance.

To improve current loop noise immunity, typically the output inductor is selected so that the inductor current ripple is at least 1A. The inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{RIPPLE} \times f_{SW}}$$

where:

V_{DDH} = Input voltage

The inductor should also be selected so that maximum load current delivery can be guaranteed by the selected POCP threshold. The MAX16712 offers three POCP thresholds (9A, 6A, and 4.5A) for each output, which can be selected by the PGM1 and PGM2 pins (see *Pin-Strap Programmability*). Due to deglitch delay from the POCP comparator tripping to the high-side MOSFET turning off, for a specific application use case, the adjusted POCP threshold should take into consideration the inductor value, input voltage, and output voltage, which can be calculated by the following equation:

$$POCP_{ADJUST} = POCP + \frac{(V_{DDH} - V_{OUT}) \times t_{POCP}}{L}$$

where:

$POCP_{ADJUST}$ = Adjusted POCP threshold

POCP = POCP level specified in the EC table

t_{POCP} = POCP deglitch delay (36ns, typ)

It needs to be verified that the peak inductor current in normal operation does not exceed the minimum adjusted POCP threshold:

$$\frac{I_{OUTMAX}}{N} + \frac{I_{RIPPLE}}{2} < POCP_{ADJUST(MIN)}$$

where:

$POCP_{ADJUST(MIN)}$ = Minimum adjusted POCP threshold, calculated with the minimum value of the POCP threshold

Table 5 shows some suitable inductor part numbers which are verified on the MAX16712 evaluation kit to offer optimal performance.

Table 5. Recommended Inductors

COMPANY	VALUE (µH)	I_{SAT} (A)	R_{DC} (mΩ)	FOOTPRINT (mm)	HEIGHT (mm)	PART NUMBER
TDK	0.22	9	8	2.5 × 2.0	1.2	TFM252012ALMAR22MTAA
TDK	0.33	8.4	10	3.2 × 2.5	1.2	TFM322512ALMAR33MTAA
Pulse	0.47	26	3.75	5.5 × 5.3	2.9	PA5003.471NLT
Pulse	0.56	22.2	4.05	5.5 × 5.3	2.9	PA5003.561NLT
Pulse	1.0	16.5	6.9	5.5 × 5.3	2.9	PA5003.102NLT
Pulse	2.2	10	13.2	5.5 × 5.3	2.9	PA5003.222NLT

Output Capacitor Selection

One major factor in determining the total required output capacitance is the output-voltage ripple. To meet the output-voltage ripple requirement, the minimum output capacitance should satisfy the following equation:

$$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \times N \times f_{SW} \times (V_{OUTRIPPLE} - ESR \times I_{RIPPLE})}$$

where:

$V_{OUTRIPPLE}$ = Maximum allowed output-voltage ripple

ESR = ESR of output capacitors

The other important factors in determining the total required output capacitance are the maximum allowable output-voltage overshoot and undershoot during load transients. For a given loading or unloading current step, the minimum required output capacitance should also satisfy the following equation:

$$C_{OUT} \geq MAX\left\{\frac{\left(\frac{\Delta I}{N} + \frac{I_{RIPPLE}}{2}\right)^2 \times L \times N}{2 \times \Delta V_{OUT} \times (V_{DDH} - V_{OUT})}, \frac{\left(\frac{\Delta I}{N} + \frac{I_{RIPPLE}}{2}\right)^2 \times L \times N}{2 \times \Delta V_{OUT} \times V_{OUT}}\right\}$$

where:

C_{OUT} = Output capacitance

$\triangle I$ = Loading or unloading current step

$\triangle V_{OUT}$ = Maximum allowed output-voltage undershoot or overshoot

Input Capacitor Selection

The selection of input capacitance is determined by the requirement of input-voltage ripple. The V_{DDH1} and V_{DDH2} pins of the MAX16712 should be connected on the PCB. When configured to dual-output operation, the input capacitance is shared between the two outputs. The minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq MAX\left\{\frac{I_{OUT1(MAX)} \times V_{OUT1}}{f_{SW1} \times V_{DDH} \times V_{INPP}}, \frac{I_{OUT2(MAX)} \times V_{OUT2}}{f_{SW2} \times V_{DDH} \times V_{INPP}}\right\}$$

where:

$I_{OUT_(MAX)}$ = Maximum output current of OUTPUT_

$V_{OUT_}$ = Output voltage of OUTPUT_

$f_{SW_}$ = Switching frequency of OUTPUT_

V_{INPP} = Peak-to-peak input voltage ripple

When configured to dual-phase operation, the minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \frac{I_{OUT(MAX)} \times V_{OUT}}{2 \times f_{SW} \times V_{DDH} \times V_{INPP}}$$

Besides the minimum required input capacitance, it is required to also place 0.1µF and 1µF high-frequency decoupling capacitors next to each $V_{DDH_}$ pin to suppress the high-frequency switching noises.

Voltage Loop Gain

For stability purposes, it is recommended that the voltage loop bandwidth (BW) be lower than 1/5 of the switching frequency. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The voltage loop BW can be estimated with the following equation:

$$BW = \frac{N \times \frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 20m\Omega \times C_{OUT}}$$

where:

R_{VGA} = The voltage loop gain resistance, which is set by the scenario selected (*Table 4*).

Typical Reference Designs

See the *Typical Application Circuits* for examples of reference schematics. Reference design examples for some common output voltages are shown in *Table 6*.

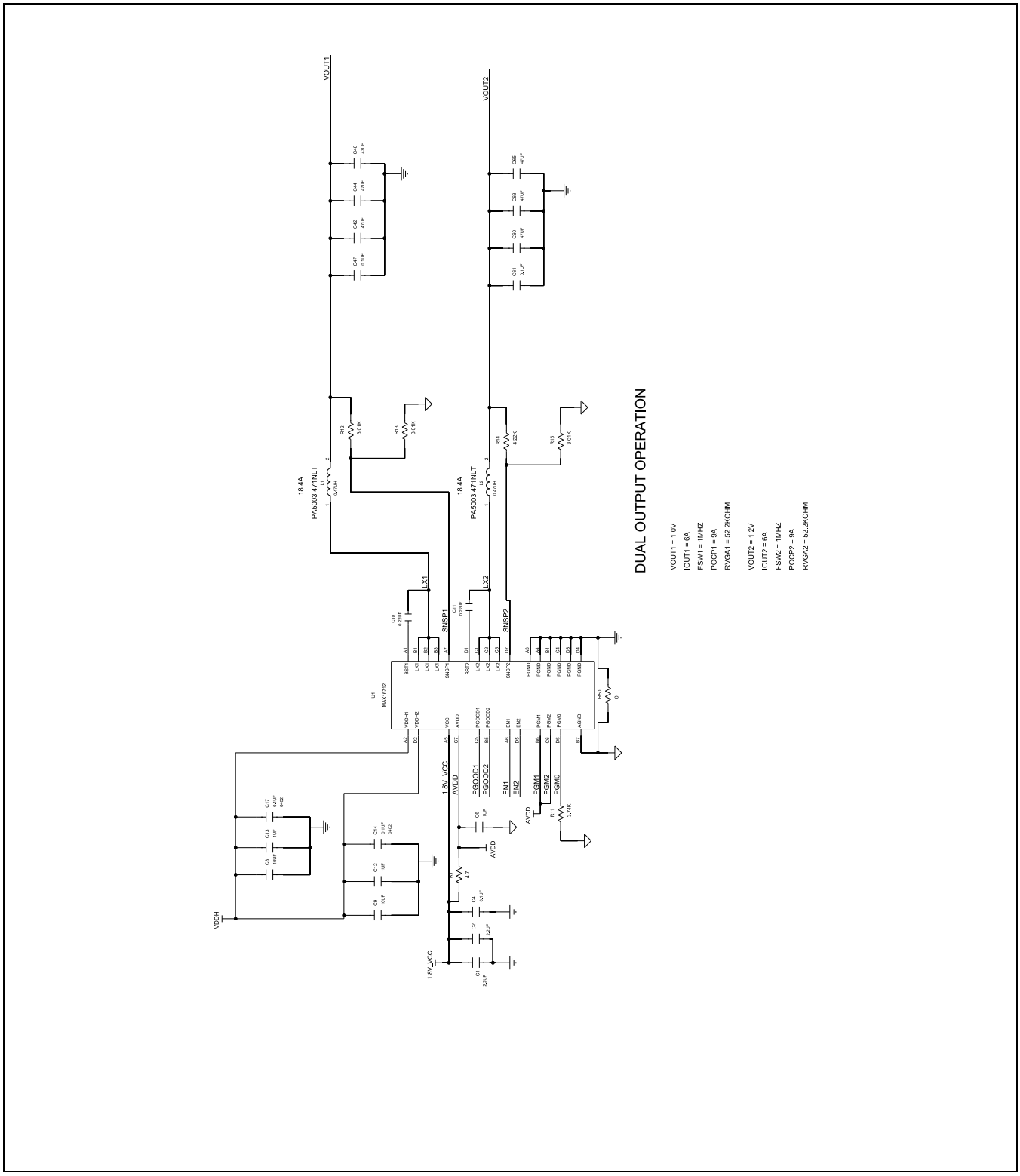
Table 6. Reference Design Examples

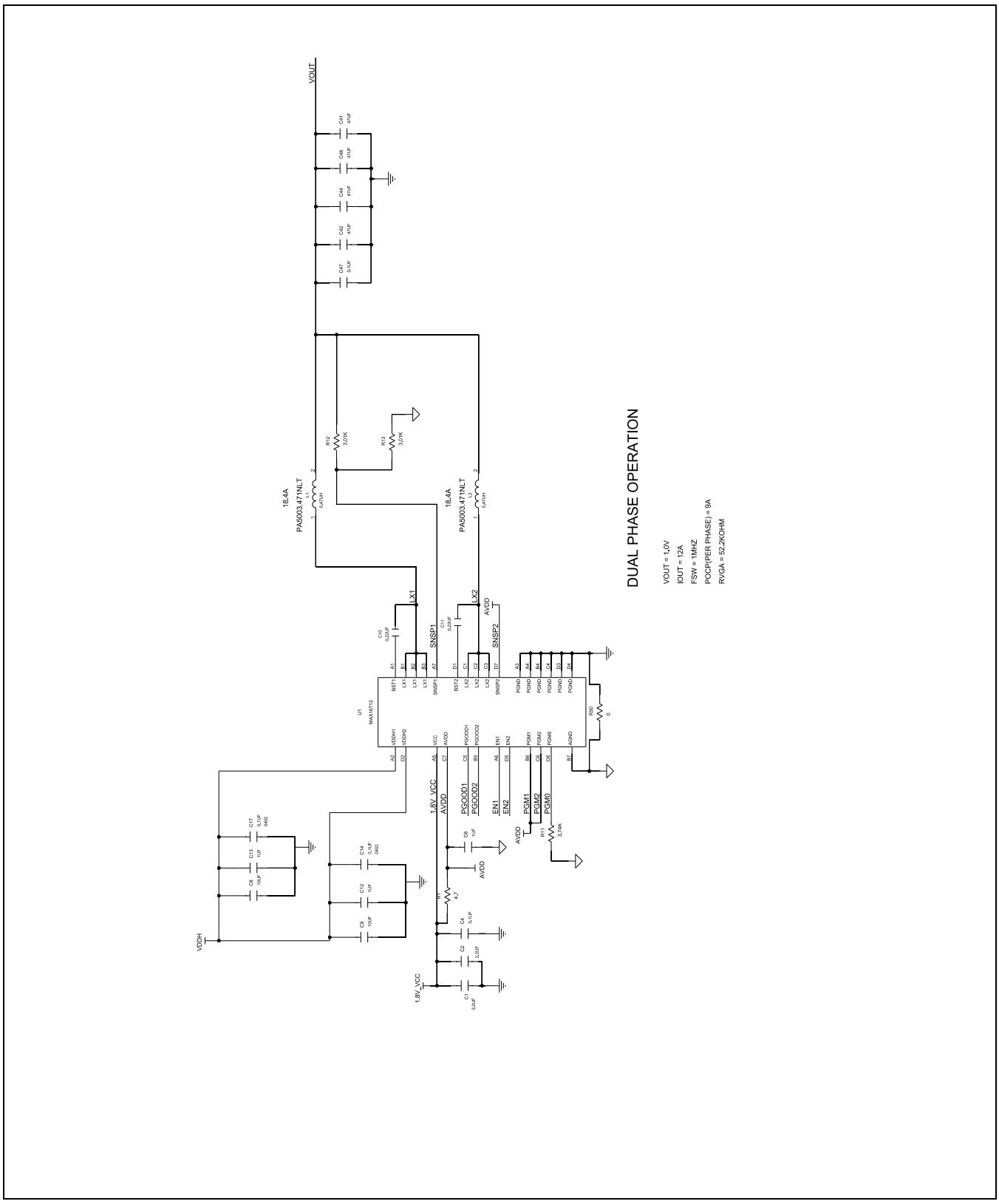
V_{OUT} (V)	I_{OUT} (A) (PER PHASE)	f_{SW} (kHz)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	PGM0 (kΩ)	PGM1 OR PGM2	L (µH)	C_{IN} (PER EACH $V_{DDH_}$ PIN)	C_{OUT}
0.8	6	750	1.82	3.01	1.62	AVDD	0.47	10µF +1µF +0.1µF	3 × 47µF
0.9	6	1000	2.40	3.01	3.74	AVDD	0.47	10µF +1µF +0.1µF	3 × 47µF
1.0	6	1000	3.01	3.01	3.74	AVDD	0.47	10µF +1µF +0.1µF	3 × 47µF
1.2	6	1000	4.22	3.01	3.74	AVDD	0.56	10µF +1µF +0.1µF	3 × 47µF
1.8	6	1500	7.87	3.01	56.2	AVDD	0.56	10µF +1µF +0.1µF	2 × 47µF
3.3	5	2000	16.9	3.01	115	AVDD	1.0	10µF +1µF +0.1µF	2 × 47µF
5.0	4	2000	22.6	2.49	115	AGND	2.2	10µF +1µF +0.1µF	1 × 47µF

PCB Layout Guidelines

- For electrical and thermal reasons, the second layer from the top and bottom of the PCB should be reserved for power ground (PGND) planes.
- The input decoupling capacitor should be located the closest to the IC and no more than 40mils from the $V_{DDH_}$ pins.
- The V_{CC} decoupling capacitors should be connected to PGND and placed as close as possible to V_{CC} pin.
- An analog ground copper polygon or island should be used to connect all analog control-signal grounds. This “quiet” analog ground copper polygon or island should be connected to the PGND through a single connection close to AGND pin. The analog ground can be used as a shield and ground reference for the control signals (PGM_ and SNSP_).
- The AVDD decoupling capacitors should be connected to AGND and placed as close as possible to AVDD pin.
- The boost capacitors should be placed as close as possible to LX_ and BST_ pins, on the same side of the PCB with the IC.
- The feedback resistor-divider and optional external compensation network should be placed close to the IC to minimize the noise injection.
- The voltage-sense line should be routed directly from an output capacitor, shielded by ground plane, and kept away from the switching node and inductor.
- Multiple vias are recommended for all paths that carry high currents and for heat dissipation.
- The input capacitors and output inductors should be placed near the IC and the traces to the components should be kept as short and wide as possible to minimize parasitic inductance and resistance.

Typical Application Circuits




DUAL PHASE OPERATION
VOUT = 1.0V
IOUT = 12A
FSW = 1MHZ
POCP(PER PHASE) = 9A
RVGA = 52.2KOHM
VOUT
18.4A
PA5003.471NLT
LX1
LX2
SNSP1
SNSP2
AVDD
VDDH
1.8V_VCC
PGOOD1
PGOOD2
EN1
EN2
PGM1
PGM2
PGM0
U1
MAX16712

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16712AWI+	-40°C to +125°C	28 WLP
MAX16712AWI+T	-40°C to +125°C	28 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/21	Initial release	—
1	2/22	Updated Benefits and Features, Detailed Description, and Reference Design Procedure	1, 11, 13, 15–17

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