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Boost Regulator with Integrated Charge Pumps, Switch Control, and High-Current Op Amp

MAX17075

General Description

The MAX17075 includes a high-voltage boost regulator, one high-current operational amplifier, two regulated charge pumps, and one MLG block for gate-driver supply modulation.

The step-up DC-DC converter is a 1.2MHz current-mode boost regulator with a built-in power MOSFET. It provides fast load-transient response to pulsed loads while producing efficiencies over 85%. The built-in 160mΩ (typ) power MOSFET allows output voltages as high as 18V boosted from inputs ranging from 2.5V to 5.5V. A built-in 7-bit digital soft-start function controls startup inrush currents.

The gate-on and gate-off charge pumps provide regulated TFT gate-on and gate-off supplies. Both output voltages can be adjusted with external resistive voltage-dividers.

The operational amplifier, typically used to drive the LCD backplane (VCOM), features high-output short-circuit current (±500mA), fast slew-rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail outputs.

The MAX17075 is available in a 24-pin thin QFN package with 0.5mm lead spacing. The package is a square (4mm x 4mm) with a maximum thickness of 0.8mm for ultra-thin LCD design. It operates over the -40°C to +105°C temperature range.

Applications

- Notebook Computer Displays
- LCD Monitor Panels
- LCD TVs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17075ETG+	-40°C to +85°C	24 TQFN-EP*
MAX17075GTG/V+	-40°C to +105°C	24 TQFN-EP*

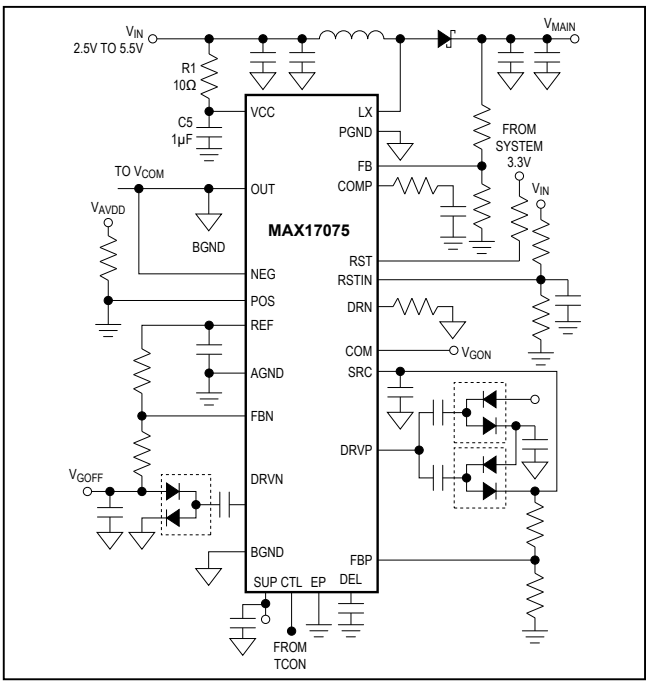
**EP = Exposed pad.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

Pin Configuration appears at end of data sheet.

Features

- 2.5V to 5.5V Input Operating Range
- Current Mode Step-Up Regulator
  - Fast-Transient Response
  - Built-In 20V, 3A, 0.16Ω n-Channel Power MOSFET
  - Cycle-by-Cycle Current Limit
  - 87% Efficiency (5V Input to 13V Output)
  - 1.2MHz Switching Frequency
  - ±1% Output Voltage Regulation Accuracy
- High-Current 18V VCOM Buffer
  - ±500mA Output Short-Circuit Current
  - 45V/µs Slew Rate
  - 20MHz -3dB Bandwidth
  - Rail-to-Rail Output
- Regulated Charge Pump for TFT Gate-On Supply
- Regulated Charge Pump for TFT Gate-Off Supply
- Logic-Controlled High-Voltage Switches with Adjustable Delay
- Soft-Start and Timed Delay Fault Latch for All Outputs
- Overload and Thermal Protection

Simplified Operating Circuit



19-4353; Rev 3; 3/26

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Absolute Maximum Ratings

VCC, CTL, RSTIN, RST to AGND ..... -0.3V to +7.5V
DEL, REF, COMP, FB, FBN, FBP to AGND ..... -0.3V to (V_{VCC} + 0.3V)
PGND, BGND to AGND ..... -0.3V to +0.3V
LX to PGND ..... -0.3V to +20V
SUP to PGND ..... -0.3V to +20V
DRVN, DRVP to PGND ..... -0.3V to (V_{SUP} + 0.3V)
SRC, COM, DRN to AGND ..... -0.3V to +40V
DRN to COM ..... -30V to +30V
SRC to SUP 23V
REF Short Circuit to AGND ..... Continuous
POS, NEG, OUT to AGND ..... -0.3V to (V_{SUP} + 0.3)
DRVN, DRVP RMS Current 200mA
LX, PGND RMS Current Rating 2.4A
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range, E Grade ..... -40°C to +85°C
Operating Temperature Range, G Grade ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 TQFN	
Package Code	**T2444+4**
Outline Number	21-0139
Land Pattern Number	90-0022
Thermal Resistance	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

24 TQFN-CU	
Package Code	**T2444+4C**
Outline Number	21-0139
Land Pattern Number	90-0022
Thermal Resistance	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to www.analog.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.
Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/thermal-tutorial.

Electrical Characteristics

(V_{VCC} = +5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = +13V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Input Supply Range		2.5		5.5	V
V_{CC} Undervoltage-Lockout (UVLO) Threshold	V_{CC} rising, hysteresis (typ) = 50mV	2.05	2.25	2.45	V
V_{CC} Shutdown Current	V_{CC} = 2V		100	200	µA
V_{CC} Quiescent Current	V_{FB} = 1.3V, not switching		1	1.5	mA
	V_{FB} = 1.0V, switching		4	5	

Electrical Characteristics (continued)

(V_{VCC} = +5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = +13V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE					
REF Output Voltage	No external load	1.238	1.250	1.262	V
REF Load Regulation	0n < I_{LOAD} < 50µA			6	mV
REF Sink Current	In regulation	10			µA
REF Undervoltage-Lockout Threshold	Rising edge, hysteresis (typ) = 200m		1	1.17	V
OSCILLATOR AND TIMING					
Frequency		1000	1200	1400	kHz
Oscillator Maximum Duty Cycle		87	90	93	%
Duration to Trigger Fault Condition	FB or FBP or FBN below threshold	47	55	65	ms
DEL Capacitor Charge Current	During startup, V_{DEL} = 1.0V	4	5	6	µA
DEL Turn-On Threshold		1.19	1.25	1.31	V
DEL Discharge Switch On-Resistance			20		Ω
STEP-UP REGULATOR					
Output Voltage Range		V_{VCC}		18	V
FB Regulation Voltage	FB = COMP, C_{COMP} = 1nF	1.238	1.250	1.262	V
FB Fault Trip Level	Falling edge	0.96	1	1.04	V
FB Load Regulation	0 < I_{LOAD} < full, transient only		-1		%
FB Line Regulation	V_{CC} = 2.5V to 5.5V	-0.2	0	+0.2	%/V
FB Input Bias Current	V_{FB} = 1.25V	50	125	200	nA
FB Transconductance	ΔI = ±2.5µA at COMP, FB = COMP	75	160	280	µS
FB Voltage Gain	FB to COMP		2600		V/V
LX Current Limit	V_{FB} = 1.1V, duty cycle = 75%	2.5	3.0	3.5	A
LX On-Resistance	I_{LX} = 200mA		0.16	0.25	Ω
LX Leakage Current	V_{LX} = 19V, T_A = +25°C		10	20	µA
Current-Sense Transresistance		0.1	0.2	0.3	V/A
Soft-Start Period	7-bit current ramp		14		ms
POSITIVE CHARGE-PUMP REGULATOR					
V_{SUP} Input Supply Range		6		18	V
V_{SUP} Overvoltage Threshold	V_{SUP} = rising, hysteresis = 200mV	19	20	21	V
Operating Frequency			0.5 x f_{OSC}		Hz
FBP Regulation Voltage		-1.5%	1.250	+1.5%	V
FBP Line Regulation Error	V_{SUP} = 12V to 18V, V_{GON} = 30V			0.2	%/V
FBP Input Bias Current	V_{FBP} = 1.5V, T_A = +25°C	-50		+50	nA
DRVP Current Limit	Not in dropout		400		mA
DRVP PCH On-Resistance			4	6	Ω
DRVP NCH On-Resistance			1.5	3	Ω
FBP Fault Trip Level	Falling edge	0.96	1	1.04	V
Positive Charge-Pump Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents		3	5	ms
NEGATIVE CHARGE-PUMP REGULATOR					
V_{SUP} Input Supply Range		6		18	V
Operating Frequency			0.5 x f_{OSC}		Hz

Electrical Characteristics (continued)

(V_{VCC} = +5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = +13V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FBN Regulation Voltage (V_{REF} - V_{FBN})	V_{REF} - V_{FBN} = 1V	-1.5%	1	+1.5%	V
FBN Input Bias Current	V_{FBN} = 0V, T_A = +25°C	-50		+50	nA
FBN Line Regulation Error	V_{SUP} = 9V to 18V, V_{GOFF} = -7V			0.2	%/V
DRVN PCH On-Resistance			4	6	Ω
DRVN NCH On-Resistance			1.5	3	Ω
DRVN Current Limit	Not in dropout		400		mA
FBN Fault Trip Level	Rising edge		450		mV
Negative Charge-Pump Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents		3	5	ms
POSITIVE GATE DRIVER TIMING AND CONTROL SWITCHES					
CTL Input Low Voltage				0.6	V
CTL Input High Voltage		2			V
CTL Input Current	V_{CTL} = 0V or V_{VCC}, T_A = +25°C	-1		+1	µA
CTL-to-COM Rising Propagation Delay	C_{LOAD} = 100pF		250		ns
SRC Input Voltage Range				36	V
SRC-to-COM Switch On-Resistance	V_{DEL} = 1.5V, CTL = V_{CC}		5	10	Ω
DRN-to-COM Switch On-Resistance	V_{DEL} = 1.5V, CTL = AGND		30	60	Ω
COM-to-GND Pulldown	V_{DEL} = 0V		1.5	2.5	kΩ
SRC Input Current	V_{DEL} = 1.5V, CTL = V_{CC}		300	600	µA
	V_{DEL} = 1.5V, CTL = AGND		200	360	
OPERATIONAL AMPLIFIERS					
SUP Supply Range		6		18	V
VSUP Undervoltage Threshold		3.8	4	4.2	V
SUP Supply Current	Buffer configuration, V_{POS} = V_{SUP}/2, no load		4	6.5	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{SUP}/2			12	mV
Input Bias Current	V_{NEG}, V_{POS} = V_{SUP}/2, T_A = +25°C	-1		+1	µA
Input Common-Mode Voltage Range		0		V_{SUP}	V
Input Common-Mode Rejection Ratio			80		dB
Output-Voltage-Swing High	I_{OUT} = 50mA	V_{SUP} - 350			mV
Output-Voltage-Swing Low	I_{OUT} = -50mA			350	mV
Large-Signal Voltage Gain	V_{OUT} = 1V to (V_{SUP} - 1)V		80		dB
Slew Rate			45		V/µs
-3dB Bandwidth			20		MHz
Short-Circuit Current	Sourcing	500			mA
	Sinking	500			
XAO CONTROL					
RSTIN Threshold	Falling edge at V_{CC} = 5V	1.225	1.250	1.275	V
	Falling edge at V_{CC} = 1.8V	1.213	1.250	1.287	
RSTIN Input Current	T_A = +25µC	-1		+1	µA
RSTIN Hysteresis			50		mV
RST Output Voltage	I_{SINK} = 1mA			0.4	V
RST Blanking Time	Counting from V_{VCC} crossing 2.25V	160	220	280	ms
XAO UVLO	V_{VCC} rising with hysteresis of 50mV		1.5	1.7	V

Electrical Characteristics (continued)

(V_{VCC} = +5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = +13V, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Input Supply Range		2.5		5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{CC} rising, hysteresis (typ) = 50mV	2.05		2.45	V
V_{CC} Shutdown Current				200	µA
V_{CC} Quiescent Current	V_{FB} = 1.3V, not switching			1.5	mA
	V_{FB} = 1.0V, switching			5	
REFERENCE					
REF Output Voltage	No external load	1.230		1.267	V
REF Load Regulation	0 < I_{LOAD} < 50µA			6	mV
REF Sink Current	In regulation	10			µA
REF Undervoltage-Lockout Threshold	Rising edge, hysteresis (typ) = 200mV			1.17	V
OSCILLATOR AND TIMING					
Frequency		1000		1400	kHz
Oscillator Maximum Duty Cycle		86		94	%
Duration to Trigger Fault Condition	FB or FBP or FBN below threshold	47		65	ms
DEL Capacitor Charge Current	During startup, V_{DEL} = 1.0V	4		6	µA
DEL Turn-On Threshold		1.19		1.31	V
STEP-UP REGULATOR					
Output Voltage Range		V_{IN}		18	V
FB Regulation Voltage	FB = COMP, C_{COMP} = 1nF	1.230		1.267	V
FB Fault Trip Level	Falling edge	0.96		1.04	V
FB Line Regulation	V_{CC} = 2.5V to 5.5V	-0.25		+0.25	%/V
FB Input Bias Current	V_{FB} = 1.25V	50		200	nA
FB Transconductance	ΔI = ±2.5µA at COMP, FB = COMP	75		280	µS
LX Current Limit	V_{FB} = 1.1V, duty cycle = 75%	2.5		3.5	A
LX On-Resistance	I_{LX} = 200mA			0.25	Ω
Current-Sense Transresistance		0.10		0.30	V/A
POSITIVE CHARGE-PUMP REGULATOR					
V_{SUP} Input Supply Range		6		18	V
V_{SUP} Overvoltage Threshold	V_{SUP} = rising, hysteresis = 200mV	19		21	V
FBP Regulation Voltage		-2%	1.25	+2%	V
FBP Line Regulation Error	V_{SUP} = 8V to 18V, V_{GON} = 30V			0.2	%/V
FBP Input Bias Current	V_{FBP} = 1.5V, T_A = +25°C	-50		+50	nA
DRVP PCH On-Resistance				6	Ω
DRVP NCH On-Resistance				3	Ω
FBP Fault Trip Level	Falling edge	0.96		1.04	V
Positive Charge-Pump Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents			5	ms

Electrical Characteristics (continued)

(V_{VCC} = +5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = +13V, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 1)

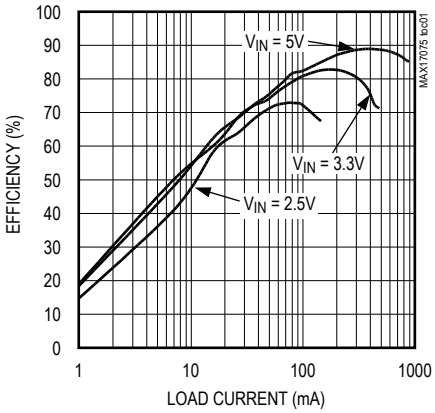
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
NEGATIVE CHARGE-PUMP REGULATOR					
V_{SUP} Input Supply Range		6		18	V
FBN Regulation Voltage (V_{REF} - V_{FBN})	V_{REF} - V_{FBN} = 1V	-2%	1	+2%	V
FBN Input Bias Current	V_{FBN} = 0V, T_A = +25°C	-50		+50	nA
FBN Line Regulation Error	V_{SUP} = 9V to 18V, V_{GOFF} = -7V			0.2	%/V
DRVN PCH On-Resistance				6	Ω
DRVN NCH On-Resistance				3	Ω
Negative Charge-Pump Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents			5	ms
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
CTL Input Low Voltage				0.6	V
CTL Input High Voltage		2			V
CTL Input Current	V_{CTL} = 0V or V_{VCC}, T_A = +25°C	-1		+1	µA
SRC Input Voltage Range				36	V
SRC-to-COM Switch On-Resistance	V_{DEL} = 1.5V, CTL = VCC			10	Ω
DRN-to-COM Switch On-Resistance	V_{DEL} = 1.5V, CTL = AGND			60	Ω
COM-to-GND Pulldown	V_{DEL} = 0V		1.5	2.5	kΩ
SRC Input Current	V_{DEL} = 1.5V, CTL = VCC			600	µA
	V_{DEL} = 1.5V, CTL = AGND			360	µA
OPERATIONAL AMPLIFIERS					
SUP Supply Range		6		18	V
V_{SUP} Undervoltage Threshold		3.8	4	4.2	V
SUP Supply Current	Buffer configuration, V_{POS} = V_{SUP}/2, no load			6.5	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{SUP}/2			12	mV
Input Bias Current	V_{NEG}, V_{POS} = V_{SUP}/2, T_A = +25°C	-1		+1	µA
Input Common-Mode Voltage Range		0		V_{SUP}	V
Output-Voltage-Swing High	I_{OUT} = 50mA	V_{SUP} - 350			mV
Output-Voltage-Swing Low	I_{OUT} = -50mA			350	mV
Short-Circuit Current	Sourcing	500			mA
	Sinking	500			
XAO CONTROL					
RSTIN Threshold	Falling edge	1.22		1.28	V
RSTIN Input Current	T_A = +25°C	-1		+1	µA
RST Output Voltage	I_{SINK} = 1mA			0.4	V
RST Blanking Time	Counting from V_{VCC} crossing 2.25V	160		280	ms
XAO UVLO	V_{CC} rising with typical hysteresis of 50mV			1.7	V

Note 1: All devices are 100% tested at +25°C. Limits over temperature are guaranteed by design.

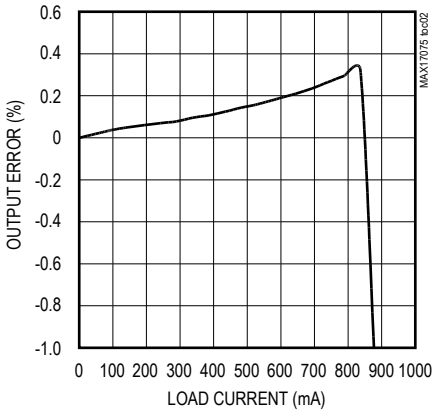
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

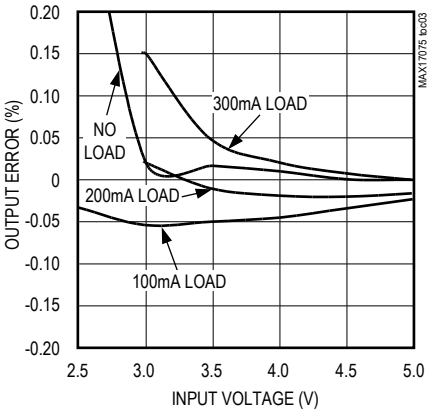
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



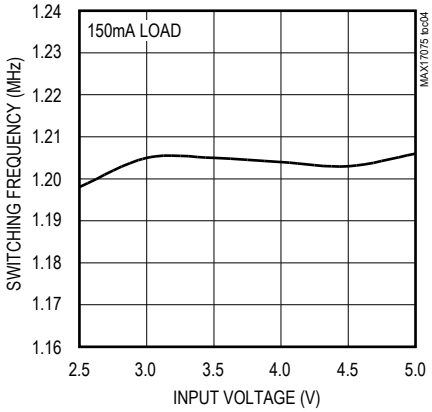
STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



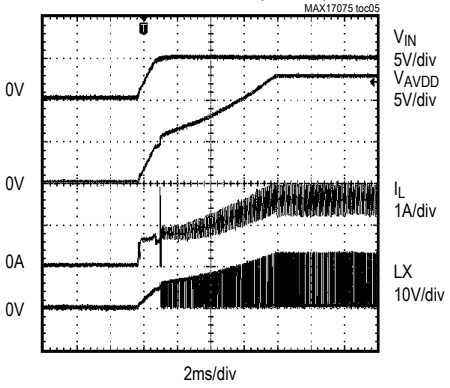
STEP-UP REGULATOR LINE REGULATION UNDER DIFFERENT LOADS



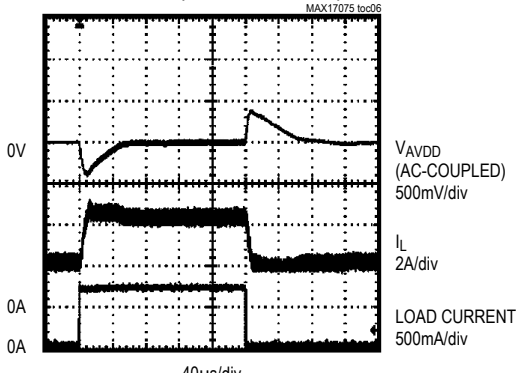
STEP-UP REGULATOR SWITCHING FREQUENCY vs. INPUT VOLTAGE



STEP-UP REGULATOR STARTUP WITH HEAVY LOAD (600mA)

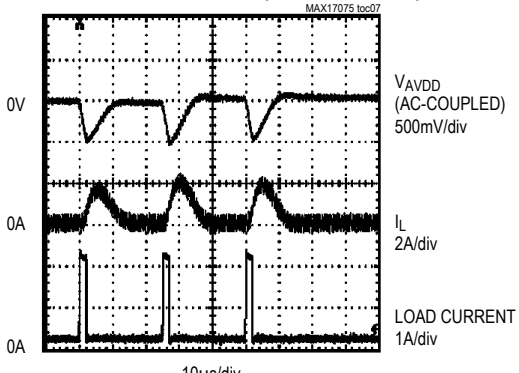


STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (100mA TO 800mA)



R_{COMP} = 82kΩ
C_{COMP1} = 220pF
C_{COMP2} = 18pF

STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE (80mA TO 2.08mA)

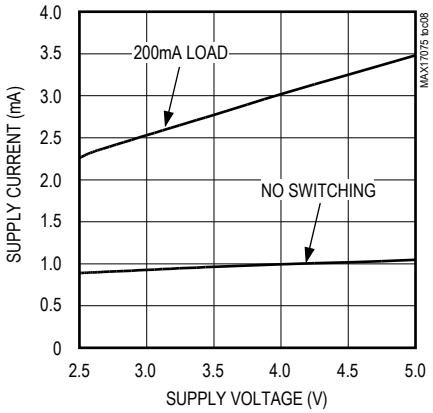


R_{COMP} = 82kΩ
C_{COMP1} = 220pF
C_{COMP2} = 18pF

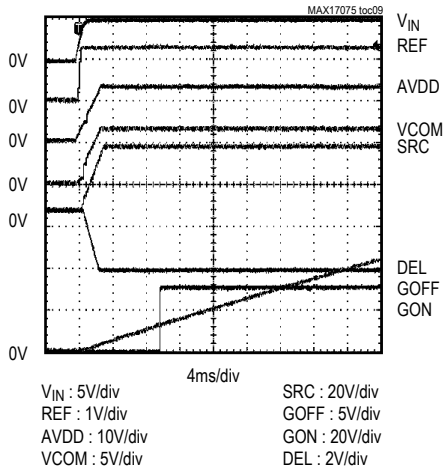
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

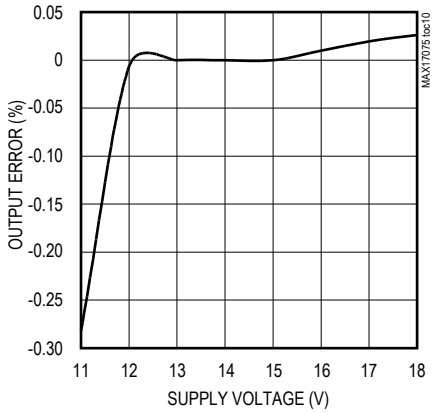
IN SUPPLY QUIESCENT CURRENT vs. IN SUPPLY VOLTAGE



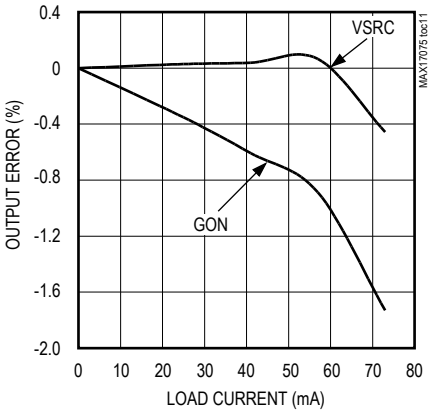
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



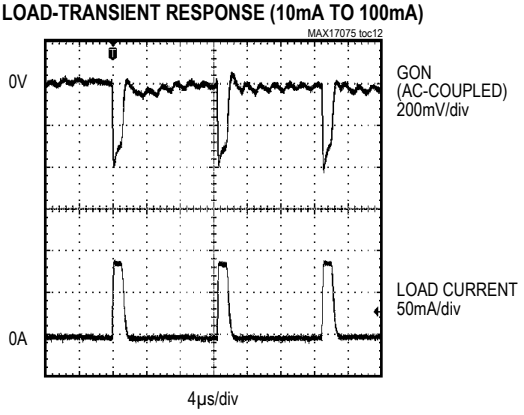
POSITIVE CHARGE-PUMP REGULATOR LINE REGULATION



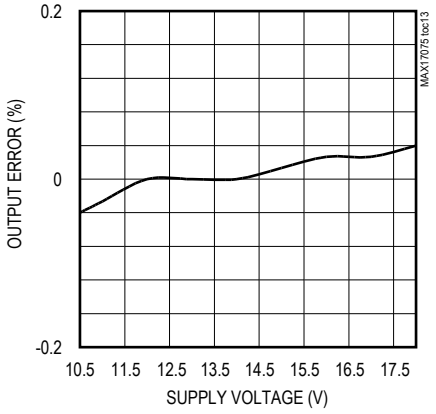
POSITIVE CHARGE-PUMP REGULATOR LOAD REGULATION



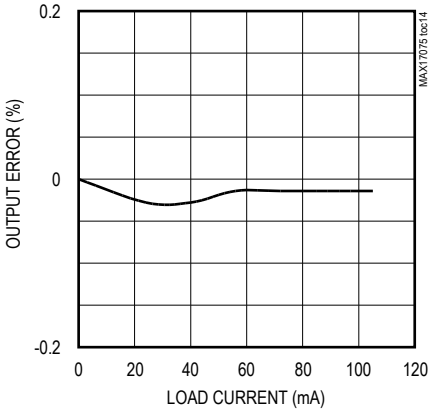
POSITIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE (10mA TO 100mA)



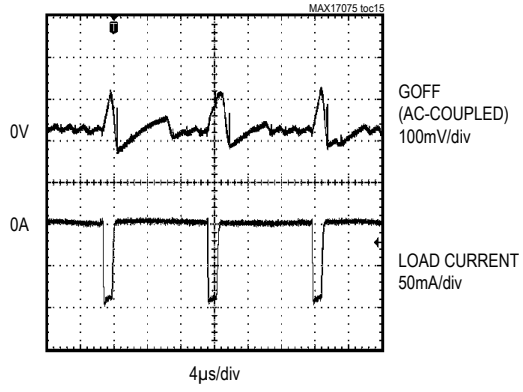
NEGATIVE CHARGE-PUMP REGULATOR LINE REGULATION



NEGATIVE CHARGE-PUMP REGULATOR LOAD REGULATION



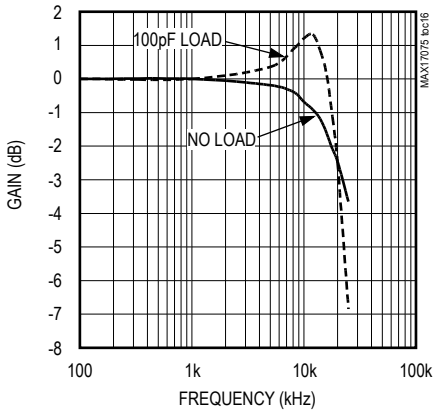
NEGATIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE (10mA TO 100mA)



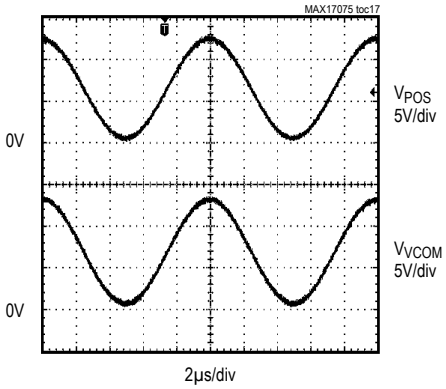
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

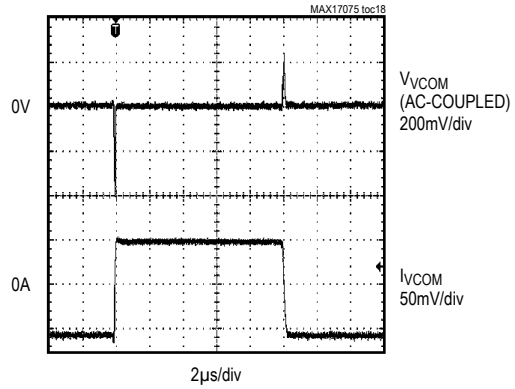
OPERATION AMPLIFIER FREQUENCY RESPONSE



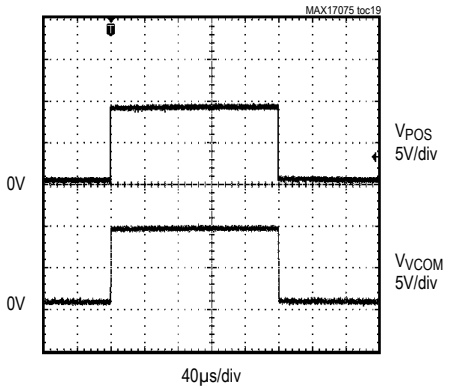
OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUPUT WAVEFORMS



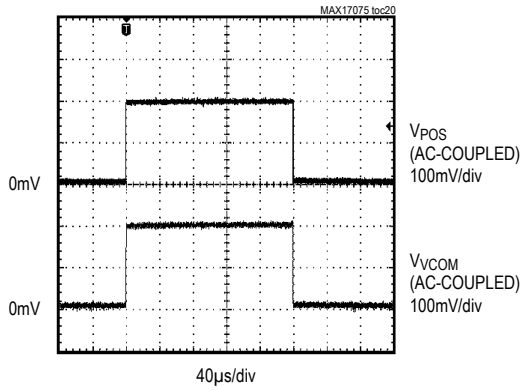
OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



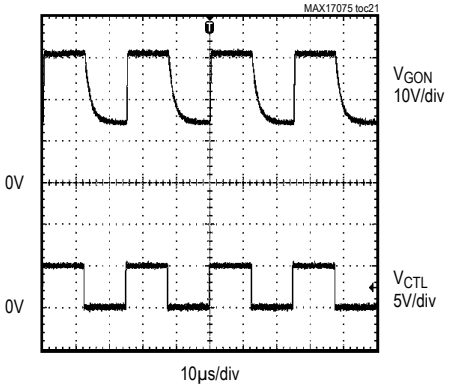
OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



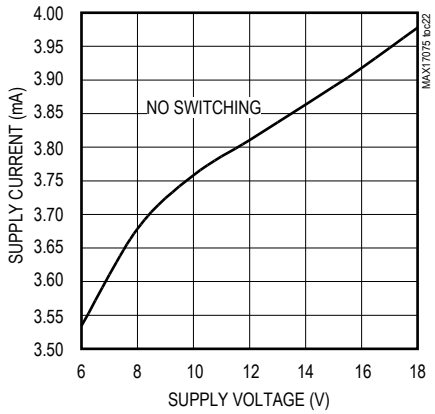
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



HIGH-VOLTAGE SWITCH CONTROL FUNCTION



SUP SUPPLY CURRENT vs. SUP SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	POS	Operational Amplifier Noninverting Input
2	NEG	Operational Amplifier Inverting Input
3	OUT	Operational Amplifier Output
4	BGND	Analog Ground for Operational Amplifier and Charge Pump. Connect to AGND underneath the IC.
5	SUP	Operational Amplifier and Charge-Pump Supply Input. Connect this pin to the output of the boost regulator (AVDD) and bypass to BGND with a minimum1µF capacitor.
6	DRVP	Positive Charge-Pump Driver Output
7	DRVN	Negative Charge-Pump Driver Output
8	CTL	High-Voltage Switch Control Input. When CTL is high, the switch between GON and SRC is on and the switch between GON and DRN is off. When CTL is low, the switch between GON and DRN is on and the switch between GON and SRC is off. CTL is inhibited by VCC UVLO and when DEL is less than 1.25V.
9	RST	Reset Output. RST is an open-drain output.
10	FBP	Positive Charge-Pump Regulator Feedback Input. Connect FBP to the center of a resistive voltage-divider between the positive charge-pump regulator output and AGND to set the positive charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBP.
11	FBN	Negative Charge-Pump Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output and REF to set the negative charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBN.
12	REF	Reference Output. Connect a 0.22µF capacitor from REF to AGND. All power outputs are disabled until REF exceeds its UVLO threshold.
13	VCC	Supplies the Internal Reference and Other Internal Circuitry. Connect VCC to the input supply voltage and bypass VCC to AGND with a minimum 1µF ceramic capacitor.
14	AGND	Analog Ground for Step-Up Regulator and Linear Regulators. Connect to power ground (PGND) underneath the IC.
15	RSTIN	Reset Input. Connect to the center of a resistor-divider from V_{IN}.
16	COMP	Compensation Pin for Error Amplifier. Connect a series RC from COMP to AGND.
17	FB	Step-Up Regulator Feedback Input. Connect FB to the center of a resistive voltage-divider between the step-up regulator output and AGND to set the regulator's output voltage. Place the resistive voltage-divider within 5mm of FB.
18, 19	PGND	Power Ground
20	LX	Step-Up Regulator Switching Node. Connect inductor and catch diode here and minimize trace area for lowest EMI power ground.
21	DRN	Switch Input. Drain of the internal high-voltage back-to-back p-channel FET connects to COM.
22	COM	Internal High-Voltage MOSFET Switch Common Terminal
23	SRC	Switch Input. Source of the internal high-voltage pFET. Bypass SRC to PGND with a minimum 0.1µF capacitor close to the pin.
24	DEL	High-Voltage Switch Delay Input. Connect a capacitor from DEL to AGND to set delay.
—	EP	Exposed Pad. Connect to AGND.

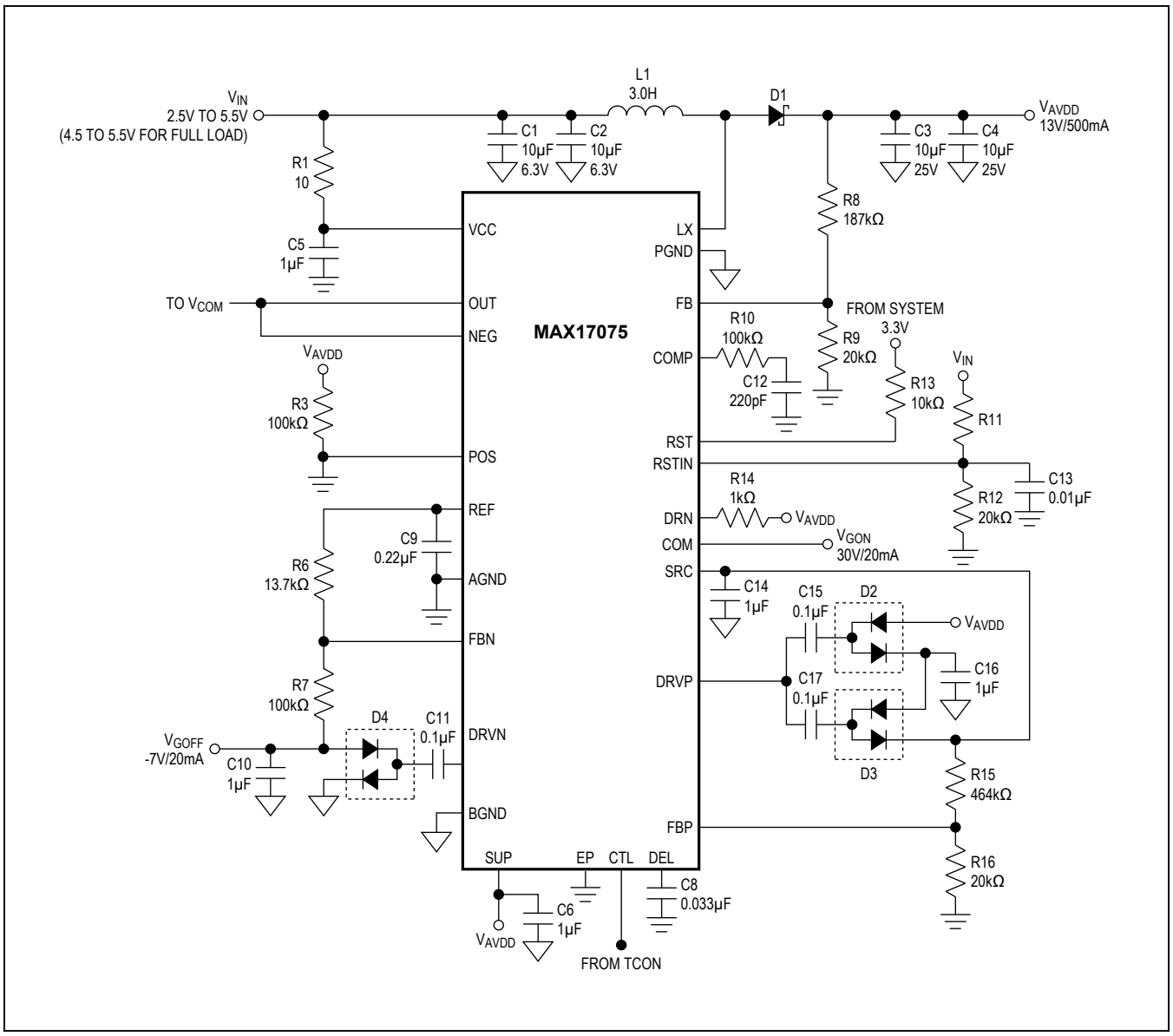


Figure 1. Typical Operating Circuit

Typical Operating Circuit

The typical operating circuit (Figure 1) of the MAX17075 is a complete power-supply system for TFT LCD panels in monitors and TVs. The circuit generates a +13V source driver supply, a +30V positive gate-driver supply, and a -7V negative gate-driver supply from a +2.5V to +5.5V input supply. Table 1 lists some selected components, and Table 2 lists the contact information for component suppliers.

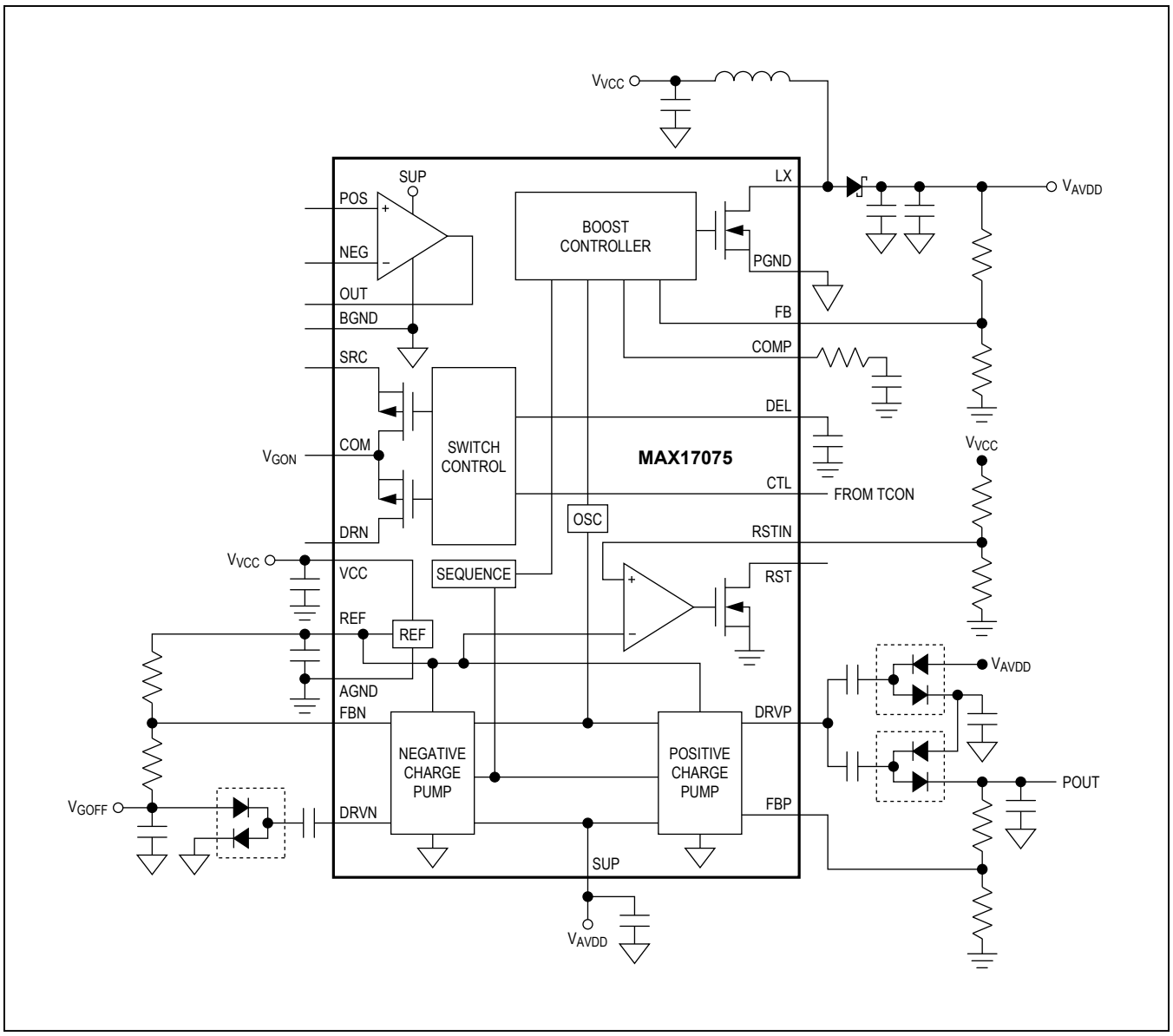


Figure 2. Functional Diagram

Detailed Description

The MAX17075 contains a step-up switching regulator to generate the source driver supply, and two charge-pump regulators to generate the gate-driver supplies. Each regulator features adjustable output voltage, digital soft-start, and timer-delayed fault protection. The step-up regulator uses fixed-frequency current-mode control architecture. The MAX17075 also includes one high-performance operational amplifier designed to drive the LCD backplane (VCOM). The amplifier features high output current, fast slew rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail outputs. In addition, the MAX17075 features a high-voltage switch-control block, a 1.25V reference output, well-defined power-up and power-down sequences, and thermal-overload protection. Figure 2 shows the MAX17075 functional block diagram.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	10µF ±20%, 6.3V X5R ceramic capacitors (0603) Murata GRM188R60J106M TDK C1608X5R0J106M
C3, C4, C7	10µF ±20%, 25V X5R ceramic capacitors (1206) Murata GRM31CR61E106M TDK C3216X5R1E106M
C10, C14	1µF ±10%, 50V X7R ceramic capacitors (1206) Murata GRM31MR71H105KA TDK C3216X7R1H105K
C11, C15, C16, C17	0.1µF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H104K TDK C1608X7R1H104K
D1	3A, 30V Schottky diode (M-Flat) Toshiba CMS02 (TE12L,Q) (Top mark S2)
D2, D3, D4	220mA, 100V dual diodes (SOT23) Fairchild MMBD4148SE (Top mark D4)
L1	3.0µH, $3A_{DC}$ inductor Sumida CDRH6D28-3R0

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild Semiconductor	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

Main Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast-transient response to pulsed loads that are typical for TFT LCD panel source drivers. The 1.2MHz switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel design. The integrated high-efficiency MOSFET and the built-in digital soft-start function reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{IN} to 18V with an external resistive voltage-divider. The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{AVDD} - V_{IN}}{V_{AVDD}}$$

where V_{AVDD} is the output voltage of the step-up regulator.

Figure 3 shows the functional diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.25V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

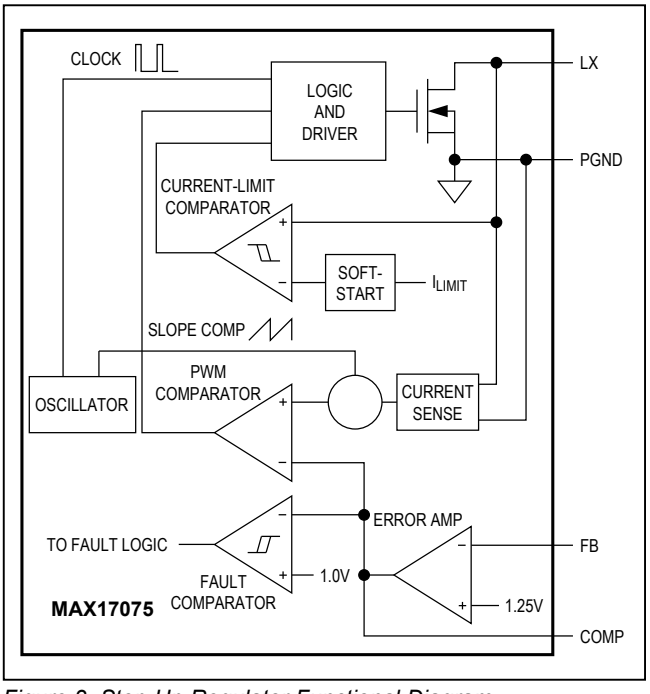


Figure 3. Step-Up Regulator Functional Diagram

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Positive Charge-Pump Regulator

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate-driver ICs. The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The number of charge-pump stages and the setting of the feedback divider determine the output voltage of the positive charge-pump regulator. The charge pump includes a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer as shown in Figure 4.

The error amplifier compares the feedback signal (FBP) with a 1.25V internal reference. If the feedback signal is below the reference, the charge-pump regulator turns on P1 and turns off N1 when the rising edge of the oscillator clock arrives, level shifting C15 and C17 by V_{SUP} volts. If the voltage across C_{POUT} plus a diode drop (V_{POUT} + V_{DIODE}) is smaller than the level-shifted flying capacitor voltage (V_{C17} + V_{SUP}), charge flows from C17 to C_{POUT} until diode D3-1 turns off. Similarly, if the voltage across C16 plus a diode drop (V_{C16} + V_{DIODE}) is smaller than the level-shifted flying capacitor voltage (V_{C15} + V_{SUP}), charge flows from C15 to C16 until diode D2-1 turns off. The falling edge of the oscillator clock turns off P1 and turns on N1, allowing V_{SUP} to charge up the flying capacitor C15 through D2-2 and C16 to charge C17 through diode D3-2. If the feedback signal is above the reference when the rising edge of the oscillator comes, the regulator ignores this clock edge and keeps N1 on and P1 off.

The MAX17075 also monitors the FBP voltage for undervoltage conditions. If the V_{FBP} is continuously below 80% of the nominal regulation voltage for approximately 50ms, the MAX17075 sets a fault latch, shutting down all outputs except REF. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

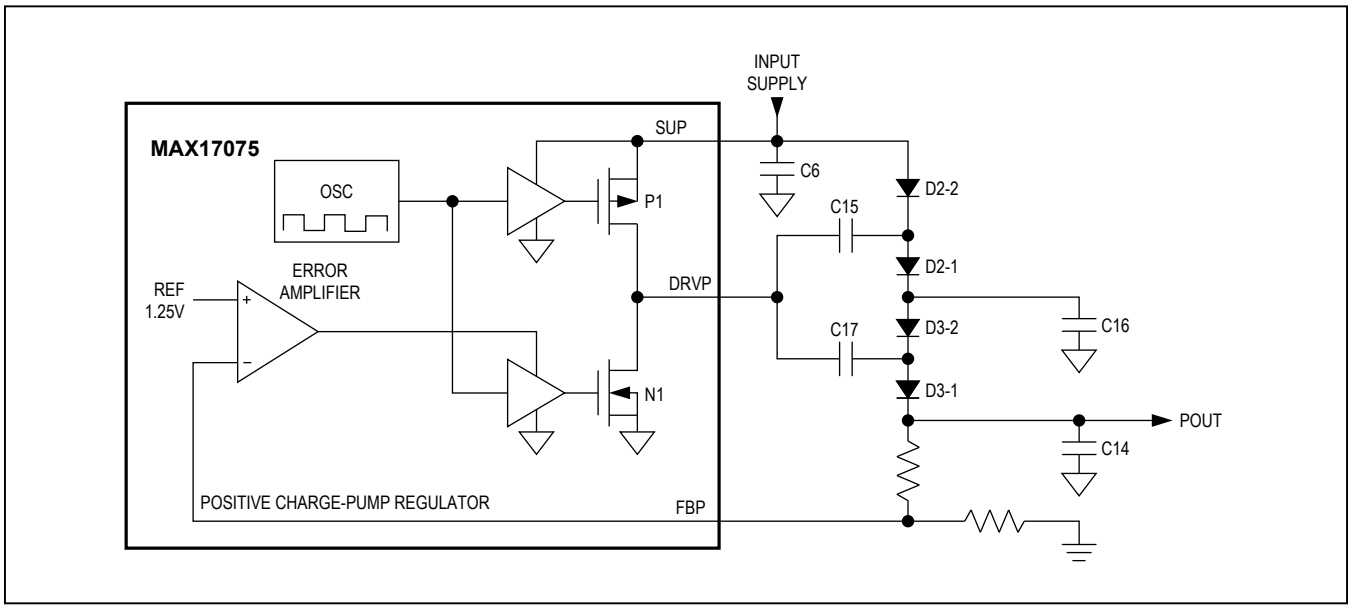


Figure 4. Positive Charge-Pump Regulator Block Diagram

Negative Charge-Pump Regulator

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge-pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P2) and a low-side n-channel MOSFET (N2) to control the power transfer as shown in Figure 5.

The error amplifier compares the feedback signal (FBN) with a 250mV internal reference. If the feedback signal is above the reference, the charge-pump regulator turns on N2 and turns off P2 when the rising edge of the oscillator clock arrives, level shifting C11. This connects C11 in parallel with reservoir capacitor C10. If the voltage across C10 minus a diode drop (V_{C10} - V_{DIODE}) is higher than the level-shifted flying capacitor voltage (-V_{C11}), charge flows from C10 to C11 until diode D4-2 turns off. The falling edge of the oscillator clock turns off N2 and turns on P2, allowing V_{SUP} to charge up flying capacitor C11 through diode D4-1. If the feedback signal is below the reference when the rising edge of the oscillator comes, the regulator ignores this clock edge and keeps P2 on and N2 off.

The MAX17075 also monitors the FBN voltage for undervoltage conditions. If the V_{FBN} is continuously below 80% of the nominal regulation voltage (V_{REF} - V_{FBN}) for approximately 50ms, the MAX17075 sets a fault latch, shutting down all outputs except REF. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

Operational Amplifiers

The MAX17075 has one operational amplifier. The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. It features ±500mA output short-circuit current, 45V/µs slew rate, and 20MHz, 3dB bandwidth.

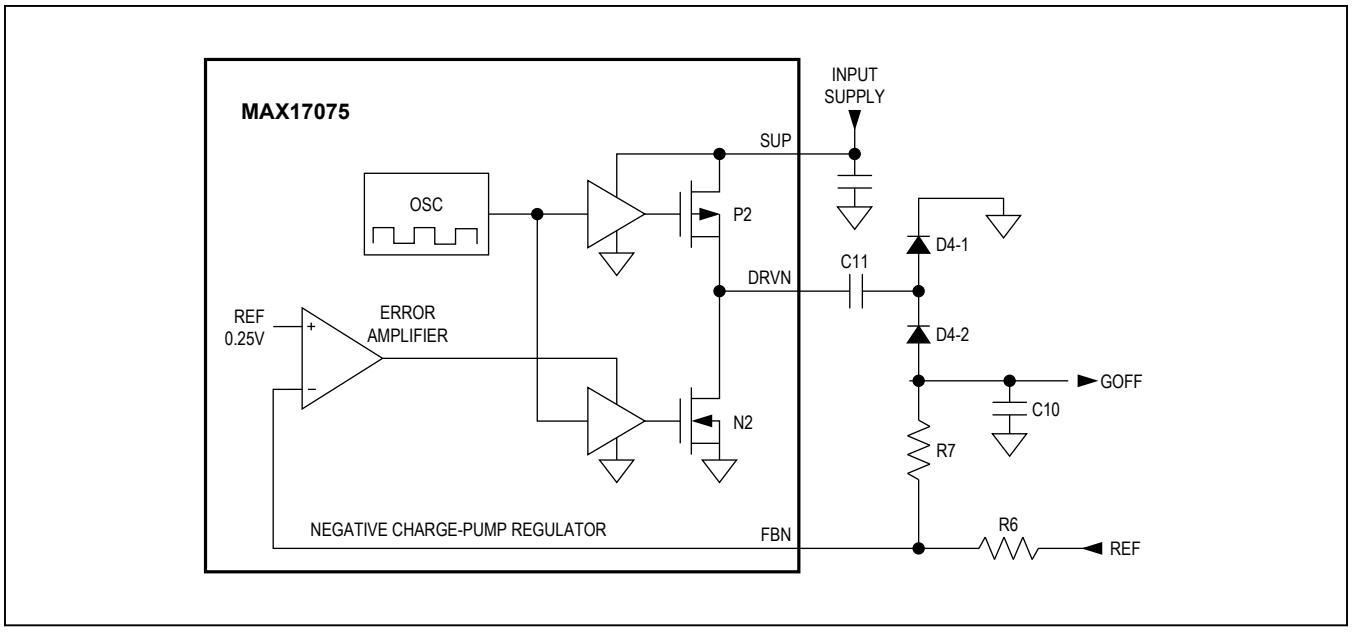


Figure 5. Negative Charge-Pump Regulator Block Diagram

Short-Circuit Current Limit and Input Clamp

The operational amplifier limits short-circuit current to approximately ±500mA if the output is directly shorted to SUP or to BGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal fault latch, shutting off all the IC's outputs. The device remains inactive until the input voltage is cycled. The operational amplifier has 4V input clamp structures in series with a 500Ω resistance and a diode (Figure 6).

Driving Pure Capacitive Load

The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUT and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

High-Voltage Switch Control

The MAX17075's high-voltage switch control block (Figure 7) consists of two high-voltage p-channel MOSFETs: Q1, between SRC and COM; and Q2, between COM and DRN. At power-up and **only** at power up, before the switch control is enabled (a 1.5kΩ pulldown is present on COM). At switch-off, COM is high impedance.

The switch control input (CTL) is not activated until all four of the following conditions are satisfied: the input voltage exceeds UVLO, the soft-start routine of all the regulators is complete, there is no fault condition detected, and V_{DEL} exceeds its turn-on threshold.

Once activated and if CTL is logic-high, Q1 turns on and Q2 turns off, connecting COM to SRC. When CTL is logic-low, Q1 turns off and Q2 turns on, connecting COM to DRN.

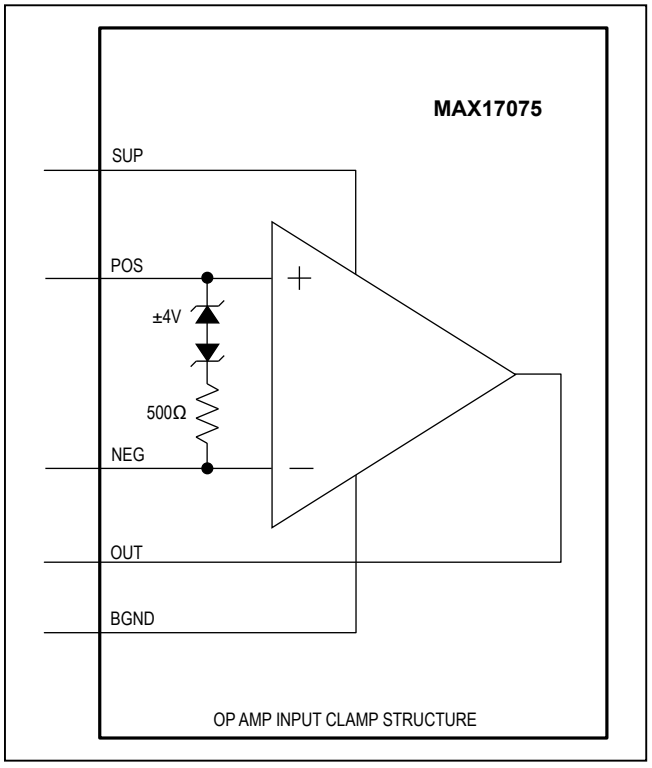


Figure 6. Op Amp Input Clamp Structure

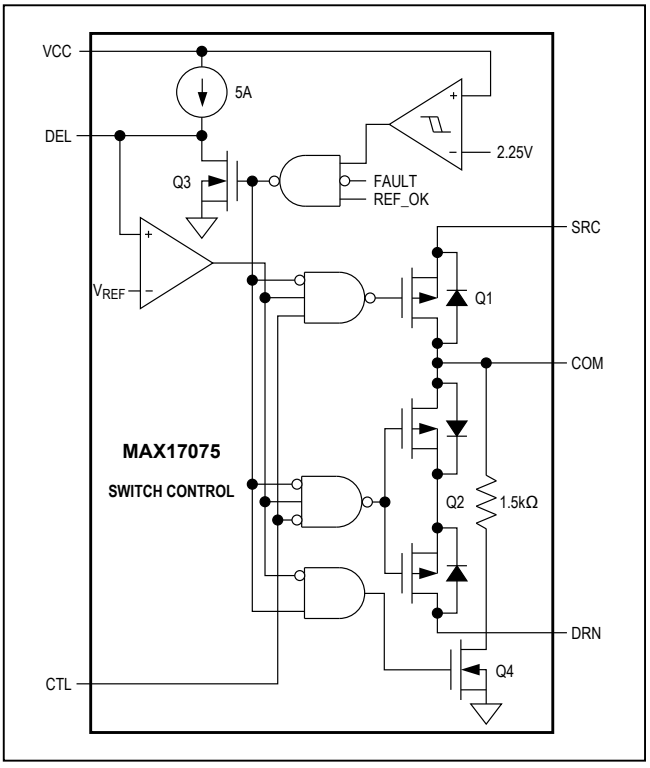


Figure 7. Switch Control

Reference Voltage (REF)

The reference voltage is nominally 1.25V, and can source at least 50µA (see the *Typical Operating Characteristics*). V_{CC} is the input of the internal reference block. Bypass REF with a 0.22µF ceramic capacitor connected between REF and AGND.

Power-Up Sequence and Soft-Start

Once the voltage on V_{CC} exceeds the XAO UVLO threshold of approximately 1.5V, the reference turns on. With a 0.22µF REF bypass capacitor, the reference reaches its regulation voltage of 1.25V in approximately 1ms. When the reference voltage exceeds 1V and V_{CC} exceeds its UVLO threshold of approximately 2.25V, the IC enables the main step-up regulator, the gate-on linear-regulator controller, and the gate-off linear-regulator controller simultaneously.

The IC employs soft-start for each regulator to minimize inrush current and voltage overshoot and to ensure a well-defined startup behavior. Each output uses a 7-bit soft-start DAC. For the step-up and the gate-on linear regulator, the DAC output is stepped in 128 steps from zero up to the reference voltage. For the gate-off linear regulator, the DAC output steps from the reference down to 250mV in 128 steps. The soft-start duration is 10ms (typ) for step-up regulator and 3ms (typ) for gate-on and gate-off regulators.

A capacitor (C_{DEL}) from DEL to AGND determines the switch-control-block startup delay. After the input voltage exceeds the UVLO threshold (2.25V typ) and the soft-start routine for each regulator is complete and there is no fault detected, a 5mA current source starts charging C_{DEL}. Once the capacitor voltage exceeds 1.25V (typ), the switch-control block is enabled as shown in Figure 8. After the switch-control block is enabled, COM can be connected to SRC or DRN through the internal p-channel switches, depending upon the state of CTL. Before startup and when V_{IN} is less than UVLO, DEL is internally connected to AGND to discharge C_{DEL}. Select C_{DEL} to set the delay time using the following equation:

$$C_{DEL} = DELAY_TIME \times \frac{5\mu A}{1.25V}$$

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at V_{CC} with the UVLO threshold (2.25V rising, 2.20V falling, typ) to ensure the input voltage is high enough for reliable operation. The 50mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins.

When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator and disables the switch-control block; the operational amplifier output is high impedance.

Fault Protection

During steady-state operation, if the output of the main regulator or any of the linear-regulator outputs exceed their respective fault-detection thresholds, the MAX17075 activates an internal fault timer. If any condition or combination of conditions indicates a continuous fault for the fault-timer duration (50ms typ), the MAX17075 sets the fault latch to shut down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time.

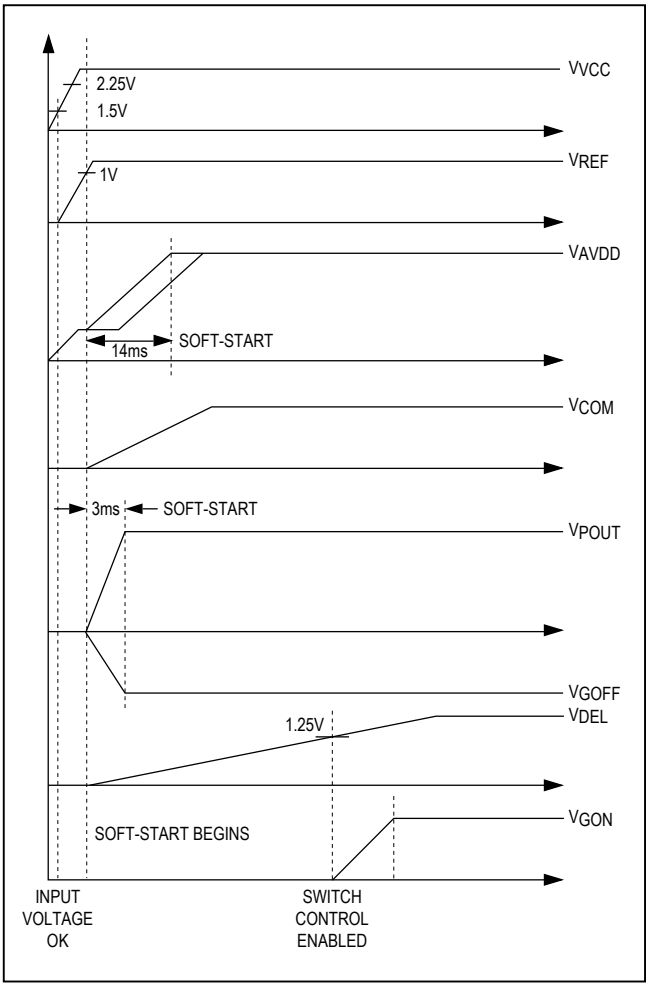


Figure 8. Power-Up Sequence

Thermal-Overload Protection

Thermal-overload protection prevents excessive power dissipation from overheating the MAX17075. When the junction temperature exceeds +160°C, a thermal sensor immediately activates the fault protection, which shuts down all outputs except the reference, allowing the device to cool down. Once the device cools down by approximately 15°C, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

XAO Voltage Detector

Based upon the input at the RSTIN and VCC pins, the XAO controller either pulls the reset pin RST low or sets it to high impedance. RST is an open-drain output. Pull it high to system 3.3V through a 10kΩ resistor. Connect RSTIN to V_{IN} through resistor-dividers R11 and R12 (Figure 1) to set the proper XAO threshold.

Once V_{CC} voltage exceeds approximately 2.25V, the controller initiates a 220ms blanking period during which the drop on V_{CC} is ignored and RST is set to high impedance. After this blanking period and if RSTIN goes below approximately 1.25V, RST is pulled low indicating low RSTIN input. RST stays low until V_{CC} falls below approximately 1V. Then RST cannot be held low any more. The controller gives up and RST is pulled up by the external resister. A 50mV hysteresis is implemented for XAO threshold.

Design Procedure

Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output voltage ripple. Size and cost are also important factors to consider.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple, and therefore reduce the peak current, which decreases core losses in the inductor and conduction losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase size and can increase conduction losses in the inductor. Low inductance values decrease the size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.6. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(MAX)}$), and the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics* section, and an estimate of LIR based on the above discussion:

$$L_{AVDD} = \left(\frac{V_{IN}}{V_{AVDD}}\right)^2 \left(\frac{V_{AVDD} - V_{IN}}{I_{AVDD(MAX)} \times f_{SW}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage ($V_{IN(MIN)}$) using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from the appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{AVDD(MAX)} \times V_{AVDD}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{AVDD_RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{AVDD} - V_{IN(MIN)}\right)}{L_{AVDD} \times V_{AVDD} \times f_{SW}}$$

$$I_{AVDD_PEAK} = I_{IN(DC,MAX)} + \frac{I_{AVDD_RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17075's LX current limit should exceed I_{AVDD_PEAK}, and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{AVDD(MAX)}$) is 500mA with a 13V output and a typical input voltage of 5V. Choosing an LIR of 0.5 and estimating efficiency of 85% at this operating point:

$$L_{AVDD} = \left(\frac{5V}{13V}\right)^2 \left(\frac{13V - 5V}{0.5A \times 1.2MHz}\right)\left(\frac{0.85}{0.5}\right) \approx 3.35\mu H$$

Using the circuit's minimum input voltage (2.5V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.5A \times 13V}{2.5V \times 0.8} \approx 3.25A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{2.5V \times (13V - 2.5V)}{3.3\mu H \times 13V \times 1.2MHz} \approx 0.51A$$

$$I_{PEAK} = 3.25A + \frac{0.51A}{2} \approx 3.51A$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{AVDD_RIPPLE} = V_{AVDD_RIPPLE(C)} + V_{AVDD_RIPPLE(ESR)}$$

$$V_{AVDD_RIPPLE(C)} \approx \frac{I_{AVDD}}{C_{AVDD}}\left(\frac{V_{AVDD} - V_{IN}}{V_{AVDD} f_{SW}}\right),$$

and

$$V_{AVDD_RIPPLE(ESR)} \approx I_{PEAK} R_{ESR_AVDD}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{AVDD_RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input-Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 10µF ceramic capacitors are used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the typical operating circuit. Ensure a low-noise supply at V_{CC} by using adequate C_{IN}. Alternately, greater voltage variation can be tolerated on C_{IN} if VCC is decoupled from C_{IN} using an RC lowpass filter (see R1 and C5 in Figure 1).

Rectifier Diode

The MAX17075's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output Voltage Selection

The output voltage of the step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{AVDD}) to ground with the center tap connected to FB (see Figure 1). Select R9 in the 10kΩ to 50kΩ range. Calculate R8 with the following equation:

$$R8 = R9 \times \left(\frac{V_{AVDD}}{V_{FB}} - 1\right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.25V. Place R8 and R9 close to the IC.

Loop Compensation

Choose R_{COMP} (R10 in Figure 1) to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} (C12 in Figure 1) to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{312.5 \times V_{IN} \times V_{AVDD} \times C_{AVDD}}{L_{AVDD} \times I_{AVDD(MAX)}}$$

$$C_{COMP} \approx \frac{V_{AVDD} \times C_{AVDD}}{10 \times I_{AVDD(MAX)} R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

Charge-Pump Regulators

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement.

The number of positive charge-pump stages is given by:

$$\eta_{POS} = \frac{V_{GON} + V_{DROPOUT} - V_{AVDD}}{V_{SUP} - 2 \times V_D}$$

where n_{POS} is the number of positive charge-pump stages, V_{GON} is the output of the positive charge-pump regulator, V_{SUP} is the supply voltage of the charge-pump regulators, V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the regulator. Use $V_{DROPOUT}$ = 600mV.

The number of negative charge-pump stages is given by:

$$\eta_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT}}{V_{SUP} - 2 \times V_D}$$

where n_{NEG} is the number of negative charge-pump stages and V_{GOFF} is the output of the negative chargepump regulator.

The above equations are derived based on the assumption that the first stage of the positive charge-pump is connected to V_{AVDD} and the first stage of the negative charge-pump is connected to ground.

Flying Capacitors

Increasing the flying capacitor C_X (connected to DRVN and DRVP) value lowers the effective source impedance and increases the output current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{SUP}$$

where n is the stage number in which the flying capacitor appears.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT_CP} \geq \frac{I_{LOAD_CP}}{2 f_{OSC} V_{RIPPLE_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple, and f_{OSC} is the switching frequency.

Output Voltage Selection

Adjust the positive charge-pump regulator's output voltage by connecting a resistive voltage-divider from the REG P output to GND with the center tap connected to FBP (Figure 1). Select the lower resistor of divider R16 in the 10kΩ to 30kΩ range. Calculate the upper resistor R15 with the following equation:

$$R15 = R16 \times \left(\frac{V_{GON}}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 1.25V (typical).

Adjust the negative charge-pump regulator's output voltage by connecting a resistive voltage-divider from V_{GOFF} to REF with the center tap connected to FBN (Figure 1). Select R6 in the 35kΩ to 68kΩ range. Calculate R7 with the following equation:

$$R7 = R6 \times \frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}$$

where V_{FBN} = 250mV, V_{REF} = 1.25V. Note that REF can only source up to 50µA, using a resistor less than 35kΩ for R6 results in higher bias current than REF can supply.

Set the XAO Threshold Voltage

XAO threshold voltage can be adjusted by connecting a resistive voltage-divider from input V_{IN} to GND with the center tap connected to RSTIN (see Figure 1). Select R12 in the 10kΩ to 50kΩ range. Calculate R11 with the following equation:

$$R11 = R12 \times \left(\frac{V_{INXAO}}{V_{RSTIN}} - 1 \right)$$

where V_{RSTIN}, the RSTIN threshold set point, is 1.25V. V_{INXAO} is the desired XAO threshold voltage. Place R11 and R12 close to the IC.

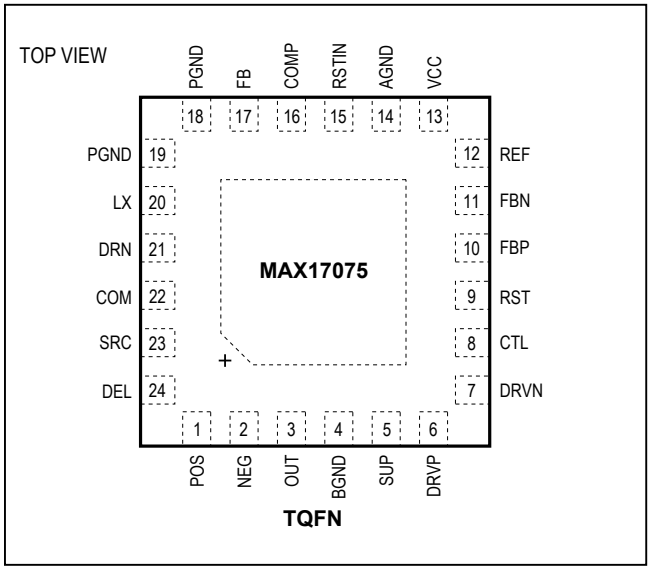
PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, the output diode, and the output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), and to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections.
- Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power-ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational amplifier divider ground connections, the COMP and DEL capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place all feedback voltage-divider resistors within 5mm of their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Take care to avoid running any feedback trace near LX or the switching nodes in the charge pumps, or provide a ground shield.
- Place the V_{CC} pin and REF pin bypass capacitors as close as possible to the device. The ground connection of the V_{CC} bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from feedback nodes (FB, FBP, and FBN) and analog ground. Use DC traces to shield if necessary.

Refer to the MAX17075 evaluation kit for an example of proper PCB layout.

Pin Configuration



Chip Information

PROCESS: S45UR

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/08	Initial release	—
1	5/12	Updated *Absolute Maximum Ratings*	2
2	12/12	Added MAX17075GTG/V+ to *Ordering Info* and corrected typos	1, 2, 4–6
3	3/26	Updated *Package Information* table	2

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