Click here for production status of specific part numbers.

MAX20030/MAX20031

Dual Buck, Sync Boost and LDO– Complete Front-End Power Supply with 17µA I_Q

General Description

The MAX20030/MAX20031 ICs are automotive 2.2MHz dual-synchronous step-down controllers with preboost controller and low-I_Q LDO. The preboost controller enables V_{OUT1} and V_{OUT2} to stay in regulation during cold-crank operation all the way down to battery input of 2V. The ICs offer two high-voltage synchronous step-down controllers that operate 180 degrees out of phase. This device operates with an input-voltage supply from 3.5V to 42V and can operate in dropout conditions by running at 97% duty cycle. It is intended for applications with mid- to high-power requirements that operate at a wide input voltage range, such as during automotive cold-crank or engine stop-start conditions.

The step-down controllers operate at a frequency of up to 2.2MHz to allow small external components, reduced output ripple, and to guarantee no AM band interference. The switching frequency is resistor-adjustable (220kHz to 2200kHz). SYNC input programmability enables three frequency modes for optimized performance: forced fixed-frequency operation, skip mode with ultra-low quiescent current, and synchronization to an external clock. The ICs have a spread-spectrum pin for frequency modulation to minimize EMI interference.

The ICs will be offered with a synchronous step-up controller. This preboost circuitry turns on during low input-voltage conditions, and is designed to provide power to step-down controller channels with input voltages as low at 2V.

The ICs feature a power-OK monitor and overvoltage and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. The MAX20030/MAX20031 are specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Instrument Cluster
- Distributed DC Power Systems
- Navigation and Radio Head Units

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

Benefits and Features

- Meets Stringent OEM Module Power Consumption and Performance Specifications
  - 17µA I_Q with 3.3V Buck On
  - 25µA I_Q with 5V Buck On
  - 25µA I_Q with LDO On
  - 65µA I_Q with All Controllers Enabled
- Enables Crank-Ready Designs
  - Synchronous Boost Converter for High-Current Capability and Efficiency
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 50ns (typ) Minimum On-Time Guarantees Skip-Free Operation for 3.3V Output from Car Battery at 2.2MHz
  - Forced Fixed-Frequency PWM Operation
  - Resistor-Programmable Frequency Between 220kHz and 2.2MHz
  - Pin-Selectable Spread Spectrum
- Integration and Thermally Enhanced Packages Save Board Space and Cost
  - Dual 2.2MHz Step-Down Controller with Synchronous Boost Controller and HV 200mA LDO
  - Current-Mode Controller with Forced-Fixed Frequency and Skip Modes
  - Thermally Enhanced 7mm x 7mm, 48-Pin TQFN Packages with Exposed Pad
- Protection Features Improve System Reliability
  - Supply Overvoltage and Undervoltage Lockout
  - Overtemperature and Short-Circuit Protections

Device Options

PART	PACKAGE
MAX20030	48-Pin TQFN, 48-Pin QFND
MAX20031	48-Pin TQFN, 48-Pin QFND

19-8485; Rev 21; 7/21

maxim integrated™

Absolute Maximum Ratings

IN, CS3P, FB3, EN1–EN4, TERM, INLDO, LX_ to AGND ..... -0.3V to +42V
OUT1, OUT2, OUT4 to AGND ..... -0.3V to +12V
CS1 to OUT1 ..... -0.3V to +0.3V
CS2 to OUT2 ..... -0.3V to +0.3V
CS3P to CS3N ..... -0.3V to +0.3V
BIAS, AGND ..... -0.3V to +6V
FSYNC, FOSC, BSTON, PGOOD_, SPS, FB1, FB2, FB4, COMP_, EXTVCC to AGND ..... +0.3V to BIAS + 0.3V
DL_ to PGND_ (Note 1) ..... -0.3V to BIAS + 0.3V
BST_ to LX_ (Note 1) ..... -0.3V to +6V
DH_ to LX (Note 1) ..... -0.3V to BIAS + 0.3V
PGND_ to AGND ..... -0.3V to +0.3V

ESD Results
Human Body Model 2.5kV
CDM (MAX20030) ..... 425V (all pins), 750V (corner pins)
CDM (MAX20030B) ..... 500V (all pins), 750V (corner pins)
CDM (MAX20031) ..... 475V (all pins), 750V (corner pins)
CDM (MAX20031B) ..... 500V (all pins), 750V (corner pins)
LU ..... ±100mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 37mW/°C above +70°C) 2963mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Package Information

PACKAGE TYPE: 48 TQFN	
Package Code	T4877+9C
Outline Number	**21-0144**
Land Pattern Number	**90-0464**
PACKAGE TYPE: 48 SW TQFN	
Package Code	T4877Y+9C
Outline Number	**21-100354**
Land Pattern Number	**90-100116**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	23.3°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal consideration see **www.maxim-ic.com/thermal-tutorial.**

Electrical Characteristics

V_{IN} = 14V, $V_{EN_}$ = 14V, C_{BIAS} = 6.8µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONOUS STEP-DOWN CONVERTERS						
Supply Voltage Range	V_{IN}	Normal operation	3.5		36	V
		t < 1s			42	
		With preboost enabled	2		36	
Supply Current	I_{IN}	V_{EN1} = V_{EN2} = V_{EN4} = 0V, EN3 = disabled		7	10	µA
		V_{EN1} = 5V, V_{OUT1} = 5V, V_{EN2} = V_{EN4} = 0V, V_{EN3} = disabled, EXTVCC = 5V (no switching)		25	40	
		V_{EN2} = 5V, V_{OUT2} = 3.3V, V_{EN1}= V_{EN4} = 0V, V_{EN3} = disabled, EXTVCC = 3.3V (no switching)		17	28	
		V_{EN1} = V_{EN2} = 5V, V_{EN3} = enabled, V_{EN4} = 0V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, EXTVCC = 3.3V, FB3 > 1.15V (no switching)		65	90	
Buck 1 Fixed Output Voltage	V_{OUT1}	V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, PWM mode	4.925	5	5.075	V
Buck 2 Fixed Output Voltage	V_{OUT2}	V_{FB2} = V_{BIAS}, V_{OUT2} = 3.3V, PWM mode	3.25	3.3	3.35	V
Output Voltage-Adjustable Range		Buck 1, Buck 2	1		10	V
Regulated Feedback Voltage	$V_{FB1,2}$		0.99	1	1.01	V
Feedback Leakage Current	$I_{FB1,2}$	T_A = +25°C		0.01	1	µA
Feedback Line Regulation Error		V_{IN} = 3.5V to 36V, V_{FB} = 1V		0.01		%/V
Transconductance (from FB1, FB2 to COMP1, COMP2)	gm_buck	$V_{FB1,2}$ = 1V, V_{BIAS} = 5V	350	700	1100	µS
Dead Time		DL low to DH rising		20		ns
		DH low to DL rising		20		
Maximum Duty Cycle		Buck 1, Buck 2	97			%
Minimum On-Time	$t_{ON,MIN}$	Buck 1, Buck 2		50	60	ns
PWM Switching-Frequency Range	f_{SW}	Programmable	0.22		2.2	MHz
Switching-Frequency Accuracy		R_{FOSC} = 12kΩ, V_{BIAS} = 5V, 3.3V	2	2.2	2.4	MHz
CS Current-Limit Voltage Threshold	$V_{LIMIT1,2}$	$V_{CS_}$ - V_{OUT}; V_{BIAS} = 5V, V_{OUT} ≥ 2.5V	68	80	92	mV
Soft-Start Ramp Time		Buck 1 and buck 2	3	5	8	ms

Electrical Characteristics (continued)

V_{IN} = 14V, $V_{EN_}$ = 14V, C_{BIAS} = 6.8µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Phase Shift Between Buck 1 and Buck 2		PWM operation (Note 3)		180		Deg
LX1,2 Leakage Current		V_{IN} = 6V, $V_{LX_}$ = V_{AGND} or V_{IN}, T_A = +25°C		0.001	10	µA
DH1,2 Pullup Resistance		V_{BIAS} = 5V, I_{DH} = -100mA		3	6	Ω
DH1,2 Pulldown Resistance		V_{BIAS} = 5V, I_{DH} = 100mA		1.5	3	Ω
DL1,2 Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		3	6	Ω
DL1,2 Pulldown Resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1.5	3	Ω
Output Overvoltage Threshold (Buck Controllers)		Detected with respect to V_{FB} rising	106	109	112	%
Output Overvoltage Threshold (Buck Controllers)		Detected with respect to V_{FB} rising MAX20030BATMx/V+ (x = A,C) MAX20031BATMx/V+ (x = A,B,C,D,F)	107	109	112	%
Output Overvoltage Hysteresis				3		%
PGOOD1,2 Threshold	PGOOD_H	% of $V_{OUT_}$, rising	93	95	97	%
	PGOOD_F	% of $V_{OUT_}$, falling	90	92	94	
PGOOD1,2 Leakage Current		$V_{PGOOD1,2}$ = 5V, T_A = +25°C		0.01	1	µA
PGOOD1,2 Output Low Voltage		I_{SINK} = 1mA			0.2	V
PGOOD1,2 Debounce Time		Fault detection, rising and falling		20		us
FSYNC INPUT						
FSYNC Frequency Range		Minimum sync pulse of 150ns, R_{FOSC} = 12kΩ	1.8		2.6	MHz
FSYNC Frequency Range		Minimum sync pulse of 150ns, R_{FOSC} = 70kΩ	250		550	kHz
FSYNC Switching Thresholds		Low threshold			0.4	V
		High threshold	1.4			
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{IN} > 6V, no load	4.5	5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.25	V
		V_{BIAS} falling	2.35	2.6		
EXTVCC Operating Range			3.25		5.5	V
EXTVCC Threshold		EXTVCC rising, hysteresis = 110mV	2.85	3	3.25	V
THERMAL OVERLOAD						
Thermal-Shutdown Temperature		(Note 3)		170		°C
Thermal-Shutdown Hysteresis		(Note 3)		20		°C
EN LOGIC INPUT						
High Threshold		EN1, EN2	1.8			V

Electrical Characteristics (continued)

V_{IN} = 14V, $V_{EN_}$ = 14V, C_{BIAS} = 6.8µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Low Threshold		EN1, EN2			0.8	V
EN1, EN2 Input Bias Current		T_A = +25°C		0.01	1	µA
SPS LOGIC INPUT						
Spread Spectrum		Spread spectrum enabled		FOSC ±6%		
Spread Spectrum Input High Threshold	V_{SPS_HI}		1.4			V
Spread Spectrum Input Low Threshold	V_{SPS_LO}				0.4	V
Spread Spectrum Input Current	I_{SPS}	T_A = +25°C		0.1	1	µA
STEP-UP CONTROLLER						
Minimum On-Time	t_{ONBST}	(Note 3)		40		ns
Minimum Off-Time	t_{OFFBST}			70		ns
Current Limit	I_{LIMBST}	V_{CS3P} - V_{CS3N}	44	50	56	mV
Dead Time		DL3 low to DH3 rising		30		ns
		DH3 low to DL3 rising		20		
DH3 Pullup Resistance		V_{BIAS} = 5V, I_{DH3} = -100mA		3	6	Ω
DH3 Pulldown Resistance		V_{BIAS} = 5V, I_{DH3} = 100mA		1	2	Ω
DL3 Pullup Resistance		V_{BIAS} = 5V, I_{DL3} = -100mA		3	6	Ω
DL3 Pulldown Resistance		V_{BIAS} = 5V, I_{DL3} = 100mA		1	2	Ω
Boost Feedback Voltage	FB3	Feedback voltage of the preboost, no load on boost output	0.99	1.005	1.02	V
Transconductance (from FB3 to COMP3)	g_{M_BOOST}	V_{FB3} = 1V, V_{BIAS} = 5V	160	250	400	µS
Boost Load Regulation Error	I_{LD3}	PWM mode, (ILOAD from 1mA to 10A)		0.001		%/A
EN3 Threshold		Falling threshold that turns ON the boost; hysteresis = 100mV (MAX20030ATMD,E,F/V+)	0.92	0.95	0.98	V
EN3 Logic-High Threshold	EN3	MAX20030,1ATMA,B,C/V+	1.8			v
EN3 Logic-Low Threshold	EN3				0.8	V
EN3 Input Current		EN3 Logic Input Only, T_A = +25°C		0.01	1	µA
TERM Resistance		I_{TERM} = 10mA		70	150	Ω
TERM Leakage Current		CS3P = TERM = 14V, V_{EN3} = disabled, T_A = +25°C		0.01	1	µA
FB3 Leakage Current		T_A = +25°C		0.01	1	µA

Electrical Characteristics (continued)

V_{IN} = 14V, $V_{EN_}$ = 14V, C_{BIAS} = 6.8µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
BSTON Leakage Current		BSTON logic input only, T_A = +25°C		0.01	1	µA
BSTON Output Low Voltage		I_{SINK} = 1mA			0.2	V
HIGH-VOLTAGE STAND-ALONE LDO						
Supply Voltage Range	V_{INLDO4}		3.5		36	V
Supply Current		I_{LOAD} = 0, V_{EN1} = V_{EN2} = 0, V_{EN3} = disabled, V_{EN4} = V_{IN}, internal feedback		25	38	µA
		I_{LOAD} = 0, V_{EN1} = V_{EN2} = 0, V_{EN3} = disabled,V_{EN4} = V_{IN}, external feedback		20	38	µA
Output-Voltage Accuracy	V_{OUT4_5V}	I_{LOAD} = 1mA to 200mA	4.9	5.0	5.1	V
	V_{OUT4_3P3V}		3.234	3.3	3.366	
Feedback Voltage	V_{FB4}	I_{LOAD} = 1mA to 300mA, MAX20030BATMI/V+, MAX20031BATMF/V+	1.2	1.25	1.275	V
Feedback Leakage Current	I_{FB4}	T_A = +25°C		0.01	1	µA
Adjustable Output Voltage Range		Resistor-divider on FB4	1.5		10	V
Dropout Voltage		I_{LOAD} = 200mA		250	500	mV
		I_{LOAD} = 300mA, MAX20030BATMI/V+, MAX20031BATMF/V+		500	1000	
LDO Current Limit		200mA	210	400		mA
		300mA	310			
Line Regulation		6V ≤ V_{IN} ≤ 36V, I_{LOAD} = 1mA		5		mV
Load Regulation		V_{IN} = 14V, I_{LOAD} = 1mA to 200mA		12		mV
		V_{IN} = 14V, I_{LOAD} = 1mA to 300mA		28		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 10mA, f = 100Hz, 500mV_{P-P} (Note 3)		65		dB
Start up Response Time	t_{START}	Rising edge of V_{IN} to V_{OUT4}, I_{LOAD} = 100mA (Note 3)		250		µs
LDO LOGIC INPUTS						
EN4 Input Low Voltage	V_{IL}				0.8	V
EN4 Input High Voltage	V_{IH}		1.8			V
Enable Input Bias Current		EN4 logic inputs only, T_A = +25°C		0.01	1	µA
Minimum Voltage on INLDO		To keep LDO out of dropout (Note 3)	V_{OUT4} + 0.5V			V

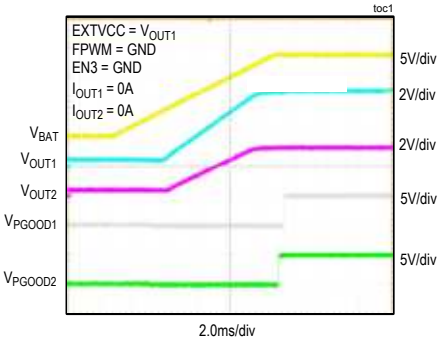
Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 3: Guaranteed by design; not production tested.

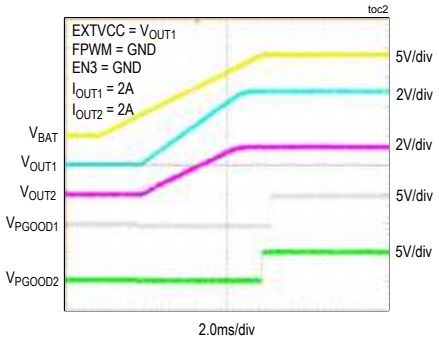
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

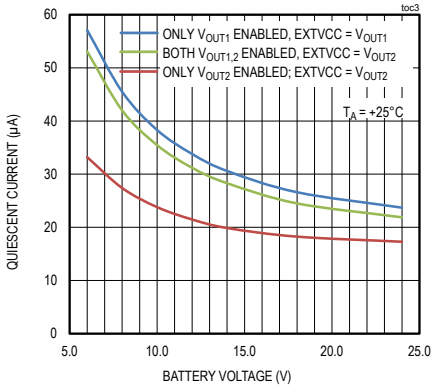
STARTUP INTO NO-LOAD



STARTUP INTO LOAD



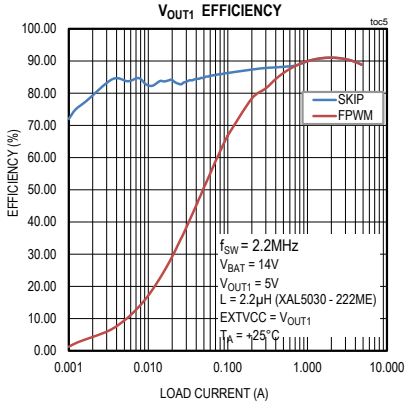
QUIESCENT CURRENT vs. BATTERY VOLTAGE



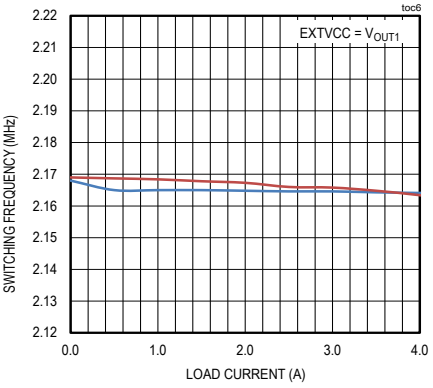
SHUTDOWN CURRENT vs. BATTERY VOLTAGE



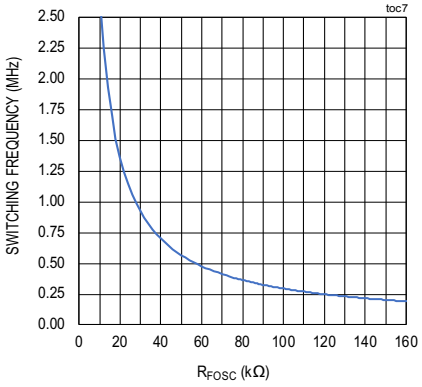
V_{OUT1} EFFICIENCY



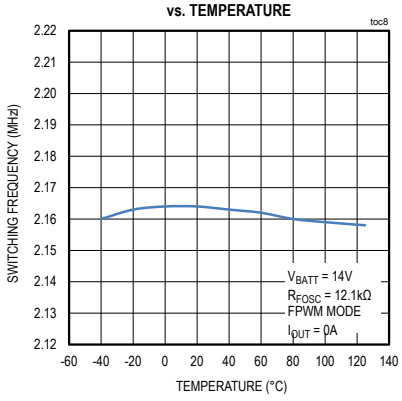
SWITCHING FREQUENCY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. R_{FOSC}



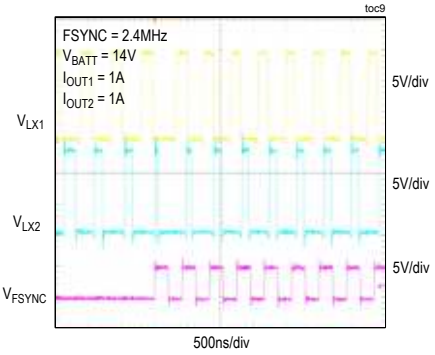
SWITCHING FREQUENCY vs. TEMPERATURE



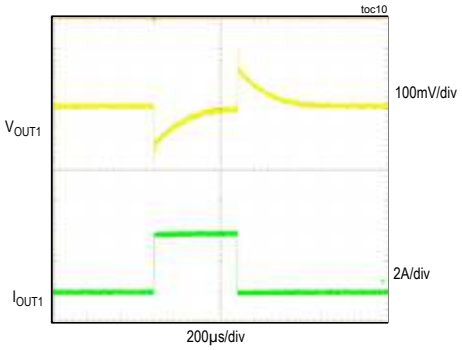
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

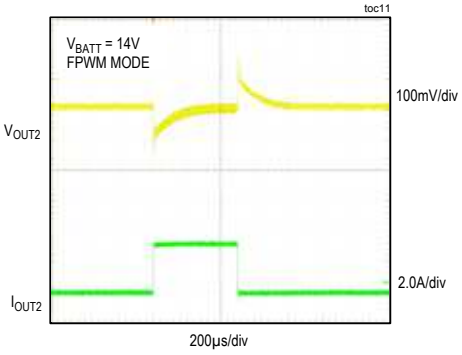
EXTERNAL FSYNC TRANSITION



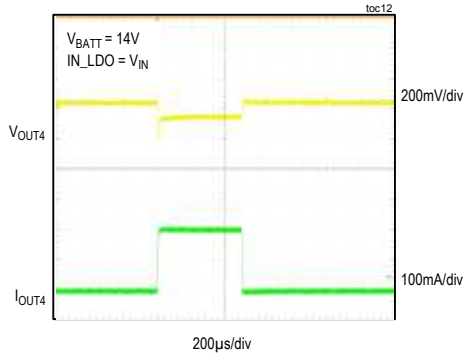
BUCK1 LOAD TRANSIENT RESPONSE



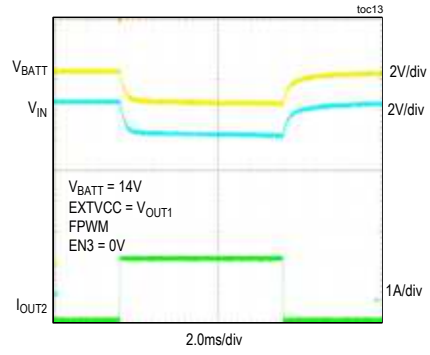
BUCK2 LOAD TRANSIENT RESPONSE



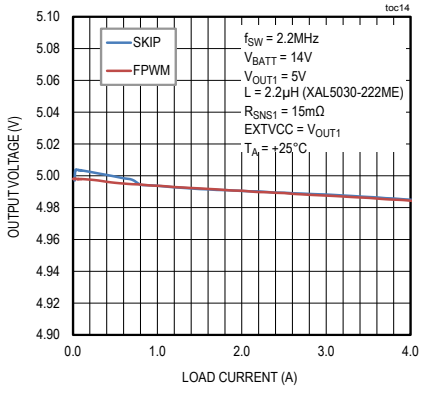
LDO LOAD TRANSIENT RESPONSE



CHARGE PUMP ACTIVATION



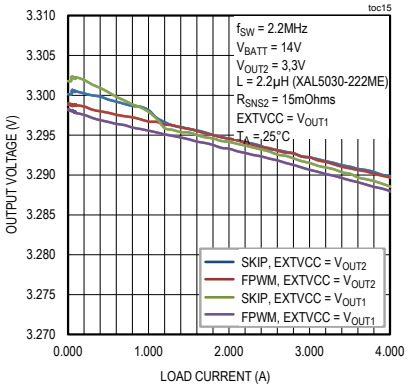
BUCK1 LOAD REGULATION



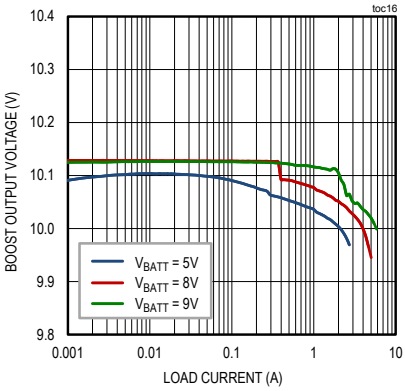
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

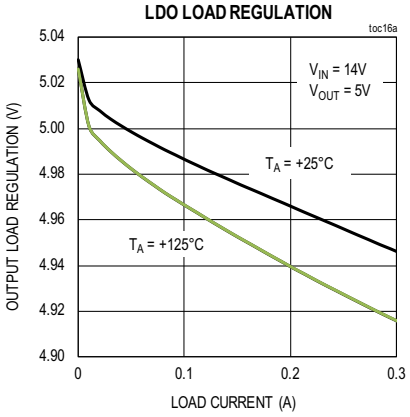
BUCK2 LOAD REGULATION



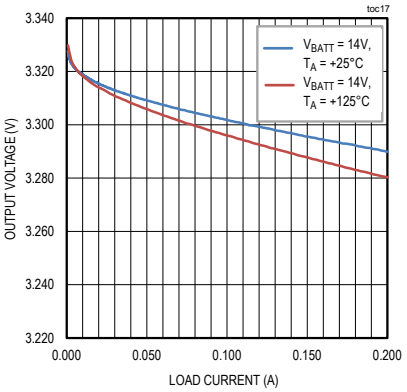
BOOST OUTPUT VOLTAGE vs. LOAD CURRENT



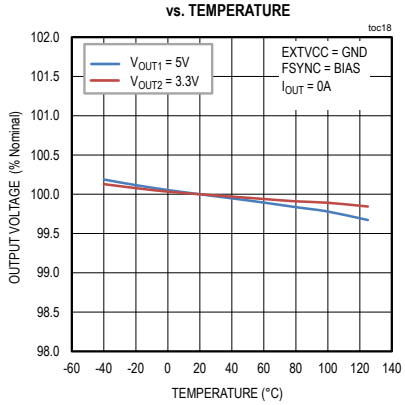
LDO LOAD REGULATION



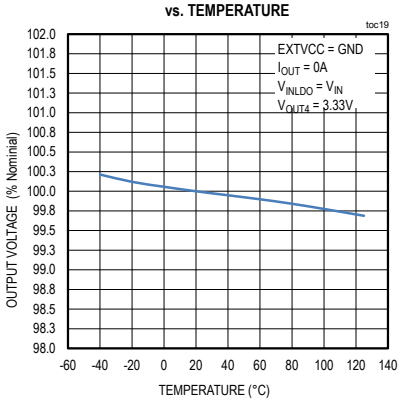
LDO LOAD REGULATION



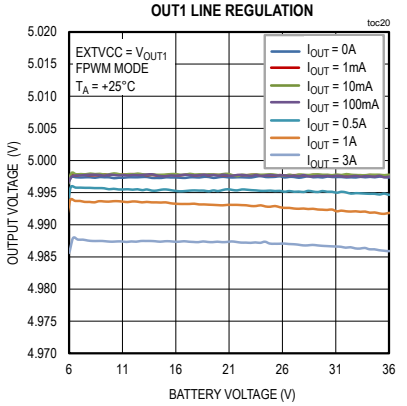
STEP DOWN OUTPUT VOLTAGE vs. TEMPERATURE



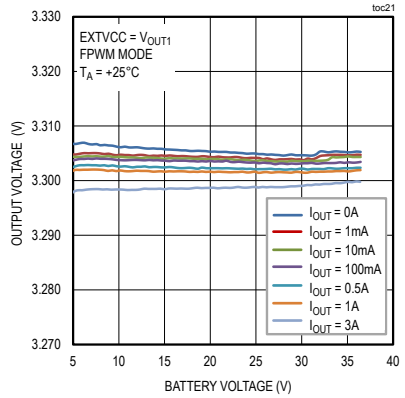
LDO OUTPUT VOLTAGE vs. TEMPERATURE



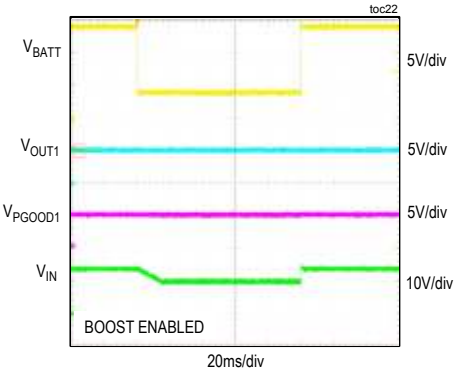
OUT1 LINE REGULATION



OUT2 LINE REGULATION



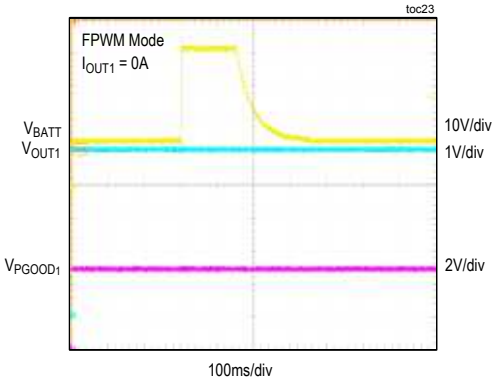
DIPS AND DROPS



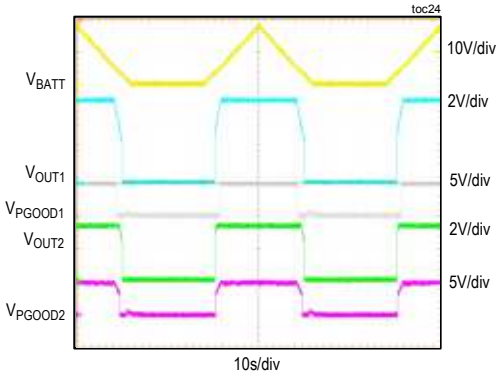
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

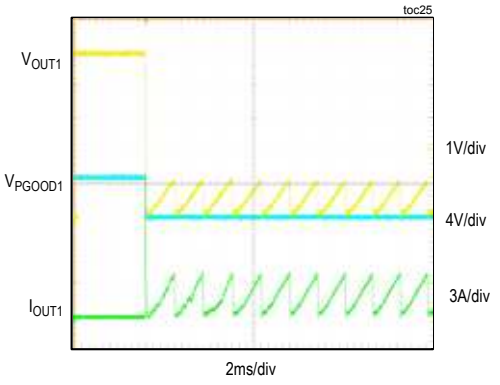
LOAD DUMP



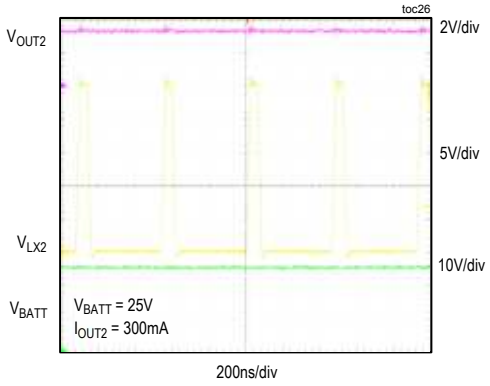
SLOW V_{IN} RAMP



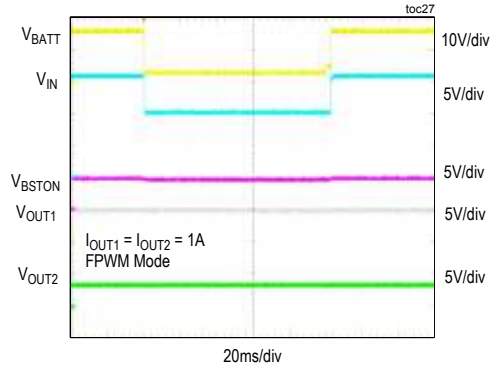
SHORT-CIRCUIT RESPONSE



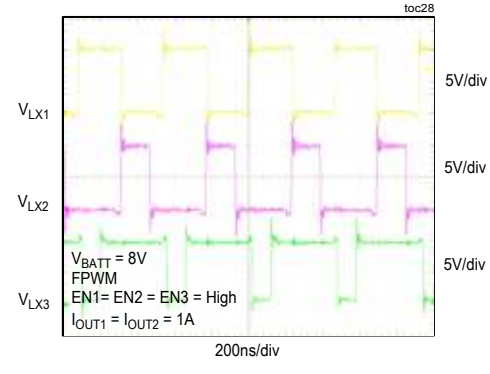
MINIMUM ON-TIME BUCK 2



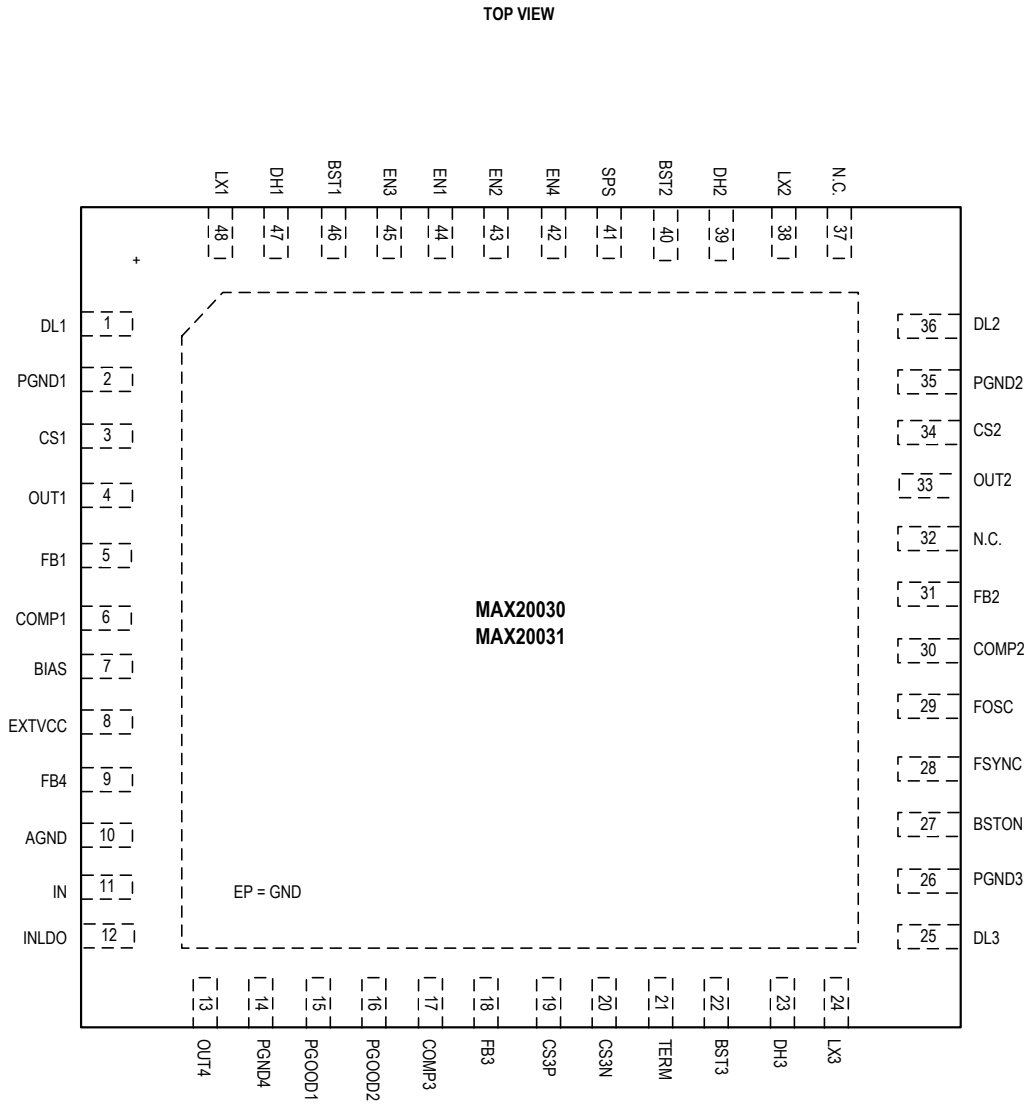
COLD CRANK (BOOST ENABLED)



LX WAVEFORMS



Pin Configuration



Pin Description

NAME	LOCATION	DESCRIPTION
DL1	1	Low-Side Gate-Driver Output for Controller One. DL1 output voltage swings from V_{PGND1} to V_{BIAS}.
PGND1	2	Power Ground for Controller One
CS1	3	Positive Current-Sense Input for Buck Controller One. Connect CS1 to the positive terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (OUT_ and CS_)* and *Current-Sense Measurement* sections.
OUT1	4	Output Sense and Negative Current-Sense Input for Buck Controller One. When using the internal preset 5V feedback-divider (FB1 = BIAS), the controller uses OUT1 to sense the output voltage. Connect OUT1 to the negative terminal of the current-sense element. See the Current Limiting and Current Sense Inputs and *Current-Sense Measurement* sections.
FB1	5	Feedback Input for Buck Controller One. Connect FB1 to BIAS for the 5V fixed output or to a resistive divider between OUT1 and GND to adjust the output voltage between 1V and 10V. In adjustable mode, FB1 regulates to 1V (typ). See the *Setting the Output Voltage in Buck Converters* section.
COMP1	6	Buck Controller One Error-Amplifier Output. Connect an RC network to COMP1 to compensate buck converter one.
BIAS	7	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 6.8µF (min) value. BIAS provides the power to the internal circuitry and external loads. See the Fixed 5V Linear Regulator (BIAS) section.
EXTVCC	8	Input Pin. The allowed voltage range is between 3.25V and 5.5V. When EXTVCC is between 3.25V and 5.5V the internal BIAS LDO is turned OFF and the IC is powered by the EXTVCC.
FB4	9	Selects the Output Voltage of the LDO. Connect a resistor-divider between OUT4, FB4, and PGND4.
AGND	10	Signal Ground for IC
IN	11	Supply Input. Connect IN to the output of the boost converter. Bypass IN with enough capacitors to supply the two out-of-phase buck converters.
INLDO	12	Input to the LDO. Use a local 4.7µF capacitor at the INLDO pin.
OUT4	13	Output of the LDO. Use a minimum of 4.7µF output capacitor to GND. The default output of the LDO is 5V with factory option of 3.3V.
PGND4	14	Power Ground Pin for LDO
PGOOD1	15	Open-Drain Power-Good Output for Buck Controller One. PGOOD1 is low if OUT1 is more than 92 % (typ) below the normal regulation point. PGOOD1 asserts low during soft-start and in shutdown. PGOOD1 becomes high impedance when OUT1 is in regulation. To obtain a logic signal, pull up PGOOD1 with an external resistor connected to BIAS.
PGOOD2	16	Open-Drain Power-Good Output for Buck Controller Two. PGOOD2 is low if OUT2 is more than 92% (typ) below the normal regulation point. PGOOD2 asserts low during soft-start and in shutdown. PGOOD2 becomes high impedance when OUT2 is in regulation. To obtain a logic signal, pull up PGOOD2 with an external resistor connected to BIAS.
COMP3	17	Boost Controller Error-Amplifier Output. Connect an RC network to COMP3 to compensate boost converter.

Pin Description (continued)

NAME	LOCATION	DESCRIPTION
FB3	18	Boost Converter Feedback Input. Connect FB3 to the center tap of a resistive divider between the boost regulator output and TERM to adjust the output voltage. FB3 regulates to 1.005V (typ). See the *Setting the Output Voltage in Boost Converter* section.
CS3P	19	Positive Current-Sense Input for Boost Controller. Connect CS3P to the positive terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (OUT_ and CS_)* and *Current-Sense Measurement* sections.
CS3N	20	Negative Current-Sense Input for Boost Controller. Connect CS3N to the negative terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (OUT_ and CS_)* and *Current-Sense Measurement* sections.
TERM	21	Ground Switch. TERM opens when the boost controller is disabled. Use TERM to terminate the boost feedback-divider.
BST3	22	Boost Flying Capacitor Connection for High-Side Gate Voltage of Boost Controller. Connect a high-voltage diode between BIAS and BST3. Connect a ceramic capacitor between BST3 and LX3. See the *High-Side Gate-Driver Supply (BST_)* section.
DH3	23	High-Side Gate-Driver Output for Boost Controller. DH3 output voltage swings from VLX3 to VBST3.
LX3	24	Inductor Connection for Boost Controller. Connect LX3 to the switched side of the inductor. LX3 serves as the lower supply rail for the DH3 high-side gate driver.
DL3	25	Boost Controller n-Channel MOSFET LS Gate-Driver Output
PGND3	26	Power Ground for Boost Controller. All high-current paths for the preboost controller should terminate to this ground.
BSTON	27	Open-Drain Output for Boost Controller. Indicates that the boost controller is ON or enabled.
FSYNC	28	External Clock-Synchronization Input. Synchronization to the controller operating-frequency ratio is 1. See the *Switching Frequency/External Synchronization* section. If FSYNC is used to transition from skip mode to PSM mode in steady state, ensure there is at least 50µA (including the resistor-divider current on $V_{OUT1,2}$) of load current if V_{BIAS} - $V_{OUT1,2}$ is > 1.3V.
FOSC	29	Frequency-Setting Input. Connect a resistor to FOSC to set the switching frequency of the DC-DC converters.
COMP2	30	Buck Controller Two Error-Amplifier Output. Connect an RC network to COMP2 to compensate buck converter two.
FB2	31	Feedback Input for Controller Two. Connect FB2 to BIAS for the 3.3V fixed output or to a resistive divider between OUT2 and GND to adjust the output voltage between 1V and 10V. In adjustable mode, FB2 regulates to 1V (typ). See the *Setting the Output Voltage in Buck Converters* section.
N.C.	32, 37	No Connection
OUT2	33	Output Sense and Negative Current-Sense Input for Controller Two. When using the internal preset 3.3V feedback-divider (FB2 = BIAS), the controller uses OUT2 to sense the output voltage. Connect OUT2 to the negative terminal of the current-sense element. See the Current Limiting and Current Sense Inputs and Current Sense Measurement sections.
CS2	34	Positive Current-Sense Input for Controller Two. Connect CS2 to the positive terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (OUT_ and CS_)* and *Current-Sense Measurement* sections.

Pin Description (continued)

NAME	LOCATION	DESCRIPTION
PGND2	35	Power Ground for Controller Two
DL2	36	Low-Side Gate-Driver Output for Controller Two. DL2 output voltage swings from VPGND2 to VBIAS.
LX2	38	Inductor Connection for Controller Two. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
DH2	39	High-Side Gate-Driver Output for Controller Two. DH2 output voltage swings from V_{LX2} to V_{BST2}.
BST2	40	Boost Flying-Capacitor Connection for High-Side Gate Voltage of Controller Two. Connect a high-voltage diode between BIAS and BST2. Connect a ceramic capacitor between BST2 and LX2. See the *High-Side Gate-Driver Supply (BST_)* section.
SPS	41	Spread-Spectrum Pin. Pull high to turn-on spread spectrum and pull low to turn it OFF.
EN4	42	High-Voltage Tolerant, Active-High Digital-Enable Input for HV 200mA LDO. Driving EN4 high enables the HV 200mA LDO regulator. EN4 should not be driven by signal of greater than 5kHz frequency.
EN2	43	High-Voltage Tolerant, Active-High Digital-Enable Input for Controller Two. Driving EN2 high enables buck controller two.
EN1	44	High-Voltage Tolerant, Active-High Digital-Enable Input for Controller One. Driving EN1 high enables buck controller one.
EN3	45	EN3 is either active high or active low (see the *Selector Guide*) for more details. For the active-low version, the EN3 pin has a precision threshold-enabling hardware solution for ON/OFF control of the boost controller.
BST1	46	Boost Flying-Capacitor Connection for High-Side Gate Voltage of Controller One. Connect a high-voltage diode between BIAS and BST2. Connect a ceramic capacitor between BST1 and LX1. See the *High-Side Gate-Driver Supply (BST_)* section.
DH1	47	High-Side Gate-Driver Output for Controller Two. DH1 output voltage swings from V_{LX1} to V_{BST1}.
LX1	48	Inductor Connection for Controller One. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
—	EP	Exposed Pad. Connect EP to ground. Connecting EP to ground does not remove the requirement for proper ground connections to PGND1 and AGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX20030/MAX20031 ICs are automotive-rated quad-output switching power supplies. Each device integrates two synchronous step-down controllers, a synchronous step-up controller, and a programmable-output 200mA LDO. They can provide up to four independently controlled power rails as follows:

1) A preboost with adjustable output voltage
2) A buck controller with a fixed 5V output voltage, or an adjustable 1V to 10V output voltage
3) A buck controller with a fixed 3.3V output voltage, or an adjustable 1V to 10V output voltage
4) An LDO with a fixed 5V/3.3V output or an adjustable 1.5V to 10V output voltage

Buck 1, buck 2, the preboost, and the LDO are enabled and disabled by the EN1, EN2, EN3, and EN4 control inputs, respectively. These can be connected directly to car battery:

- EN1 and EN2 enable the respective buck controllers; connect EN1 and EN2 directly to V_{BAT} or to power-supply sequencing logic
- EN3 controls the boost controller
- EN4 controls the LDO

In standby mode, the total supply current is reduced to 17µA (typ). When all three controllers are disabled, the total current drawn is further reduced to 7µA.

Fixed 5V Linear Regulator (BIAS)

The internal circuitry of the ICs requires a 5V bias supply. An internal 5V linear regulator (BIAS) generates this bias supply. Bypass BIAS with a 6.8µF or greater ceramic capacitor to guarantee stability under the full-load condition.

The internal linear regulator can source up to 100mA (150mA under EXTVCC switchover; see the *EXTVCC Switchover* section). Use the following equation to estimate the internal current requirements for the ICs:

$$I_{BIAS} = I_{CC} + f_{SW} (QG_DH3 + QG_DL3 + QG_DH1 + QG_DL1 + QG_DH2 + QG_DL2) = 10mA \text{ to } 50mA \text{ (typ)}$$

Where I_{CC} is the internal supply current, 5mA (typ), f_{SW} is the switching frequency, and QG_ is the MOSFET's total gate charge (specification limits at V_{GS} = 5V). To minimize the internal power dissipation, bypass BIAS to an external 5V rail.

The BIAS node is in high impedance when all three controllers are disabled. If any current-leakage path to BIAS exists, a pulldown resistor from BIAS to AGND is recommended to keep BIAS under the maximum rating range.

EXTVCC Switchover

The internal linear regulator can be bypassed by connecting an external 3.25V to 5.5V supply, or the output of one of the buck converters to EXTVCC. BIAS internally switches to EXTVCC and the internal linear regulator turns off. This configuration has several advantages:

- Reduces the internal power dissipation of the ICs
- Improves low-load efficiency as the internal supply current is scaled down proportionally to the duty cycle

If V_{EXTVCC} drops below $V_{TH,EXTVCC}$ = 2.85V (min), the internal regulator enables and switches back to BIAS.

Undervoltage Lockout (UVLO)

The BIAS input undervoltage-lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its 2.6V (typ) UVLO falling threshold. Once the 5V bias supply (BIAS) rises above its UVLO rising threshold and EN1 and EN2 enable the buck controllers, the controllers start switching and the output voltages begin to ramp up using soft-start.

Buck Controllers

The ICs provide two buck controllers with synchronous rectification. The step-down controllers use a PWM, current-mode control scheme. External MOSFETs allow for optimized load-current design. Fixed-frequency operation with optimal interleaving minimizes input ripple current from the minimum to the maximum input voltages. Output-current sensing provides an accurate current limit with a sense resistor, or power dissipation can be reduced using lossless current sensing across the inductor.

Soft-Start

Once a buck controller is enabled by driving the corresponding EN_ high, the soft-start circuitry gradually ramps up the reference voltage during soft-start time (t_{SSTART} = 5ms (typ)) to reduce the input surge currents during startup. Before the device can begin the soft-start, the following conditions must be met:

- V_{BIAS} exceeds the 3.25V (max) undervoltage lockout threshold
- $V_{EN_}$ goes logic-high

Switching Frequency/External Synchronization

The MAX20030/MAX20031 ICs provide an internal oscillator, adjustable from 220kHz to 2.2MHz. High-frequency operation optimizes the application for the smallest component size, trading off efficiency to higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space. To set the switching frequency, connect a resistor (R_{FOSC}) from FOSC to AGND:

$$f_{SW} = \frac{25.5 + \sqrt{\frac{R_{FOSC}}{6}}}{R_{FOSC}}$$

See TOC in the *Typical Operating Characteristics* section to determine the relationship between switching frequency and R_{FOSC}.

The ICs can be synchronized to an external clock by connecting the external clock signal to FSYNC. A rising edge on FSYNC resets the internal clock. The FSYNC signal should have a 150ns (min) high pulse width.

Light-Load Efficiency Skip Mode (V_{FSYNC} = 0V)

Drive FSYNC low to enable skip mode. In skip mode, the ICs stop switching until the FB voltage drops below the reference voltage. Once the FB voltage has dropped below the reference voltage, the ICs begin switching until the inductor current reaches 30% of the maximum current defined by the inductor DCR or output shunt resistor.

Forced-PWM Mode (V_{FSYNC})

Driving FSYNC high prevents the devices from entering skip mode, by disabling the zero-crossing detection of the inductor current. This forces the low-side gate-driver waveform to constantly be the complement of the high-side gate-driver waveform, so the inductor current reverses at light loads and discharges the output capacitor. The benefit of forced-PWM mode is to keep the switching frequency constant under all load conditions; however, forced-frequency operation diverts a considerable amount of the output current to PGND, reducing the efficiency under light-load conditions.

Forced-PWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Maximum Duty-Cycle Operation

The ICs have a maximum duty cycle of 97% (min). The internal logic of the IC looks for approximately 10 consecutive high-side FET ON pulses and decides to turn-on the low-side FET for 150ns (typ) every 12µs. The input voltage at which the ICs enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the ICs enter dropout can be approximated as:

$$V_{OUT_} = [V_{OUT_} + (I_{OUT_} \times R_{ON_H})]/0.97$$

Note: The above equation does not take into account the efficiency and switching frequency, but is a good first-order approximation. Use the R_{ON_H} max number from the data sheet of the high-side MOSFET used.

Spread Spectrum

The ICs feature enhanced EMI performance. They perform ±6% dithering of the switching frequency to reduce peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent emission limits. All of this is controlled by a pin on the IC. When using an external clock source (i.e., driving the FSYNC input with an external clock), spread spectrum is disabled.

MOSFET Gate Drivers (DH_ and DL_)

The DH_ high-side n-channel MOSFET drivers are powered from capacitors at BST_, while the low-side drivers (DL_) are powered by the 5V linear regulator (BIAS). On each channel, a shoot-through protection circuit monitors the gate-to-source voltage of the external MOSFETs to prevent a MOSFET from turning on until the complementary switch is fully off. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the protection circuits to work properly. Follow the instructions listed to provide the necessary low-resistance and low-inductance path:

- Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver)

It may be necessary to decrease the slew rate for the gate drivers to reduce switching noise or to compensate for low-gate charge capacitors. For the low-side drivers, use 1nF to 5nF gate capacitors from DL_ to GND. For the high-side drivers, connect a small 5Ω to 1Ω resistor between BST_ and the bootstrap capacitor.

Note: Gate drivers must be protected during shutdown, at the absence of the supply voltage (V_{BIAS} = 0V) when the gate is pulled high either capacitively or by the leakage path on the PCB. Therefore, external gate pulldown resistors are needed, especially at DL3, to prevent making a direct path from V_{BAT} to GND.

High-Side Gate-Driver Supply (BST_)

The high-side MOSFET is turned on by closing an internal switch between BST_ and DH_ and transferring

the bootstrap capacitor's (at BST_) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX_ voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor.

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values (CBST_ in the *Typical Operating Circuit*) according to the following equation:

$$C_{BST_} = QG/\Delta V_{BST_}$$

where QG is the total gate charge of the high-side MOSFET and $\Delta V_{BST_}$ is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose $V_{BST_}$ such that the available gate-drive voltage is not significantly degraded (e.g., $\Delta V_{BST_}$ = 100mV to 300mV) when determining $C_{BST_}$. The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases.

Current Limiting and Current-Sense Inputs (OUT_ and CS_)

The current-limit circuit uses differential current-sense inputs (OUT_ and CS_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold ($V_{LIMIT1,2}$ = 80mV (typ)), the PWM controller turns off the high-side MOSFET. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half of the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle ($V_{OUT_}/V_{IN}$).

For the most accurate current sensing, use a current-sense shunt resistor (R_{SH}) between the inductor and the output capacitor. Connect CS_ to the inductor side of R_{SH} and OUT_ to the capacitor side. Dimension R_{SH} such that the maximum inductor current (I_L, MAX = I_{LOAD}, MAX + 1/2 $I_{RIPPLE, P-P}$) induces a voltage of $V_{LIMIT1,2}$ across R_{SH}, including all tolerances. For higher efficiency, the current can also be measured directly across the inductor. This method could cause up to 30% error over the entire temperature range and requires a filter network in the current-sense circuit. See the *Current-Sense Measurement* section.

Voltage Monitoring (PGOOD_)

The ICs include several power-monitoring signals to facilitate power-supply sequencing and supervision. PGOOD_ can be used to enable circuits that are supplied by the corresponding voltage rail, or to turn-on subsequent supplies.

Each PGOOD_ goes high (high impedance) when the corresponding regulator output voltage is in regulation. Each PGOOD_ goes low when the corresponding regulator output voltage drops below 92% (typ) or rises above 95% (typ) of its nominal regulated voltage. Connect a 10kΩ (typ) pullup resistor from PGOOD_ to the relevant logic rail to level-shift the signal. PGOOD_ asserts low during soft-start, soft-discharge, and when either buck converter is disabled (i.e., EN1 or EN2 is low).

Boost Controller

The ICs include a synchronous current-mode boost controller with adjustable output. This boost controller can be used independently, but is ideally suited for applications that need to stay fully functional during input voltage drop-outs, typical for automotive cold-crank or start-stop. The boost controller is designed to support a minimum input supply voltage of 2V after first power-up. The minimum off-time of the boost controller is 70ns (typ) and 110ns (max) for the MAX20030CATMA and MAX20031CATMD. If the off-time exceeds these values, then the output voltage adjusts itself to satisfy the minimum off time.

The preboost is turned on by bringing EN3 high.

EN3 can be used for power-supply sequencing and implementing a boost timeout to prevent overheating the components used for the boost converter.

Enabling the Boost Controller

The boost controller has three options on the EN3 pin. For the MAX20030, there is an internal comparator on the EN3 pin and for the boost to be enabled, the internal BIAS voltage of the IC needs to be high. For the MAX20030, EN3 can further be factory configured to be active high or active low. If configured as active high, it functions as a standard logic pin. If configured as active low, the boost controller is enabled as soon as EN3 drops below 0.95V (typ).

In a typical start-stop application, the boost controller is enabled after one of the buck controllers is already ON. But in cases where the boost controller is required to be turned ON at low battery, either EN1 or EN2 should be connected to EN3 (active-high version). Now when EN3 along with EN1 or EN2 goes high, the BIAS rises above UVLO and turns ON the boost controller.

For the MAX20031, EN3 is an active-high digital input that controls the turn-on or turn-off of the boost, independently of the buck controllers.

Increasing the Efficiency of the Boost Circuit (TERM Pin and Bypass MOSFET)

The ICs provide two features to improve the efficiency of the boost circuit when it is not active:

- TERM provides a switch to GND for the FB3 voltage-divider. This switch opens during standby and shutdown modes to reduce the quiescent current by 240µA, assuming that resistors used in the voltage-divider network are 100kΩ.
- The preboost synchronous high-side FET automatically turns 100% ON when either of the buck controllers is not operating in standby mode. This is determined by monitoring the number of consecutive LX_ pulses. If six consecutive LX_ pulses are seen at either buck controller's LX_ node, the boost synchronous MOSFET turns ON 100%. This high-side FET of the boost controller turns ON irrespective of EN3 state. To prevent negative inductor current, the boost controller should be enabled before battery voltage drops below V_{OUT3}. Once the boost controller is enabled, the zero-crossing detection becomes active and prevents any negative current.

Current Limit in Boost Controller

A current-sense resistor ($R_{CS_}$), connected to CS3P and CS3N, sets the current limit of the boost converter. The CS_ input has a voltage trip level ($V_{CS_}$) of 50mV (typ). The low 50mV current-limit threshold reduces the power dissipation in the current-sense resistor. Use a current-sense filter to reduce capacitive coupling during turn-on. See the *Shunt Resistor Selection in Boost Converter* section.

Thermal-Overload, Overcurrent, Overvoltage, and Undervoltage Behavior

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the ICs. When the junction temperature exceeds +170°C, an internal thermal sensor shuts down the ICs, allowing them to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 20°C.

Overcurrent Protection

If the inductor current on the ICs exceeds the maximum current limit programmed at CS_ and OUT_, the respective driver turns off. In an overcurrent mode, this results in shorter and shorter high-side pulses. A hard short results in a minimum on-time pulse every clock cycle. Choose the components so they can withstand the short-circuit current if required.

Overvoltage Protection

The ICs limit the output voltage of the buck converters by turning off the high-side gate driver at approximately 108% of the regulated output voltage. The output voltage needs to come back in regulation before the high-side gate driver starts switching again.

Design Procedure

Effective Input Voltage Range in Buck Converters

Although the ICs can operate from input supplies up to 36V (42V transients) and regulate down to 1V, the minimum voltage conversion ratio ($V_{OUT_}/V_{IN}$) might be limited by the minimum controllable on-time. For proper fixed-frequency PWM operation and optimal efficiency, buck 1 and buck 2 should operate in continuous conduction during normal operating conditions. For continuous conduction, set the voltage conversion ratio as follows:

$$\frac{V_{OUT_}}{V_{IN}} > t_{ON(MIN)} \times f_{SW}$$

where $t_{ON(MIN)}$ is 50ns (typ) and f_{SW} is the switching frequency in hertz. If the desired voltage conversion does not meet the above condition, pulse skipping occurs to decrease the effective duty cycle. Decrease the switching frequency if constant switching frequency is required. The same is true for the maximum voltage-conversion ratio.

The maximum voltage-conversion ratio is limited by the maximum duty cycle of 97% and the maximum allowed output voltage of 10V:

$$\frac{V_{OUT_}}{V_{IN} - V_{DROP}} < 0.97$$

where $V_{DROP} = I_{OUT_} (R_{ON,HS} + R_{DCR})$ is the sum of the parasitic voltage drops in the high-side path, and f_{SW} is the programmed switching frequency. During low-drop operation, the ICs reduce f_{SW} to ~80kHz. In practice, the above condition should be met with adequate margin for good load-transient response.

Setting the Output Voltage in Buck Converters

Connect FB1 and FB2 to BIAS to enable the fixed buck controller output voltages (5V and 3.3V) set by a preset internal resistive voltage-divider connected between the feedback (FB_) and AGND. To externally adjust the output voltage between 1V and 10V, connect a resistive divider from the output (OUT_) to FB_ to AGND (see the *Typical Operating Circuit*. Calculate R_{FB1} and R_{FB2} with the following equation:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT_}}{V_{FB_}}\right) - 1\right]$$

where $V_{FB_}$ = 1V (typ) (see the *Electrical Characteristics* table). DC output accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold, $V_{FB_}$ = 1V (typ). When the inductor conducts continuously, the ICs regulate the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output-ripple voltage.

In discontinuous-conduction mode (skip or STDBY active and $I_{OUT_} < I_{LOAD(SKIP)}$), the ICs regulate the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold.

Inductor Selection in Buck Converters

Three key inductor parameters must be specified for operation with the ICs: Inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To determine the optimum inductance, knowing the typical duty cycle (D) is important:

$$D = \frac{V_{OUT_}}{V_{IN}} \text{ or } D = \frac{V_{OUT_}}{V_{IN} - I_{OUT_}(R_{DS(ON)} + R_{DCR})}$$

if the R_{DCR} of the inductor and $R_{DS(ON)}$ of the MOSFET are available with $V_{IN} = (V_{BAT} - V_{DIODE})$. All values should be typical to optimize the design for normal operation.

Inductance

The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, efficiency, and transient response requirements:

- Lower inductor values increase LIR, which minimizes size and cost and improves transient response at the cost of reduced efficiency due to higher peak currents.
- Higher inductance values decrease LIR, which increases efficiency by reducing the RMS current at the cost of requiring larger output capacitors to meet load-transient specifications.

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L[\mu H] = \frac{(V_{IN} - V_{OUT_}) \times D}{f_{SW}[MHz] \times I_{OUT_} \times LIR}$$

where V_{IN}, $V_{OUT_}$, and $I_{OUT_}$ are typical values (so that efficiency is optimum for typical conditions).

Peak Inductor Current

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current, in addition to half of the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is calculated as:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT_}(V_{IN} - V_{OUT_})}{V_{IN} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in mA, L is in µH, and f_{SW} is in kHz.

Once the peak current and the inductance are known, the inductor can be selected. The saturation current should be larger than I_{PEAK} or at least in a range where the inductance does not degrade significantly. The MOSFETs are required to handle the same range of current without dissipating too much power.

MOSFET Selection in Buck Converters

Each step-down controller drives two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include the items in the following sections.

Threshold Voltage

All four n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V. If the internal regulator is bypassed (e.g., V_{EXTVCC} = 3.3V), then the n-channel MOSFETs should be chosen to have guaranteed on-resistance at that gate-to-source voltage.

Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)

All MOSFETs must be chosen with an appropriate V_{DS} rating to handle all V_{IN} voltage conditions.

Current Capability

The n-channel MOSFETs must deliver the average current to the load and the peak current during switching. Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V or $V_{GS} = V_{EXTVCC}$ when the internal linear regulator is bypassed. For load currents below ~3A, dual MOSFETs in a single package can be an economical solution. To reduce switching noise for smaller MOSFETs, use a series resistor in the BST_ path and additional gate capacitance. Contact the factory for guidance using gate resistors.

Bootstrap Diode Selection in Buck Converters

The bootstrap diode provides the charging path to charge the bootstrap capacitor, CBST_. The Schottky diode or silicon diode with lower forward voltage and fast recovery time is preferred to improve the high-side gate driver loss. Another parameter to consider when choosing the bootstrap diode is its reverse leakage-current specification, especially at high temperature. High reverse leakage current can fully discharge the bootstrap capacitor at high temperature to cause high-side MOSFET turn-on issues. The bootstrap diode with lower reverse leakage-current specification must be chosen to avoid any unexpected high-side MOSFET off.

Current-Sense Measurement

For the best current-sense accuracy and overcurrent protection, use a ±1% tolerance current-sense resistor between the inductor and output, as shown in Figure 1A. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. Use low-inductance current-sense resistors for accurate measurement.

Alternatively, high-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 1B) with an equivalent time constant:

$$R_{CSHL} = \left(\frac{R2}{R1 + R2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}} \left(\frac{1}{R1} + \frac{1}{R2}\right)$$

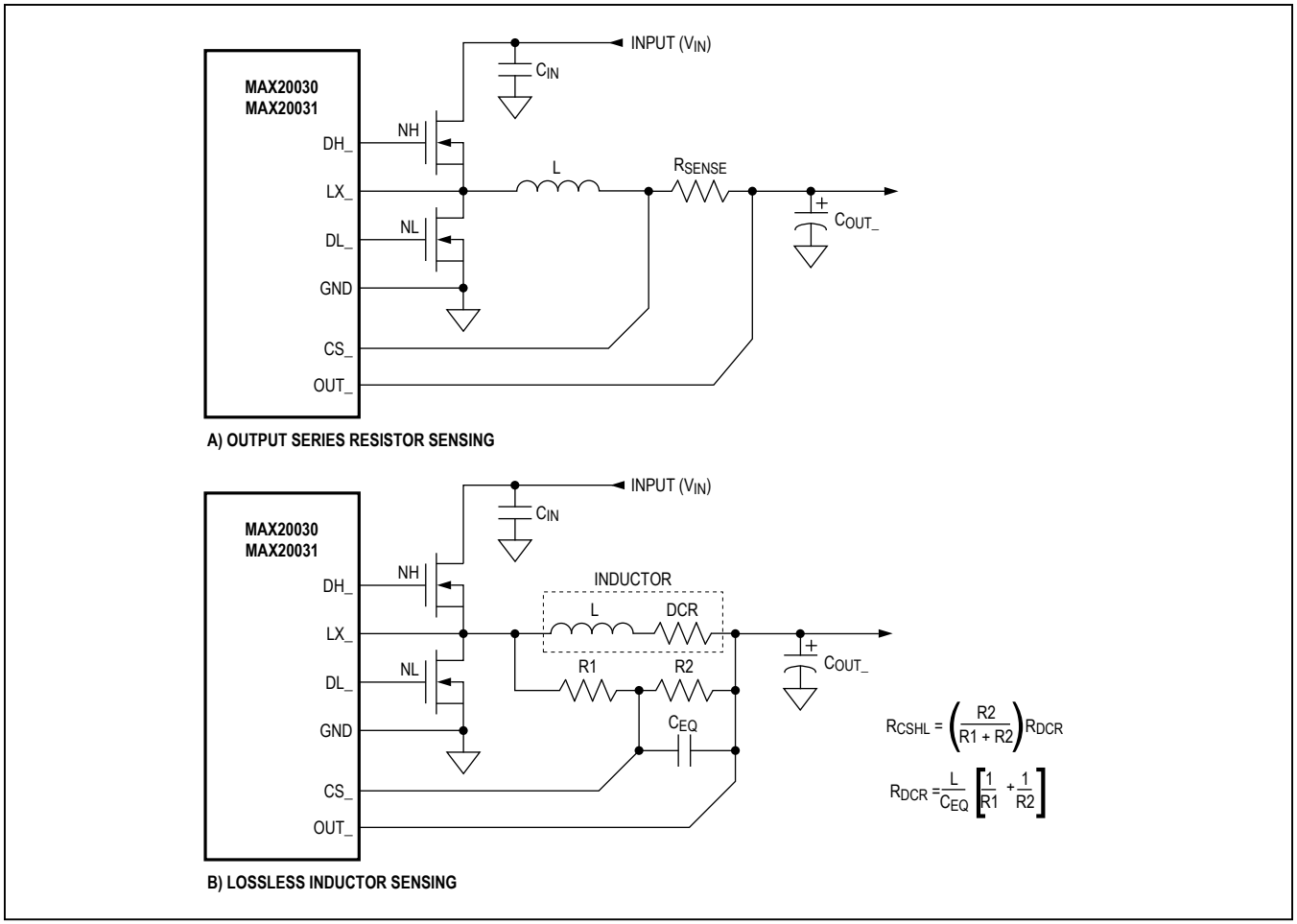


Figure 1. Current-Sense Configurations

where R_{CSHL} is the required current-sense resistor and R_{DCR} is the inductor's series DC resistor. Use the inductance and R_{DCR} values provided by the inductor manufacturer. If DCR sense is the preferred current-sense method, then the recommended resistor value for R1 (Figure 1B) is ≤ 1kΩ.

Carefully observe the PCB layout guidelines to ensure the noise and DC errors do not corrupt the differential current-sense signals seen by CS_ and OUT_. Place the sense resistor close to the ICs with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

Input Capacitor in Buck Converters

The discontinuous input current of the buck converter causes large input ripple currents and therefore the input capacitor must be carefully chosen to withstand the input ripple current and the input voltage ripple kept within design requirements. The 180-degree ripple phase operation increases the frequency of the input capacitor ripple current to twice the individual converter switching frequency. When using ripple phasing, the worst-case input capacitor ripple current is when the converter with the highest output current is on.

The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} that peaks at the end of an on-cycle. Calculate the input capacitance and ESR required for a specific ripple using the following equation:

$$ESR[\Omega] = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN}[\mu F] = \frac{I_{LOAD(MAX)} \times \left(\frac{V_{OUT_}}{V_{IN}}\right)}{\left(\Delta V_Q \times f_{SW}\right)}$$

where:

$$\Delta I_{P-P} = \frac{\left(V_{IN} - V_{OUT_}\right) \times V_{OUT_}}{V_{IN} \times f_{SW} \times L}$$

$I_{LOAD(MAX)}$ is the maximum output current in A, ΔI_{P-P} is the peak-to-peak inductor current in A, f_{SW} is the switching frequency in MHz, and L is the inductor value in µH.

The internal 5V linear regulator (BIAS) includes an output UVLO with hysteresis to avoid unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. At lower input voltage, additional input capacitance helps avoid possible undershoot below the undervoltage-lockout threshold during transient loading.

Output Capacitor in Buck Converters

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. The capacitor is usually selected by ESR and the voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the *Current Limit in Boost Controller* section). However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

The total voltage sag (V_{SAG}) can be calculated as follows:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2}{2C_{OUT_}\left(\left(V_{IN} \times D_{MAX}\right) - V_{OUT_}\right)} + \frac{\Delta I_{LOAD(MAX)}\left(t - \Delta t\right)}{C_{OUT_}}$$

The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT_}V_{OUT_}}$$

ESR Considerations

The output-filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. When using high-capacitance low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple. So the output capacitor's size depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

In standby mode, the inductor current becomes discontinuous, with peak currents set by the idle-mode current-sense threshold ($V_{CS_,SKIP}$ = 26mV (typ)).

Compensation-Components Calculation (Buck Controllers)

The ICs use a current-mode-control scheme for boost controller. A single series resistor (R_C) and capacitor (C_C) is all that is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 2). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to AGND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier, as shown in Figure 2. The power modulator has a DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor ($C_{OUT_}$), and its ESR. The loop response is set by the following equations:

$$GAIN_{MOD(dc)} = g_{mc} \times R_{LOAD}$$

where R_{LOAD} = $V_{OUT_}/I_{LOUT(MAX)}$ in Ω and g_{mc} = 1/(A_{V_CS} x R_{DC}) in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 11V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

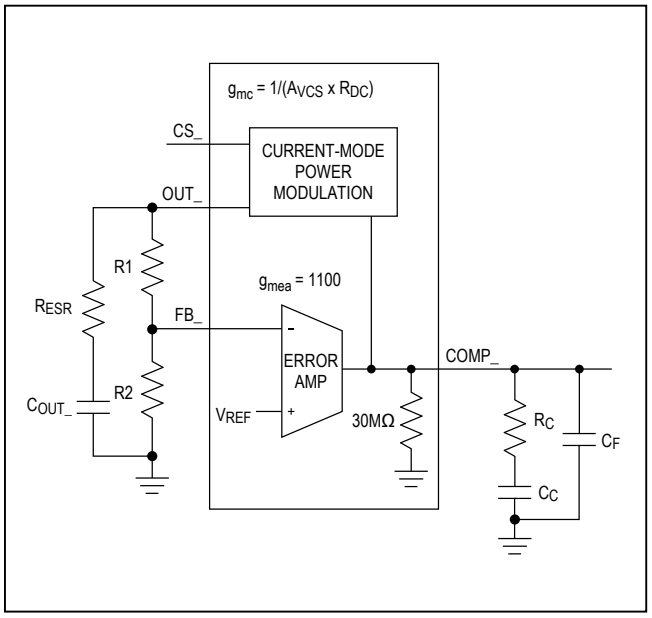


Figure 2. Compensation Network

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT_} \times R_{LOAD}}$$

The unity gain frequency of the power stage is set by C_{OUT} and g_{mc}:

$$f_{UGAINpMOD} = \frac{g_{mc}}{2\pi \times C_{OUT_}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT_}}$$

When $C_{OUT_}$ is composed of “n” identical capacitors in parallel, the resulting $C_{OUT_}$ = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}$/n. Note that the capacitor zero for a parallel combination of similar capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB}$ = $V_{FB}/V_{OUT_}$, where $V_{FB_}$ is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)}$ = $g_{m,EA}$ x $R_{OUT,EA}$, where $g_{m,EA}$ is the error-amplifier transconductance, which is 1100µS (max), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 30MΩ (typ) (see the *Electrical Characteristics* table.)

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB). Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/15th of the switching frequency and much higher than the power-modulator pole (f_{pMOD}). Select a value for f_C in the range of:

$$f_{pMOD} << f_C \le \frac{f_{SW}}{15}$$

At the crossover frequency, the total loop gain must be equal to 1. So:

$$GAIN_{MOD(fC)} \times \frac{V_{FB_}}{V_{OUT_}} \times GAIN_{EA(fC)} = 1$$

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{fp_{MODE}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB_}}{V_{OUT_}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT_}}{g_{m,EA} \times V_{FB_} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to AGND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

Boost Converter Design Procedure

Setting the Output Voltage in Boost Converter

Adjust the boost converter output voltage by connecting a resistive divider from the output of the boost converter to FBBST to TERM (Figure 3) and R_{B2} (FB3 to TERM resistor). Calculate R_{B1} ($V_{OUT_(BOOST)}$ to FBBST resistor) using the following equation:

$$R_{B1} = R_{B2}\left[\left(\frac{V_{OUT_(BOOST)}}{V_{FB3}}\right) - 1\right]$$

where V_{FB3} = 1.005V (typ) (see the *Electrical Characteristics* table).

Inductor Selection in Boost Converter

Duty cycle and frequency are important to calculate the inductor size, as the inductor current ramps up during the on-time of the switch and ramps down during its off-time. A higher switching frequency generally improves transient response and reduces component size; however, if the boost components are to be used as the input filter components during nonboost operation, a low frequency is advantageous.

The duty-cycle range of the boost converter depends on the effective input-to-output voltage ratio. In the following calculations, the duty cycle refers to the on-time of the boost MOSFET:

$$D_{MAX} = \frac{V_{OUT_(MAX)} - V_{BAT(MIN)}}{V_{OUT_(MAX)}}$$

or including the voltage drops across the inductor, MOSFET ($V_{ON,FET}$), and the boost diode (V_D):

$$D_{MAX} = \frac{V_{OUT_(MAX)} - V_{BAT(MIN)} + V_D + (I_{OUT_} \times R_{DC})}{V_{OUT_(MAX)}}$$

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L[\mu H] = \frac{V_{IN} \times D}{f_{SW}[MHz] \times LIR}$$

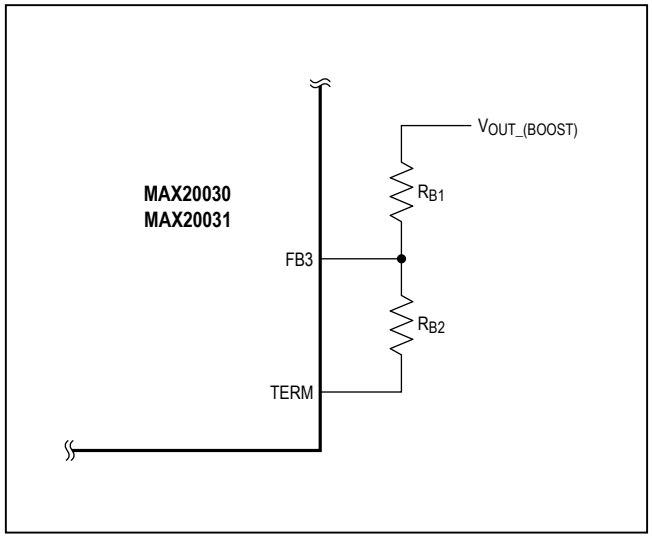


Figure 3. Boost Converter Adjustable Output Voltage

where:

$D = (V_{OUT_} - V_{IN})/V_{OUT_}$
V_{IN} = Typical input voltage
$V_{OUT_}$ = Typical output voltage

$LIR = 0.3 \times I_{OUT}/1 - D$

Select the inductor with a saturation current rating higher than the peak switch current limit of the converter:

$$I_{L,PEAK} > I_{L,MAX} + \frac{\Delta I_{L,RIP,MAX}}{2}$$

Running a boost converter in continuous-conduction mode introduces a right-half plane zero into the transfer function. To avoid the effect of this right-half plane zero, the crossover frequency for the control loop should be ≤ 1/3 x f_{RHP_ZERO}. If faster bandwidth is required, a smaller inductor and higher switching frequency is recommended.

MOSFET Selection in Boost Converter

The key selection parameters to choose the n-channel MOSFET used in the boost converter are as follows.

Threshold Voltage

The boost n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V.

Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)

The MOSFET must be chosen with an appropriate V_{DS} rating to handle all V_{IN} voltage conditions.

Current Capability

The n-channel MOSFET must deliver the input current ($I_{IN(MAX)}$):

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \frac{D_{MAX}}{1 - D_{MAX}}$$

Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V.

Bootstrap Diode Selection in Boost Converter

The bootstrap diode charges the bootstrap capacitor when the boost low-side MOSFET is turned on. The Schottky diode or silicon diode with lower forward voltage and fast recovery time is preferred to improve the high-side gate driver loss. Also, its reverse leakage-current specification is another important parameter to consider. The reverse leakage current increases exponentially at higher temperature. The bootstrap diode with significant reverse leakage current provides a current path from BST3 to BIAS. This current path charges the BIAS capacitor with diode reverse leakage current, and causes the BIAS voltage to rise above its maximum rating. The bootstrap diode with lower reverse leakage-current specification must be chosen to avoid BIAS voltage drift-up issue.

Input Capacitor Selection in Boost Converter

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and the maximum ESR using the following equations:

$$C_{BAT} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where:

$$\Delta I_L = \frac{(V_{BAT} - V_{DS}) \times D}{L \times f_{SW}}$$

V_{DS} is the total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR. ΔI_L is the peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) are equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source, especially at high output-to-input differential.

Output Capacitor Selection in Boost Converter

In a boost converter, the output capacitor supplies the load current when the boost MOSFET is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT_}}$$

$$C_{OUT_} = \frac{I_{OUT_} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

$I_{OUT_}$ is the load current in A, f_{SW} is in MHz, $C_{OUT_}$ is in µF, ΔV_Q is the portion of the ripple due to the capacitor discharge, and ΔV_{ESR} is the contribution due to the ESR

of the capacitor. D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

Shunt Resistor Selection in Boost Converter

The current-sense resistor ($R_{CS_}$), connected between the battery and the inductor, sets the current limit. The CS_ input has a voltage trip level ($V_{CS_}$) of 50mV (typ).

Set the current-limit threshold high enough to accommodate the component variations. Use the following equation to calculate the value of $R_{CS_}$:

$$R_{CS_} = \frac{V_{CS_}}{I_{IN(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

$$I_{IN(MAX)} = I_{LOAD(MAX)} / (1 - D_{MAX})$$

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (DL3) quickly terminates the on-cycle.

Compensation-Components Calculation (Boost Controller)

The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier, as shown in Figure 4. The power modulator has a DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor ($C_{OUT_}$), and its ESR. The loop response is set by the following equations:

$$G_{MOD} = g_{MC} \times R_{LOAD} \times \left(\frac{1-D}{2}\right) \times \left(\frac{1 + j\frac{f}{f_{zMOD}}}{1 + j\frac{f}{f_{pMOD}}}\right) \times \left(1 - j\frac{f}{f_{Rph_zMOD}}\right)$$

where R_{LOAD} = $V_{OUT_}/I_{LOUT(MAX)}$ in Ω and g_{mc} = $1/(A_{V_CS_} \times R_{DC})$ in S. $A_{V_CS_}$ is the voltage gain of the current-sense amplifier and is typically 12V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{\pi \times R_{LOAD} \times C_{OUT_}}$$

The output capacitor and its ESR also introduce a zero at: The right-half plane zero is at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT_}}$$

$$f_{Rph_zMOD} = \frac{R_{LOAD}}{2\pi \times L} \times (1-D) \times (1-D)$$

When $C_{OUT_}$ is composed of “n” identical capacitors in parallel, the resulting $C_{OUT_}$ = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of similar capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB_}$ = $V_{FB_}/V_{OUT_}$, where $V_{FB_}$ is 1.005V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)}$ = $g_{m,EA}$ x $R_{OUT,EA}$, where $g_{m,EA}$ is the error-amplifier transconductance, which is 400µS (max), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 10MΩ (typ) (see the *Electrical Characteristics* table.)

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB). Thus:

$$f_{pEA} = \frac{1}{2\pi \times (R_{OUT,EA} + R_C) \times C_C}$$

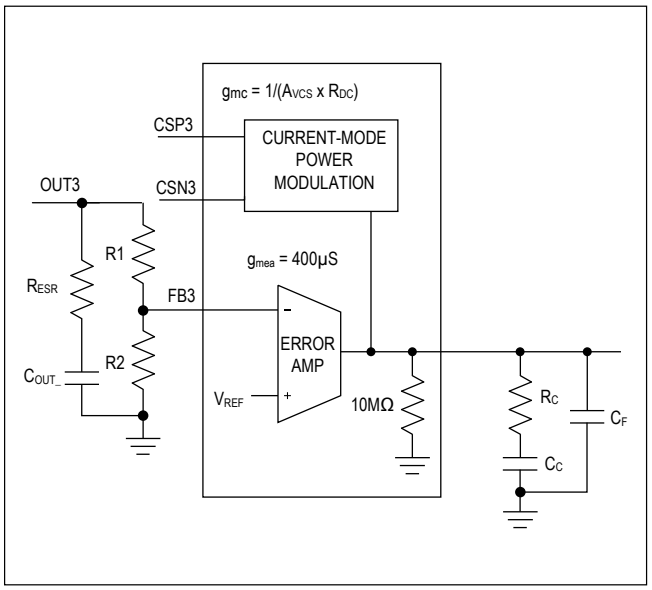


Figure 4. BOOST Controller Compensation Network

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{p2EA} = \frac{1}{2\pi \times R_C \times C_F}$$

The loop gain crossover frequency (f_C) should be ≤ 1/3 of right-half plane zero frequency.

$$f_C \le \frac{f_{Rph_zMOD}}{3}$$

At the crossover frequency, the total loop gain must be equal to 1. So:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB_}}{V_{OUT_}} \times GAIN_{EA(f_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB_}}{V_{OUT_}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT_}}{g_{m,EA} \times V_{FB_} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP3 to AGND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

LDO

The ICs include a low-quiescent current, high-voltage stand-alone linear regulator and are ideal for use in automotive and battery-operated systems. The ICs operate from an input voltage of +3.5V to +36V, deliver up to 200mA of load current, and consume only 25µA of quiescent current at no load. The input is +42V tolerant and is designed to operate under load-dump conditions. This LDO can be user configured as either a fixed output voltage (+3.3V or +5V) or an adjustable output voltage using an external resistive divider. The LDO includes an enable input short-circuit protection and thermal shutdown.

Output-Voltage Options for the LDO

The MAX20030/MAX20031 LDO comes factory trimmed with three different options: fixed 5V output voltage, fixed 3.3V output voltage, or externally adjustable output voltage. In case of externally adjustable output voltage, a resistor-divider should be placed from OUT4 to FB4 to GND.

Enable

The LDO comes with a dedicated enable input (EN4). EN4 is an active-high, logic-level enable input that turns the device on or off. Drive EN4 high to turn the device on. The EN4 pin can also be connected directly to the battery for always-on applications.

Output Short-Circuit Current Limit

The LDO features a 400mA current limit. The output can be shorted to GND continuously without damage to the device. During a short circuit, the power dissipated across the pass transistor can quickly heat the device. When the die temperature reaches +175°C, the ICs turn off the pass transistor and automatically restart after the die temperature has cooled by +25°C.

Output Capacitor Selection and Regulator Stability

For stable operation over the full temperature range, with fixed 3.3V and 5.0V output voltages, use a low-ESR 4.7µF capacitor. Use larger output capacitor values such as 22µF to reduce noise, improve load-transient response and power-supply rejection. Some ceramic dielectrics exhibit large capacitance and ESR variations with temperature. To improve power-supply rejection and transient response, use a capacitor larger than the minimum 1µF capacitor between IN and GND.

Available Output Current

The LDO provides up to 200mA of continuous output current. The input voltage range extends to 36V. Package power dissipation limits the amount of output current available for a given input/output voltage and ambient temperature.

Applications Information

PCB Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (see Figure 5). If possible, mount all power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full load efficiency by 1% or more.
- Minimize current-sensing errors by connecting CS_ and OUT_. Use kelvin sensing directly across the current-sense resistor ($R_{SENSE_}$).
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (FB_, CS_, and OUT_).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side FET, C_{IN}, $C_{OUT_}$, and Schottky). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite NL_ and NH_ to keep LX_, GND, DH_, and the DL_ gate drive lines short and wide. To keep the driver impedance low and for proper adaptive dead-time sensing, the DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST_ diode and capacitor and LDO bypass capacitor, BIAS) together as close as possible to the controller IC. Be aware that gate currents of up to 1A flow from the bootstrap capacitor to BST_, from DH_ to the gate of the external HS switch, and from the LX_ pin to the inductor. Up to 100mA of current flow from the BIAS capacitor through the bootstrap diode to the bootstrap capacitor. Dimension those traces accordingly.
4) Make the DC-DC controller ground connections as shown in Figure 5. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly under the IC.
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close as possible to the load.

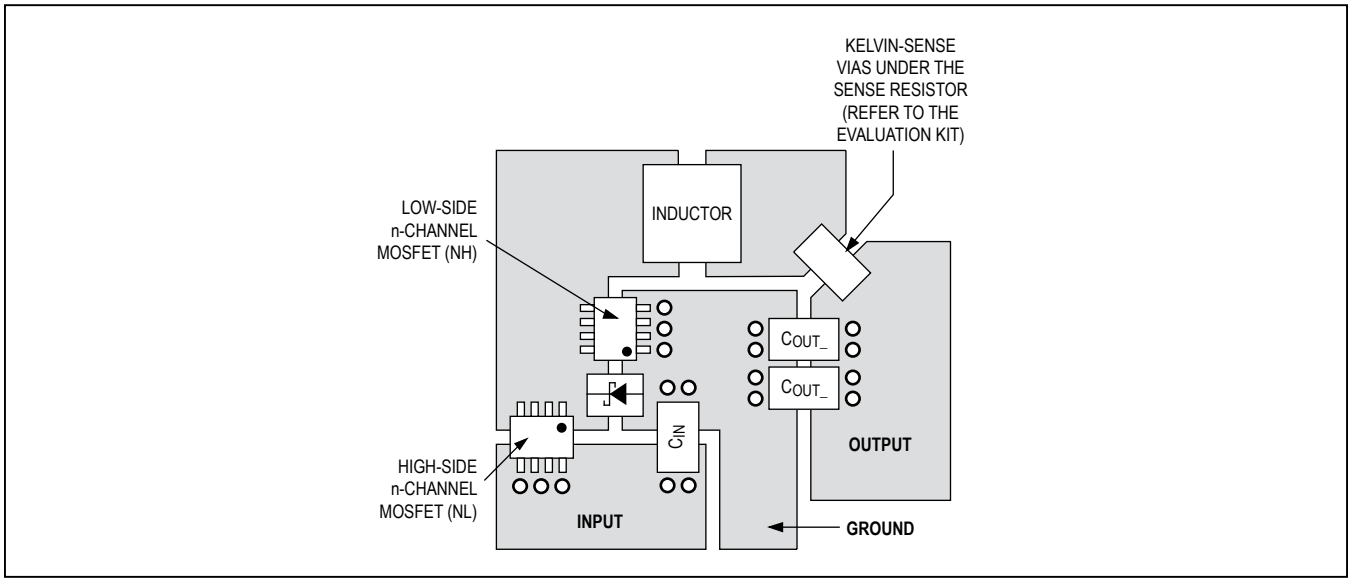
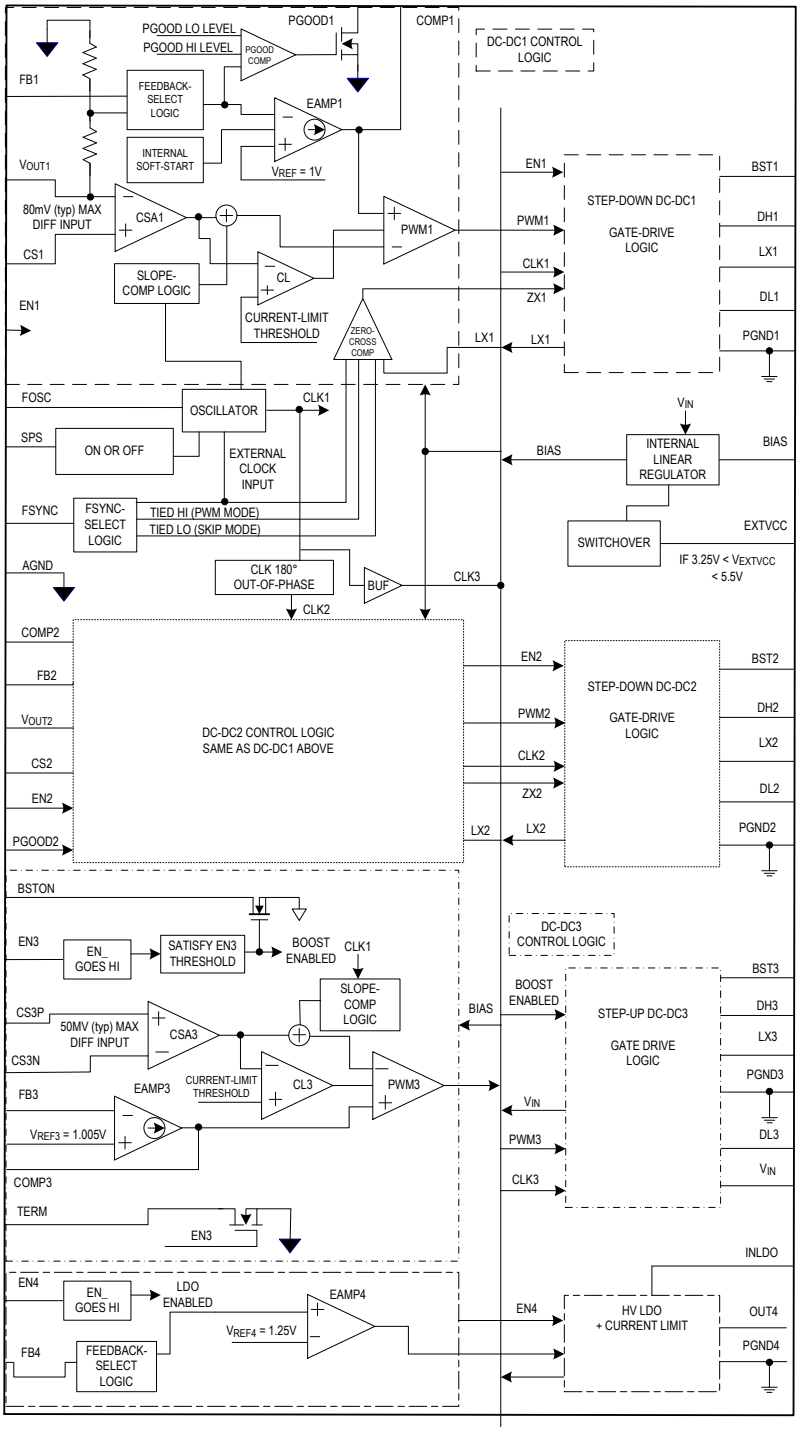


Figure 5. Layout Example

Block Diagram



Selector Guide

PART	EN3 (BOOST)	LDO	BOOST ZERO CROSS	BOOST UVLO	BIAS VOLTAGE NEEDS TO BE > UVLO BEFORE EN3 ACTIVATES THE BOOST	LDO UVLO
MAX20030BATMA/V+	Active High	5V (fixed), 200mA	Enabled	Enabled	Yes	Disabled
MAX20030BATMB/V+	Active High	Adjustable, 200mA	Enabled	Enabled	Yes	
MAX20030BATMC/V+	Active High	3.3V (fixed), 200mA	Enabled	Enabled	Yes	
MAX20030BATMD/V+	Active Low	5V (fixed), 200mA	Enabled	Enabled	Yes	
MAX20030BATME/V+*	Active Low	Adjustable, 200mA	Enabled	Enabled	Yes	
MAX20030BATMF/V+*	Active Low	3.3V (fixed), 200mA	Enabled	Enabled	Yes	
MAX20030BATMG/V+*	Active High	Adjustable, 200mA	Enabled	Disabled	Yes	
MAX20030BATMH/V+*	Active High	3.3V (fixed), 200mA	Disabled	Disabled	Yes	
MAX20030BATMI/V+	Active High	Adjustable, 300mA	Enabled	Enabled	Yes	
MAX20030CATMA/V+	Active High	5V (fixed), 200mA	Enabled	Enabled	Yes	Enabled
MAX20031BATMA/V+	Active High	5V (fixed), 200mA	Enabled	Enabled	No, EN3 turns on BIAS voltage and activates BOOST	Disabled
MAX20031BATMB/V+	Active High	Adjustable, 200mA	Enabled	Enabled	No, EN3 turns on BIAS voltage and activates BOOST	
MAX20031BATMC/V+	Active High	3.3V (fixed), 200mA	Enabled	Enabled	No, EN3 turns on BIAS voltage and activates BOOST	
MAX20031BATMD/V+	Active High	3.3V (fixed), 200mA	Disabled	Enabled	No, EN3 turns on BIAS voltage and activates BOOST	
MAX20031BATME/V+	Active High	Adjustable, 200mA	Disabled	Enabled	No, EN3 turns on BIAS voltage and activates BOOST	
MAX20031BATMF/V+	Active High	Adjustable, 300mA	Enabled	Enabled	No, EN3 turns on BIAS voltage and activates BOOST	
MAX20031CATMD/V+	Active High	3.3V (fixed), 200mA	Disabled	Enabled	No, EN3 turns on BIAS voltage and activates BOOST	Enabled

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*

Ordering Information

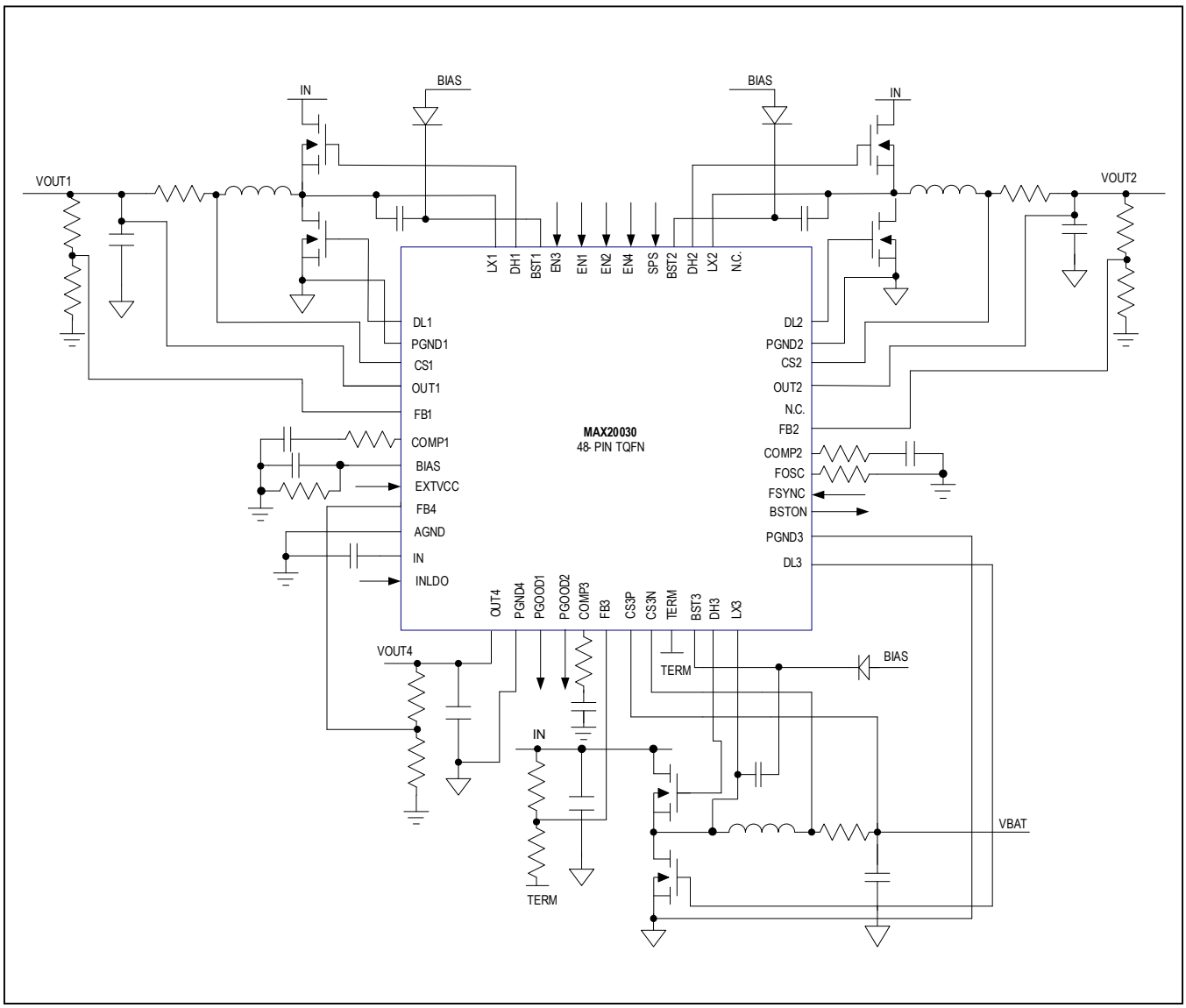
PART	TEMP RANGE	PIN-PACKAGE
MAX20030_TM_/V+	-40°C to +125°C	48 TQFN-EP†
MAX20031_TM_/V+	-40°C to +125°C	48 TQFN-EP†

/V denotes an automotive qualified part.
/VY denotes an automotive qualified part with side wettable package.
+Denotes a lead(Pb)-free/RoHS-compliant package.
†Exposed pad.

Chip Information

PROCESS: BiCMOS

Typical Operating Circuit



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/16	Initial release	—
1	7/16	Removed future product designation from MAX20030ATMC/V+ in *Selector Guide*	29
2	11/16	Various changes throughout the data sheet	1, 4, 6, 13–17
3	12/16	Removed future product designation from MAX20031ATMC/V+ in *Selector Guide*	29
4	4/17	Changed LX1,2 leakage current max in *Electrical Characteristics* from 1 to 10	3
5	5/17	Changed juntion-to-ambient thermal resistance in *Package Thermal Characteristics* and updated FSYNC (pin 28) in *Pin Description* sections, and removed future product designations from MAX20030ATMB/V+ and MAX20031ATMB/V+ in *Selector Guide*	2, 13, 29
6	7/17	Added ESD Results in *Absolute Maximum Ratings* section	2
7	8/17	Updated CDM in *Absolute Maximum Ratings* section	2
8	9/17	Updated ESD Results in *Absolute Maximum Ratings* section and Supply Current in *Electrical Characteristics table;* added three new future product variants in the *Selector Guide* (MAX20030BATMA/V+, MAX20031BATMA/V+, MAX20031BATMD/V+)	2, 29
8.1		Corrected typo	29
9	10/17	Updated *Block Diagram* and *Selector Guide*	28, 29
9.1		Corrected LDO values (swapped in error) for the MAX20030BATMC/V+ and MAX20030BATMD/V+ in the *Selector Guide*	29
10	1/18	Added LDO Current Limit conditions, TOC 16a, updated *Selector Guide* header, removed future product asterisks (MAX20030BATMA/V+, MAX20030BATMC/V, MAX20031BATMA/V+, MAX20031BATMB/V, MAX20031BATMC/V+, MAX20030BATM_V+, MAX20031BATM_V+)	6, 9, 29, 30
11	2/18	Updated the Feedback Voltage, Dropout Voltage, LDO Current Limit, and Load Regulation at Feedback in the *Electrical Characteristics* table	5, 6
12	5/18	Updated TOC7, TOC16a, *Switching Frequency/External Synchronization* and *Compensation-Components Calculation (Buck Controllers)* sections, the *Block Diagram*, and removed the future product designation from MAX20030BATMB/V+	7, 9, 16, 22, 28–29
13	11/18	Updated *Benefits and Features, Package Information, Electrical Characteristics,* and *Detailed Description* sections; removed MAX20030ATMB/V+, MAX20030ATMC/V+, MAX20031ATMA/V+, MAX20031ATMB/V+ and MAX20031ATMC/V+, and added MAX20031BATME/V+ from the *Selector Guide*; removed MAX20031ATM_/V+, and added MAX20030ATMA/V+MAX20030BATM_/VY+ and MAX20031BATM_/VY+ to the *Ordering Information* table	1–2, 5, 15, 29–30
14	3/19	Updated the *Electrical Characteristics* table and removed future product designation from MAX20031BATME/V+ in the *Selector Guide* table	6, 29
15	8/19	Updated *Design Procedure*, *Selector Guide*, and *Ordering Information* sections	15, 17, 19, 24, 29
16	9/19	Updated *Selector Guide* to add MAX20031BATMF/V+*	29
17	10/19	Updated the *Electrical Characteristics* table and *Typical Operating Circuit*	6, 31
18	1/20	Updated *Electrical Characteristics* table and *Selector Guide* table	4, 29
19	4/20	Updated *Selector Guide* table to remove future-product notation from MAX20031BATMF/V+	29
20	5/21	Updated *Detailed Description* section	17
21	7/21	Updated *Selector Guide*	29

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