MAX263/MAX264/ MAX267/MAX268

Pin Programmable Universal and Bandpass Filters

General Description

The MAX263/264 and MAX267/268 CMOS switched-capacitor active filters are designed for precision filtering applications. Center frequency, Q, and operating mode are all selected via pin-strapped inputs. The MAX263/264 uses no external components for a variety of bandpass, lowpass, highpass, notch and allpass filters. The MAX267/268 is dedicated to bandpass applications and includes an uncommitted op-amp. Two second-order filter sections are included in both devices.

An input clock and a 5-bit programming input precisely set the filter center/corner frequency. Q is also programmed from 0.5 to 64. Separate clock inputs for each filter half operate with either an external clock or a crystal.

The MAX263 and 267 operate with center frequencies up to 57kHz while the MAX264 and 268 extend the f_0 range to 140kHz by employing lower f_{CLK}/f_0 ratios. The MAX263/264 is supplied in 28 pin wide DIP and small outline packages while the MAX267/268 is supplied in 24 pin narrow DIP and wide SO packages. All devices are available in commercial, extended, and military temperature ranges.

Applications

Sonar and Avionics Instruments

Anti-Aliasing Filters

Digital Signal Processing

Vibration and Audio Analysis

Matched Tracking Filters

Features

- 32-Step Center Frequency Control
- 128-Step Q Control
- Independent Q and f_0 Programming
- Guaranteed Clock to f_0 Ratio—1% (A grade)
- 75kHz f_0 Range (MAX264/268)
- Single +5V and ±5V Operation

Ordering Information

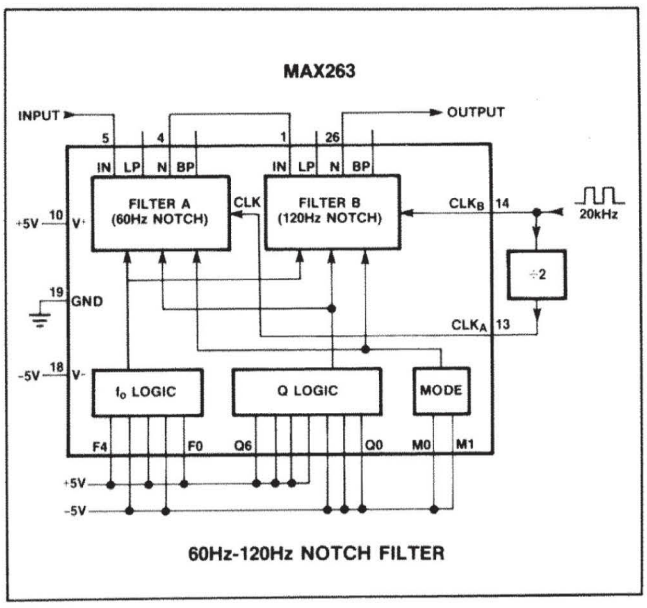
PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX263ACPI	0°C to +70°C	Plastic DIP	1%
MAX263BCPI	0°C to +70°C	Plastic DIP	2%
MAX263AEPI	-40°C to +85°C	Plastic DIP	1%
MAX263BEPI	-40°C to +85°C	Plastic DIP	2%
MAX263ACWI	0°C to +70°C	Wide SO	1%
MAX263BCWI	0°C to +70°C	Wide SO	2%
MAX263AMJI	-55°C to +125°C	CERDIP	1%
MAX263BMJI	-55°C to +125°C	CERDIP	2%
MAX264ACPI	0°C to +70°C	Plastic DIP	1%
MAX264BCPI	0°C to +70°C	Plastic DIP	2%

(Ordering Information continued at end of data sheet.)

* *MAX263/264 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" wide SO (Small Outline).*

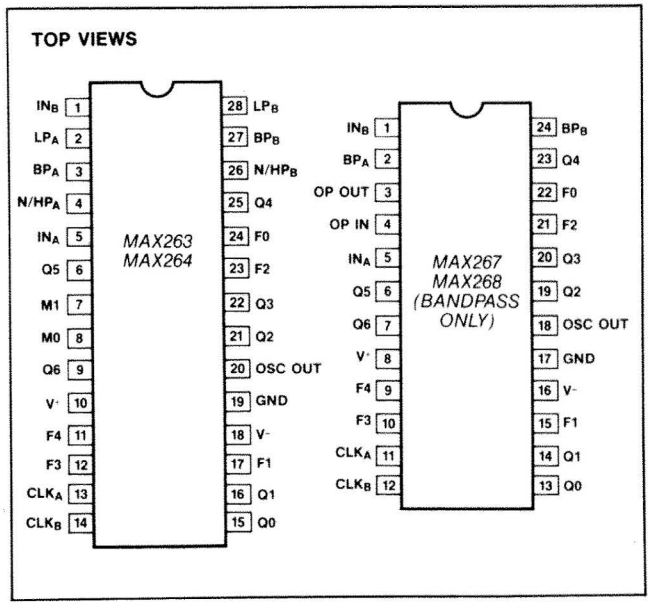
MAX267/268 packages are 24-pin 0.3" narrow DIP and 24-pin 0.3" wide SO (Small Outline).

Typical Application



60Hz-120Hz NOTCH FILTER

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-0597; Rev 4; 12/07

Pin Programmable Universal and Bandpass Filters

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage, any pin ..... V^-–0.3V to V^++0.3V
Input Current, any pin ..... ±50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above 70°C) ... 660mW
  CERDIP (derate 12.5mW/°C above 70°C) 1000mW
  Wide SO (derate 11.8mW/°C above 70°C) 944mW

Operating Temperature
  MAX26XXCXX ..... 0°C to +70°C
  MAX26XXEXX ..... -40°C to +85°C
  MAX26XXMXX ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V, 1.5MHz, f_{CLK}/f_0 = 197.92 for MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, "1" = V^+ and "0" = V^- on F and Q inputs, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				See Table 1		
Maximum Clock Frequency				See Table 1		
f_{CLK}/f_0 Ratio Error (Note 1)	T_A = T_{MIN} to T_{MAX}	MAX26XA MAX26XB		±0.2 ±0.2	±1.0 ±2.0	%
f_0 Temperature Coefficient				-5		ppm/°C
Q Accuracy (deviation from ideal continuous filter) (Note 2)	T_A =T_{MIN} to T_{MAX} Q = 0.5 to 8 Q = 0.5 to 8 Q = 16 to 32 Q = 16 to 32 Q = 64 Q = 64	 MAX26XA MAX26XB MAX26XA MAX26XB MAX26XA MAX26XB		 ±1 ±1 ±2 ±2 ±4 ±4	 ±6 ±10 ±10 ±15 ±20 ±25	%
Q Temperature Coefficient				±20		ppm/°C
DC Lowpass Gain Accuracy		MAX263/4		±0.1	±0.5	dB
Gain Temperature Coefficient	Lowpass (at D.C.) Bandpass (at f_0)			-5 +20		ppm/°C
Output Offset Voltage (Note 3)	T_A = T_{MIN} to T_{MAX}, Q = 4 Mode 1 BP Output	 MAX263/67A MAX263/67B MAX264/68A MAX264/68B		 ±0.05 ±0.05 ±0.05 ±0.05	 ±0.20 ±0.30 ±0.20 ±0.30	V
	Mode 1 LP,N Outputs	MAX263A MAX263B MAX264A MAX264B		±0.40 ±0.80 ±0.40 ±0.80	±1.00 ±1.60 ±1.20 ±1.60	
	Mode 3 BP, HP Outputs	MAX263A MAX263B MAX264A MAX264B		±0.10 ±0.10 ±0.10 ±0.10	±0.20 ±0.30 ±0.20 ±0.30	
	Mode 3 LP Output	MAX263A MAX263B MAX264A MAX264B		±0.50 ±0.90 ±0.50 ±0.90	±1.10 ±1.60 ±1.30 ±1.60	
Offset Voltage Temperature Coefficient	f_{CLK}/f_0 = 100.53, Q = 4 T_A = T_{MIN} to T_{MAX}			±0.75		mV/°C
Clock Feedthrough				±4		mV
Crosstalk				-70		dB
Wideband Noise (Note 4)	Q = 1, 2nd-Order, LP/BP 4th-Order LP 4th-Order BP			See Typ. Oper. Char. 90 100		μV_{RMS}

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V, 1.5MHz, f_{CLK}/f_0 = 197.92 for MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, "1" = V^+ and "0" = V^- on F and Q inputs, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Harmonic Distortion at f_0	Q = 4, V_{IN} = $1.5V_{PP}$			-67		dB
Supply Voltage Range	T_A = T_{MIN} to T_{MAX}		±2.37	±5	±6.3	V
Power Supply Current (Note 5)	T_A = T_{MIN} to T_{MAX}	MAX263/67 MAX264/68		14 14	20 20	mA
Shutdown Supply Current (Note 5)	Q0-Q6 = all 0			2.5		mA
f_0, Q Programming Inputs	T_A = T_{MIN} to T_{MAX}, F0-F4, Q0-Q6 High Threshold Low Threshold		V^+-0.5		 V^-+0.5	V
Clock Inputs	T_A = T_{MIN} to T_{MAX}, CLK_A, CLK_B High Threshold Low Threshold		2.4		 0.8	V
Input Leakage Current	T_A = T_{MIN} to T_{MAX} CLK_B = V^+ or V^- CLK_A = V^+ or V^- M0, M1, F0-F4, Q0-Q6 = V^+-0.5V or V^-+0.5V M0, M1, F0-F4, Q0-Q6 = V^+ or V^-			 6 20 5	10 60 200 	µA
INTERNAL AMPLIFIERS						
Output Signal Swing	T_A = T_{MIN} to T_{MAX}, 10kΩ load			±4.75		V
Output Short Circuit Current	Source Sink			50 2		mA
Power Supply Rejection Ratio	0Hz to 10kHz			-70		dB
Gain Bandwidth Product				2.5		MHz
Slew Rate				6		V/µs

ELECTRICAL CHARACTERISTICS (for V± = ±2.5V ±5%)

(V^+ = +2.37V, V^- = -2.37V, CLK_A = CLK_B = ±2.5V 1MHz f_{CLK}/f_0 = 197.92 for the MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				(Note 6)		
Maximum Clock Frequency				(Note 6)		
f_{CLK}/f_0 Ratio Error (Notes 1, 7)	Q = 8	MAX26XA MAX26XB		±0.1 ±0.1	±1 ±2	%
Q Accuracy (deviation from ideal continuous filter) (Notes 2, 7)	Q = 8 f_{CLK}/f_0 = 197.92 f_{CLK}/f_0 = 138.23	 MAX263/67A MAX263/67B MAX264/68A MAX264/68B		 ±2 ±2 ±2 ±2	 ±6 ±10 ±6 ±10	%
Output Signal Swing	All Outputs			±2		V
Power Supply Current				7		mA
Shutdown Current				0.45		mA

Note 1: f_{CLK}/f_0 accuracy is tested at 197.92 on the MAX263/67, and at 138.23 on the MAX264/68.

Note 2: Q accuracy tested at Q = 8, 32, and 64. Q of 32 and 64 tested at 1/2 stated clock frequency.

Note 3: The Offset Voltage is specified for the entire filter. Offset is virtually independent of Q and f_{CLK}/f_0 ratio setting. The test clock frequency for Mode 3 is 750kHz.

Note 4: Output noise is measured with an RC output smoothing filter at 4 x f_0 to remove clock feedthrough.

Note 5: TTL logic levels are: HIGH = 2.4V, LOW = 0.8V. Power supply current is typically 4mA higher with TTL clock input levels.

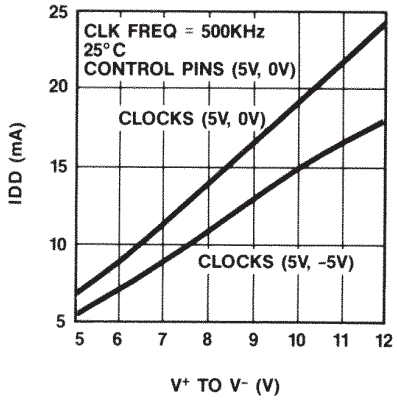
Note 6: At ±2.5V supplies, the f_0 range and maximum clock frequency are typically 75% of values listed in Table 1.

Note 7: f_{CLK}/f_0 and Q accuracy are a function of the accuracy of internal capacitor ratios. No increase in error is expected at ±2.5V as compared to ±5V, however these parameters are only tested to the extent indicated by the MIN or MAX limits.

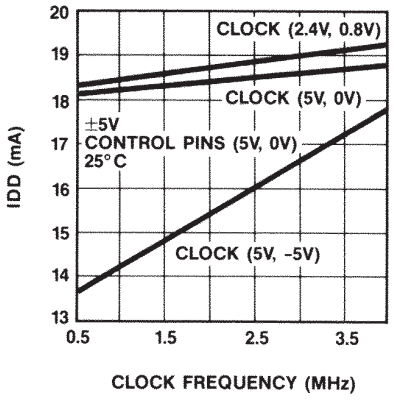
Pin Programmable Universal and Bandpass Filters

Typical Operating Characteristics

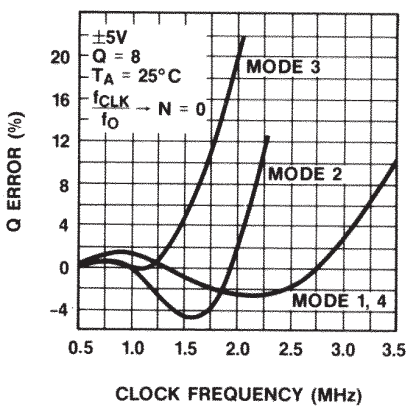
IDD vs POWER SUPPLY VOLTAGE



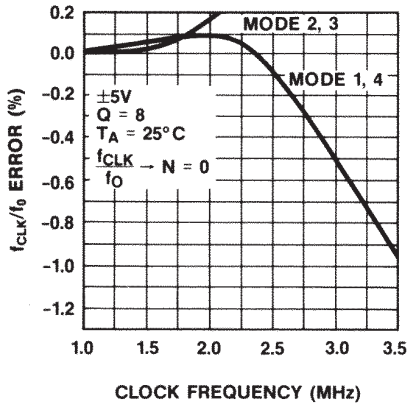
IDD vs CLOCK FREQUENCY



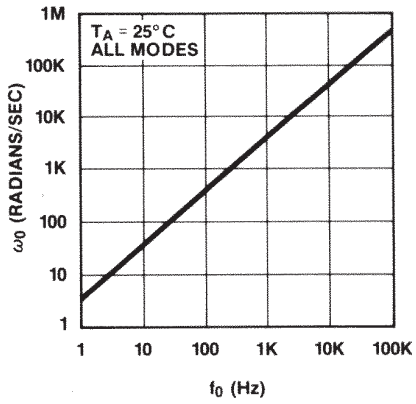
Q vs CLOCK FREQUENCY



f_{CLK}/f_0 vs CLOCK FREQUENCY



ω_0 vs f_0



Wideband RMS Noise (db ref. to $2.47V_{RMS}$, $7V_{p-p}$), ±5V Operation

Mode	Q = 1			Q = 8			Q = 64		
	LP	BP	HP/AP/N	LP	BP	HP/AP/N	LP	BP	HP/AP/N
1	-84	-90	-84	-80	-82	-85	-72	-73	-85
2	-88	-90	-88	-84	-82	-84	-77	-73	-76
3	-84	-90	-88	-80	-82	-82	-73	-73	-74
4	-83	-89	-84	-79	-81	-85	-71	-73	-85

Notes:
1. f_{CLK} = 1MHz
2. f_{CLK}/f_0 ratio programmed at N = 31 (see Table 2)
3. Clock feedthrough is removed with an RC lowpass at $4f_0$, i.e. R = 3.9kΩ, C = 2000pF for MAX263.

Noise Spectral Distribution (MAX263/67, f_{CLK} = 1 MHz, dB ref. to $2.47V_{RMS}$, $7V_{p-p}$)

Measurement Bandwidth	Q=1	Q=8	Q=64
Wideband	-84	-80	-72
3kHz	-87	-87	-86
C Message Weighted	-93	-93	-93

Pin Description

MAX263 MAX264 PIN #	MAX267 MAX268 PIN #	NAME	FUNCTION
10	8	V^+	Positive supply voltage
18	16	V^-	Negative supply voltage
19	17	GND	Analog Ground. Connect to the system ground for dual supply operation or mid-supply for single supply operation. GND should be well bypassed in single supply applications.
13	11	CLK_A	Input to the oscillator and clock input to section A. This clock is internally divided by 2.
14	12	CLK_B	Clock input to filter B. This clock is internally divided by 2.
20	18	OSC OUT	Connects to crystal for self clocked operation
5, 1	5, 1	IN_A, IN_B	Filter inputs
3, 27	2, 24	BP_A, BP_B	Bandpass outputs
2, 28		LP_A, LP_B	Lowpass outputs (MAX263/264 only)
4, 26		HP_A, HP_B	Highpass/Notch/Allpass outputs (MAX263/264 only)
8, 7		M0, M1	Mode select inputs (MAX267/268 are fixed in Mode 1)
24, 17, 23 12, 11	22, 15, 21 10, 9	F0-F4	Clock/center frequency ratio (f_{CLK}/f_0) programming inputs
15, 16, 21 22, 25, 6 9	13, 14, 19 20, 23, 6 7	Q0-Q6	Q programming inputs
	4	OP IN	Inverting input of uncommitted op-amp on MAX267/268 only. Noninverting input is internally connected to ground.
	3	OP OUT	Output of uncommitted op-amp on MAX267/268 only.

Pin Programmable Universal and Bandpass Filters

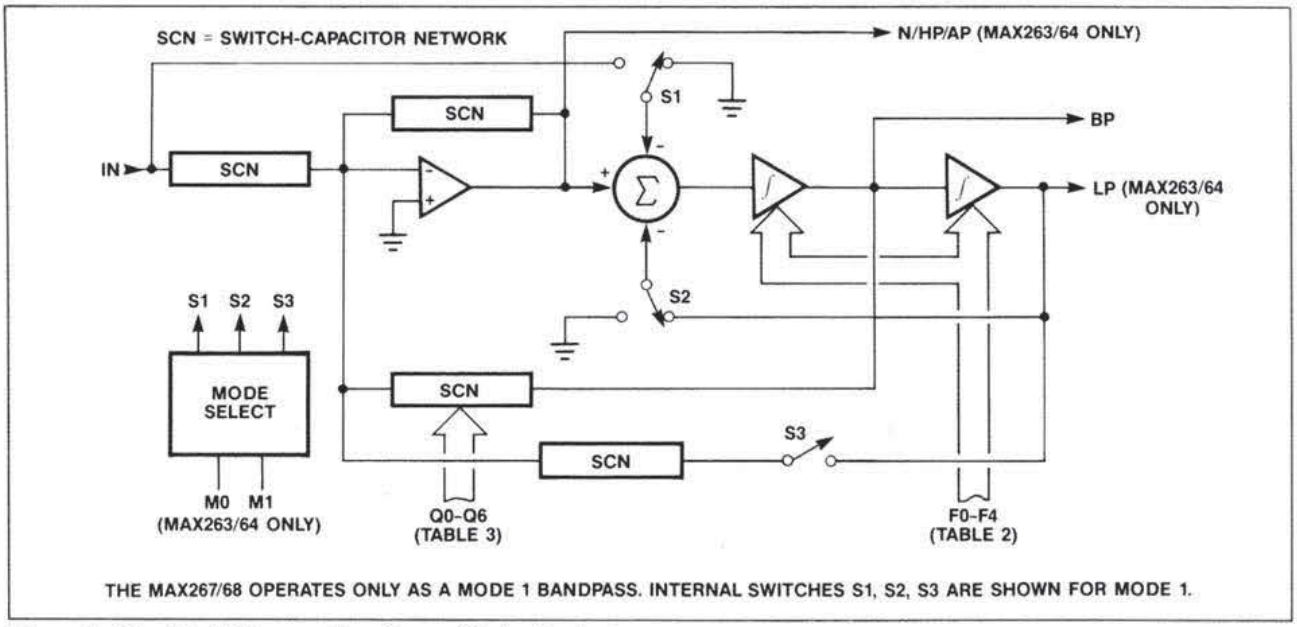


Figure 1. Filter Block Diagram (One Second-Order Section)

Introduction

Each MAX26X device contains two second-order filters. In Figure 1, a block diagram of the state variable topology employed in one filter section shows how on-chip switched capacitor networks provide adjustable feedback to control f_0 and Q. Shared programming inputs require that both halves of the filter be set for the same f_{CLK}/f_0 ratio and Q. In the MAX263 and MAX264 universal filters, switches S1-S3 are controlled by inputs M0 and M1 to set the filter operating mode. The MAX267/68 bandpass filter operates only in Mode 1.

The MAX264/68 uses a lower range of sampling (f_{CLK}/f_0) ratios than the MAX263/67 to allow higher signal bandwidths and a wider programming range. The reduced f_{CLK}/f_0 ratios result in somewhat more deviation from ideal continuous filter parameters than with the MAX263/67, however these differences can be compensated using Figure 17 (See "Applications Hints") or Maxim's filter design software.

The second-order sections in the MAX263/64/67/68 are identical and may be used as matched dual tracking filters, or can be cascaded to form higher-order filters. They can also be combined with external resistors and amplifiers for multiple feedback all-pole bandpass filters.

In all MAX26X series filters, the internal sample rate is one half the input clock rate (CLK_A or CLK_B) due to an internal division by two. All clock related data, tables, and other discussions in this data sheet refer to the frequency at the CLK_A or CLK_B input, i.e. twice the internal sample rate, unless specifically stated otherwise.

Detailed Description

f_0 and Q Programming

Figure 2 shows a block diagram of a complete filter. Each 2nd-order filter section has its own clock input, however, package pin limitations require that f_0, Q, and Mode control be shared by both sections. The actual center frequency is a function of the filter's clock rate, 5-bit f_0 control word (see Table 2), and operating Mode.

For some filter designs, the MAX263/64/67/68 may require separate clocks for each second-order section since separate programming inputs are not provided. Such designs may be implemented with different clock inputs, or, in the case of bandpass filters, by using multiple feedback and one clock (see "Description of Filter Functions"). When implementing two or more matched filters, however, the programming restrictions are easily overcome and one clock can still be used as demonstrated by the design example in Figure 21. Another alternative is to use the MAX260/261/262 microprocessor programmed filters or the MAX265/266 resistor programmed filters which allow independent programming of each filter section. Refer to the device data sheets for further details on those products.

Table 1. Typical Clock and Center Frequency Limits (MAX267/268 are operated in Mode 1 only.)

PART	Q	MODE	f_{CLK}	f_0
MAX263/ 267	1	1	40Hz-4.0MHz	0.4Hz-40kHz
	1	2	40Hz-4.0MHz	0.5Hz-57kHz
	1	3	40Hz-4.0MHz	0.4Hz-40kHz
	1	4	40Hz-4.0MHz	0.4Hz-40kHz
	8	1	40Hz-2.7MHz	0.4Hz-27kHz
	8	2	40Hz-2.1MHz	0.5Hz-30kHz
	8	3	40Hz-1.7MHz	0.4Hz-17kHz
	8	4	40Hz-2.7MHz	0.4Hz-27kHz
	64	1	40Hz-2.0MHz	0.4Hz-20kHz
	90	2	40Hz-1.2MHz	0.4Hz-18kHz
	64	3	40Hz-1.2MHz	0.4Hz-12kHz
	64	4	40Hz-2.0MHz	0.4Hz-20kHz

PART	Q	MODE	f_{CLK}	f_0
MAX264/ 268	1	1	40Hz-4.0MHz	1.0Hz-100kHz
	1	2	40Hz-4.0MHz	1.4Hz-140kHz
	1	3	40Hz-4.0MHz	1.0Hz-100kHz
	1	4	40Hz-4.0MHz	1.0Hz-100kHz
	8	1	40Hz-2.5MHz	1.0Hz-60kHz
	8	2	40Hz-1.4MHz	1.4Hz-50kHz
	8	3	40Hz-1.4MHz	1.0Hz-35kHz
	8	4	40Hz-2.5MHz	1.0Hz-60kHz
	64	1	40Hz-1.5MHz	1.0Hz-37kHz
	90	2	40Hz-0.9MHz	1.4Hz-32kHz
	64	3	40Hz-0.9MHz	1.0Hz-22kHz
	64	4	40Hz-1.5MHz	1.0Hz-37kHz

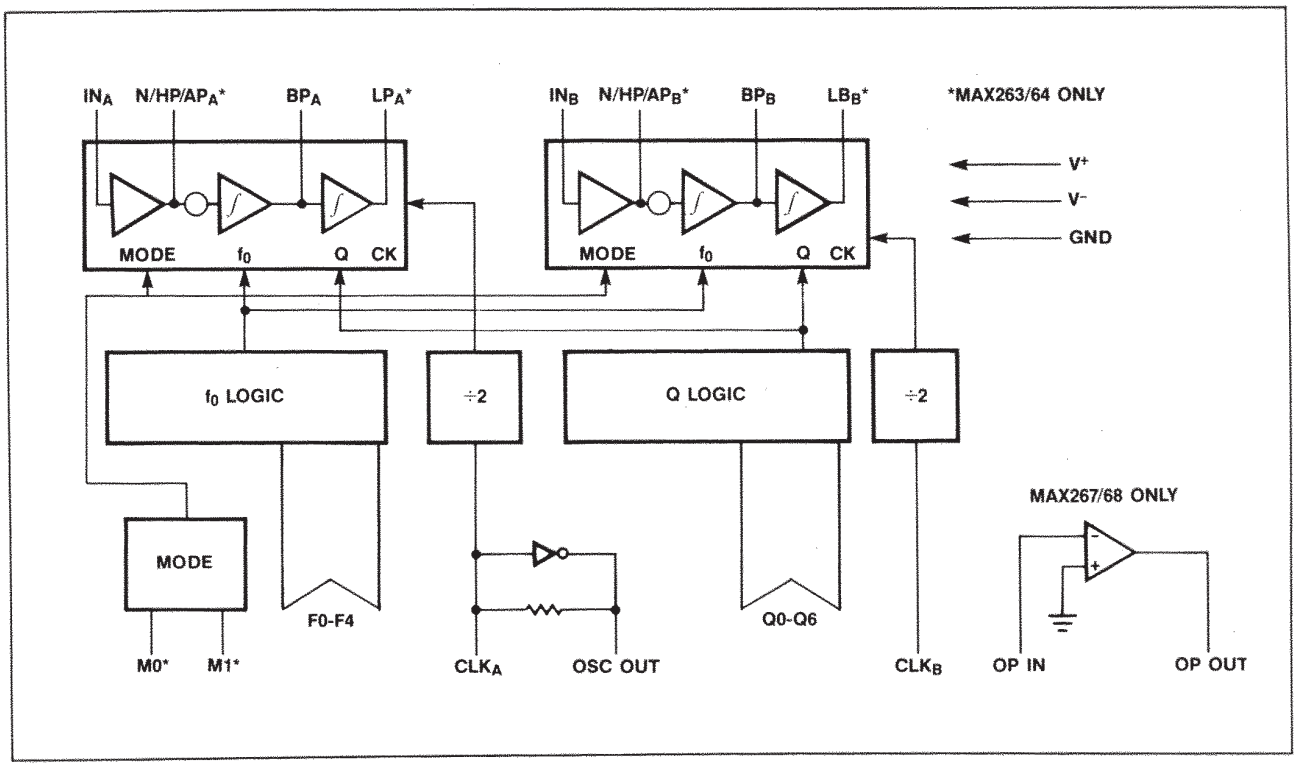


Figure 2. MAX263/264/267/268 Block Diagram

Table 2. f_{CLK}/f_0 Program Selection Table

f_{CLK}/f_0 RATIO				PROGRAM CODE					
MAX263/67		MAX264/68							
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F4	F3	F2	F1	F0
100.53	71.09	40.84	28.88	0	0	0	0	0	0
103.67	73.31	43.98	31.10	1	0	0	0	0	1
106.81	75.53	47.12	33.32	2	0	0	0	1	0
109.96	77.75	50.27	35.54	3	0	0	0	1	1
113.10	79.97	53.41	37.76	4	0	0	1	0	0
116.24	82.19	56.55	39.99	5	0	0	1	0	1
119.38	84.42	59.69	42.21	6	0	0	1	1	0
122.52	86.64	62.83	44.43	7	0	0	1	1	1
125.66	88.86	65.97	46.65	8	0	1	0	0	0
128.81	91.80	69.12	48.87	9	0	1	0	0	1
131.95	93.30	72.26	51.10	10	0	1	0	1	0
135.08	95.52	75.40	53.31	11	0	1	0	1	1
138.23	97.74	78.53	55.54	12	0	1	1	0	0
141.37	99.97	81.68	57.76	13	0	1	1	0	1
144.51	102.89	84.82	59.98	14	0	1	1	1	0
147.65	104.41	87.96	62.20	15	0	1	1	1	1
150.80	106.63	91.11	64.42	16	1	0	0	0	0
153.98	108.85	94.25	66.64	17	1	0	0	0	1
157.08	111.07	97.39	68.86	18	1	0	0	1	0
160.22	113.29	100.53	71.09	19	1	0	0	1	1
163.36	115.52	102.67	73.31	20	1	0	1	0	0
166.50	117.74	106.81	75.53	21	1	0	1	0	1
169.65	119.96	109.96	77.75	22	1	0	1	1	0
172.79	122.18	113.10	79.97	23	1	0	1	1	1
175.93	124.40	116.24	82.19	24	1	1	0	0	0
179.07	126.62	119.38	84.81	25	1	1	0	0	1
182.21	128.84	122.52	86.64	26	1	1	0	1	0
185.35	131.07	125.66	88.86	27	1	1	0	1	1
188.49	133.29	128.81	91.08	28	1	1	1	0	0
191.64	135.51	131.95	93.30	29	1	1	1	0	1
194.78	137.73	135.09	95.52	30	1	1	1	1	0
197.92	139.95	138.23	97.74	31	1	1	1	1	1

Notes: 1) For the MAX263/67, $f_{CLK}/f_0 = \pi(N+32)$ in Mode 1, 3, and 4, where N varies form 0 to 31.
2) For the MAX264/68, $f_{CLK}/f_0 = \pi(N+13)$ in Mode 1, 3, and 4, where N varies 0 to 31.
3) In Mode 2, all f_{CLK}/f_0 ratios are divided by $\sqrt{2}$.

Pin Programmable Universal and Bandpass Filters

Table 3. Q Program Selection Table (Continued on following page)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Note 4	Note 4	0	0	0	0	0	0	0	0
0.504	0.713	1	0	0	0	0	0	0	1
0.508	0.718	2	0	0	0	0	0	1	0
0.512	0.724	3	0	0	0	0	0	1	1
0.516	0.730	4	0	0	0	0	1	0	0
0.520	0.736	5	0	0	0	0	1	0	1
0.525	0.742	6	0	0	0	0	1	1	0
0.529	0.748	7	0	0	0	0	1	1	1
0.533	0.754	8	0	0	0	1	0	0	0
0.538	0.761	9	0	0	0	1	0	0	1
0.542	0.767	10	0	0	0	1	0	1	0
0.547	0.774	11	0	0	0	1	0	1	1
0.552	0.780	12	0	0	0	1	1	0	0
0.556	0.787	13	0	0	0	1	1	0	1
0.561	0.794	14	0	0	0	1	1	1	0
0.566	0.801	15	0	0	0	1	1	1	1
0.571	0.808	16	0	0	1	0	0	0	0
0.577	0.815	17	0	0	1	0	0	0	1
0.582	0.823	18	0	0	1	0	0	1	0
0.587	0.830	19	0	0	1	0	0	1	1
0.593	0.838	20	0	0	1	0	1	0	0
0.598	0.846	21	0	0	1	0	1	0	1
0.604	0.854	22	0	0	1	0	1	1	0
0.609	0.862	23	0	0	1	0	1	1	1
0.615	0.870	24	0	0	1	1	0	0	0
0.621	0.879	25	0	0	1	1	0	0	1
0.627	0.887	26	0	0	1	1	0	1	0
0.634	0.896	27	0	0	1	1	0	1	1
0.640	0.905	28	0	0	1	1	1	0	0
0.646	0.914	29	0	0	1	1	1	0	1
0.653	0.924	30	0	0	1	1	1	1	0
0.660	0.933	31	0	0	1	1	1	1	1
0.667	0.943	32	0	1	0	0	0	0	0
0.674	0.953	33	0	1	0	0	0	0	1
0.681	0.963	34	0	1	0	0	0	1	0
0.688	0.973	35	0	1	0	0	0	1	1
0.696	0.984	36	0	1	0	0	1	0	0
0.703	0.995	37	0	1	0	0	1	0	1
0.711	1.01	38	0	1	0	0	1	1	0
0.719	1.02	39	0	1	0	0	1	1	1
0.727	1.03	40	0	1	0	1	0	0	0
0.736	1.04	41	0	1	0	1	0	0	1
0.744	1.05	42	0	1	0	1	0	1	0
0.753	1.06	43	0	1	0	1	0	1	1
0.762	1.08	44	0	1	0	1	1	0	0
0.771	1.09	45	0	1	0	1	1	0	1
0.780	1.10	46	0	1	0	1	1	1	0
0.790	1.12	47	0	1	0	1	1	1	1
0.800	1.13	48	0	1	1	0	0	0	0
0.810	1.15	49	0	1	1	0	0	0	1
0.821	1.16	50	0	1	1	0	0	1	0
0.831	1.18	51	0	1	1	0	0	1	1
0.842	1.19	52	0	1	1	0	1	0	0
0.853	1.21	53	0	1	1	0	1	0	1
0.865	1.22	54	0	1	1	0	1	1	0
0.877	1.24	55	0	1	1	0	1	1	1
0.889	1.26	56	0	1	1	1	0	0	0
0.901	1.27	57	0	1	1	1	0	0	1
0.914	1.29	58	0	1	1	1	0	1	0
0.928	1.31	59	0	1	1	1	0	1	1
0.941	1.33	60	0	1	1	1	1	0	0
0.955	1.35	61	0	1	1	1	1	0	1
0.969	1.37	62	0	1	1	1	1	1	0
0.985	1.39	63	0	1	1	1	1	1	1
1.00	1.41	64	1	0	0	0	0	0	0
1.02	1.44	65	1	0	0	0	0	0	1
1.03	1.46	66	1	0	0	0	0	1	0
1.05	1.48	67	1	0	0	0	0	1	1
1.07	1.51	68	1	0	0	0	1	0	0
1.08	1.53	69	1	0	0	0	1	0	1
1.10	1.56	70	1	0	0	0	1	1	0
1.12	1.59	71	1	0	0	0	1	1	1
1.14	1.62	72	1	0	0	1	0	0	0
1.16	1.65	73	1	0	0	1	0	0	1
1.19	1.68	74	1	0	0	1	0	1	0
1.21	1.71	75	1	0	0	1	0	1	1
1.23	1.74	76	1	0	0	1	1	0	0
1.25	1.77	77	1	0	0	1	1	0	1
1.28	1.81	78	1	0	0	1	1	1	0
1.31	1.85	79	1	0	0	1	1	1	1
1.33	1.89	80	1	0	1	0	0	0	0
1.36	1.93	81	1	0	1	0	0	0	1
1.39	1.97	82	1	0	1	0	0	1	0
1.42	2.01	83	1	0	1	0	0	1	1
1.45	2.06	84	1	0	1	0	1	0	0
1.49	2.10	85	1	0	1	0	1	0	1
1.52	2.16	86	1	0	1	0	1	1	0
1.56	2.21	87	1	0	1	0	1	1	1
1.60	2.26	88	1	0	1	1	0	0	0
1.64	2.32	89	1	0	1	1	0	0	1
1.68	2.40	90	1	0	1	1	0	1	0
1.73	2.45	91	1	0	1	1	0	1	1
1.78	2.51	92	1	0	1	1	1	0	0
1.83	2.59	93	1	0	1	1	1	0	1
1.88	2.66	94	1	0	1	1	1	1	0
1.94	2.74	95	1	0	1	1	1	1	1

Notes: 4) Writing all 0s into Q0-Q6 activates a low power shutdown mode. BOTH filter sections are deactivated. 0 = V-, 1 = V+.

Table 3. Q Program Selection Table (Continued)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
2.00	2.83	96	1	1	0	0	0	0	0
2.06	2.92	97	1	1	0	0	0	0	1
2.13	3.02	98	1	1	0	0	0	1	0
2.21	3.12	99	1	1	0	0	0	1	1
2.29	3.23	100	1	1	0	0	1	0	0
2.37	3.35	101	1	1	0	0	1	0	1
2.46	3.48	102	1	1	0	0	1	1	0
2.56	3.62	103	1	1	0	0	1	1	1
2.67	3.77	104	1	1	0	1	0	0	0
2.78	3.96	105	1	1	0	1	0	0	1
2.91	4.11	106	1	1	0	1	0	1	0
3.05	4.31	107	1	1	0	1	0	1	1
3.20	4.53	108	1	1	0	1	1	0	0
3.37	4.76	109	1	1	0	1	1	0	1
3.56	5.03	110	1	1	0	1	1	1	0
3.76	5.32	111	1	1	0	1	1	1	1
4.00	5.66	112	1	1	1	0	0	0	0
4.27	6.03	113	1	1	1	0	0	0	1
4.57	6.46	114	1	1	1	0	0	1	0
4.92	6.96	115	1	1	1	0	0	1	1
5.33	7.54	116	1	1	1	0	1	0	0
5.82	8.23	117	1	1	1	0	1	0	1
6.40	9.05	118	1	1	1	0	1	1	0
7.11	10.1	119	1	1	1	0	1	1	1
8.00	11.3	120	1	1	1	1	0	0	0
9.14	12.9	121	1	1	1	1	0	0	1
10.7	15.1	122	1	1	1	1	0	1	0
12.8	18.1	123	1	1	1	1	0	1	1
16.0	22.6	124	1	1	1	1	1	0	0
21.3	30.2	125	1	1	1	1	1	0	1
32.0	45.3	126	1	1	1	1	1	1	0
64.0	90.5	127	1	1	1	1	1	1	1

Notes: 5) In Modes 1, 3, and 4: Q = 64/(128-N)

6) In Mode 2, the listed Q values are those of Mode 1 multiplied by $\sqrt{2}$. Then Q = 90.51/(128-N)

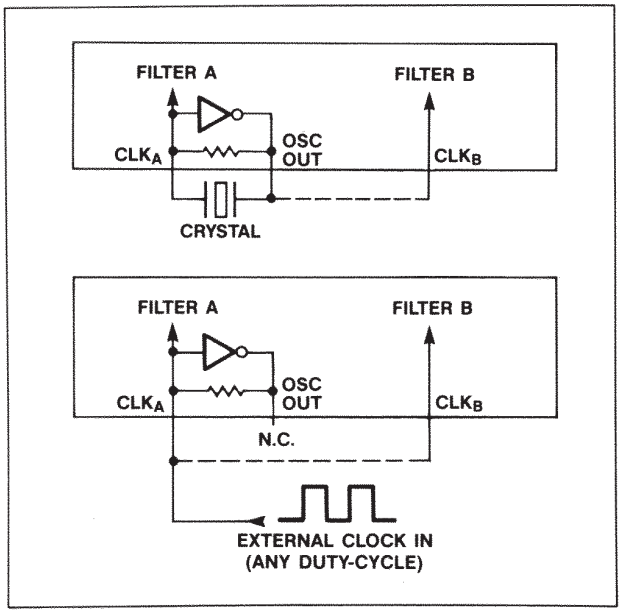


Figure 3. Clock Input Connections

Oscillator and Clock Inputs

The clock circuitry of the MAX263/64/67/68 can operate with a crystal or an external clock generator as shown in Figure 3. The duty cycle of the clock at CLK_A and CLK_B is unimportant because the input is internally divided by two to generate the sampling clock for each filter section. It is important to note that this internal division also halves the sample rate when considering aliasing and other sampled system phenomenon.

Shutdown Mode

The filter enters a shutdown mode when all Q inputs, Q0-Q6, are tied low. When shut down, power consumption with ±5V supplies typically drops to 25mW. When reactivating the filter after shutdown, allow 2ms to return to full operation.

Filter Operating Modes (MAX263/264 Only)

The MAX263/264's filter sections can be configured in four basic "Modes" as selected by inputs M0 and M1 (see Table 4). The MAX267/68 operates only in Mode 1. A fifth mode, 3A, uses an external op amp and resistors but is selected the same way and uses the same internal configuration as Mode 3.

Figures 4 through 8 show symbolic representations of the MAX263/64 filter modes. Only one second-order section is shown in each case, however the f_0, Q, and Mode select inputs are common to both halves of the IC. The f_0, f_N (notch), Q, and various output gains for each mode are shown in Table 4.

Filter Mode Selection

All operating modes listed in this section can be used with the MAX263/64. The MAX267/68 bandpass filter operates only in Mode 1.

MODE 1 (Figure 4) is useful when implementing all-pole lowpass and bandpass filters such as Butterworth, Chebyshev, Bessel, etc. It can also be used for notch filters, but only second-order notches because the relative pole and zero locations are fixed. Higher order notch filters require more latitude in f_0 and f_N, which is why they are more easily implemented with Mode 3A.

Pin Programmable Universal and Bandpass Filters

Table 4. Filter Modes for Second-Order Functions—MAX263/264 (MAX267/268 = MODE 1, BP only)

MODE	M1, M0	FILTER FUNCTIONS	f_0	Q	f_N	H_{OLP}	H_{OBP}	H_{ON1} ($f \rightarrow 0$)	H_{ON2} ($f \rightarrow f_{CLK}/4$)	OTHER
1	0, 0	LP, BP, N	SEE TABLE 2	SEE TABLE 3	f_0	-1	-Q	-1	-1	
2	0, 1	LP, BP, N			$f_0\sqrt{2}$	-0.5	$-Q/\sqrt{2}$	-0.5	-1	
3	1, 0	LP, BP, HP				-1	-Q			$H_{OHP} = -1$
3A	1, 0	LP, BP, HP, N			$f_0\sqrt{\frac{R_H}{R_L}}$	-1	-Q	$+\frac{R_G}{R_L}$	$+\frac{R_G}{R_H}$	$H_{OHP} = -1$
4	1, 1	LP, BP, AP				-2	-2Q			$H_{OAP} = -1$ $f_Z = f_0$, $Q_Z = Q$

Notes: f_0 = Center Frequency
f_N = Notch Frequency
H_{OLP} = Lowpass Gain at DC
H_{OBP} = Bandpass Gain at f_0
H_{OHP} = Highpass Gain as f approaches $f_{CLK}/4$
H_{ON1} = Notch Gain as f approaches DC
H_{ON2} = Notch Gain as f approaches $f_{CLK}/4$
H_{OAP} = Allpass Gain
f_Z, Q_Z = f and Q of Complex Pole Pair

Mode 1, along with Mode 4, supports the highest clock frequencies (see Table 1) because the input summing amplifier is outside the filter's resonant loop (Figure 4). The gain of the lowpass and notch outputs is 1, while the bandpass gain at the center frequency is Q. For bandpass gains other than Q, the filter input or output can be scaled by a resistive divider or op amp. In multiple feedback filters, the gain is set by the feedback resistors.

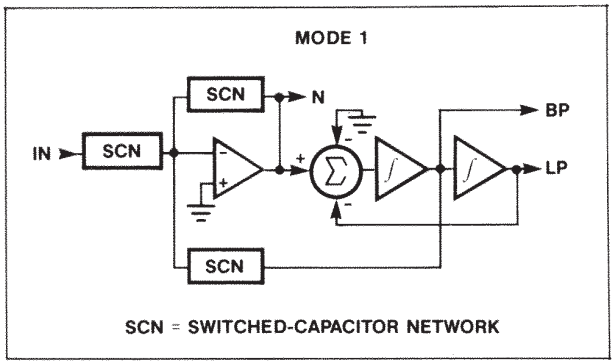


Figure 4. Filter Mode 1: Second-Order Bandpass, Lowpass and Notch

MODE 2 (Figure 5) is used for all-pole lowpass and bandpass filters. Key advantages compared to Mode 1 are higher available Qs (see Table 3) and lower output noise. Mode 2's available f_{CLK}/f_0 ratios are $\sqrt{2}$ less than with Mode 1 (see Table 2) so a wider overall range of f_0s can be selected from a single clock when both modes are used together.

MODE 3 (Figure 6) is the only mode which produces high-pass filters. The maximum clock frequency is somewhat less than with Mode 1 (see Table 1).

MODE 3A (Figure 7) uses a separate op amp to sum the highpass and lowpass outputs of Mode 3, creating a separate notch output. This output allows the notch to be set independently of f_0 by adjusting the op amp's feedback resistor ratio (R_H, R_L). R_H, R_L, and R_G are external resistors. Because the notch can be independently set, Mode 3A is also useful when designing pole-zero filters such as elliptics.

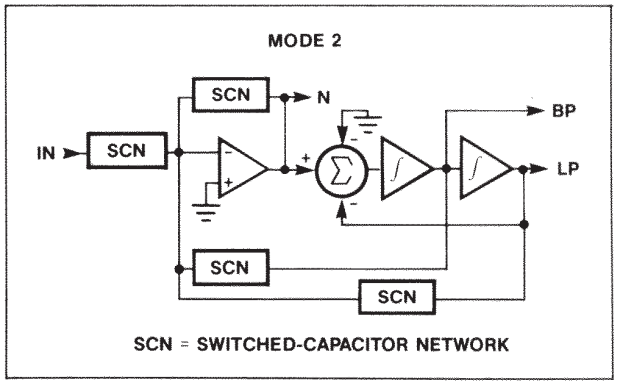


Figure 5. Filter Mode 2: Second-Order Bandpass, Lowpass and Notch

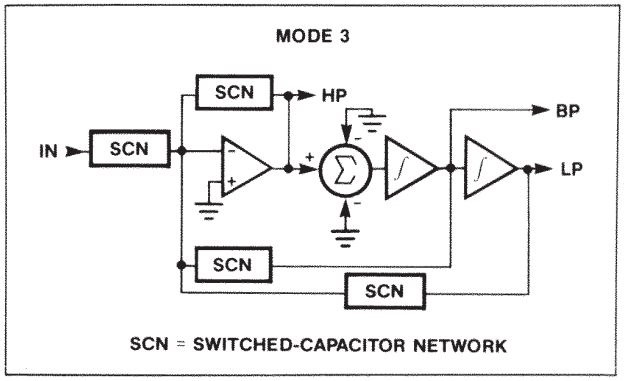


Figure 6. Filter Mode 3: Second-Order Bandpass, Lowpass and Highpass

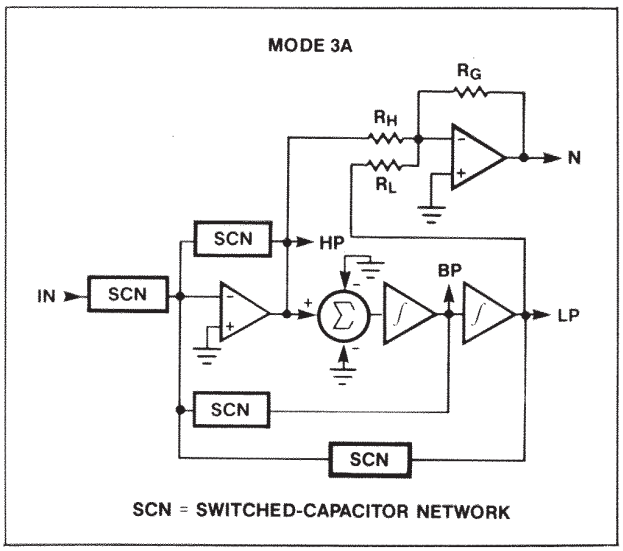


Figure 7. Filter Mode 3A: Second-Order Bandpass, Lowpass, Highpass and Notch. For elliptic LP, BP, HP and Notch, the N output is used.

MODE 4 (Figure 8) is the only mode that provides an allpass output. This is useful when implementing group delay equalization. In addition to this, Mode 4 can also be used in all pole lowpass and bandpass filters. Along with Mode 1, it is the fastest operating mode for the filter, although the gains are different than in Mode 1. When the allpass function is used, note that some amplitude peaking occurs (approximately 0.3dB when Q = 8) at f_0. Also note that f_0 and Q sampling errors are highest in Mode 4 (see Figure 17).

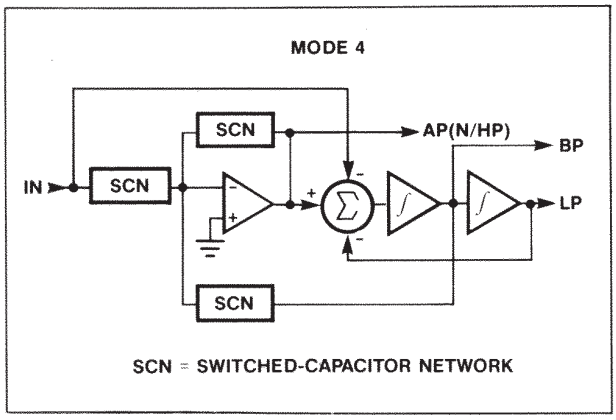


Figure 8. Filter Mode 4: Second-Order Bandpass, Lowpass and Allpass

Description of Filter Functions

The MAX263/64 performs all filter functions listed in this section. The MAX267/68 operates only as a bandpass filter.

BANDPASS (Figure 9)

For all pole bandpass and lowpass filters (Butterworth, Bessel, Chebyshev) use Mode 1 if possible. If appropriate f_{CLK}/f_0 or Q values are not available in Mode 1, Mode 2 may provide a selection that is closer to the required values. Mode 1 however has the highest bandwidth (see Table 1). For pole-zero filters such as elliptics see Mode 3A.

$$G(s) = H_{OBP}\frac{s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Bandpass output gain at $\omega = \omega_o$

f_0 = $\omega_o/2\pi$ = The center frequency of the complex pole pair. Input-output phase shift is -180° at f_0.

Q = The quality factor of the complex pole pair. Also the ratio of f_0 to -3dB bandwidth of the second-order bandpass response.

LOWPASS See Bandpass text. (Figure 10)

$$G(s) = H_{OLP}\frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = Lowpass output gain at DC

f_0 = $\omega_0/2\pi$

HIGHPASS (Figure 11)

Mode 3 is the only mode with a highpass output. It will work for all pole filter types such as Butterworth, Bessel and Chebyshev. Use mode 3A for filters employing both poles and zeros such as elliptics.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = Highpass output gain as f approaches $f_{CLK}/4$

f_0 = $\omega_0/2\pi$

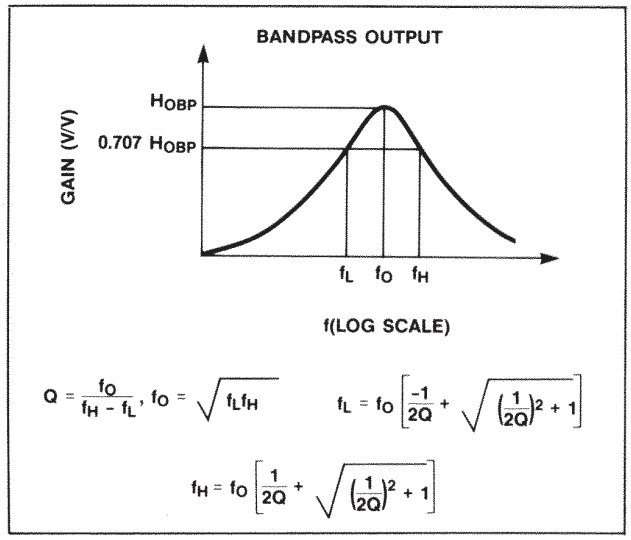


Figure 9. Second-Order Bandpass Characteristics

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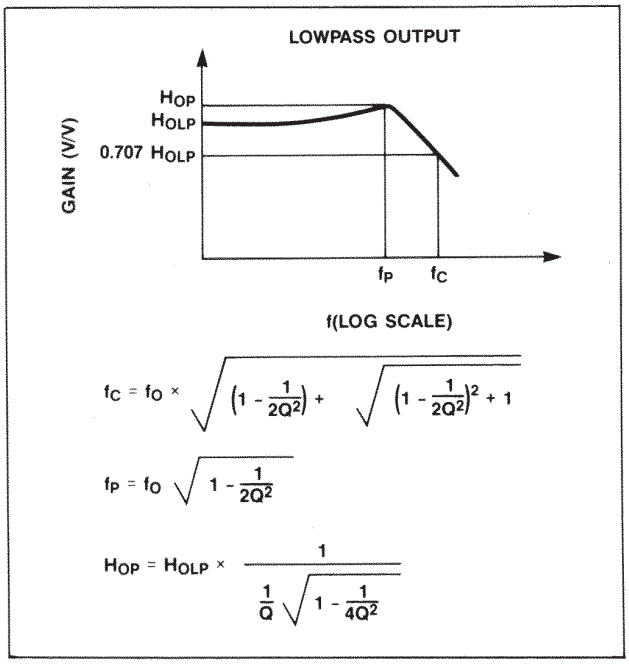


Figure 10. Second-Order Lowpass Characteristics

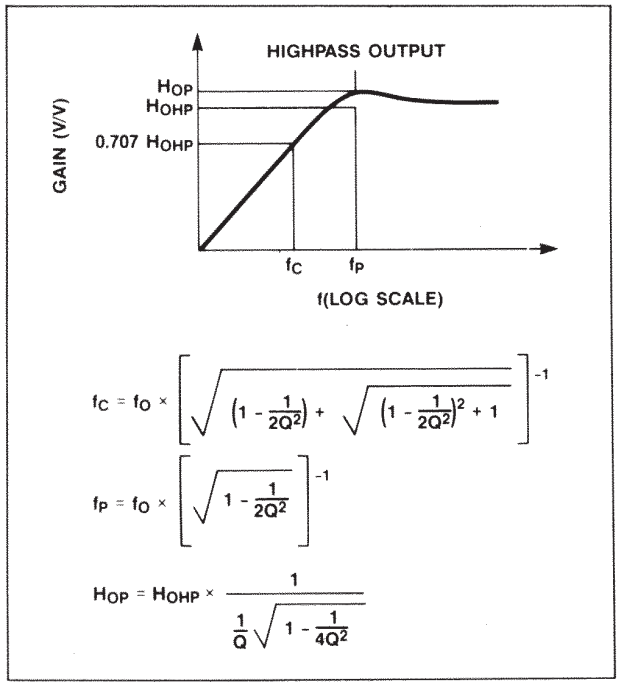


Figure 11. Second-Order Highpass Characteristics

NOTCH (Figure 12)

Mode 3A is recommended for multi-pole notch filters. In 2nd order filters, Mode 1 can also be used. The advantages of Mode 1 are higher bandwidth compared to mode 3 (Higher f_N can be implemented) and no need for external components as required in Mode 3A.

$$G(s) = H_{ON2} \frac{s^2 + \omega_n^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = Notch output gain as f approaches $f_{CLK}/4$

H_{ON1} = Notch output gain as f approaches DC

$f_n = \omega_n/2\pi$

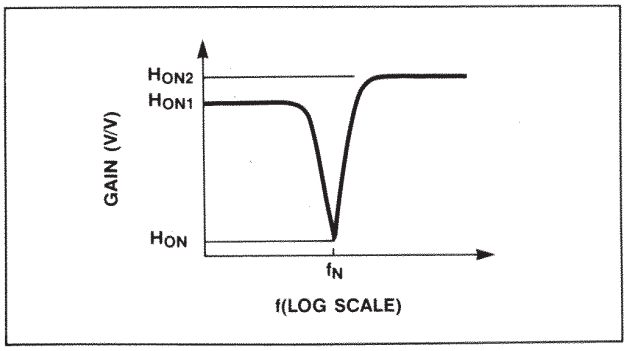


Figure 12. Second-Order Notch Characteristics

ALL PASS

Mode 4 is the only configuration in which an allpass function can be realized.

$$G(s) = H_{OAP} \frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = All pass output gain for $DC < f < f_{CLK}/4$

$f_0 = \omega_0/2\pi$

Filter Design Procedure

The procedure for most filter designs is to first convert the required frequency response specifications to f_0s and Qs for the appropriate number of second-order sections that implement the filter. This can be done by using design equations or tables in available literature, or can be conveniently calculated using Maxim's filter design software. Once the f_0 and Qs have been found, the next step is to turn them into the digital program coefficients required by the filter. An operating Mode and clock frequency (or clock/center frequency ratio) must also be selected.

Next, if the sample rate ($f_{CLK}/2$) is low enough to cause significant errors, the selected f_0s and Qs should be corrected to account for sampling effects by using Figure 17 or Maxim's design software. In most cases, the sampling errors are small enough to require no correction, i.e. less than 1%. In any case, with or without correction, the required f_0s and Qs can then be selected from Tables 2 and 3. Maxim's filter design software can also perform this last step. The desired f_0s and Qs are stated, and the appropriate digital coefficients are supplied.

Multiple Feedback Bandpass Filters

An alternate implementation of all-pole bandpass filters (i.e. Butterworth, Chebyshev) requires only one clock and common programming for all second-order sections. This can be useful with MAX26X pin-programmed filters since the two second-order halves must be programmed with the same f_{CLK}/f_0 ratio and Q (although they may use different clocks).

As shown in Figure 13, external resistors connect the outputs of cascaded filter sections to a summing op-amp at the input. Since each 2nd-order section inverts (gain = -Q) the output from odd numbered sections (except for the first) must be inverted before being fed back as in the 8th-order example in Figure 13. The MAX267/68 has an on-chip amplifier for this purpose but the MAX263/64 requires external op-amp(s).

In multiple feedback filters, the bandpass response is a function of the clock, f_{CLK}/f_0 ratio, Q, and feedback resistor ratios. In Table 5, constants for calculating resistor ratios in common bandpass configurations are listed. Maxim's filter design program "BP" also selects resistors for multiple feedback bandpass designs. A 4th-order design example (Figure 13) best illustrates how Table 5 is used.

Multiple Feedback Example

Requirements: 4th-order Chebyshev with 1 dB passband ripple, f_0 = 10kHz, and bandwidth (BW) = 2kHz.

1) The overall filter Q is $Q_F = f_0/BW$ = 10kHz/2kHz = 5
2) From Table 5: K_Q = 1.8219
3) The Q of each 2nd-order selection is $Q_R = Q_F \times K_Q$ = 5 x 1.8219 = 9.09
4) R_F is selected, 10kΩ is a convenient value.
5) $R_2 = K_2 R_F (Q_R/2)^2$ = 1.5039 x 10k x $(9.109/2)^2$ = 312k
   In higher order filters, the general equation is: $R_N = K_N R_F (Q_R/2)^N$
6) R_0 sets the overall gain, A: $R_0 = K_0 R_F (Q_R/2)^2/A$, so for a gain of 1: R_0 = 1.0930 x 10k x $(9.109/2)^2/1$ = 226.8k. In higher order filters the general equation is $R_0 = K_0 R_F (Q_R/2)^M$ where M = (order of filter)/2.
7) The filter f_0 can be programmed using a wide range of clock frequencies and f_{CLK}/f_0 ratios. If f_{CLK} = 1MHz, then f_{CLK}/f_0 = 100 (code 00000 = 100.53) results in f_0 = 10kHz.
8) A 2.5pF to 10pF capacitor may be required across R_2 to prevent response peaking.

Cascading Filters

In some designs, such as very narrow band filters, several second-order sections with identical center frequency may be cascaded without multiple feedback. The total Q of the resultant filter is:

$$\text{Total } Q_T = \frac{Q}{\sqrt{(2^{1/N} - 1)}}$$

Q is the Q of each individual filter section, and N is the number of sections. In Table 6, the Total Q and

Table 5. Multiple Feedback Bandpass Filter Constants

TYPE (RIPPLE)	ORDER	K0	K2	K3	K4	KQ
Butterworth	4	2.0000	4.0000			1.4142
(3.0 dB)	6	2.3704	2.6667	9.1429		1.5000
	8	2.9142	2.000	5.8284	14.315	1.5307
Chebyshev	4	1.6983	2.9512			0.8430
(0.1 dB)	6	1.3183	1.2137	4.5125		1.5473
	8	0.7986	0.5782	1.8809	2.0343	2.2176
Chebyshev	4	1.5757	2.5998			1.0378
(0.2 dB)	6	1.1128	0.9894	3.7271		1.8413
	8	0.5891	0.4551	1.4954	1.3309	2.6057
Chebyshev	4	1.3405	2.0161			1.4029
(0.5 dB)	6	0.8143	0.6897	2.6447		2.3944
	8	0.3389	0.3040	1.0114	0.6365	3.3406
Chebyshev	4	1.0930	1.5039			1.8219
(1.0 dB)	6	0.5822	0.4756	1.8475		3.0354
	8	0.1869	0.2038	0.6840	0.3002	4.1981
Chebyshev	4	0.9192	1.1934			2.1688
(1.5 dB)	6	0.4515	0.3616	1.4145		3.5705
Chebyshev	4	0.7850	0.9767			2.4881
(2.0 dB)	6	0.3641	0.2878	1.1308		4.0660
Chebyshev	4	0.6769	0.8148			2.7962
(2.5 dB)	6	0.3005	0.2353	0.9275		4.5462
Chebyshev	4	0.5875	0.6886			3.1013
(3.0 dB)	6	0.2519	0.1959	0.7739		5.0231

Pin Programmable Universal and Bandpass Filters

Table 6. Cascading Identical Bandpass Filter Sections

Total Sections	Total B.W.	Total Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Note: B = individual stage bandwidth, Q = individual stage Q.

bandwidth are listed for up to five identical second-order sections. B is the bandwidth of each section.

In high order bandpass filters that do not use multiple feedback, stages with different f_0s and Qs may also be cascaded. When this happens the overall filter gain at the bandpass center frequency is not simply the product of the individual gains because f_0s, the frequency where each section's gain is specified, is different for each second-order section. The gain of each section at the cascaded filter's center frequency must be determined to obtain the total gain.

For all-pole filters the gain, $H(f_0)$, at each second-order section's f_0 is divided by an adjustment factor, G, to obtain that section's gain, $H(f_{0BP})$, at the overall center frequency:

$H_1(f_{0BP}) = H(f_{01})/G_1$ = Section 1's Gain at f_{0BP}

$$G_1 = \frac{Q_1[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1}$$

where $F_1 = f_{01}/f_{OBP}$

G_1, Q_1, and f_{01} are the gain adjustment factor, Q, and f_0 for the first of the cascaded second-order sections. The gain of the other sections (2, 3 etc.) at f_{0BP} is determined the same way. The overall gain is:

$H(f_{0BP}) = H_1(f_{0BP}) \times H_2(f_{0BP}) \times$ etc.

For cascaded filters with zeros (f_Z) such as elliptics, the gain adjustment factor for each stage is:

$$G_1 = \frac{Q_1[F_{Z1}^2 - F_1^2]\,[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1^2(F_{Z1}^2 - 1)}$$

where $F_{Z1} = f_{Z1}/f_{0BP}$, and F_1 is the same as above.

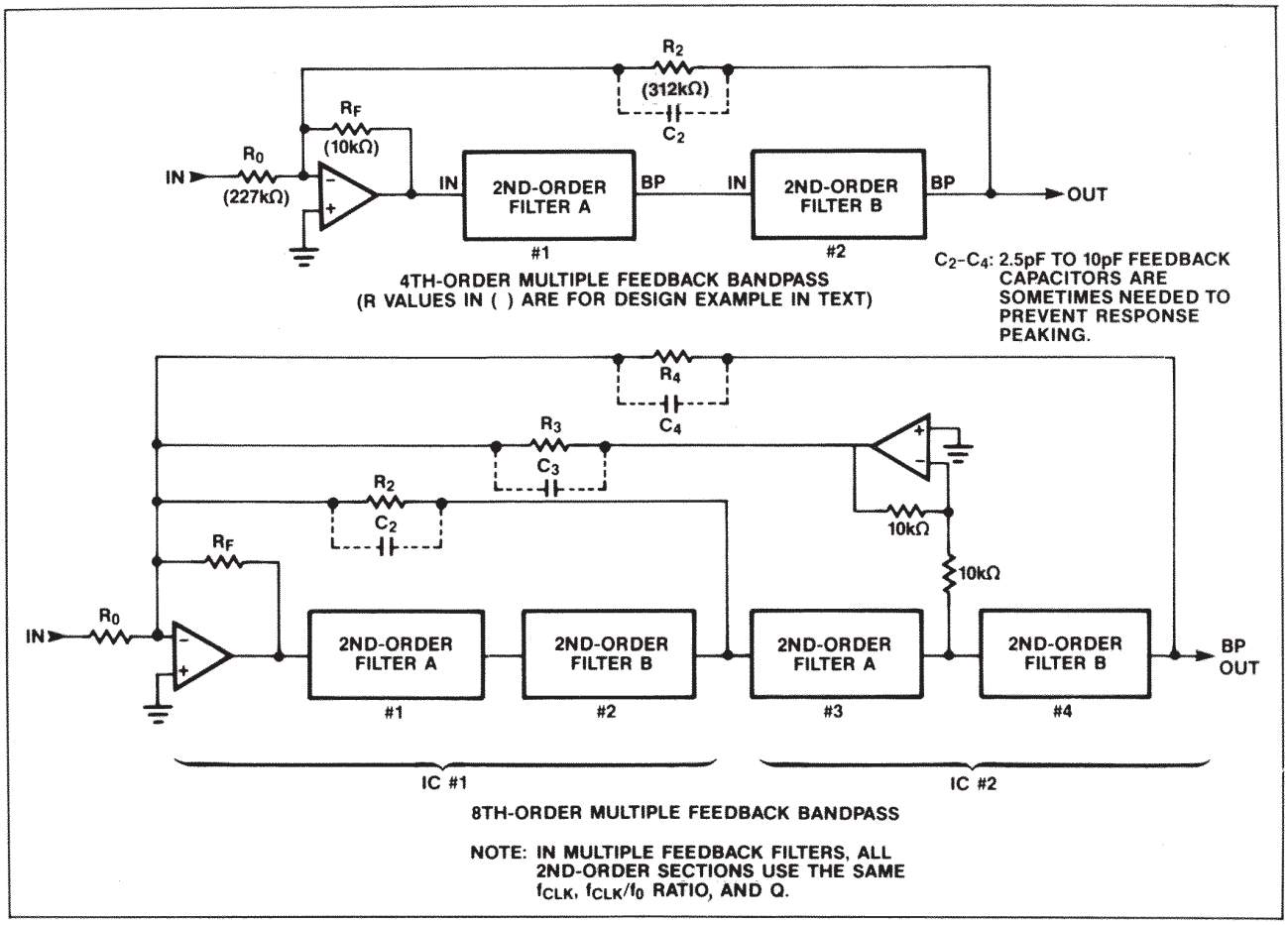


Figure 13. Multiple Feedback Bandpass Block Diagram (See Text for R Values)

Application Hints

Power Supplies

The MAX263/64/67/68 can be operated with a variety of power supply configurations including +5V to +12V single supply, or ±2.5V to ±6V dual supplies. When a single supply is used, V^- is connected to system ground and the filter's GND pin should be biased at $V^+/2$. The input signal is then either capacitively coupled to the filter input or biased to $V^+/2$. Figure 14 shows circuit connections for single supply operation.

Power consumption at ±5V is reduced if CLK_A and CLK_B are driven with ±5V, rather than TTL or 0 to 5V levels. Operation with +5V or ±2.5V power lowers power consumption but also reduces bandwidth by approximately 25% compared to +12V or ±5V supplies.

Best performance is achieved if V^+ and V^- are bypassed to ground with 4.7µF electrolytic (Tantalum is preferred.) and 0.1µF ceramic capacitors. These should be located as close to the supply pins as possible. The lead length of the bypass capacitors should be shortest at the V^+ and V^- pins. When using a single supply V^+ and GND should be bypassed to V^- as shown in Figure 14.

Output Swing and Clipping

MAX26X outputs are designed to swing to within 0.15V of each supply rail with a 10kΩ load.

To ensure that the outputs are not driven beyond their maximum range (output clipping), the peak amplitude response, individual section gains (H_{OBP}, H_{OLP}, H_{OHP}), input signal level, and filter offset voltages must be carefully considered. It is especially important to check UNUSED outputs for clipping (i.e. the lowpass output in a bandpass hookup) because overload at ANY filter stage severely distorts the overall response. The maximum signal swing with ±4.75V supplies and a 1.0V filter offset is approximately ±3.5V.

For example let's assume a fourth-order lowpass filter is being implemented with a Q of 2 using Mode 1. With a single 5V supply (i.e. ±2.5V with respect to chip GND) the maximum output signal is ±2V (w.r.t. GND). Since in Mode 1 the maximum signal is Q times the input signal, the input should not exceed ±(2/Q)V, or ±1V in this case.

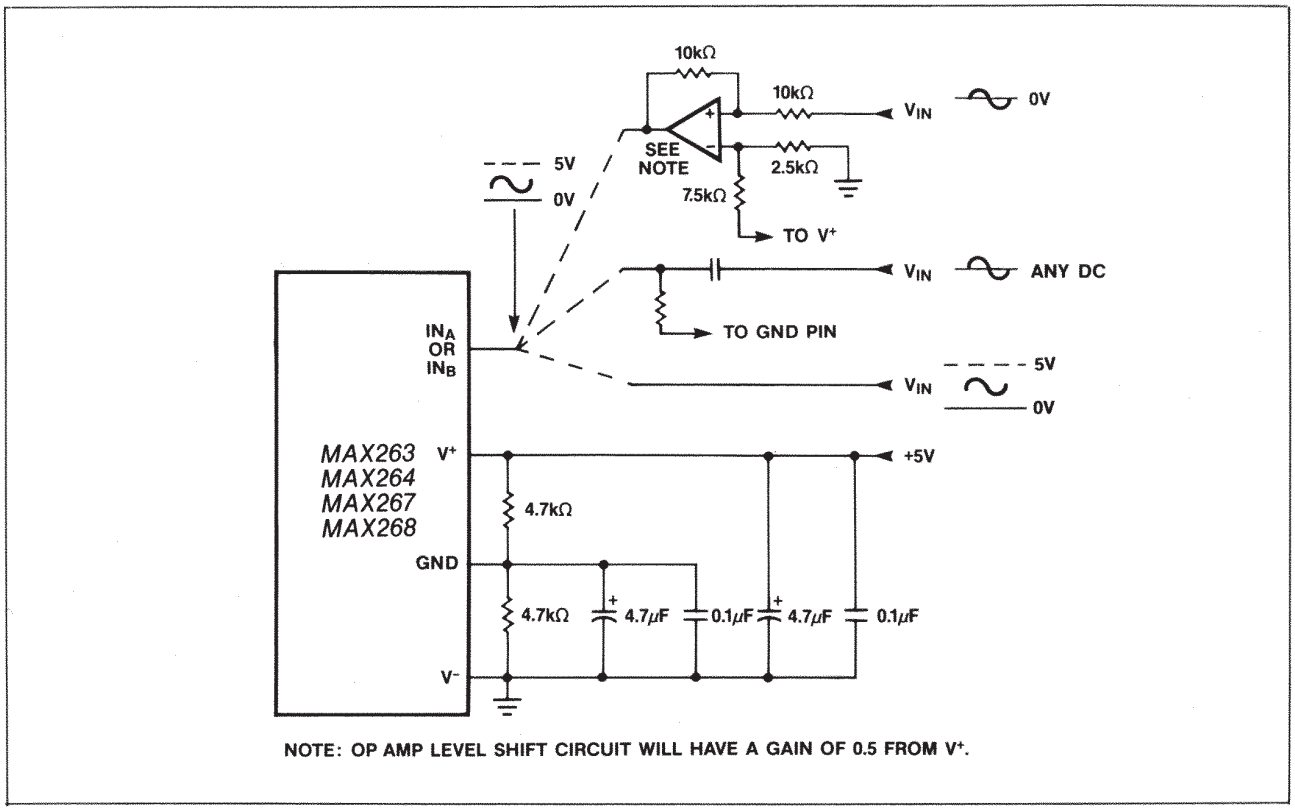


Figure 14. Power Supply and Input Connections for Single Supply Operation

Pin Programmable Universal and Bandpass Filters

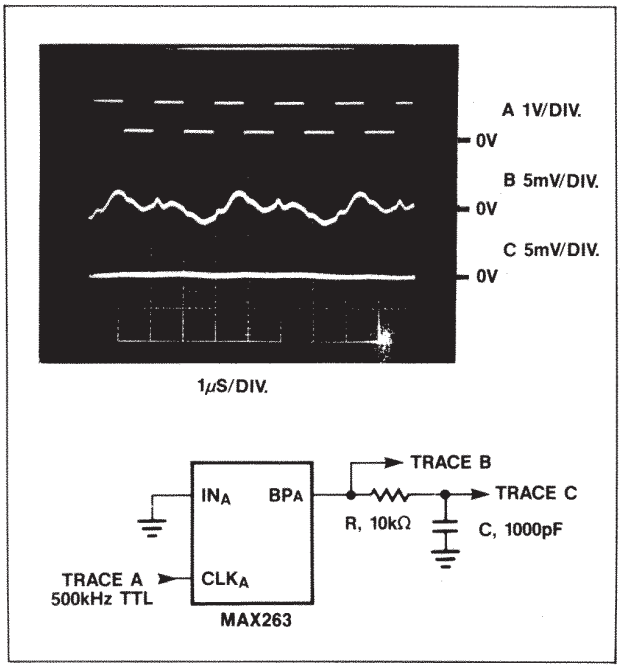


Figure 15. MAX263 Bandpass Output Clock Noise

Clock Feedthrough and Noise

Typical wideband noise for MAX26X series devices is $0.5mV_{pp}$ from DC to 100kHz. The noise is virtually independent of clock frequency. In multistage filters, the section with the highest Q should be placed first for lower output noise.

The output waveform of the MAX26X series and other switched capacitor filters appears as a sampled signal with stepping or "staircasing" of the output waveform occurring at the internal sample rate ($f_{CLK}/2$). This stepping, if objectionable, can be removed by adding a single pole RC filter. With no input signal, clock related feedthrough is approximately $8mV_{pp}$. This can also be attenuated with an RC smoothing filter as shown with the MAX263 in Figure 15.

Input Impedance

The filter input model is shown in Figure 16. Input capacitor C_A is shunted by C_B which is switched at one half the input clock frequency ($F_{CLK}/2$). The input impedance is described by: $R_{IN} = 2/(C_A \times f_{CLK})$. There is also a fixed stray capacitance of about 5pF to ground.

Digital Inputs

Filter programming is accomplished by tying input pins M0, M1, F0-F4, and Q0-Q6 to high or low voltage levels, typically V^+ and V^-. Inputs are not internally pulled up or down, so these inputs must not be left unconnected. Input thresholds are guaranteed to be no higher than V^+ –0.5V and no lower than V^- +0.5V. When driving the digital inputs (i.e., the digital inputs

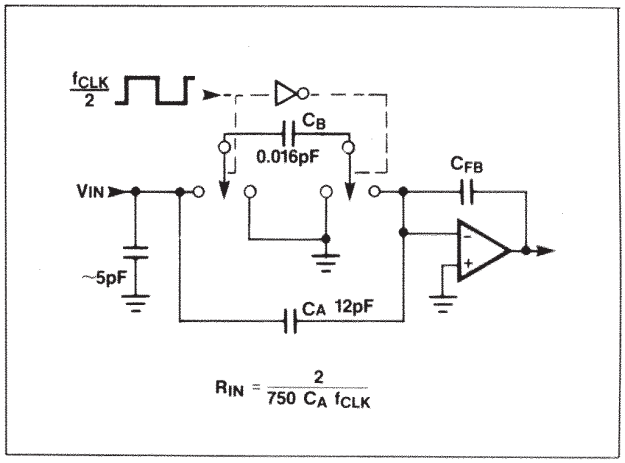


Figure 16. MAX263/64/67/68 Input Model

are tied to microprocessor I/O lines), additional protection is provided by placing a 1kΩ resistor in series with the programming pins. If pull-up resistors are used with switches at the programming inputs, as might be the case in prototype breadboards, the pull-up resistors should be no more than 3.3kΩ.

f_0 and Q at Low Sample Rates

When low f_{CLK}/f_0 ratios and low Q settings are selected, deviation from ideal continuous filter response may be noticeable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Figure 17 quantifies these differences. Since the errors are predictable, the graphs can be used to correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX26X series devices and in fact occur with all sampled filters. Consequently, these corrections can be applied to other switched-capacitor filters. In the majority of cases, the errors are not significant, i.e. less than 1%, and correction is not needed. However, the MAX264/68 does employ a lower range of f_{CLK}/f_0 ratios than the MAX263/67 and is more prone to sampling errors as the tables show.

Maxim's filter design software applies the previous corrections automatically as a function of desired f_{CLK}/f_0, and Q. Therefore, Figure 17 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

The data plotted in Figure 17 applies for Modes 1 and 3. When using Figure 17 for Mode 4, the f_0 error obtained from the graph should be multiplied by 1.5 and the Q error should be multiplied by 3.0. In Mode 2 the value of f_{CLK}/f_0 should be multiplied by $\sqrt{2}$ and the programmed Q should be divided by $\sqrt{2}$ before using the graphs.

Pin Programmable Universal and Bandpass Filters

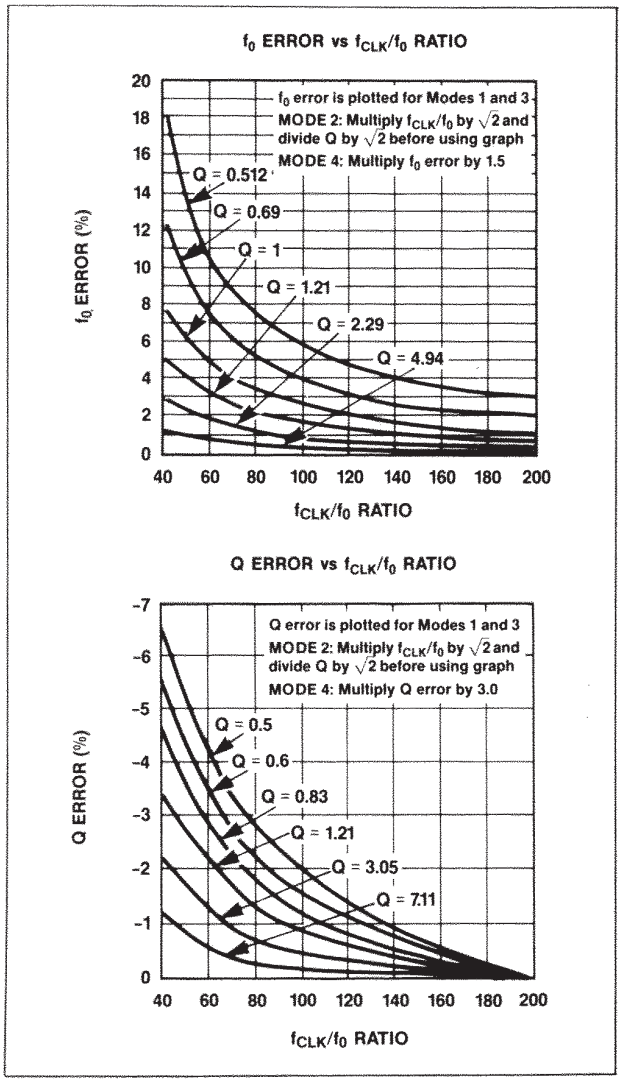


Figure 17. Sampling Errors in f_{CLK}/f_0 and Q at Low f_{CLK}/f_0 and Q Settings

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, (f_{CLK} = 200kHz) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Remember that with the MAX26X series filters, the nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can cause aliasing. In many cases the input signal itself may be band limited and require no special anti-alias filtering. The wideband MAX264/68 uses lower f_{CLK}/f_0 ratios than the MAX263/67 and for this reason is more likely to require input filtering than the MAX263 or MAX267.

Trimming DC Offset

The DC offset voltage at the LP or Notch output can be adjusted with the circuit in Figure 18. This circuit also uses the input op-amp to implement a single pole anti-alias filter. Note that the total offset will generally be less in multistage filters than when only one section is used since each offset is typically negative and each section inverts. When the HP or BP outputs are used, the offset can be removed with capacitor coupling.

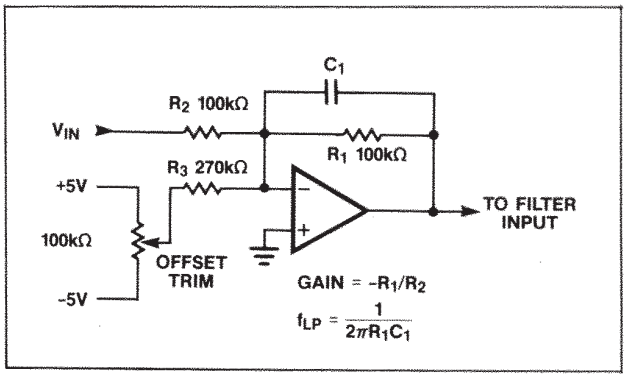


Figure 18. Circuit for DC Offset Adjustment

Design Examples

4th-Order Multiple Feedback Bandpass—MAX268

In Figure 19, a pin-programmed MAX268 operates as a 4th-order 50kHz Chebyshev bandpass. The specifications are:

Center frequency (f_0) = 50kHz
Pass bandwidth = 10kHz
Max. passband ripple = 0.1dB
Gain at center freq. = 1V/V

Two identical 2nd-order sections and the internal op amp are used with multiple feedback. The general form is as in Figure 13. Maxim's design program, BP, generates the programming codes and feedback resistor values. With a 2.5MHz crystal clock the realized parameters are:

Center frequency = 50.305kHz
Pass Bandwidth = 10.07kHz
Programmed f_{CLK}/f_0 ratio = 50.27 (N = 3)
Programmed Q = 4.27 (N = 113)
(desired Q = 4.215)
Actual Q (with error correction) = 4.21
Resistors: R_2 = 131kΩ, R_0 = 75kΩ, R_F = 10kΩ

Pin Programmable Universal and Bandpass Filters

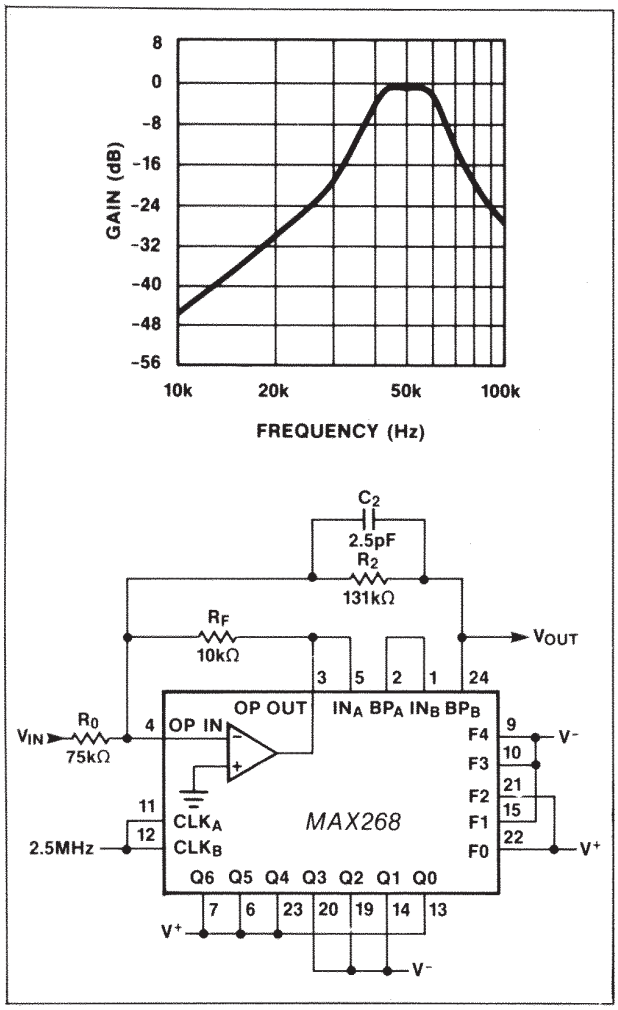


Figure 19. 4th-Order 50kHz Chebyshev Bandpass Using Multiple Feedback

Other clock rates and f_{CLK}/f_0 ratios can be chosen to implement the same filter, but larger f_{CLK}/f_0 ratios provide performance closer to the ideal. Capacitor C_2 may be needed to prevent response peaking at the passband edge. In this example C_2 = 2.5pF.

Multiple feedback can also be extended to 8th-order designs while still using one clock by adding a second MAX268 and 2 additional feedback resistors. These can also be calculated with the design program, BP. Note that for filter order above 4, the feedback signal from odd filter sections is inverted before it is summed (see Figure 13).

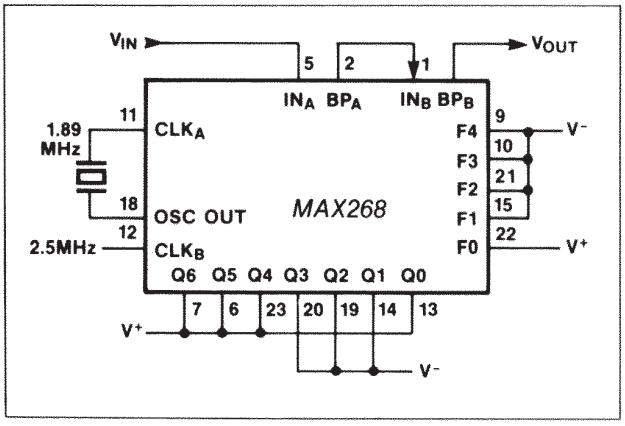


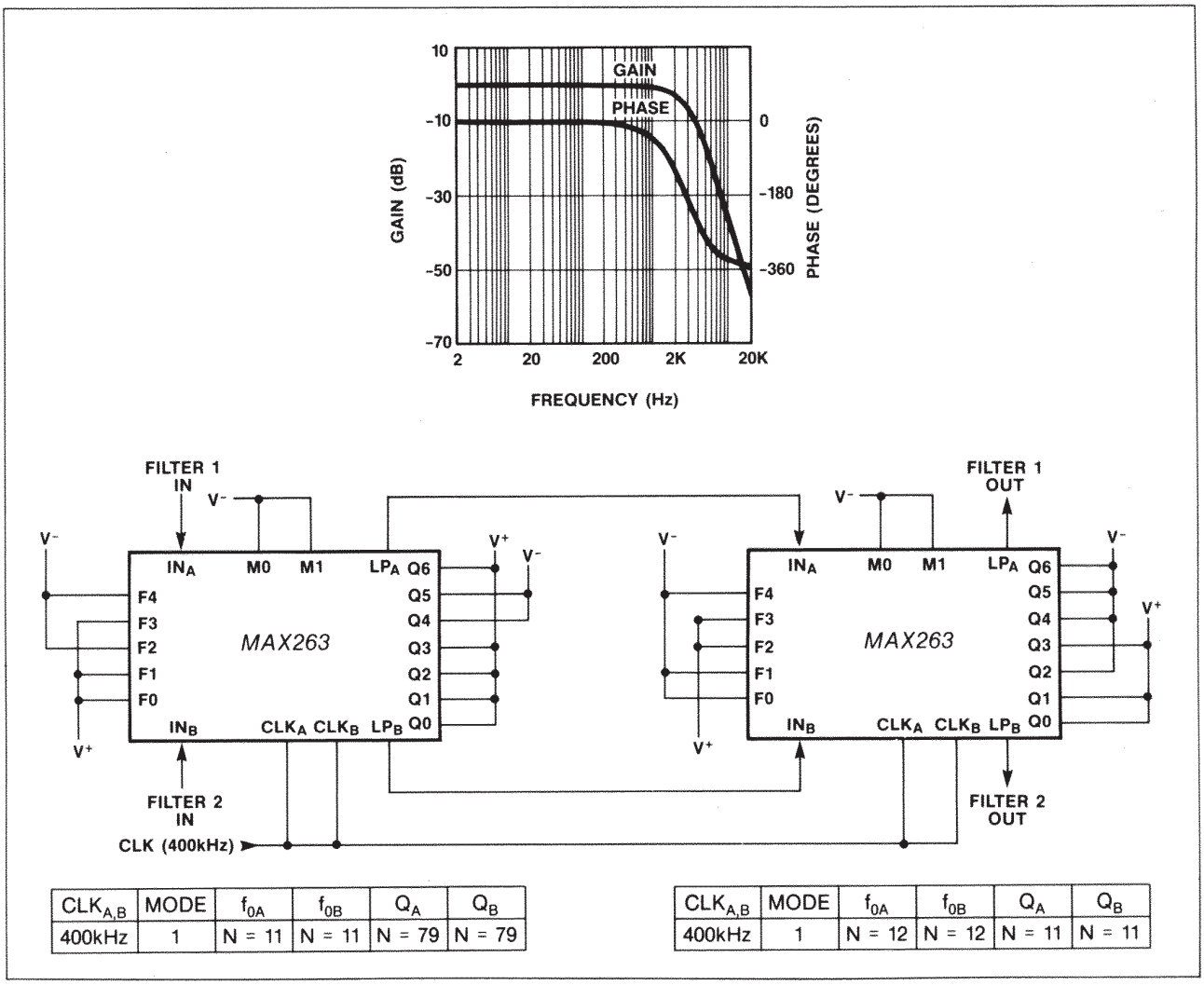
Figure 20. 4th-Order 50kHz Chebyshev Bandpass Using No External Resistors

4th-Order Bandpass (No Multiple Feedback)—MAX268

Without multiple feedback, the previous example can be implemented with no external components, however separate clocks are required for CLK_A and CLK_B (Figure 20). The target specifications are the same as before. The realized parameters are now:

CLK_A = 1.89MHz, CLK_B = 2.5MHz
Center frequency = 50kHz
Pass bandwidth = 10kHz
Programmed f_{CLK}/f_0 ratio = 43.98 (N = 1)
Programmed Q = 4.27 (N = 113) (desired Q = 4.215)
Actual Q (with error correction) = 4.2

With the chosen f_{CLK}/f_0 ratio, a crystal may be used at CLK_A while a divided system clock, if available (2.5, 5, 10, or 20MHz), drives CLK_B. This is suggested because CLK_A has internal circuitry to drive a crystal while CLK_B does not. Other clock sources may be used with a different programmed f_{CLK}/f_0 as long as the ratio between CLK_A and CLK_B remains the same as above. Another advantage of this circuit is that higher center frequencies can be achieved relative to equivalent multiple feedback designs because lower Q sections are used compared to multiple feedback.



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400kHz	1	N = 11	N = 11	N = 79	N = 79

$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400kHz	1	N = 12	N = 12	N = 11	N = 11

Figure 21. Dual Tracking 3kHz 4th-Order Lowpass

Dual 4th-Order Tracking Lowpass—MAX263

In Figure 21, two Butterworth lowpass filters are set up to accurately track each other. By "splitting" two MAX263s only one clock is needed. The specifications are:

Cutoff frequency = 3kHz
$f_{0A} = f_{0B} = 3kHz$
$Q_A = 1.307$, $Q_B = 0.541$

These values can be programmed directly into the filter. However, since the Qs are low, sampling errors may be large enough to deserve attention. From Figure 17, if f_{CLK}/f_0 is near 130 (f_{CLK} is 400kHz), f_{0A} and f_{0B} will be about 4% and 1.5% high respectively. Q_A and Q_B will be 1.2% and 0.5% low. These errors may not be large enough to worry about but are corrected here (within the programming resolution of the MAX263) by the filter design programs PZ and MPP. f_{0A} and f_{0B} are programmed to different values ($N_A = 11$, $N_B = 12$) for this reason.

Mode 1, $CLK_A = CLK_B = 400kHz$
$f_{CLK}/f_{0A} = 135.08$, N = 11
(target $f_{0A} = 2961Hz$, actual = 3008Hz)
$f_{CLK}/f_{0B} = 138.23$, N = 12
(target $f_{0B} = 2894Hz$, actual = 3015Hz)
$Q_A = 1.31$, N = 79 (actual $Q_A = 1.30$)
$Q_B = 0.547$, N = 11 (actual $Q_A = 0.542$)

Pin Programmable Universal and Bandpass Filters

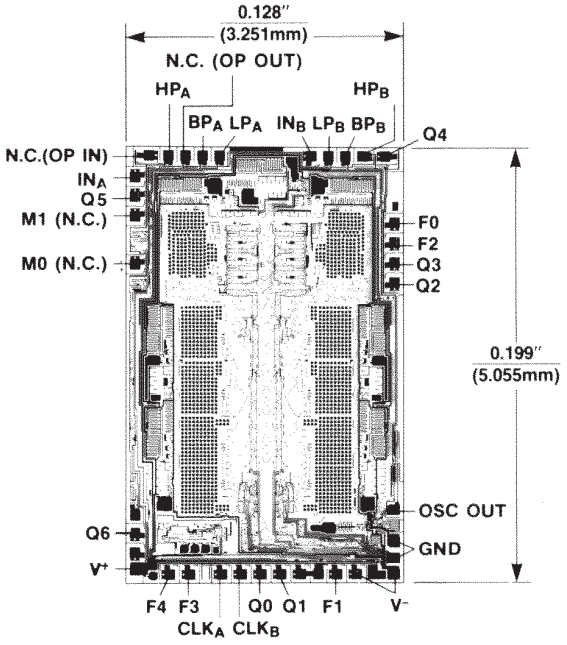
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX264AEPI	-40°C to +85°C	Plastic DIP	1%
MAX264BEPI	-40°C to +85°C	Plastic DIP	2%
MAX264ACWI	0°C to +70°C	Wide SO	1%
MAX264BCWI	0°C to +70°C	Wide SO	2%
MAX264AMJI	-55°C to +125°C	CERDIP	1%
MAX264MBJI	-55°C to +125°C	CERDIP	2%
MAX267ACNG	0°C to +70°C	Plastic DIP	1%
MAX267BCNG	0°C to +70°C	Plastic DIP	2%
MAX267AENG	-40°C to +85°C	Plastic DIP	1%
MAX267BENG	-40°C to +85°C	Plastic DIP	2%
MAX267ACWG	0°C to +70°C	Wide SO	1%
MAX267BCWG	0°C to +70°C	Wide SO	2%
MAX267AMRG	-55°C to +125°C	CERDIP	1%
MAX267BMRG	-55°C to +125°C	CERDIP	2%
MAX268ACNG	0°C to +70°C	Plastic DIP	1%
MAX268BCNG	0°C to +70°C	Plastic DIP	2%
MAX268AENG	-40°C to +85°C	Plastic DIP	1%
MAX268BENG	-40°C to +85°C	Plastic DIP	2%
MAX268ACWG	0°C to +70°C	Wide SO	1%
MAX268BCWG	0°C to +70°C	Wide SO	2%
MAX268AMRG	-55°C to +125°C	CERDIP	1%
MAX268BMRG	-55°C to +125°C	CERDIP	2%

* *MAX263/264 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" wide SO (Small Outline).*

MAX267/268 packages are 24-pin 0.3" narrow DIP and 24-pin 0.3" wide SO (Small Outline).

Chip Topography

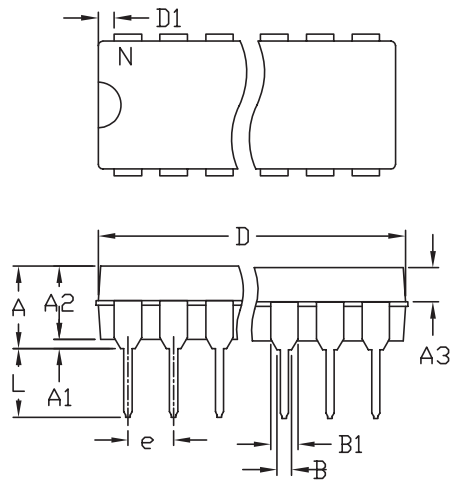


NOTE: LABELS IN PARENTHESES ( ) ARE FOR MAX 267/268 ONLY

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

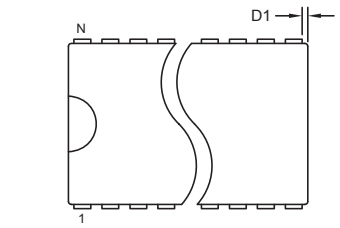
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

PROPRIETARY INFORMATION	TITLE		DOCUMENT CONTROL NUMBER	REV
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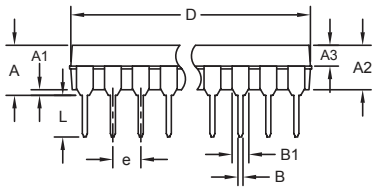
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(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

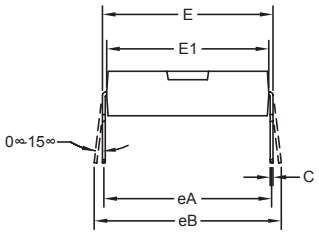
PDIPW.EPS



TOP VIEW



FRONT VIEW



SIDE VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.200	-	5.08
A1	0.015	-	0.39	-
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.21	0.30
D1	0.005	0.009	0.13	0.22
E	0.600	0.625	15.24	15.87
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC	
eB	-	0.700	-	17.78
L	0.120	0.150	3.05	3.81

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS011
D	1.230	1.270	31.24	32.26	24	AA
D	1.430	1.470	36.32	37.34	28	AB
D	2.025	2.075	51.44	52.71	40	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MS011.
5. N = NUMBER OF PINS.

PROPRIETARY INFORMATION

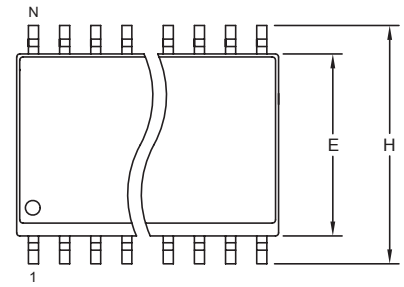
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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICW.EPS

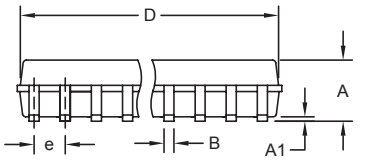


TOP VIEW

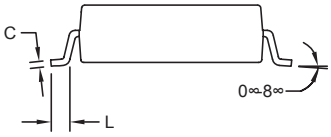
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

PROPRIETARY INFORMATION

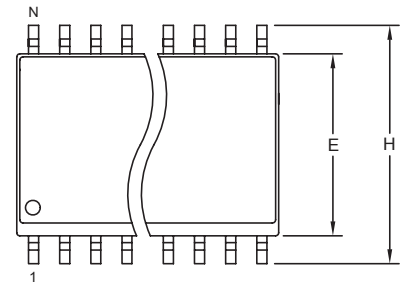
TITLE: PACKAGE OUTLINE, .300" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0042	B	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICW.EPS

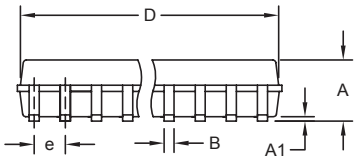


TOP VIEW

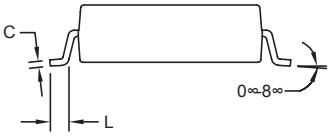
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

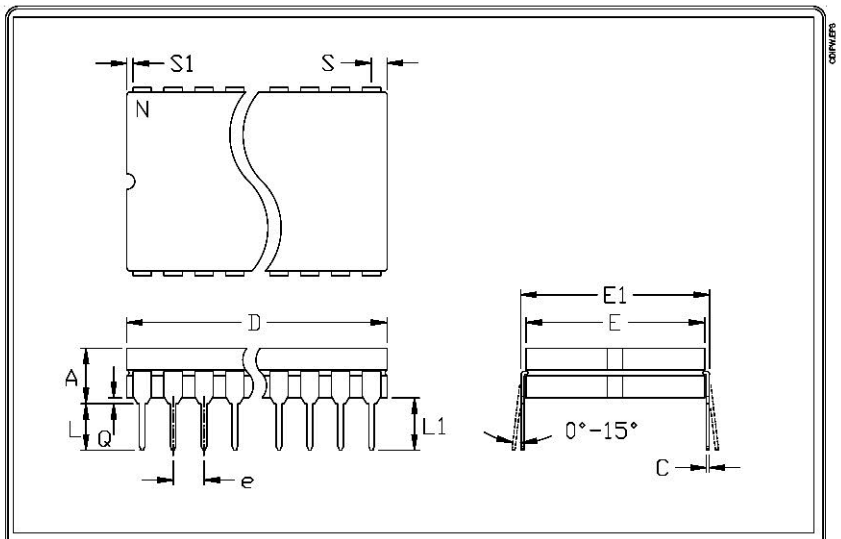
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .300" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0042	B	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.232	---	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.500	0.620	12.70	15.75
E1	0.590	0.630	14.99	16.00
e	0.100		2.54	
L	0.120	0.200	3.05	5.08
L1	0.150	---	3.81	---
Q	0.015	0.075	0.38	1.91
S	---	0.100	---	2.54
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	1.290	---	32.77	24	J:D3
D	---	1.490	---	37.85	28	D10
D	---	2.096	---	53.24	40	Q:D5

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: CDIP .600" | 1/1 | 21-0046 A | DOCUMENT CONTROL NUMBER | REV

Pin Programmable Universal and Bandwidth Filters

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	12/07	Removed information related to available design software	1, 6, 7, 24

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