19-0393; Rev 1; 9/02

MAXIM

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

General Description

The MAX517/MAX518/MAX519 are 8-bit voltage output digital-to-analog converters (DACs) with a simple 2-wire serial interface that allows communication between multiple devices. They operate from a single 5V supply and their internal precision buffers allow the DAC outputs to swing rail-to-rail.

The MAX517 is a single DAC and the MAX518/MAX519 are dual DACs. The MAX518 uses the supply voltage as the reference for both DACs. The MAX517 has a reference input for its single DAC and each of the MAX519's two DACs has its own reference input.

The MAX517/MAX518/MAX519 feature a serial interface and internal software protocol, allowing communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers of the dual devices to be updated individually or simultaneously. In addition, the devices can be put into a low-power shutdown mode that reduces supply current to 4µA. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

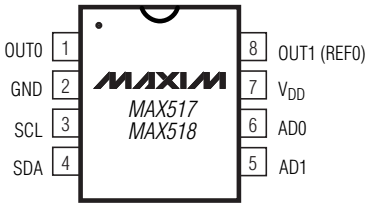
The MAX517/MAX518 are available in space-saving 8-pin DIP and SO packages. The MAX519 comes in 16-pin DIP and SO packages.

Applications

Minimum Component Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

Pin Configurations

TOP VIEW



DIP/SO

( ) ARE FOR MAX517

Pin Configurations continued at end of data sheet.

Features

- **Single +5V Supply**
- **Simple 2-Wire Serial Interface**
- **I²C Compatible**
- **Output Buffer Amplifiers Swing Rail-to-Rail**
- **Space-Saving 8-pin DIP/SO Packages (MAX517/MAX518)**
- **Reference Input Range Includes Both Supply Rails (MAX517/MAX519)**
- **Power-On Reset Clears All Latches**
- **4µA Power-Down Mode**

Ordering Information

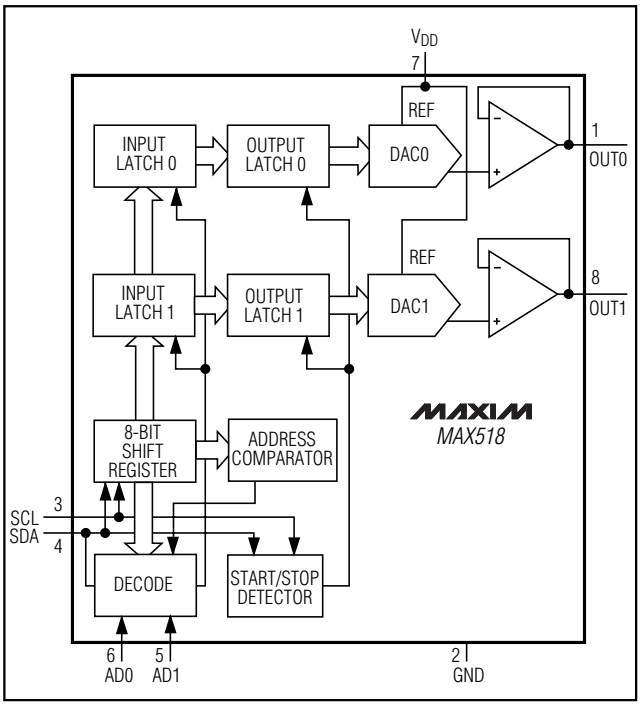
PART	TEMP RANGE	PIN-PACKAGE	TUE (LSB)
MAX517ACPA	0°C to +70°C	8 Plastic DIP	1
MAX517BCPA	0°C to +70°C	8 Plastic DIP	1.5
MAX517ACSA	0°C to +70°C	8 SO	1
MAX517BCSA	0°C to +70°C	8 SO	1.5
MAX517BC/D	0°C to +70°C	Dice*	1.5

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
OUT_ .....-0.3V to (V_{DD} + 0.3V)
REF_ (MAX517, MAX519).....-0.3V to (V_{DD} + 0.3V)
AD_.....-0.3V to (V_{DD} + 0.3V)
SCL, SDA to GND.....-0.3V to +6V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)..842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX51_C_ _ .....0°C to +70°C
MAX51_E_ _.....-40°C to +85°C
MAX51_MJB .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V (MAX517, MAX519), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error (Note 1)	TUE		MAX51 _A			±1	LSB
			MAX51 _B			±1.5	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic				±1	LSB
Zero-Code Error	ZCE	Code = 00 hex	MAX51 _C			18	mV
			MAX51 _E			20	
			MAX51 _BM			20	
Zero-Code-Error Supply Rejection		Code = 00 hex	MAX51 _C		±1		mV
			MAX51 _E		±1		
			MAX51 _BM		±1		
Zero-Code-Error Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex, MAX518 unloaded	MAX51 _C			±18	mV
			MAX51 _E			±20	
			MAX51 _BM			±20	
Full-Scale-Error Supply Rejection		MAX517, MAX519 Code = FF hex V_{DD} = +5V ±10%	MAX51 _C		±1		mV
			MAX51 _E		±1		
			MAX51 _BM		±1		
Full-Scale-Error Temperature Coefficient		Code = FF hex			±10		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V (MAX517, MAX519), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUTS (MAX517, MAX519)							
Input Voltage Range				0		V_{DD}	V
Input Resistance	R_{IN}	Code = 55 hex (Note 2)		16	24		kΩ
Input Current		Power-down mode				±10	µA
Input Capacitance		Code = FF hex (Note 3)			30		pF
Channel-to-Channel Isolation (MAX519)		(Note 4)			-60		dB
AC Feedthrough		(Note 5)			-70		dB
DAC OUTPUTS							
Full-Scale Output Voltage				0		V_{DD}	V
Output Load Regulation		OUT_ = 4V, 0mA to 2.5mA			0.25		LSB
		MAX51 _C/E, REF_ = V_{DD} (MAX517, MAX519), code = FF hex, 0µA to 500µA			1.5		
		MAX51 _M, REF_ = V_{DD} (MAX517, MAX519), code = FF hex, 0µA to 500µA			2.0		
Output Leakage Current		OUT_ = 0V to V_{DD}, power-down mode				±10	µA
DIGITAL INPUTS SCL, SDA							
Input High Voltage	V_{IH}			0.7V_{DD}			V
Input Low Voltage	V_{IL}					0.3V_{DD}	V
Input Leakage Current	I_{IN}	0V ≤ V_{IN} ≤ V_{DD}				±10	µA
Input Hysteresis	V_{HYST}			0.05V_{DD}			V
Input Capacitance	C_{IN}	(Note 6)				10	pF
DIGITAL INPUTS AD0, AD1, AD2, AD3							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}				±10	µA
DIGITAL OUTPUT SDA (Note 7)							
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
		I_{SINK} = 6mA				0.6	
Three-State Leakage Current	I_L	V_{IN} = 0V to V_{DD}				±10	µA
Three-State Output Capacitance	C_{OUT}	(Note 6)				10	pF
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		Positive and negative	MAX51 _C		2.0		V/µs
			MAX51 _E		1.4		
			MAX51 _M		1.0		
Output Settling Time		To 1/2 LSB, 10kΩ and 100pF load (Note 8)			6		µs
Digital Feedthrough		Code = 00 hex, all digital inputs from 0V to V_{DD}			5		nV-s

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V (MAX517, MAX519), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital-Analog Glitch Impulse		Code 128 to 127			12		nV-s
Signal to Noise + Distortion Ratio (MAX517, MAX519)	SINAD	$V_{REF_}$ = 4Vp-p at 1kHz, V_{DD} = 5V, Code = FF hex			87		dB
Multiplying Bandwidth (MAX517, MAX519)		$V_{REF_}$ = 4Vp-p, 3dB bandwidth			1		MHz
Wideband Amplifier Noise					60		μV_{RMS}
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.5		5.5	V
Supply Current	I_{DD}	Normal mode, output(s) unloaded, all digital inputs at 0V or V_{DD}	MAX517C		1.5	3.0	mA
			MAX517E/M		1.5	3.5	
			MAX518C, MAX519C		2.5	5	
			MAX518E/M, MAX519E/M		2.5	6	
		Power-down mode			4	20	µA

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

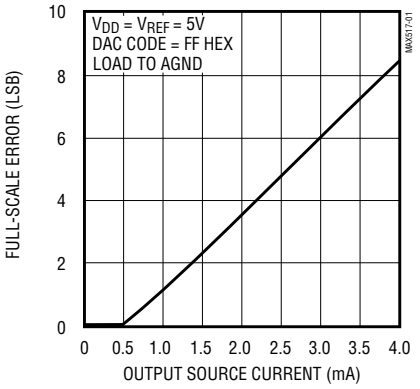
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) Start Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 9)	0		0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 10)	20 + 0.1Cb		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Note 10)	20 + 0.1Cb		300	ns
Fall Time of SDA Transmitting	t_F	I_{SINK} ≤ 6mA (Notes 7, 10)	20 + 0.1Cb		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	Cb				400	pF
Pulse Width of Spike Suppressed	t_{SP}	(Notes 6, 11)	0		50	ns

Note 1: For the MAX518 (full-scale = V_{DD}) the last three codes are excluded from the TUE and DNL specifications, due to the limited output swing when loaded with 10kΩ to GND.
Note 2: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
Note 3: Input capacitance is code dependent. The highest input capacitance occurs at code FF hex.
Note 4: $V_{REF_}$ = $4V_{P-P}$, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
Note 5: $V_{REF_}$ = 4Vp-p, 10kHz, DAC code = 00 hex.
Note 6: Guaranteed by design.
Note 7: I^2C compatible mode. R_{PULLUP} = 1.7kΩ.
Note 8: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.
Note 9: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 10: Cb = total capacitance of one bus line in pF. t_R and t_F measured between $0.3V_{DD}$ and $0.7V_{DD}$.
Note 11: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

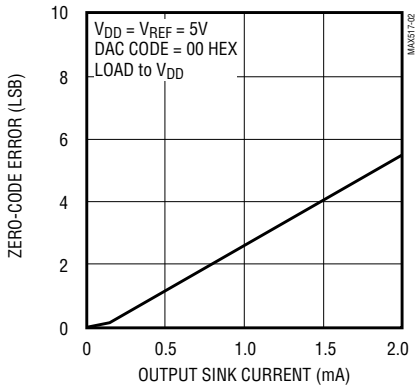
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

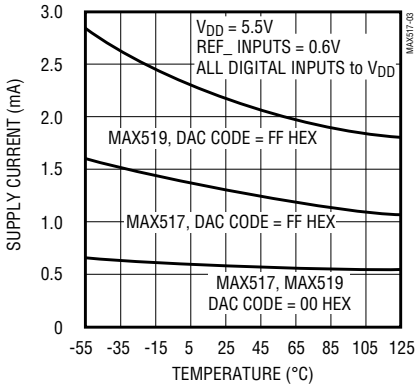
FULL-SCALE ERROR vs. SOURCE CURRENT (V_{REF} = V_{DD})



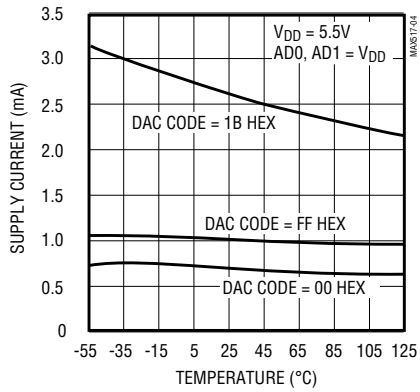
ZERO-CODE ERROR vs. SINK CURRENT



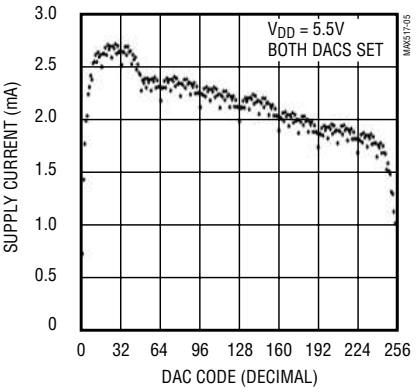
MAX517/MAX519 SUPPLY CURRENT vs. TEMPERATURE



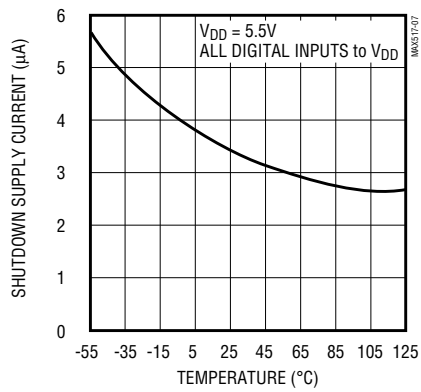
MAX518 SUPPLY CURRENT vs. TEMPERATURE



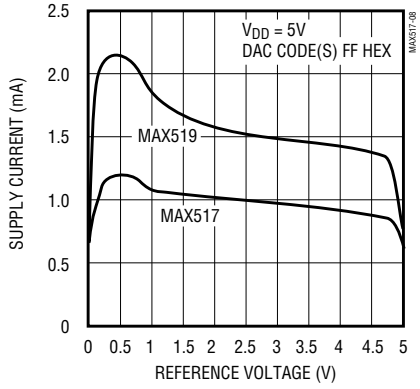
MAX518 SUPPLY CURRENT vs. DAC CODE



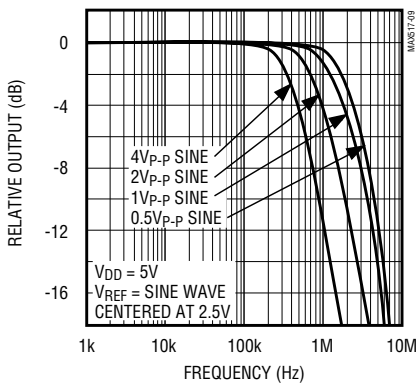
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



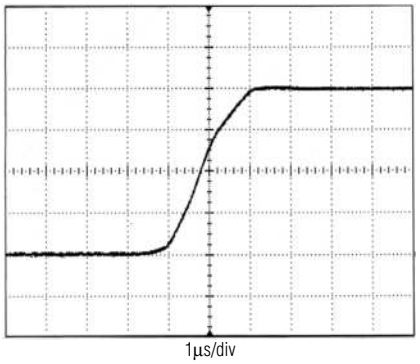
MAX517/MAX519 SUPPLY CURRENT vs. REFERENCE VOLTAGE



MAX517/MAX519 REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



POSITIVE FULL-SCALE STEP RESPONSE



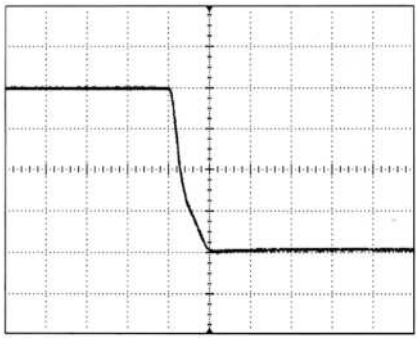
OUT0 LOADED WITH 10kΩ II 100pF
REF0 = 4V (MAX517/MAX519)
DAC CODE = 00 HEX to FF HEX

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

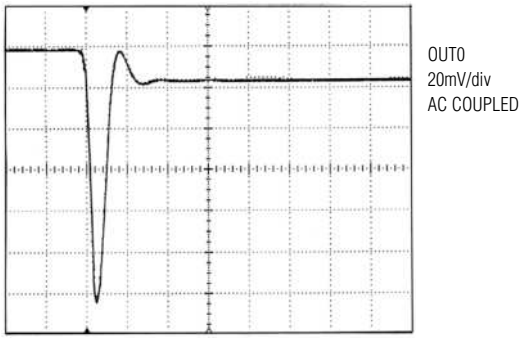
(T_A = +25°C, unless otherwise noted.)

NEGATIVE FULL-SCALE STEP RESPONSE



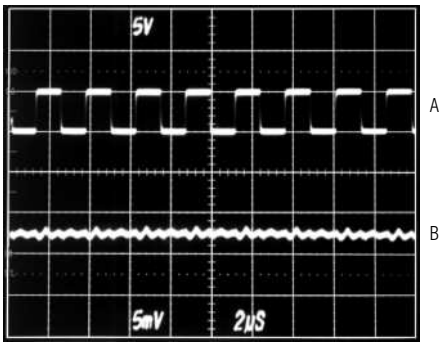
OUT0 LOADED WITH 10kΩ II 100pF
REF0 = 4V (MAX517/MAX519)
DAC CODE = FF HEX to 00 HEX

WORST-CASE 1LSB STEP CHANGE



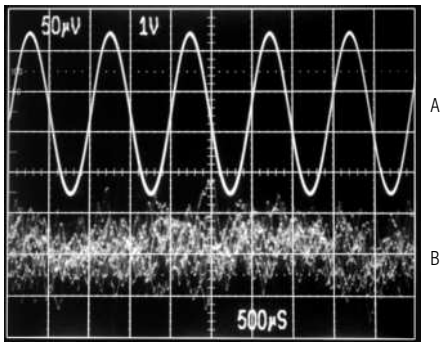
REF0 = 5V (MAX517/MAX519)
DAC CODE = 80 HEX to 7F HEX

CLOCK FEEDTHROUGH



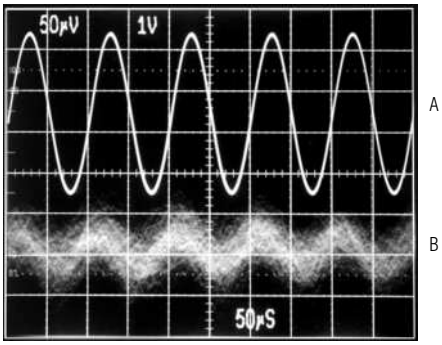
A = SCL, 400kHz, 5V/div
B = OUT0, 5mV/div
DAC CODE = 7F HEX
REF0 = 5V (MAX517/MAX519)

MAX517/MAX519
REFERENCE FEEDTHROUGH AT 1kHz



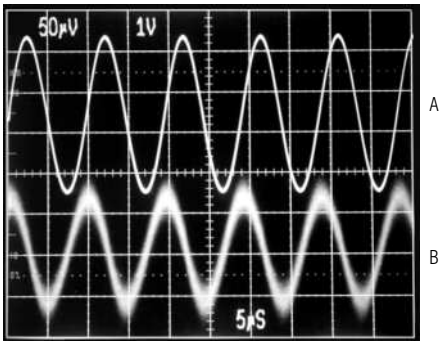
A = REF0, 1V/div ($4V_{P-P}$)
B = OUT0, 50µV/div, UNLOADED
FILTER PASSBAND = 100Hz to 10kHz
DAC CODE = 00 HEX

MAX517/MAX519
REFERENCE FEEDTHROUGH AT 10kHz



A = REF0, 1V/div ($4V_{P-P}$)
B = OUT0, 50µV/div, UNLOADED
FILTER PASSBAND = 1kHz to 100kHz
DAC CODE = 00 HEX

MAX517/MAX519
REFERENCE FEEDTHROUGH AT 100kHz



A = REF0, 1V/div ($4V_{P-P}$)
B = OUT0, 50µV/div, UNLOADED
FILTER PASSBAND = 10kHz to 1MHz
DAC CODE = 00 HEX

Pin Description

PIN			NAME	FUNCTION
MAX517	MAX518	MAX519		
1	1	1	OUT0	DAC0 Voltage Output
2	2	4	GND	Ground
—	—	5	AD3	Address Input 3; sets IC's slave address
3	3	6	SCL	Serial Clock Input
4	4	8	SDA	Serial Data Input
—	—	9	AD2	Address Input 2; sets IC's slave address
5	5	10	AD1	Address Input 1; sets IC's slave address
6	6	11	AD0	Address Input 0; sets IC's slave address
7	7	12	VDD	Power Supply, +5V; used as reference for MAX518
—	—	13	REF1	Reference Voltage Input for DAC1
8	—	15	REF0	Reference Voltage Input for DAC0
—	8	16	OUT1	DAC1 Voltage Output
—	—	2, 3, 7, 14	N.C.	No Connect—not internally connected.

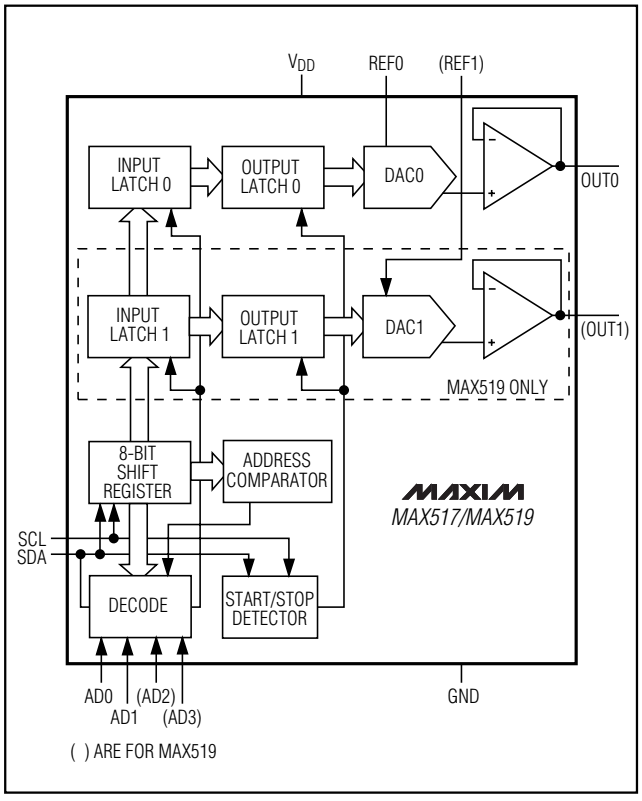


Figure 1. MAX517/MAX519 Functional Diagram

Detailed Description

Serial Interface

The MAX517/MAX518/MAX519 use a simple 2-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor (µP) port. Figure 2 shows the timing diagram for signals on the 2-wire bus. Figure 3 shows a typical application. The 2-wire bus can have several devices (in addition to the MAX517/MAX518/MAX519) attached. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. External pull-up resistors are not required on these lines. The MAX517/MAX518/MAX519 can be used in applications where pull-up resistors are required (such as in I^2C systems) to maintain compatibility with existing circuitry.

The MAX517/MAX518/MAX519 are receive-only devices and must be controlled by a bus master device. They operate at SCL rates up to 400kHz. A master device sends information to the devices by transmitting their address over the bus and then transmitting the desired information. Each transmission consists of a START condition, the MAX517/MAX518/MAX519's programmable slave-address, one or more command-byte/output-byte pairs (or a command byte alone, if it is the last byte in the transmission), and finally, a STOP condition (Figure 4).

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

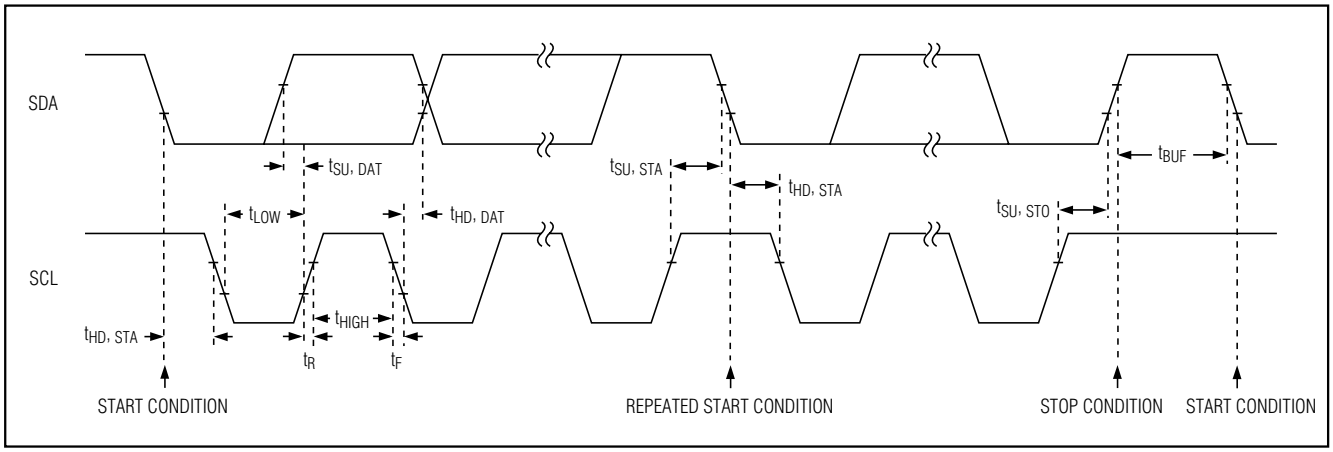


Figure 2. Two-Wire Serial Interface Timing Diagram

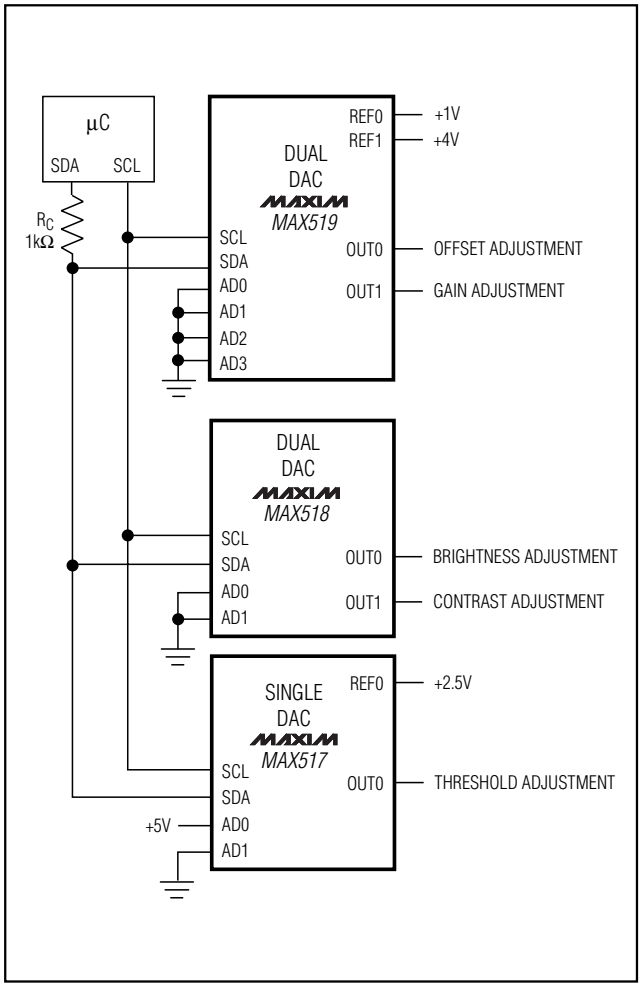


Figure 3. MAX517/MAX518/MAX519 Application Circuit

The address byte and pairs of command and output bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, with the exception of START and STOP conditions. SDA's state is sampled, and therefore must remain stable while SCL is high. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer the data bits to the MAX517/MAX518/MAX519. Set SDA low during the 9th clock cycle as the MAX517/MAX518/MAX519 pull SDA low during this time. R_C (see Figure 3) limits the current that flows during this time if SDA stays high for short periods of time.

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 5). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

The Slave Address

The MAX517/MAX518/MAX519 each have a 7-bit long slave address (Figure 6). The first three bits (MSBs) of the slave address have been factory programmed and are always 010. In addition, the MAX517 and MAX518 have the next two bits factory programmed to 1s. The logic state of the address inputs (AD0 and AD1 on the MAX517/MAX518; AD0, AD1, AD2, and AD3 on the MAX519) determine the LSB bits of the 7-bit slave address. These input pins may be connected to VDD or DGND, or they may be actively driven by TTL or CMOS logic levels. The MAX517/MAX518 have four possible slave addresses and therefore a maximum of four of

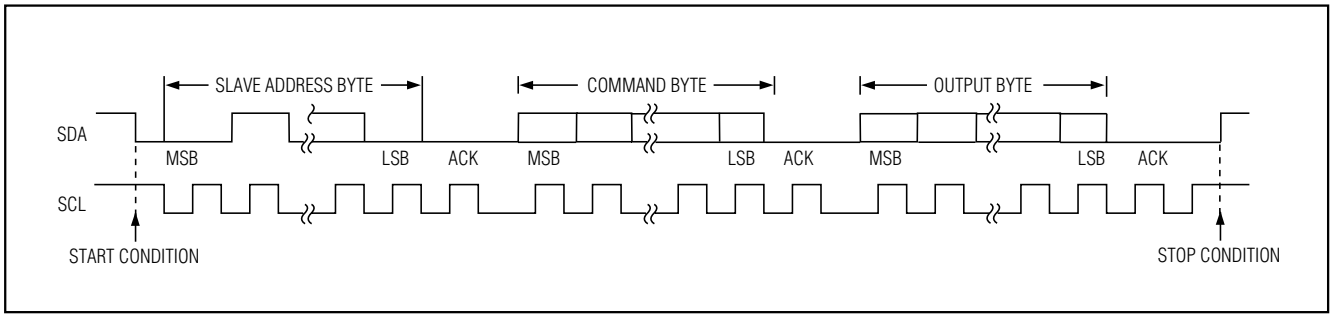


Figure 4. A Complete Serial Transmission

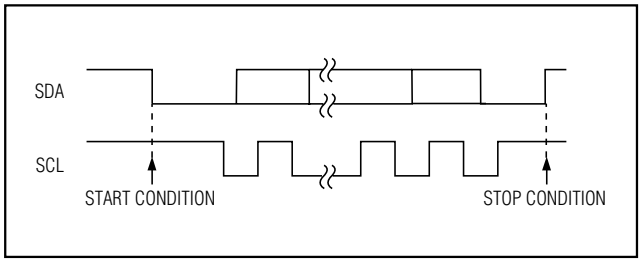


Figure 5. All communications begin with a START condition and end with a STOP condition, both generated by a bus master.

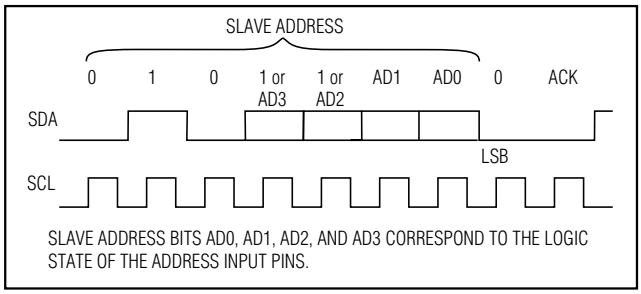


Figure 6. Address Byte

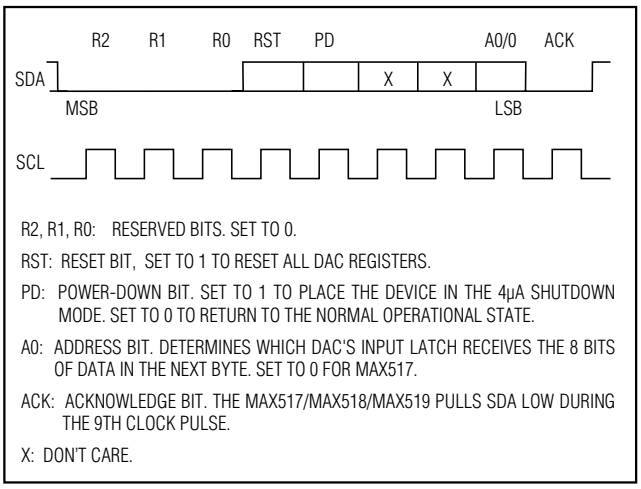


Figure 7. Command Byte

these devices may share the bus. The MAX519 has 16 possible slave addresses. The eighth bit (LSB) in the slave address byte should be low when writing to the MAX517/MAX518/MAX519.

The MAX517/MAX518/MAX519 monitor the bus continuously, waiting for a START condition followed by their slave address. When a device recognizes its slave address, it is ready to accept data.

The Command Byte and Output Byte

A command byte follows the slave address. Figure 7 shows the format for the command byte. A command byte is usually followed by an output byte unless it is the last byte in the transmission. If it is the last byte, all bits except PD (power-down) and RST (reset) are ignored. If an output byte follows the command byte, A0 of the command byte indicates the digital address of the DAC whose input data latch receives the digital output data. Set this bit to 0 when writing to the MAX517. The data is transferred to the DAC's output latch during the STOP condition following the transmission. This allows both DACs of the MAX518/MAX519 to be updated simultaneously (Figure 8).

Setting the PD bit high powers down the MAX517/MAX518/MAX519 following a STOP condition (Figure 9a). If a command byte with PD set high is followed by an output byte, the addressed DAC's input latch will be updated and the data will be transferred to the DAC's output latch following the STOP condition (Figure 9b).

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

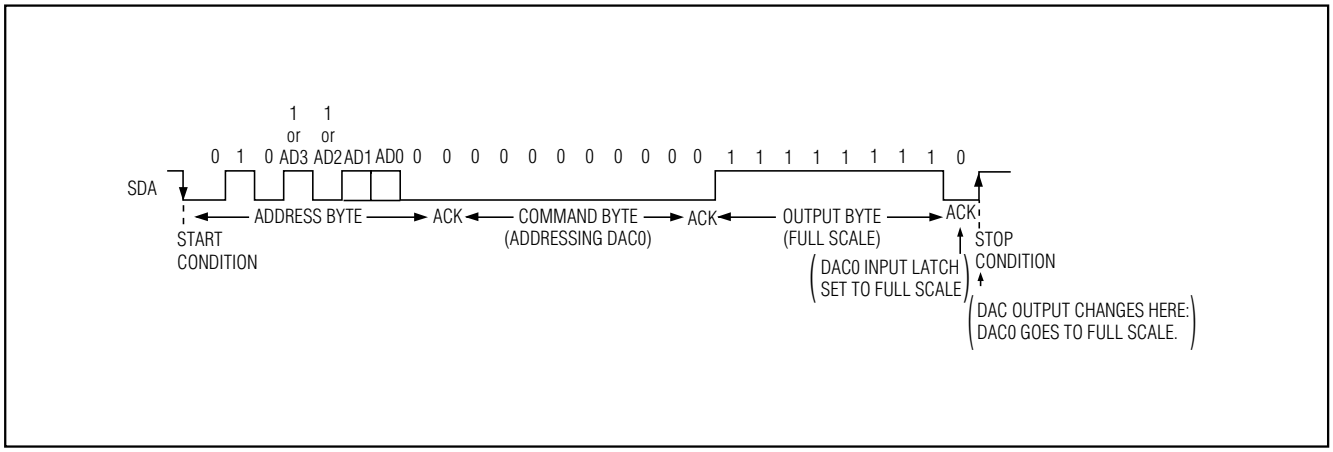


Figure 8a. Setting One DAC Output (MAX517/MAX518/MAX519)

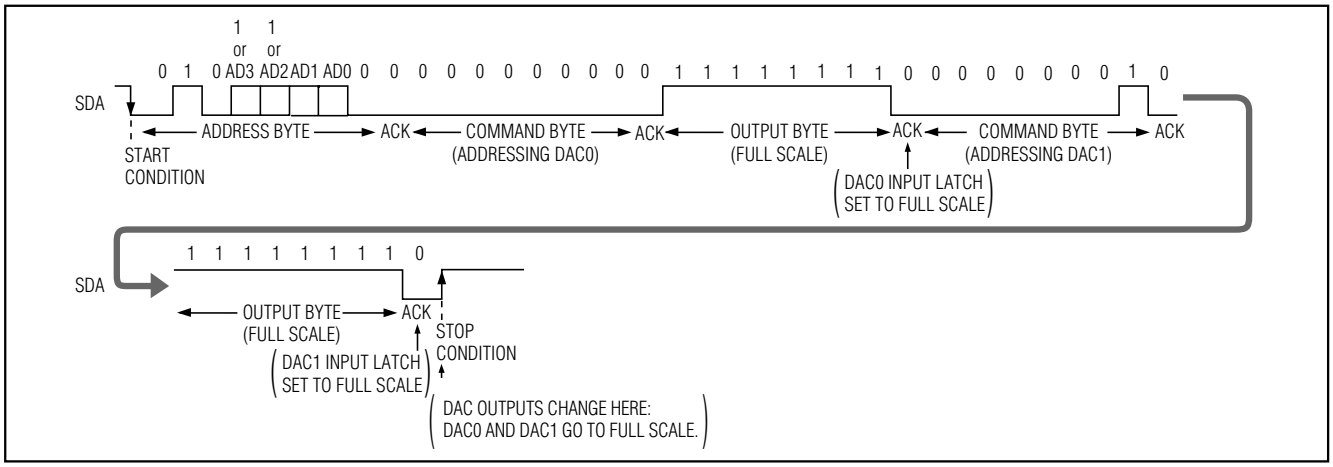


Figure 8b. Setting Both DAC Outputs (MAX518/MAX519)

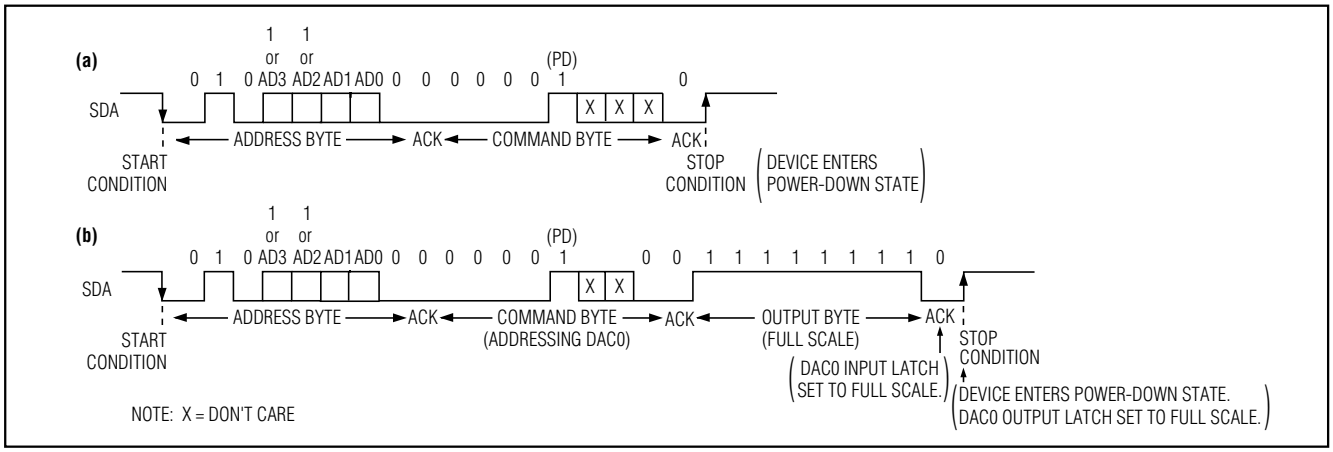


Figure 9. Entering the Power-Down State

Furthermore if the transmission's last command byte has PD high, the output latches are updated, but voltage outputs will not reflect the newly entered data because the DAC enters power-down mode when the STOP condition is detected. When in power-down, the DAC outputs float. In this mode, the supply current is a maximum of 20µA. A command byte with the PD bit low returns the MAX517/MAX518/MAX519 to normal operation following a STOP condition, with the voltage outputs reflecting the output-latch contents (Figures 10a and 10b). Because each subsequent command byte overwrites the previous PD bit, only the last command byte of a transmission affects the power-down state.

Setting the RST bit high clears the DAC input latches. The DAC outputs remain unchanged until a STOP condition is detected (Figure 11a). If a reset is issued, the following output byte is ignored. Subsequent pairs of command/output bytes overwrite the input latches (Figure 11b).

All changes made during a transmission affect the MAX517/MAX518/MAX519's outputs only when the transmission ends and a STOP has been recognized.

The R0, R1, and R2 bits are reserved and must be set to zero.

I²C Compatibility

The MAX517/MAX518/MAX519 are fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the 9th clock pulse. Figure 12 shows a typical I²C application.

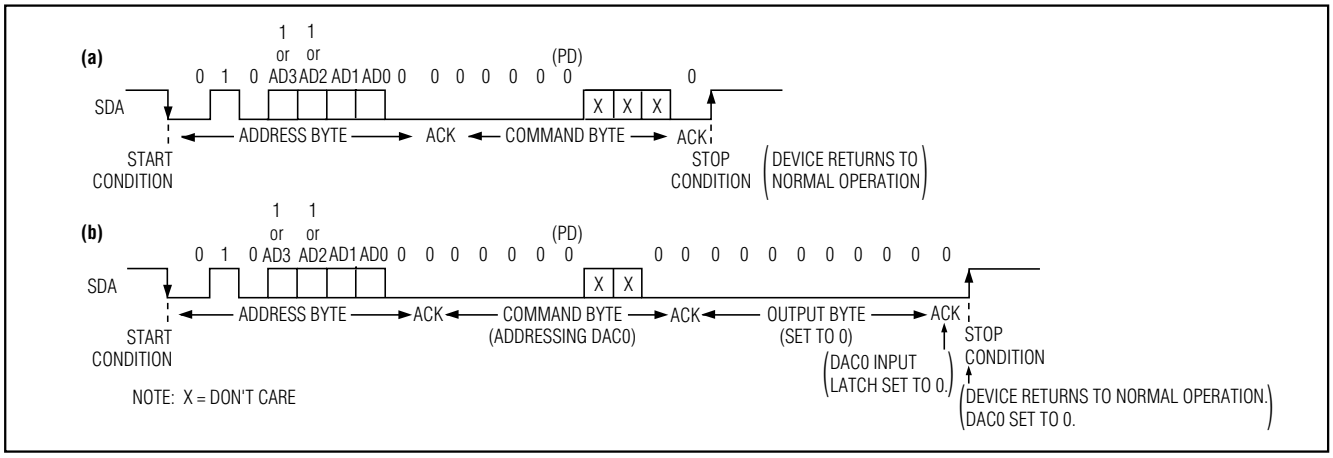


Figure 10. Returning to Normal Operation from Power-Down

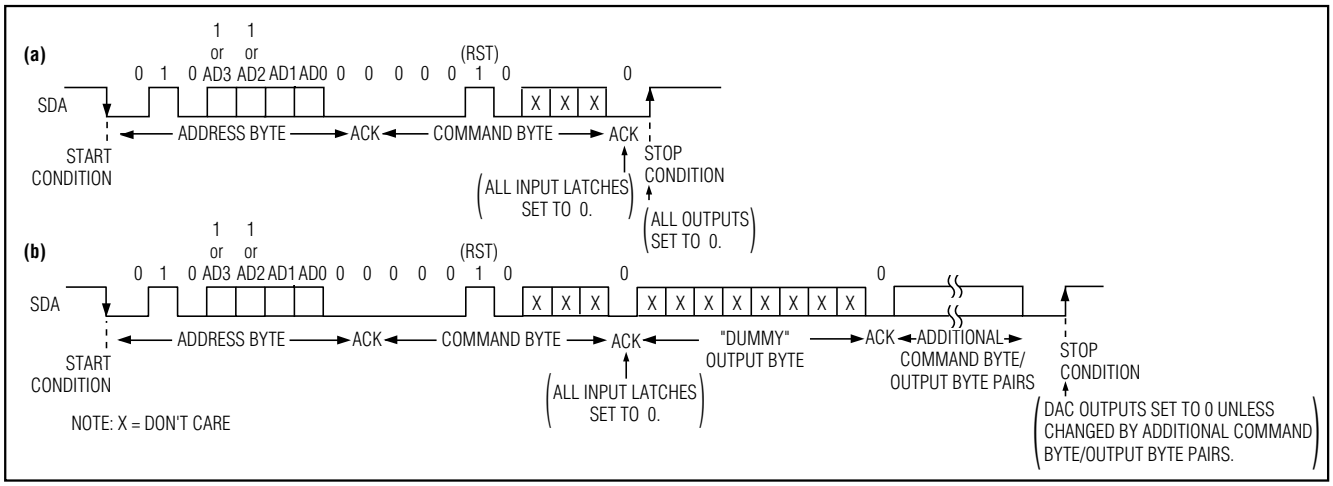


Figure 11. Resetting DAC Outputs

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

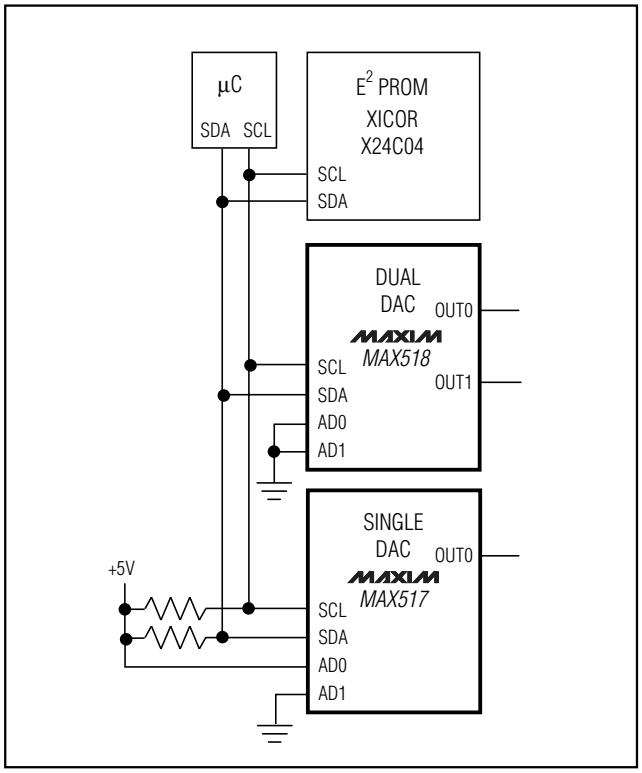


Figure 12. MAX517/MAX518/MAX519 Used in a Typical I²C Application Circuit

Additional START Conditions

It is possible to interrupt a transmission to a device with a new START (repeated start) condition (perhaps addressing another device), which leaves the input latches with data that has not been transferred to the output latches (Figure 13). Only the currently addressed device will recognize a STOP condition and transfer data to its output latches. If the device is left with data in its input latches, the data can be transferred to the output latches the next time the device is addressed, as long as it receives at least one command byte and a STOP condition.

Early STOP Conditions

The addressed device recognizes a STOP condition at any point in a transmission. If the STOP occurs during a command byte, all previous uninterrupted command and output byte pairs are accepted, the interrupted command byte is ignored, and the transmission ends (Figure 14a). If the STOP occurs during an output byte, all previous uninterrupted command and output byte pairs are accepted, the final command byte's PD and RST bits are accepted, the interrupted output byte is ignored, and the transmission ends (Figure 14b).

Analog Section

DAC Operation

The MAX518 and MAX519 contain two matched voltage-output DACs. The MAX517 contains a single DAC. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. The MAX518 has both DAC's reference inputs connected to V_{DD}. Figure 15 shows a simplified diagram of one DAC.

MAX517/MAX519 Reference Inputs

The MAX517 and MAX519 can be used for multiplying applications. The reference accepts a 0V to V_{DD} volt-

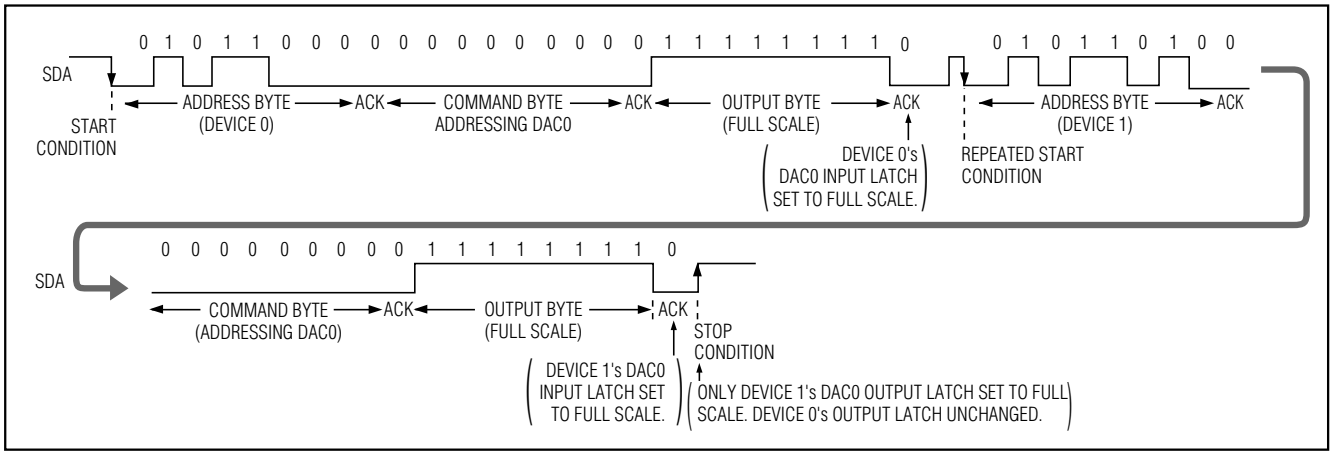


Figure 13. Repeated START Conditions

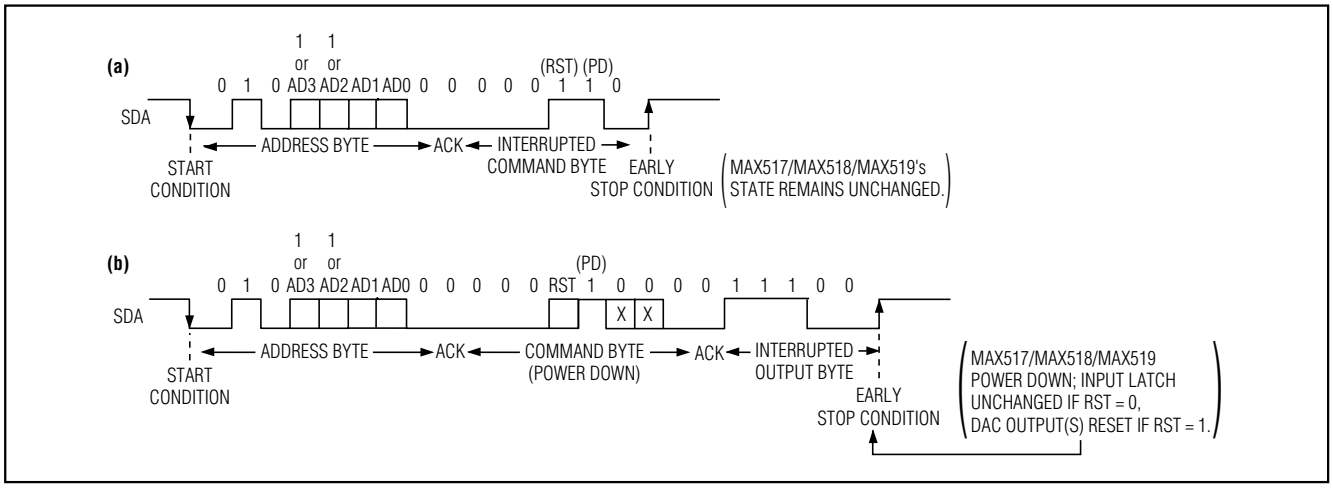


Figure 14. Early STOP Conditions

Table 1. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
11111111	$+ V_{REF}\left(\frac{255}{256}\right)$
10000001	$+ V_{REF}\left(\frac{129}{256}\right)$
10000000	$+ V_{REF}\left(\frac{128}{256}\right) = \frac{V_{REF}}{2}$
01111111	$+ V_{REF}\left(\frac{127}{256}\right)$
00000001	$+ V_{REF}\left(\frac{1}{256}\right)$
00000000	0V

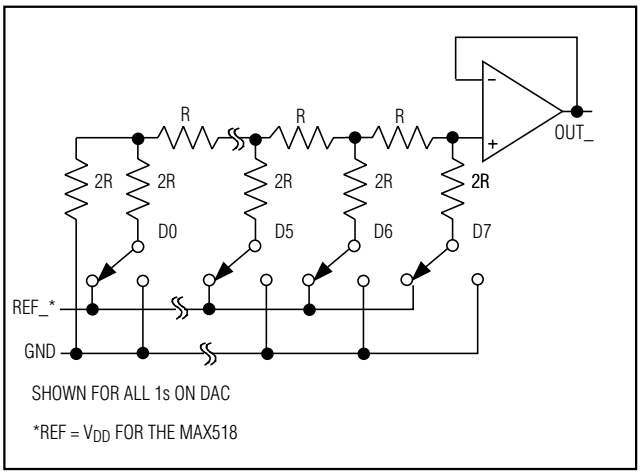


Figure 15. DAC Simplified Circuit Diagram

age, both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC. The reference voltage must be positive. The DAC's input impedance is code dependent, with the lowest value occurring when the input code is 55 hex or 0101 0101, and the maximum value occurring when the input code is 00 hex. Since the REF input resistance (RIN) is code dependent, it must be driven by a circuit with low output impedance (no more than RIN ÷ 2000) to maintain output linearity. The REF input capacitance is also code dependent, with the maximum value occurring at code FF hex (typically 30pF). The output voltage for any DAC can be represented by a digitally programmable voltage source as: $V_{OUT} = (N \times V_{REF}) / 256$, where N is the numerical value of the DAC's binary input code.

Output Buffer Amplifiers

The DAC voltage outputs are internally buffered precision unity-gain followers that slew up to 1V/µs. The outputs can swing from 0V to V_{DD}. With a 0V to 4V (or 4V to 0V) output transition, the amplifier outputs typically settle to 1/2LSB in 6µs when loaded with 10kΩ in parallel with 100pF. The buffer amplifiers are stable with any combination of resistive loads ≥2kΩ and capacitive loads ≤300pF.

The MAX517/MAX518/MAX519 are designed for unipolar-output, single-quadrant multiplication where the output voltages and the reference inputs are positive with respect to AGND. Table 1 shows the unipolar code.

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

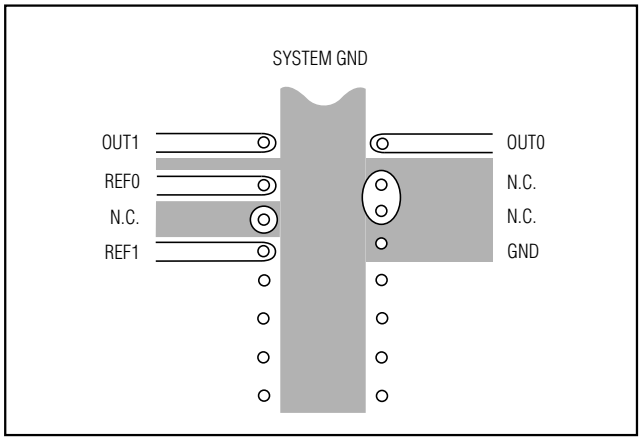


Figure 16. PC Board Layout for Minimizing MAX519 Crosstalk (bottom view)

Applications Information

Power-Supply Bypassing and Ground Management

Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and GND as possible. Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figure 16 shows the suggested PC board layout to minimize crosstalk.

When using the MAX518 (or the MAX517/MAX519 with V_{DD} as the reference), you may want to add a noise filter to the V_{DD} supply (Figure 17) or to the reference input(s) (Figure 18), especially in noisy environments. The reference input's bandwidth exceeds 1MHz for AC signals, so disturbances on the reference input can easily affect the DAC output(s).

The maximum input current for a single reference input is $V_{REF}/16k\Omega = I_{REF}$ (max). In Figure 17, choose R_F so that changes in the reference input current will have little effect on the reference voltage. For example, with $R_F = 6\Omega$, the maximum output error due to R_F is given by:

$$6\Omega \times I_{REF} \text{ (max)} = 1.9mV \text{ or } 0.1LSB$$

In Figure 18, there is a voltage drop across R_F that adds to the TUE. This voltage drop is due to the sum of the reference input current ($V_{REF}/16k\Omega$ maximum), supply current (6mA maximum), and the amplifier output current (V_{REF}/R_{LOAD}). Choose R_F to limit this voltage drop to an acceptable value. For example, with a 10kΩ load, you can limit the error due to R_F to 0.5LSB (9.8mV) by selecting R_F so that:

$$R_F = V_{R_F} / I_{R_F} \le 9.8mV / (5V / 16k\Omega + 6mA + 5V / 10k\Omega)$$

$$R_F \le 1.4\Omega$$

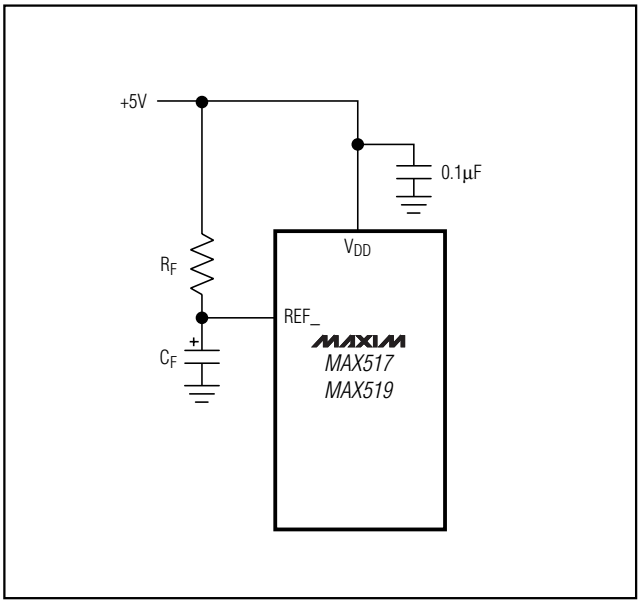


Figure 17. Reference Filter When Using V_{DD} as a Reference

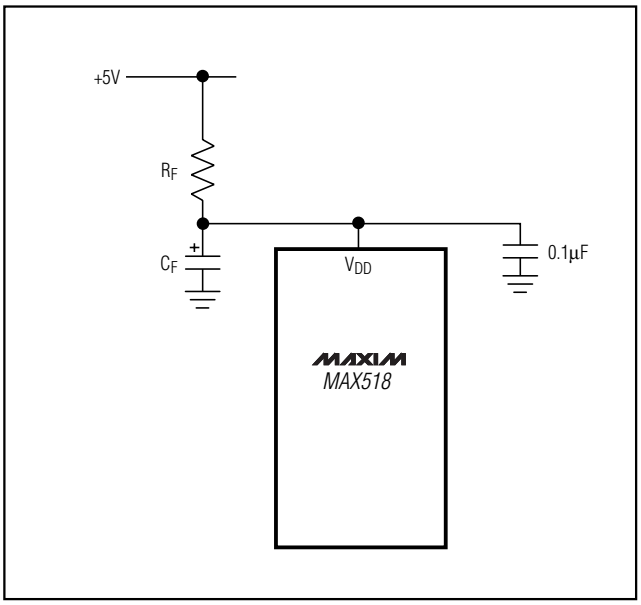
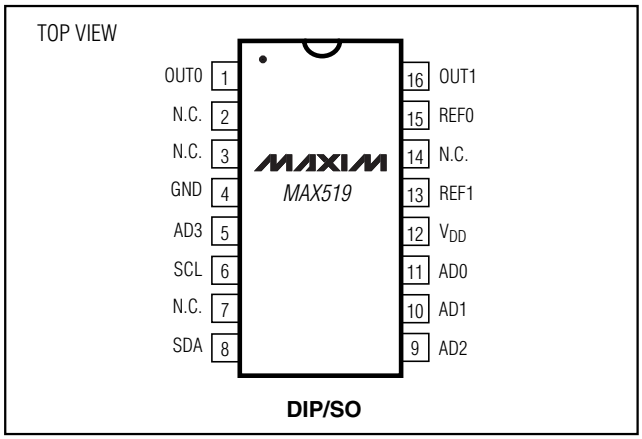
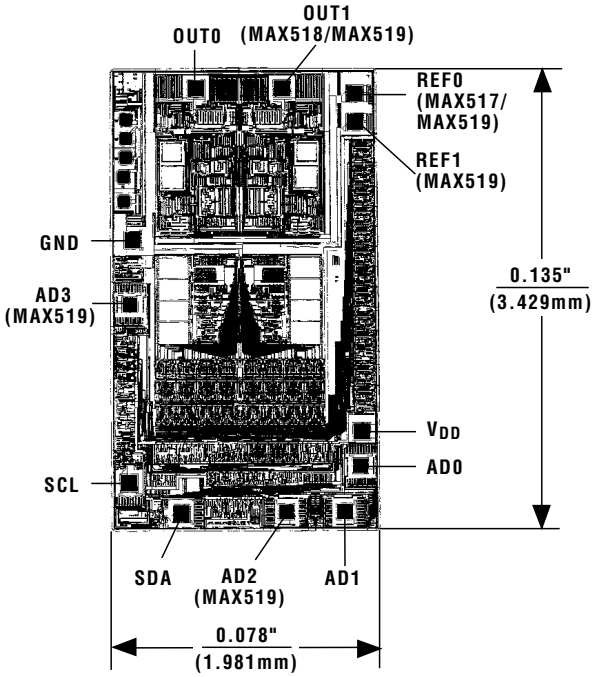


Figure 18. V_{DD} Filter When Using V_{DD} as a Reference

Pin Configurations (continued)



Chip Topography



TRANSISTOR COUNT: 1797
SUBSTRATE CONNECTED TO V_{DD}

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TUE (LSB)
MAX517AEPA	-40°C to +85°C	8 Plastic DIP	1
MAX517BEPA	-40°C to +85°C	8 Plastic DIP	1.5
MAX517AESA	-40°C to +85°C	8 SO	1
MAX517BESA	-40°C to +85°C	8 SO	1.5
MAX517BMJA	-55°C to +125°C	8 CERDIP**	1.5
MAX518ACPA	0°C to +70°C	8 Plastic DIP	1
MAX518BCPA	0°C to +70°C	8 Plastic DIP	1.5
MAX518ACSA	0°C to +70°C	8 SO	1
MAX518BCSA	0°C to +70°C	8 SO	1.5
MAX518BC/D	0°C to +70°C	Dice*	1.5
MAX518AEPA	-40°C to +85°C	8 Plastic DIP	1
MAX518BEPA	-40°C to +85°C	8 Plastic DIP	1.5
MAX518AESA	-40°C to +85°C	8 SO	1
MAX518BESA	-40°C to +85°C	8 SO	1.5
MAX518BMJA	-55°C to +125°C	8 CERDIP**	1.5
MAX519ACPE	0°C to +70°C	16 Plastic DIP	1
MAX519BCPE	0°C to +70°C	16 Plastic DIP	1.5
MAX519ACSE	0°C to +70°C	16 Narrow SO	1
MAX519BCSE	0°C to +70°C	16 Narrow SO	1.5
MAX519BC/D	0°C to +70°C	Dice*	1.5
MAX519AEPE	-40°C to +85°C	16 Plastic DIP	1
MAX519BEPE	-40°C to +85°C	16 Plastic DIP	1.5
MAX519AESE	-40°C to +85°C	16 Narrow SO	1
MAX519BESE	-40°C to +85°C	16 Narrow SO	1.5
MAX519BMJE	-55°C to +125°C	16 CERDIP**	1.5

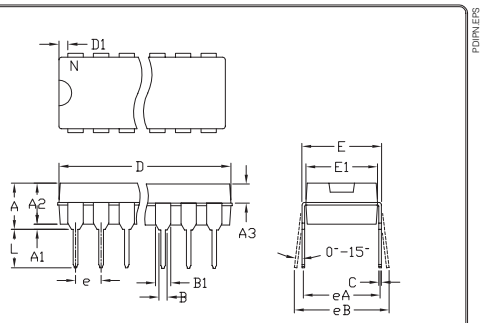
*Dice are specified at T_A = +25°C, DC parameters only.
**Contact factory for availability and processing to MIL-STD-883.

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



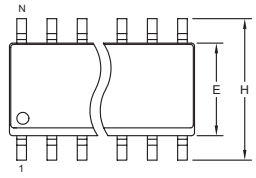
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006)
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 D (DOCUMENT CONTROL NUMBER / REV)

SOICN_EPS

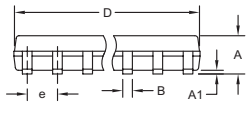


TOP VIEW

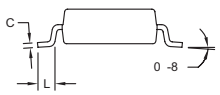
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, .150" SOIC
APPROVAL | DOCUMENT CONTROL NO. 21-0041 | REV. B | 1/1

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