19-0378; Rev 3; 9/96

MAXIM

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

General Description

The MAX520/MAX521 are quad/octal, 8-bit voltage-output digital-to-analog converters (DACs) with simple 2-wire serial interfaces that allow communication between multiple devices. They operate from a single +5V supply and their reference input range includes both supply rails.

The MAX521 includes rail-to-rail output buffer amplifiers for reduced system size and component count when driving loads. The MAX520's unbuffered voltage outputs reduce the device's total supply current to 4µA and provide increased accuracy at low output currents.

The MAX520/MAX521 feature a serial interface and internal software protocol, allowing communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers to be updated individually or simultaneously. In addition, the devices can be put into a low-power shutdown mode that reduces supply current to 4µA. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

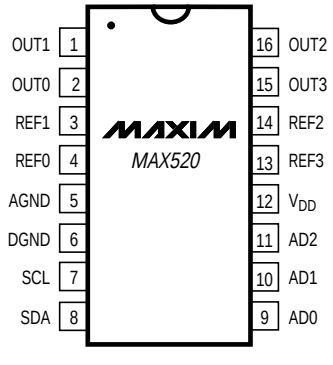
The MAX520 is available in 16-pin DIP and wide SO packages, as well as a space-saving 20-pin SSOP. The MAX521 comes in 20-pin DIP and 24-pin SO packages, as well as a space-saving 24-pin SSOP.

Applications

Minimum Component Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations continued at end of data sheet.

Features

- ♦ **Single +5V Supply**
- ♦ **Simple 2-Wire Serial Interface**
- ♦ **I²C Compatible**
- ♦ **Outputs Swing Rail to Rail:**
  Unbuffered Outputs (MAX520)
  Buffered Outputs (MAX521)
- ♦ **1%-Accurate Trimmed Output Resistance (MAX520A)**
- ♦ **Ultra-Low 4µA Supply Current (MAX520)**
- ♦ **Individual DACs Have Separate Reference Inputs**
- ♦ **Power-On Reset Clears All Latches**
- ♦ **4µA Power-Down Mode**

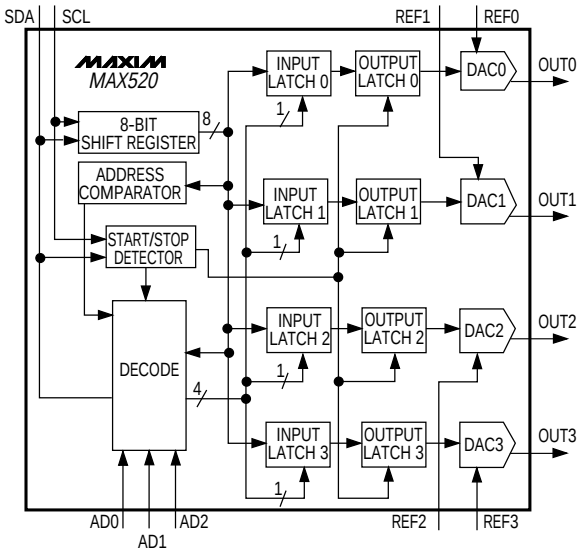
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX520ACPE	0°C to +70°C	16 Plastic DIP	1
MAX520BCPE	0°C to +70°C	16 Plastic DIP	1
MAX520ACWE	0°C to +70°C	16 Wide SO	1
MAX520BCWE	0°C to +70°C	16 Wide SO	1

Ordering Information continued at end of data sheet.

†*MAX520 "A" grade parts include a 1%-accurate, factory-trimmed output resistance.*

Functional Diagrams



Functional Diagrams continued at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V to +6V
V_{DD} to AGND.....-0.3V to +6V
OUT_ .....-0.3V to (V_{DD} + 0.3V)
REF_ .....-0.3V to (V_{DD} + 0.3V)
AD0, AD1, AD2.....-0.3V to (V_{DD} + 0.3V)
SCL, SDA to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C).....762mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C)....941mW
20-Pin SSOP (derate 8.00mW/°C above +70°C).....640mW
24-Pin SSOP (derate 8.00mW/°C above +70°C).....640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C)....800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C)....889mW
Operating Temperature Ranges
MAX520_C_ _/MAX521_C_ _.....0°C to +70°C
MAX520_E_ _/MAX521_E_ _ .....-40°C to +85°C
MAX520_MJE/MAX521BMJP .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V, R_L = ∞ (MAX520), R_L = 10kΩ (MAX521), C_L = 0pF (MAX520), C_L = 100pF (MAX521), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE		MAX520_			±1	LSB
			MAX521A			±1.5	
			MAX521B			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1.0	LSB
Zero-Code Error	ZCE	Code = 00 hex	MAX520_			8	mV
			MAX521_C			18	
			MAX521_E			20	
			MAX521BM			20	
Zero-Code-Error Supply Rejection		Code = 00 hex			±1		mV
Zero-Code-Error Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex	MAX520_			8	mV
			MAX521_C			18	
			MAX521_E			20	
			MAX521BM			20	
Full-Scale-Error Supply Rejection		Code = FF hex, V_{DD} = 5V ±10%			±1		mV
Full-Scale-Error Temperature Coefficient					±10		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V, R_L = ∞ (MAX520), R_L = 10kΩ (MAX521), C_L = 0pF (MAX520), C_L = 100pF (MAX521), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
REFERENCE INPUTS								
Input Voltage Range					0		V_{DD}	V
Input Resistance	R_{IN}	Code = 55 hex (Note 1)	MAX520_		8	12		kΩ
			MAX521_	REF4	4	6		
				REF0–REF3	16	24		
Input Current		PD = 1					±10	µA
Input Capacitance		Code = FF hex (Note 2)	MAX520_			30		pF
			MAX521_	REF4		120		
				REF0–REF3		30		
Channel-to-Channel Isolation		(Note 3)	MAX520_			-70		dB
			MAX521_			-60		
AC Feedthrough		(Note 4)				-70		dB
DAC OUTPUTS								
Full-Scale Output Voltage					0		V_{DD}	V
Output Resistance (Note 5)		MAX520A	T_A = +25°C		15.8	16	16.2	kΩ
			T_A = T_{MIN} to T_{MAX}		15.6	16	16.4	
		MAX520B			8.4		16.4	
Output Load Regulation		MAX521_, OUT_ = 4V, 0mA to 2.5mA				0.25		LSB
		MAX521_C/E, $V_{REF_}$ = V_{DD}, code = FF hex, 0µA to 500µA				1.5		
		MAX521BM, $V_{REF_}$ = V_{DD}, code = FF hex, 0µA to 500µA				2.0		
Output Leakage Current		MAX521_, OUT_ = 0V to V_{DD}, PD = 1					±10	µA
DIGITAL INPUTS SCL, SDA								
Input High Voltage	V_{IH}				0.7V_{DD}			V
Input Low Voltage	V_{IL}						0.3V_{DD}	V
Input Current	I_{IN}	0V ≤ V_{IN} ≤ V_{DD}					±10	µA
Input Hysteresis	V_{HYST}	(Note 5)			0.05V_{DD}			V
Input Capacitance	C_{IN}	(Note 5)					10	pF
DIGITAL INPUTS AD0, AD1								
Input High Voltage	V_{IH}				2.4			V
Input Low Voltage	V_{IL}						0.8	V
Input Leakage	I_{IN}	V_{IN} = 0V to V_{DD}					±10	µA
DIGITAL OUTPUT SDA (Note 6)								
Output Low Voltage	V_{OL}	I_{SINK} = 3mA					0.4	V
		I_{SINK} = 6mA					0.6	
Three-State Leakage Current	I_L	V_{IN} = 0V to V_{DD}					±10	µA
Three-State Output Capacitance	C_{OUT}	(Note 5)					10	pF

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±10%, $V_{REF_}$ = 4V, R_L = ∞ (MAX520), R_L = 10kΩ (MAX521), C_L = 0pF (MAX520), C_L = 100pF (MAX521), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		Positive and negative	MAX521_C		1.0		V/µs
			MAX521_E		0.7		
			MAX521BM		0.5		
Output Settling Time		MAX520_, to 1/2LSB, no load			2		µs
		MAX521_, to 1/2LSB, 10kΩ and 100pF load (Note 7)			6		
Digital Feedthrough		Code = 00 hex, all digital inputs from 0V to V_{DD}			5		nV-s
Digital-Analog Glitch Impulse		Code 128 to 127			12		nV-s
Signal to Noise + Distortion Ratio	SINAD	$V_{REF_}$ = 4Vp-p at 1kHz, V_{DD} = 5V, code = FF hex			87		dB
Multiplying Bandwidth		$V_{REF_}$ = 4Vp-p, 3dB bandwidth			1		MHz
Wideband Amplifier Noise		MAX521_			60		μV_{RMS}
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.5		5.5	V
Supply Current	I_{DD}	Operating mode, output unloaded, all digital inputs 0V or V_{DD}	MAX520_		4	20	µA
			MAX521_C		10	20	mA
			MAX521_E/BM		10	24	
		Power-down mode (PD = 1)			4	20	µA

Note 1: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
Note 2: Input capacitance is code dependent. The highest input capacitance occurs at code = FF hex.
Note 3: $V_{REF_}$ = 4Vp-p, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
Note 4: $V_{REF_}$ = 4Vp-p, 10kHz, DAC code = 00 hex.
Note 5: Guaranteed by design.
Note 6: I^2C-compatible mode.
Note 7: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

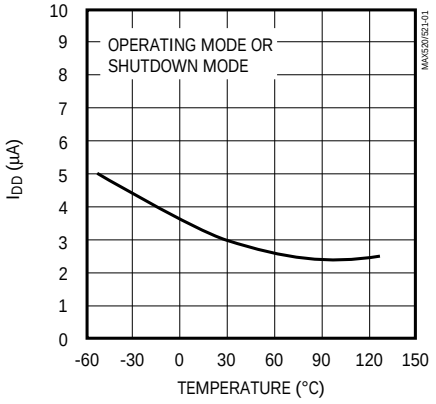
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) Start Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 8)	0		0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 9)	20 + 0.1Cb		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Note 9)	20 + 0.1Cb		300	ns
Fall Time of SDA Transmitting (Note 6)	t_F	$I_{SINK} \leq$ 6mA (Note 9)	20 + 0.1Cb		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	Cb				400	pF
Pulse Width of Spike Suppressed	t_{SP}	(Notes 10, 11)	0		50	ns

Note 8: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 9: Cb = total capacitance of one bus line in pF. t_R and t_f measured between 0.3V_{DD} and 0.7V_{DD}.
Note 10: An input filter on the SDA and SCL input suppresses noise spikes less than 50ns.
Note 11: Guaranteed by design.

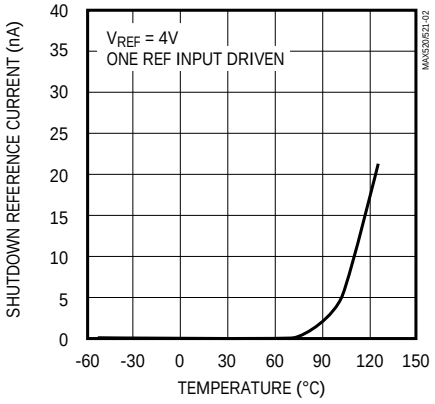
Typical Operating Characteristics

(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

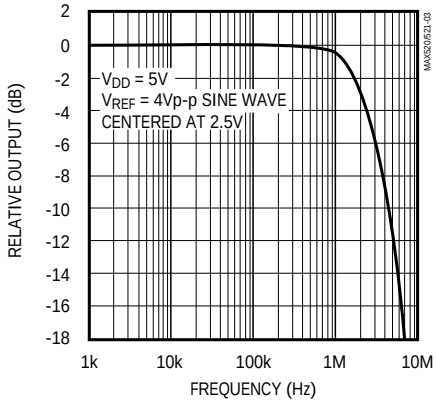
MAX520
SUPPLY CURRENT vs. TEMPERATURE



MAX520
REFERENCE INPUT CURRENT vs. TEMPERATURE (SHUTDOWN MODE)



MAX520
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE

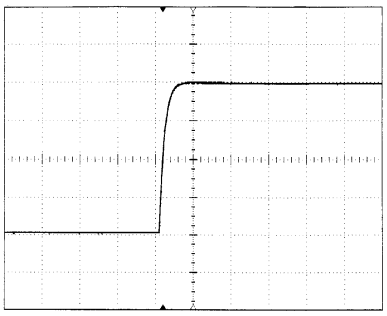


Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

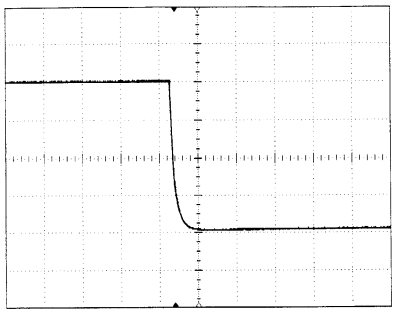
(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

MAX520
POSITIVE SETTLING TIME



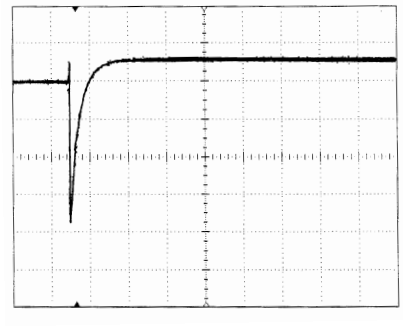
OUT2 = NO LOAD, REF2 = 4V,
DAC CODE = 00 HEX to FF HEX

MAX520
NEGATIVE SETTLING TIME



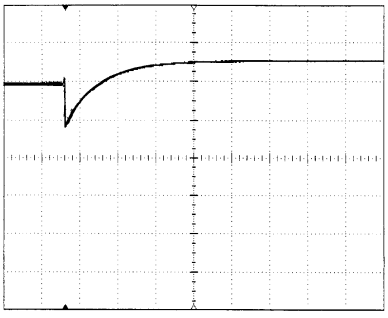
OUT2 = NO LOAD, REF2 = 4V,
DAC CODE = FF HEX to 00 HEX

MAX520
WORST-CASE 1LSB DIGITAL STEP CHANGE
(CAPACITIVE LOAD < 5pF)



REF2 = 4V, DAC CODE = 7F HEX to 80 HEX

MAX520
WORST-CASE 1LSB DIGITAL STEP CHANGE
(CAPACITIVE LOAD = 25pF)

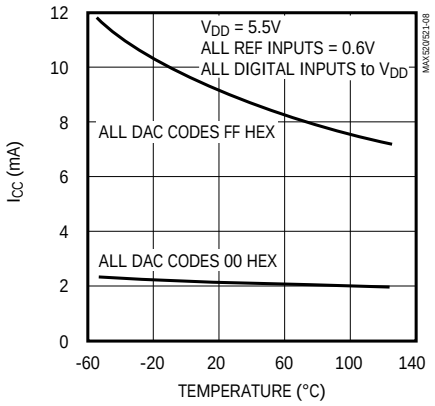


REF2 = 4V, DAC CODE = 7F HEX to 80 HEX

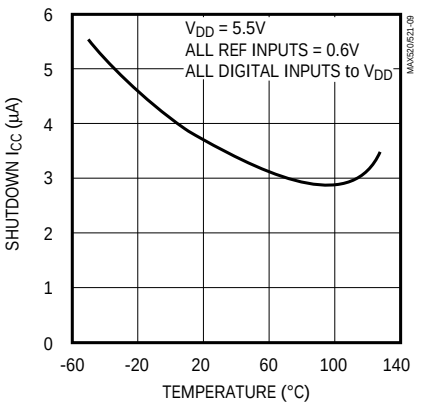
Typical Operating Characteristics

(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

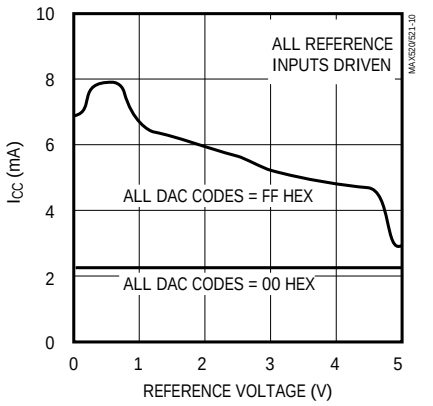
MAX521
SUPPLY CURRENT vs. TEMPERATURE



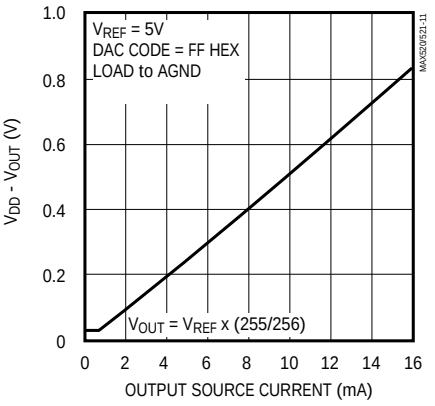
MAX521
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



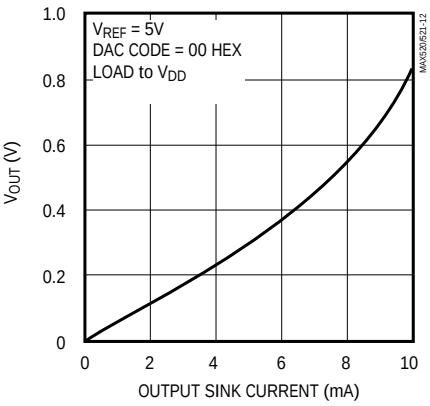
MAX521
SUPPLY CURRENT vs. REFERENCE VOLTAGE



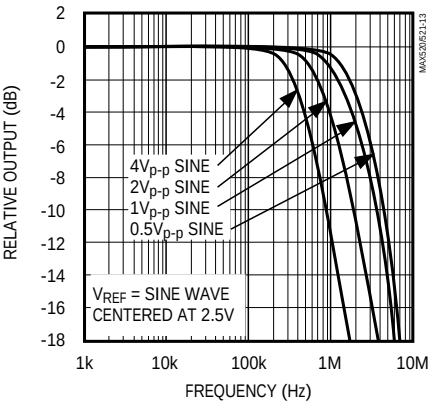
MAX521
DAC OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT



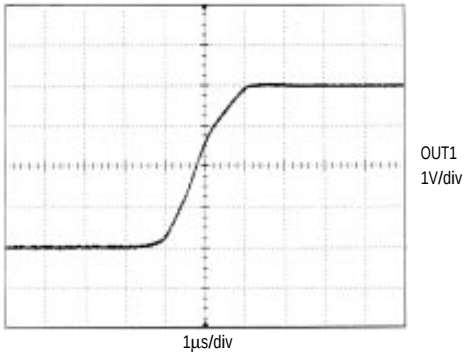
MAX521
DAC OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



MAX521
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE

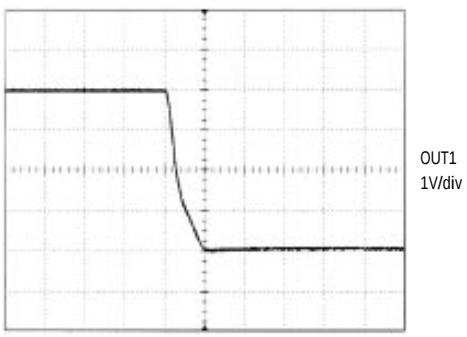


MAX521
POSITIVE SETTLING TIME



OUT1 LOADED WITH 10kΩ II 100pF, REF1 = 4V,
DAC CODE = 00 HEX to FF HEX

MAX521
NEGATIVE SETTLING TIME



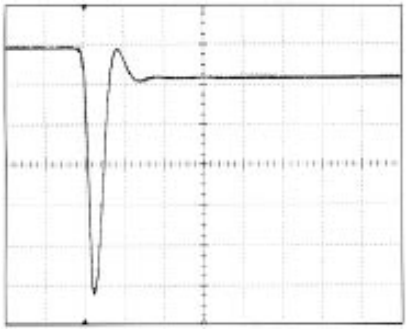
OUT1 LOADED WITH 10kΩ II 100pF, REF1 = 4V,
DAC CODE = FF HEX to 00 HEX

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

(V_{DD} = 5V, DAC outputs unloaded, T_A = +25°C, unless otherwise noted.)

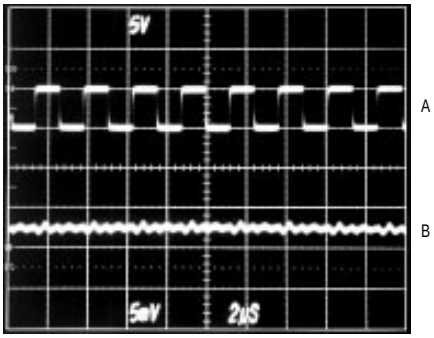
MAX521
WORST-CASE 1LSB DIGITAL STEP CHANGE



500ns/div

REF1 = 5V, DAC CODE = 80 HEX to 7F HEX

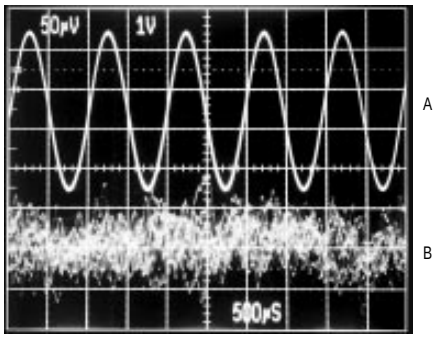
CLOCK FEEDTHROUGH



A = SCL, 400kHz, 5V/div
B = OUT1, 5mV/div

REF1 = 5V, DAC CODE = 7F HEX

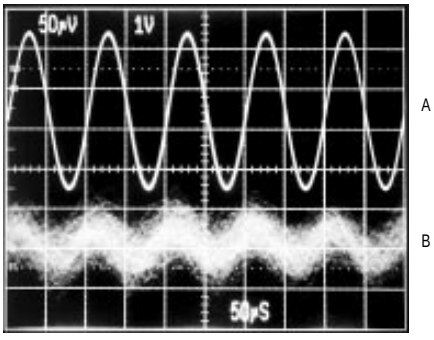
REFERENCE FEEDTHROUGH AT 1kHz



A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED

FILTER PASSBAND = 100Hz to 10kHz, DAC CODE = 00 HEX

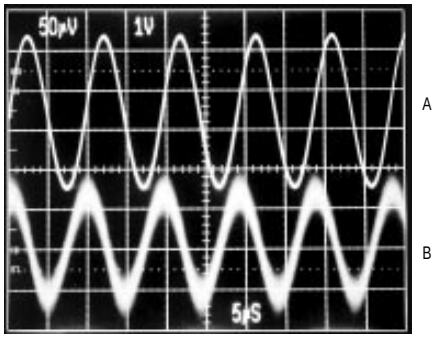
REFERENCE FEEDTHROUGH AT 10kHz



A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED

FILTER PASSBAND = 1kHz to 100kHz, DAC CODE = 00 HEX

REFERENCE FEEDTHROUGH AT 100kHz



A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED

FILTER PASSBAND = 10kHz to 1MHz, DAC CODE = 00 HEX

Pin Description

PIN				NAME	FUNCTION
MAX520		MAX521			
DIP/SO	SSOP	DIP	SO/SSOP		
1	1	1	1	OUT1	DAC1 Voltage Output
2	2	2	2	OUT0	DAC0 Voltage Output
3	3	3	3	REF1	Reference Voltage Input for DAC1
4	5	4	4	REF0	Reference Voltage Input for DAC0
—	4, 7, 14, 17	—	7, 9, 16, 20	N.C.	No Connect—not internally connected
6	8	5	5	DGND	Digital Ground
5	6	6	6	AGND	Analog Ground
7	9	7	8	SCL	Serial Clock Input
8	10	8	10	SDA	Serial Data Input
—	—	9	11	OUT4	DAC4 Voltage Output
—	—	10	12	OUT5	DAC5 Voltage Output
—	—	11	13	OUT6	DAC6 Voltage Output
—	—	12	14	OUT7	DAC7 Voltage Output
9	11	13	15	AD0	Address Input 0; sets IC's slave address
10	12	14	17	AD1	Address Input 1; sets IC's slave address
11	13	—	—	AD2	Address Input 2; sets IC's slave address
12	15	15	18	V_{DD}	Power Supply, +5V
—	—	16	19	REF4	Reference Voltage Input for DACs 4, 5, 6, and 7
13	16	17	21	REF3	Reference Voltage Input for DAC3
14	18	18	22	REF2	Reference Voltage Input for DAC2
15	19	19	23	OUT3	DAC3 Voltage Output
16	20	20	24	OUT2	DAC2 Voltage Output

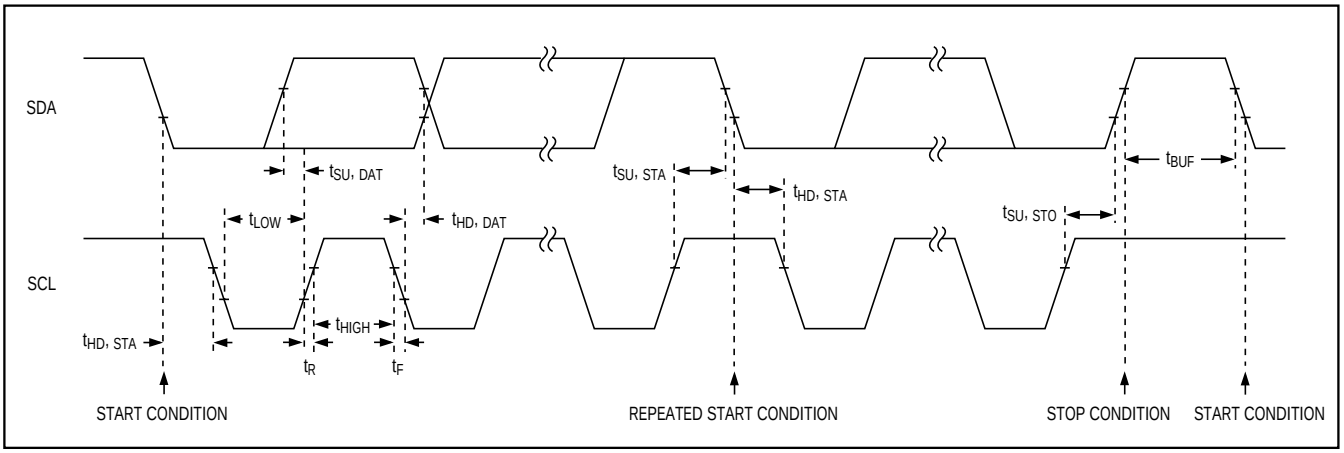


Figure 1. 2-Wire Serial-Interface Timing Diagram

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Detailed Description

Serial Interface

The MAX520/MAX521 use a simple 2-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor (µP) port. Figure 1 shows the timing diagram for signals on the 2-wire bus. Figure 2 shows the typical application of the MAX520/MAX521. The 2-wire bus can have several devices (in addition to the MAX520/MAX521) attached. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. External pull-up resistors are not required on these lines. The MAX520/MAX521 can be used in applications where pull-up resistors are required (such as in I^2C systems) to maintain compatibility with the existing circuitry.

The MAX520/MAX521 are receive-only devices and must be controlled by a bus master device. They operate at SCL rates up to 400kHz. A master device sends information to the devices by transmitting their address over the bus and then transmitting the desired information. Each transmission consists of a START condition, the MAX520/MAX521's programmable slave-address, one or more command-byte/output-byte pairs (or a command byte alone, if it is the last byte in the transmission), and finally, a STOP condition (Figure 3).

The address byte and pairs of command and output bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low. SDA's state is sampled, and therefore must remain stable while SCL is high. The only exceptions to this are the START and STOP conditions. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer the data bits to the MAX520/MAX521. Set SDA low during the 9th clock cycle as the MAX520/MAX521 pull SDA low during this time. R_C (Figure 2) limits the current that flows during this time if SDA stays high for short periods of time.

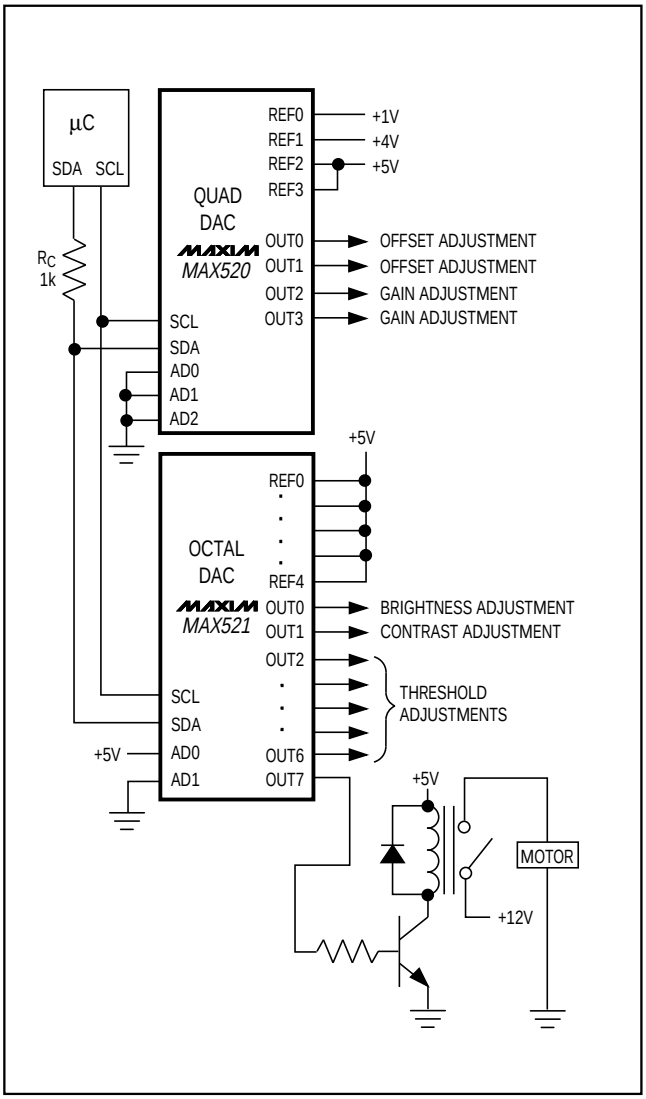


Figure 2. Typical Application Circuit

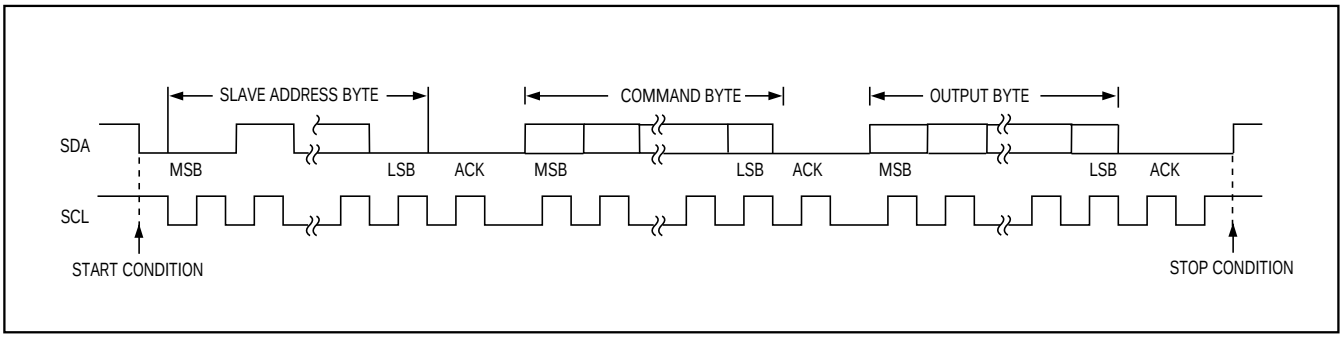


Figure 3. A Complete Serial Transmission

START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

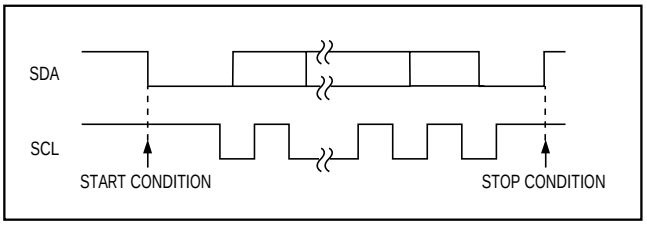


Figure 4. All communications begin with a START condition and end with a STOP condition, both generated by a bus master.

Slave Address

The MAX520/MAX521 each have a 7-bit-long slave address (Figure 5). The first four bits (MSBs) of the slave address have been factory programmed and are always 0101. In addition, the MAX521 has the next bit factory programmed to 0. The logic state of the address input pins (AD0, AD1, and AD2 of the MAX520; AD0 and AD1 of the MAX521) determine the least significant bits of the 7-bit slave address. These input pins may be connected to V_{DD} or DGND, or they may be actively driven by TTL or CMOS logic levels. There are four possible slave addresses for the MAX521, and therefore a maximum of four such devices may be on the bus at one time. The MAX520 has eight possible slave addresses. The eighth bit (LSB) in the slave address byte should be low when writing to the MAX520/MAX521.

The MAX520/MAX521 monitor the bus continuously, waiting for a START condition followed by its slave address. When a device recognizes its slave address, it is ready to accept data.

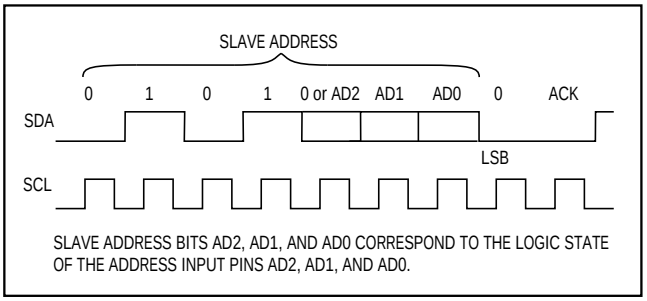


Figure 5. Address Byte

Command Byte and Output Byte

A command byte follows the slave address. Figure 6 shows the format for the command byte. A command byte is usually followed by an output byte unless it is the last byte in the transmission. If it is the last byte, all bits except PD and RST are ignored. If an output byte follows the command byte, A0–A2 of the command byte indicate the digital address of the DAC whose input data latch receives the digital output data. The data is transferred to the DAC's output latch during the STOP condition following the transmission. This allows all DACs to be updated and the new outputs to appear simultaneously (Figure 7).

Setting the PD bit high powers down the MAX520/MAX521 following a STOP condition (Figure 8a). If a command byte with PD set high is followed by an output byte, the addressed DAC's input latch will be updated and the data will be transferred to the DAC's output latch following the STOP condition (Figure 8b). If the transmission's last command byte has PD high, the voltage outputs will not reflect the newly entered data because the DAC will enter power-down mode when the STOP condition is detected. When in power-down, the MAX521's DAC outputs float, and the MAX520's unbuffered outputs look like a 16kΩ resistor to AGND. In this mode, the supply current is a maximum of 20µA. A command byte with the PD bit low returns the MAX520/MAX521 to normal operation following a STOP condition, and the voltage outputs reflect the current output-latch contents (Figures 9a and 9b). Because each subsequent command byte overwrites the previous PD bit, only the last command byte of a transmission affects the power-down state.

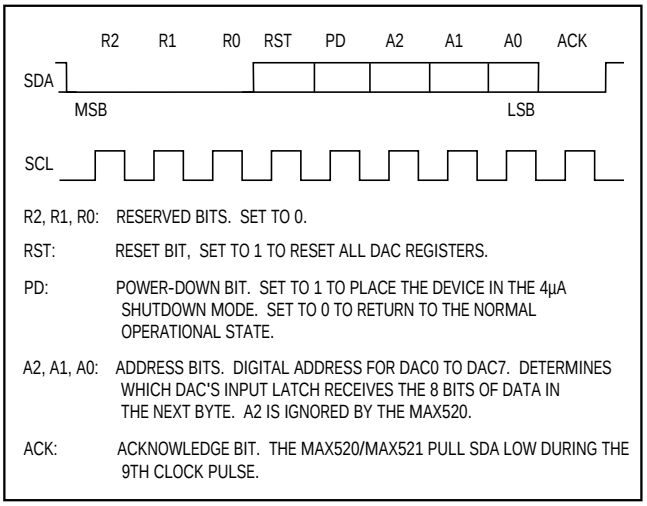


Figure 6. Command Byte

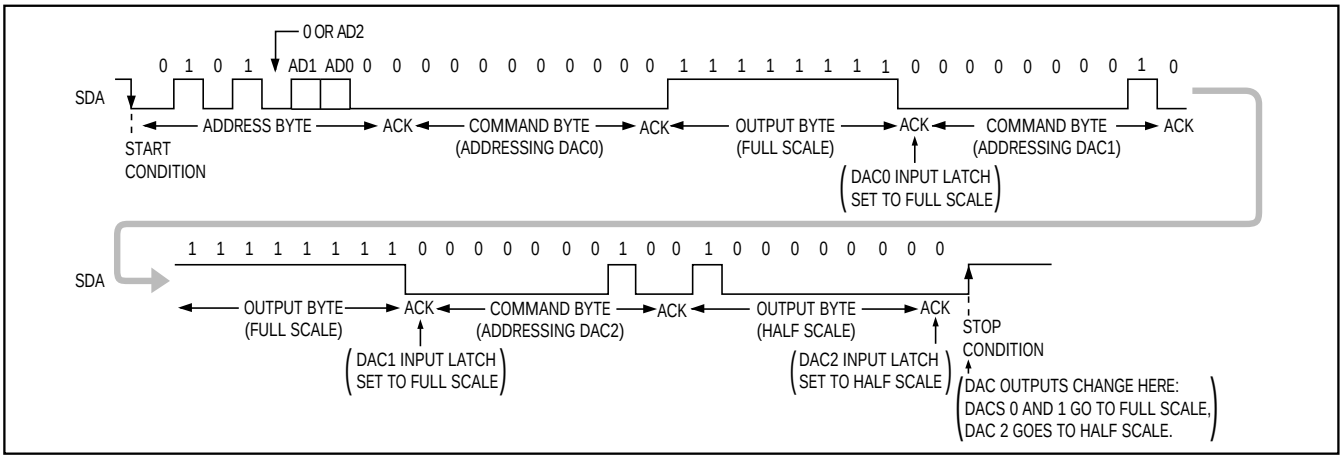


Figure 7. Setting DAC Outputs

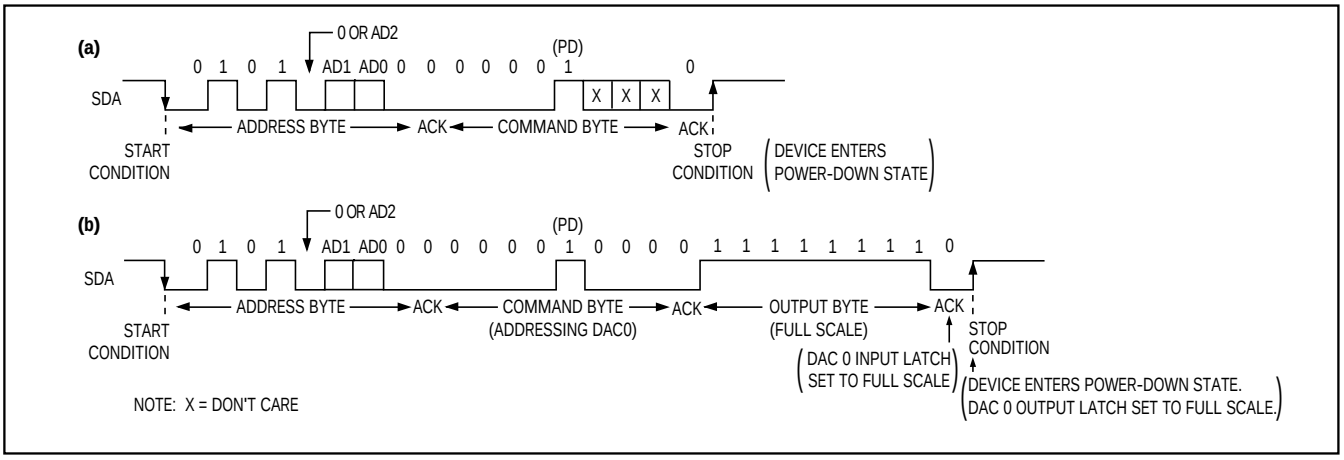


Figure 8. Entering the Power-Down State

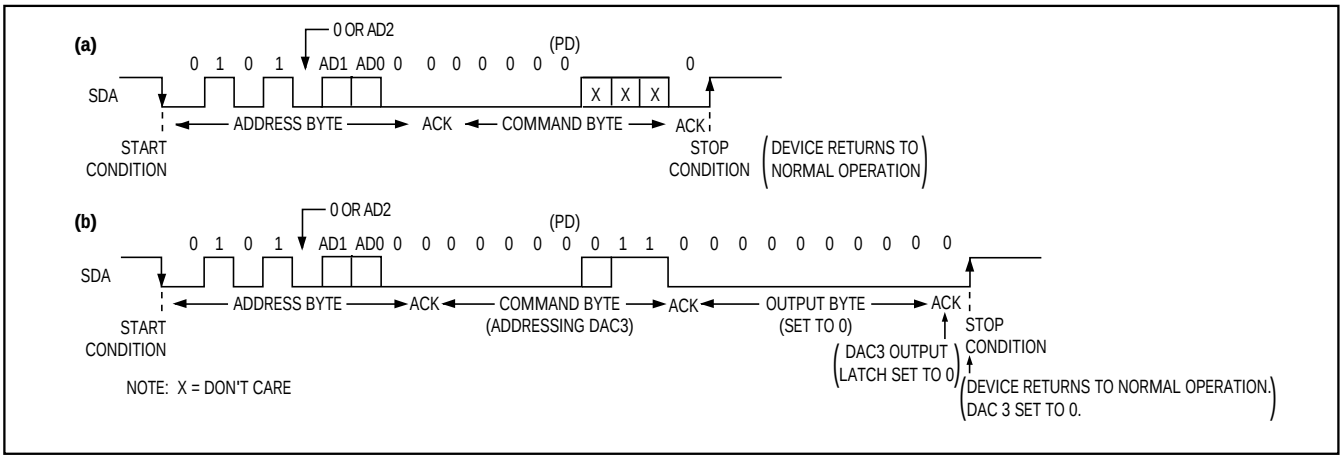


Figure 9. Returning to Normal Operation from Power-Down

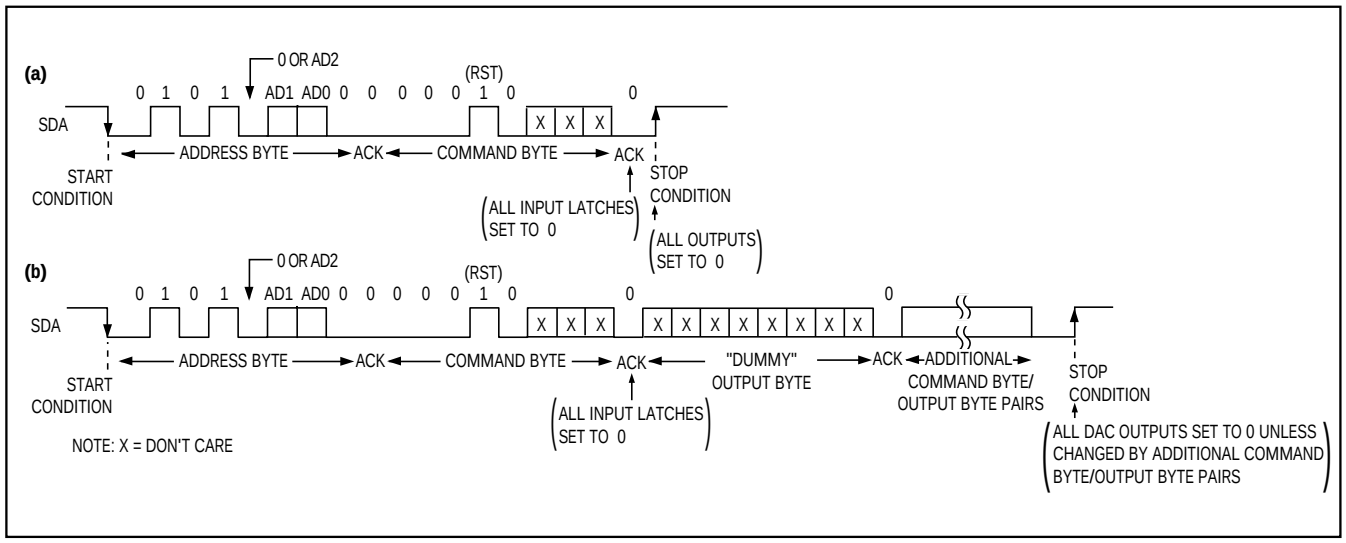


Figure 10. Resetting DAC Outputs

Setting the RST bit high clears all DAC input latches. The DAC outputs remain unchanged until a STOP condition is detected (Figure 10a). If a reset is issued, the following output byte is ignored. Subsequent pairs of command/output bytes overwrite the input latches (Figure 10b).

All changes made during a transmission affect the MAX520/MAX521's outputs only when the transmission ends and a STOP has been recognized. The R0, R1, and R2 bits are reserved bits that must be set to zero.

I²C Compatibility

The MAX520/MAX521 are fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain which pulls the data line low during the 9th clock pulse. Figure 11 shows a typical I²C application.

Additional START Conditions

It is possible to interrupt a transmission to a MAX520/MAX521 with a new START (repeated start) condition (perhaps addressing another device), which leaves the input latches with data that has not been transferred to the output latches (Figure 12). Only the currently addressed device will recognize a STOP condition and transfer data to its output latches. If the device is left with data in its input latches, the data can be transferred to the output latches the next time the device is addressed, as long as it receives at least one command byte and a STOP condition.

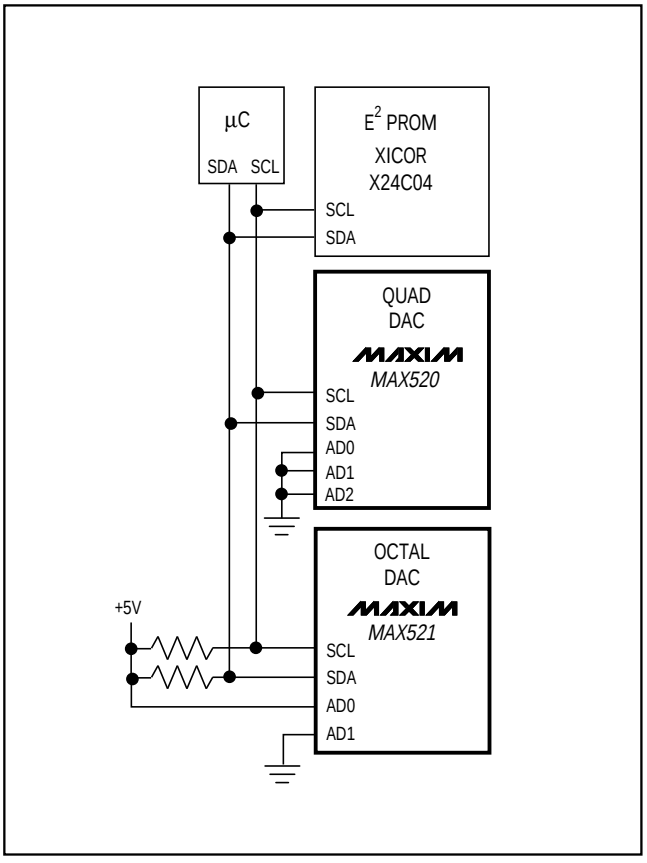


Figure 11. Typical I²C Application Circuit

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

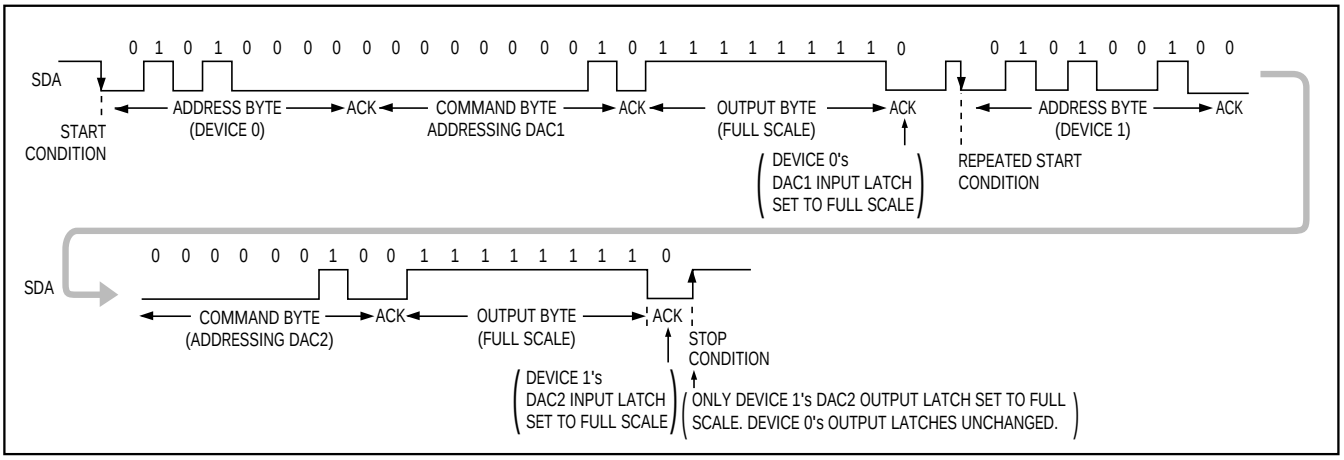


Figure 12. Repeated START Conditions

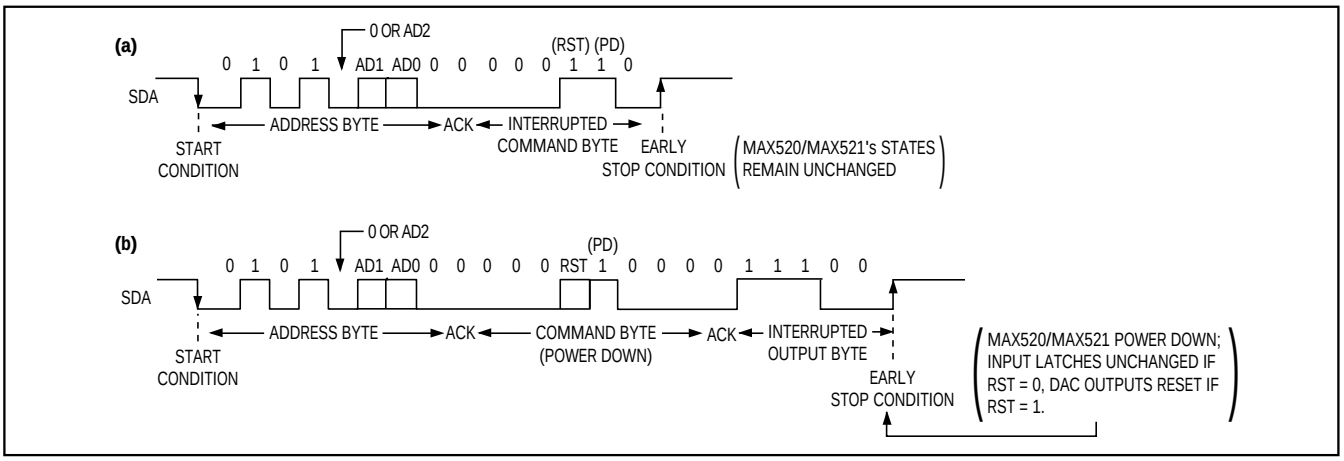


Figure 13. Early STOP Conditions

Early Stop Conditions

The addressed device recognizes a STOP condition at any point in a transmission. If the STOP occurs during a command byte, all previous uninterrupted command and output byte pairs are accepted, the interrupted command byte is ignored, and the transmission ends (Figure 13a). If the STOP occurs during an output byte, all previous uninterrupted command and output byte pairs are accepted, the final command byte's PD and RST bits are accepted, the interrupted output byte is ignored, and the transmission ends (Figure 13b).

Analog Section

DAC Operation

The MAX520 contains four matched voltage-output DACs, and the MAX521 contains eight. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. For both devices, DAC0–DAC3 each have separate reference inputs, while the MAX521's DAC4–DAC7 all share a common reference input. Figure 14 shows a simplified diagram of one DAC.

Reference Inputs

The MAX520/MAX521 can be used for multiplying applications. The reference accepts a 0V to V_{DD} voltage, both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC(s). The reference voltage must be positive. The DAC's input impedance is code dependent, with the lowest value occurring when the input code is 55 hex or 0101 0101, and the maximum value occurring when the input code is 00 hex. Since the REF input resistance

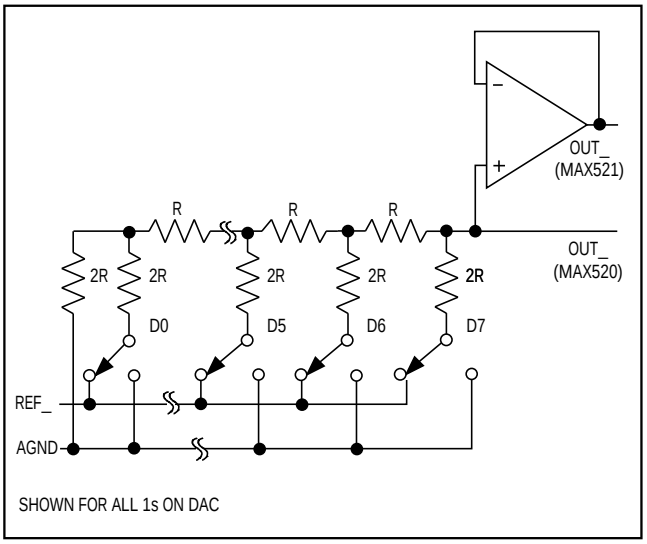


Figure 14. DAC Simplified Circuit Diagram

(R_{IN}) is code dependent, it must be driven by a circuit with low output impedance (no more than $R_{IN} \div 2000$) to maintain output linearity. The REF input capacitance is also code dependent, with the maximum value occurring at code FF hex (typically 30pF for the MAX520/MAX521's REF0–REF3, and 120pF for the MAX521's REF4). The output voltage for any DAC can be represented by a digitally programmable voltage source as: $V_{OUT} = (N \times V_{REF}) / 256$, where N is the numerical value of the DAC's binary input code. Table 1 shows the unipolar code.

Table 1. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
11111111	$+ V_{REF}\left(\frac{255}{256}\right)$
10000001	$+ V_{REF}\left(\frac{129}{256}\right)$
10000000	$+ V_{REF}\left(\frac{128}{256}\right) = \frac{V_{REF}}{2}$
01111111	$+ V_{REF}\left(\frac{127}{256}\right)$
00000001	$+ V_{REF}\left(\frac{1}{256}\right)$
00000000	0V

MAX520 Unbuffered DAC Outputs

The unbuffered DAC outputs (OUT0–OUT3) connect directly to the internal 16kΩ R-2R network. The outputs swing from 0V to V_{DD}.

The MAX520 has no output buffer amplifiers, giving it very low supply current. The output-offset voltage is lower without the output buffer, and the output can also slew and settle faster if capacitive loading is minimized. Resistive loading should be very light for highest accuracy. Any output loading generates some gain error, increasing full-scale error. The R-2R ladder's output resistance is 16kΩ, so a 1µA output current creates a 16mV error. Linearity is not affected because the ladder output resistance does not change with DAC code. Ladder-resistance changes with temperature are also very small.

DACs are often used in trimming applications to replace hardware potentiometers. Figure 15a shows a typical application, which requires a buffered output so that a precise current can be injected into the summing node through precision resistor R_T. For this application, the MAX520A features a precise ±1% (T_A = +25°C, ±2.5% over temperature) factory-trimmed output resistance. Because the MAX520A's output resistance is precisely trimmed, there is no need for an internal buffer or external precision resistor (Figure 15b). For applications where the output resistance value is not critical, use the MAX520B.

All DACs exhibit output glitches during code transitions. An output filter is sometimes used to reduce these glitches in sensitive applications. The MAX520 simplifies output filtering because its internal resistive ladder network serves as the "R" in an RC filter. Simply connect a small capacitor from the DAC output to ground. See the *Typical Operating Characteristics* for oscilloscope photos of the worst-case 1LSB step change both without and with 25pF of capacitance on the MAX520's output.

MAX521 Output Buffer Amplifiers

The MAX521 voltage outputs (OUT0–OUT7) are internally buffered precision unity-gain followers that slew up to 1V/µs. The outputs can swing from 0V to V_{DD}. With a 0V to 4V (or 4V to 0V) output transition, the amplifier outputs typically settle to 1/2LSB in 6µs when loaded with 10kΩ in parallel with 100pF. The buffer amplifiers are stable with any combination of resistive loads ≥2kΩ and capacitive loads ≤300pF.

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

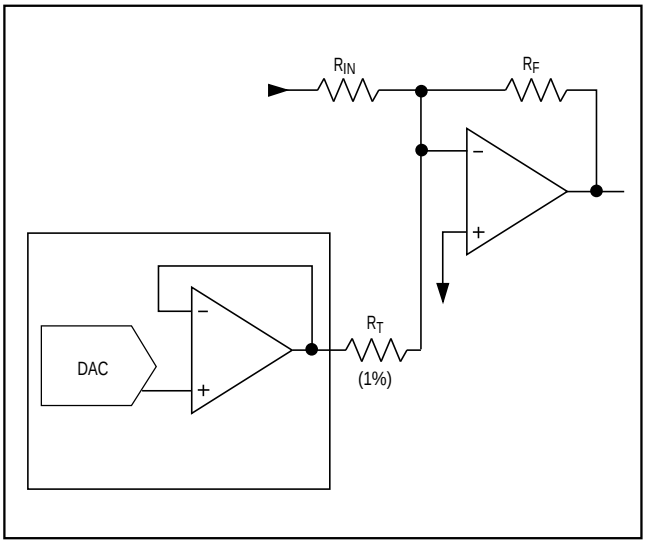


Figure 15a. Typical Trimming Circuit

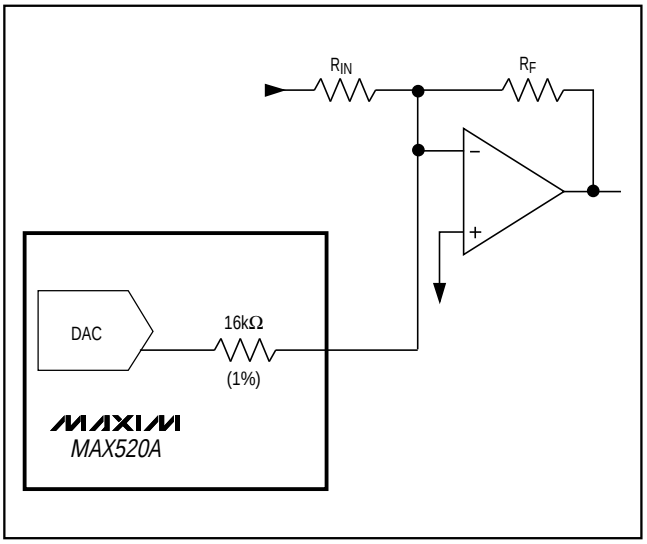


Figure 15b. MAX520A Trimming Circuit

Applications Information

Shutdown Mode

In shutdown mode, the MAX520/MAX521 reference inputs are disconnected from the R-2R ladder inputs, which saves power when the reference is not powered down. In addition, the MAX521's output buffers are disabled, greatly reducing the supply current. The MAX520's operating supply current does not change in shutdown mode. The *Command Byte and Output Byte* section describes how to enter and exit shutdown mode.

Power-Supply Bypassing and Ground Management

Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and DGND as possible. The analog ground (AGND) and digital ground (DGND) pins should be connected in a "star" configuration to the highest quality ground available, which should be located as close to the MAX521 as possible.

Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figure 16 shows the suggested PC board layout to minimize crosstalk.

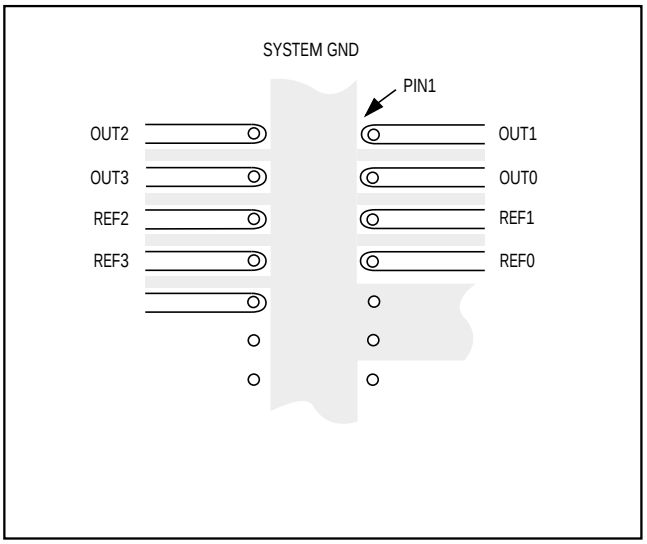
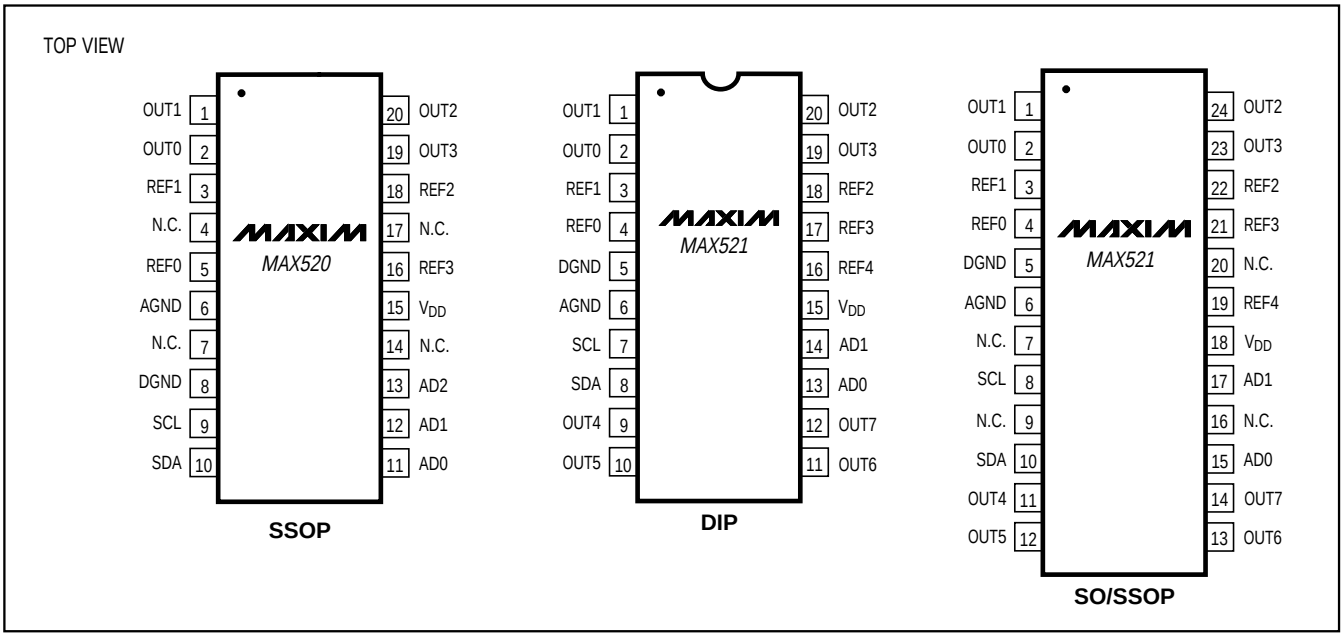
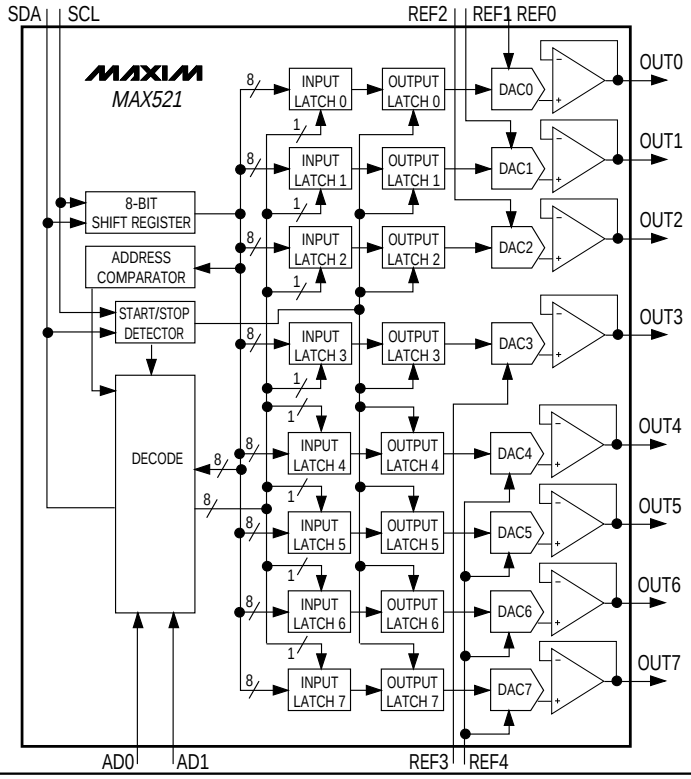


Figure 16. PC Board Layout for Minimizing Crosstalk (MAX521 bottom view, DIP package)

Pin Configurations (continued)



Functional Diagrams (continued)



Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

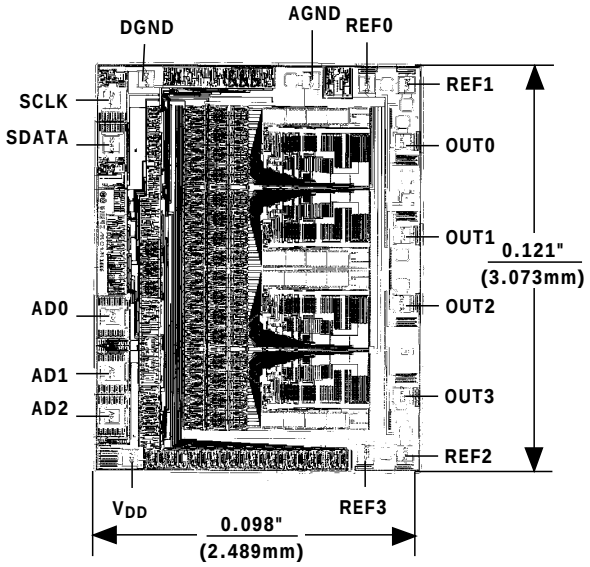
Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX520ACAP	0°C to +70°C	20 SSOP	1
MAX520BCAP	0°C to +70°C	20 SSOP	1
MAX520AC/D	0°C to +70°C	Dice*	1
MAX520BC/D	0°C to +70°C	Dice*	1
MAX520AEPE	-40°C to +85°C	16 Plastic DIP	1
MAX520BEPE	-40°C to +85°C	16 Plastic DIP	1
MAX520AEWE	-40°C to +85°C	16 Wide SO	1
MAX520BEWE	-40°C to +85°C	16 Wide SO	1
MAX520AEAP	-40°C to +85°C	20 SSOP	1
MAX520BEAP	-40°C to +85°C	20 SSOP	1
MAX520AMJE	-55°C to +125°C	16 CERDIP	1
MAX520BMJE	-55°C to +125°C	16 CERDIP	1
MAX521ACPP	0°C to +70°C	20 Plastic DIP	1
MAX521BCPP	0°C to +70°C	20 Plastic DIP	2
MAX521ACWG	0°C to +70°C	24 Wide SO	1
MAX521BCWG	0°C to +70°C	24 Wide SO	2
MAX521ACAG	0°C to +70°C	24 SSOP	1
MAX521BCAG	0°C to +70°C	24 SSOP	2
MAX521BC/D	0°C to +70°C	Dice*	2
MAX521AEPP	-40°C to +85°C	20 Plastic DIP	1
MAX521BEPP	-40°C to +85°C	20 Plastic DIP	2
MAX521AEWG	-40°C to +85°C	24 Wide SO	1
MAX521BEWG	-40°C to +85°C	24 Wide SO	2
MAX521AEAG	-40°C to +85°C	24 SSOP	1
MAX521BEAG	-40°C to +85°C	24 SSOP	2
MAX521BMJP	-55°C to +125°C	20 CERDIP	2

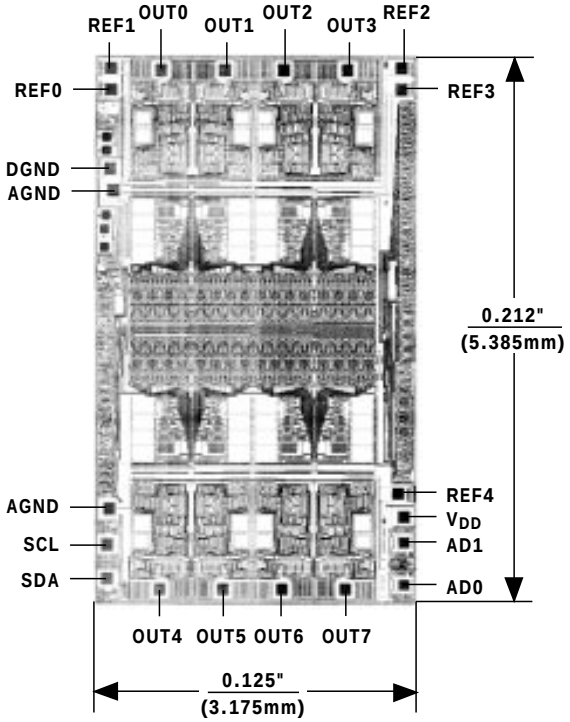
** Dice are specified at T_A = +25°C, DC parameters only.*
† MAX520 "A" grade parts include a 1%-accurate, factory-trimmed output resistance.

Chip Topographies

MAX520

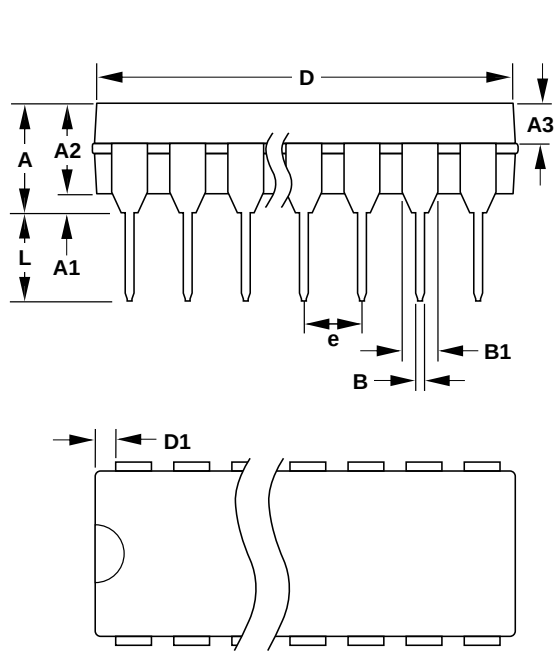


MAX521



TRANSISTOR COUNT: 4518
SUBSTRATE CONNECTED TO V_{DD}

Package Information

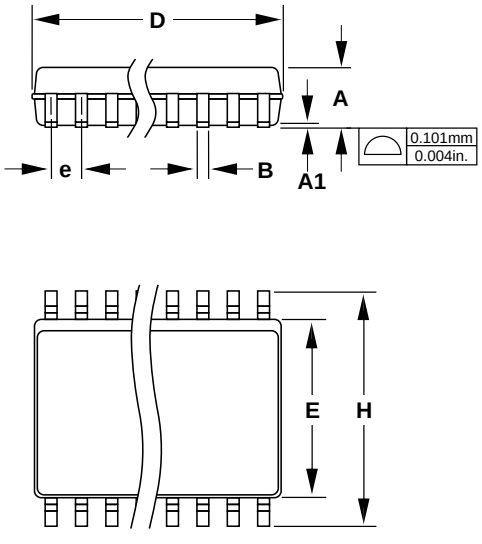


Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

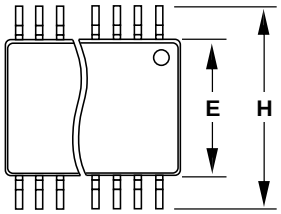
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

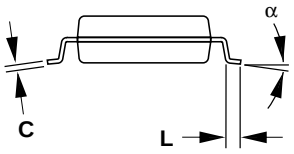
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

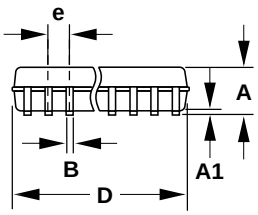
21-0042A

Quad/Octal, 2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Package Information (continued)







SSOP
SHRINK
SMALL-OUTLINE
PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

21-0056A

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