



600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

General Description

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z high-frequency step-down converters are optimized for dynamically powering the power amplifier (PA) in WCDMA or NCDMA handsets. The devices integrate a high-efficiency PWM step-down converter for medium- and low-power transmission, and a 60mΩ typical bypass FET to power the PA directly from the battery during high-power transmission. Dual 200mA low-noise, high-PSRR low-dropout regulators (LDOs) for PA biasing are also integrated.

Two switching frequency options are available (2MHz for the MAX8805W/MAX8805Y and 4MHz for the MAX8805X/MAX8805Z), allowing optimization for smallest solution size or highest efficiency. Fast switching allows the use of small ceramic 2.2μF input and output capacitors while maintaining low ripple voltage. The feedback network is integrated, further reducing external component count and total solution size.

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z use an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The REFIN to OUT gain is available in two options (2V/V for the MAX8805Y/MAX8805Z and 2.5V/V for the MAX8805W/MAX8805X). At high-duty cycle, the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z automatically switch to the bypass mode, connecting the input to the output through a low-impedance (60mΩ typ) MOSFET. The user can also enable the bypass mode directly through a logic-control input.

The LDOs in the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z are designed for low-noise operation (35μVRMS typ). Each LDO is individually enabled through its own logic control interface.

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z are available in 16-bump, 2mm x 2mm WLP and UCSP™ packages (0.7mm max height).

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- ♦ **PA Step-Down Converter**
 - 7.5μs (typ) Settling Time for 0.8V to 3.4V Output Voltage Change
 - Dynamic Output Voltage Setting from 0.4V to VBATT
 - 60mΩ pFET and 100% Duty Cycle for Low Dropout
 - 2MHz or 4MHz Switching Frequency
 - Low Output-Voltage Ripple
 - 600mA (MAX8805Y/MAX8805Z) or 650mA (MAX8805W/MAX8805X) Output Drive Capability
 - 2% Gain Accuracy
 - Tiny External Components
- ♦ **Dual Low-Noise LDOs**
 - Low 35μVRMS (typ) Output Noise
 - High 70dB (typ) PSRR
 - Guaranteed 200mA Output Drive Capability
 - Individual ON/OFF Control
- ♦ **Low 0.1μA Shutdown Current**
- ♦ **2.7V to 5.5V Supply Voltage Range**
- ♦ **Thermal Shutdown**
- ♦ **Tiny 2mm x 2mm x 0.7mm WLP and UCSP Packages (4 x 4 Grid)**

Applications

WCDMA/NCDMA Cellular Handsets
Wireless PDAs
Smartphones

Pin Configuration appears at end of data sheet.

Ordering Information

PART	PIN-PACKAGE	SWITCHING FREQUENCY	REFIN TO OUT GAIN
MAX8805WERExy+T*	16 UCSP	2MHz	2.5V/V
MAX8805XERExy+T*	16 UCSP	4MHz	2.5V/V
MAX8805YERExy+T*	16 UCSP	2MHz	2V/V
MAX8805ZERExy+T*	16 UCSP	4MHz	2V/V

+Denotes a lead-free/RoHS-compliant package.

T = Tape and reel.

*xy is the output voltage code (see Table 1).

Note: All devices are specified over the -40°C to +85°C operating temperature range.

Ordering Information continued at end of data sheet.



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ABSOLUTE MAXIMUM RATINGS

IN1A, IN1B, IN2, REFIN, EN2, REFBP to AGND-0.3V to +6.0V
 PAA, PAB, PA_EN, HP to AGND-0.3V to (VIN1A/VIN1B + 0.3V)
 LDO1, LDO2, EN1 to AGND-0.3V to (VIN2 + 0.3V)
 IN2 to IN1B/IN1A-0.3V to +0.3V
 PGND to AGND-0.3V to +0.3V
 LX Current0.7A_{RMS}
 IN1A/IN1B and PAA/PAB Current2A_{RMS}

PAA and PAB Short Circuit to PGND or IN1Continuous
 Continuous Power Dissipation (T_A = +70°C)
 16-Bump UCSP (derate 12.5mW/°C above +70°C)1W
 16-Bump WLP (derate 12.5mW/°C above +70°C)1W
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Bump Temperature (soldering, reflow)+260°C

Note: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPF and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VIN1A = VIN1B = VIN2 = VPA_EN = VEN1 = VEN2 = 3.6V, VHP = 0V, VREFIN = 0.9V (MAX8805Y/MAX8805Z), VREFIN = 0.72V (MAX8805W/MAX8805X), T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage	VIN1A, VIN1B, VIN2		2.7		5.5	V
Input Undervoltage Threshold	VIN1A, VIN1B, VIN2 rising, 180mV typical hysteresis		2.52	2.63	2.70	V
Shutdown Supply Current	VPA_EN = VEN1 = VEN2 = 0V	TA = +25°C		0.1	4	μA
		TA = +85°C		0.1		
No-Load Supply Current	VPA_EN = 0V, ILDO1 = ILDO2 = 0mA			150	250	μA
	VEN1 = VEN2 = 0V, IPA = 0mA, switching	MAX8805W/MAX8805Y		3500		
		MAX8805X/MAX8805Z		5000		
	VEN1 = VEN2 = 0V, VHP = 3.6V			150		
THERMAL PROTECTION						
Thermal Shutdown	TA rising, 20°C typical hysteresis			+160		°C
LOGIC CONTROL						
PA_EN, EN1, EN2, HP Logic-Input High Voltage	2.7V ≤ VIN1A = VIN1B = VIN2 ≤ 5.5V		1.4			V
PA_EN, EN1, EN2, HP Logic-Input Low Voltage	2.7V ≤ VIN1A = VIN1B = VIN2 ≤ 5.5V				0.4	V
Logic-Input Current (PA_EN, EN1, EN2, HP)	VIL = 0V or VIH = VIN1A = 5.5V	TA = +25°C		0.01	1	μA
		TA = +85°C		0.1		
REFIN						
REFIN Common-Mode Range	MAX8805Y/MAX8805Z		0.1		2.2	V
	MAX8805W/MAX8805X		0.1		1.76	
REFIN to PA_ Gain	VREFIN = 0.4V, 0.9V, 1.7V, 2.2V (ILX = 0mA)	MAX8805Y/MAX8805Z	1.96	2.00	2.04	V/V
	VREFIN = 0.32V, 0.75V, 1.32V, 1.76V (ILX = 0mA)	MAX8805W/MAX8805X	2.45	2.50	2.55	
REFIN Input Resistance	MAX8805Y/MAX8805Z			540		kΩ
	MAX8805W/MAX8805X			320		

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN1A} = V_{IN1B} = V_{IN2} = V_{PA_EN} = V_{EN1} = V_{EN2} = 3.6V$, $V_{HP} = 0V$, $V_{REFIN} = 0.9V$ (MAX8805Y/MAX8805Z), $V_{REFIN} = 0.72V$ (MAX8805W/MAX8805X), $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	
REFIN Dual Mode™ Threshold	VREFIN rising, 50mV hysteresis	MAX8805Y/MAX8805Z	0.44 x VIN2	0.465 x VIN2	0.48 x VIN2	V	
		MAX8805W/MAX8805X	0.36 x VIN2	0.372 x VIN2	0.39 x VIN2		
LX							
On-Resistance	p-channel MOSFET switch, ILX = -40mA		0.18			Ω	
	n-channel MOSFET rectifier, ILX = 40mA		0.15				
LX Leakage Current	VIN1A = VIN1B = VIN2 = 5.5V, VLX = 0V	TA = +25°C	0.1			μA	
		TA = +85°C	1				
Peak Current Limit (p-Channel MOSFET)	VLX = 0V	MAX8805Y/MAX8805Z	0.7	0.9	1.1	A	
		MAX8805W/MAX8805X	0.75	0.95	1.15		
Valley Current Limit (n-Channel MOSFET)	MAX8805Y/MAX8805Z		0.5	0.7	0.9	A	
	MAX8805W/MAX8805X		0.55	0.75	0.95		
Minimum On- and Off-Times	MAX8805Y/MAX8805Z		0.1			μs	
	MAX8805W/MAX8805X		0.07				
Power-Up Delay	From PA_EN rising to LX rising		150			250	μs
BYPASS							
On-Resistance	p-channel MOSFET bypass, IOUT = -90mA	TA = +25°C	0.060			Ω	
		TA = +85°C	0.1				
Bypass Current Limit	VPA_ = 0V		0.8	1.2	1.8	A	
Step-Down Current Limit in Bypass	VLX = 0V	MAX8805Y/MAX8805Z	0.7	0.9	1.1	A	
		MAX8805W/MAX8805X	0.75	0.95	1.15		
Total Bypass Current Limit	VLX = VPA_ = 0V	MAX8805Y/MAX8805Z	1.5	2.1	2.9	A	
		MAX8805W/MAX8805X	1.55	2.15	2.95		
Bypass Off-Leakage Current	VIN1A = VIN1B = VIN2 = 5.5V, VPAA = VPAB = 0V	TA = +25°C	0.01			μA	
		TA = +85°C	1				
LDO1							
Output Voltage VLDO1	VIN2 = 5.5V, ILDO1 = 1mA; VIN2 = 3.4V, ILDO1 = 100mA	MAX8805_E_EAA+T	1.746	1.8	1.854	V	
		MAX8805_E_EBC+T	2.425	2.5	2.575		
		MAX8805_E_ECC+T	2.619	2.7	2.781		
		MAX8805_E_EDD+T	2.716	2.8	2.884		
		MAX8805_E_EEE+T	2.765	2.85	2.936		
		MAX8805_E_EGG+T	2.910	3.0	3.090		
Output Current			200			mA	
Current Limit	VLDO1 = 0V		250	550	750	mA	
Dropout Voltage	ILDO1 = 100mA, TA = +25°C (VLDO1 ≥ 2.5V)		70			200	mV
Line Regulation	VIN2 stepped from 3.5V to 5.5V, ILDO1 = 100mA		2.4			mV	
Load Regulation	ILDO1 stepped from 50μA to 200mA		25			mV	
Power-Supply Rejection	10Hz to 10kHz, CLDO1 = 1μF, ILDO1 = 30mA		70			dB	

Dual Mode is a trademark of Maxim Integrated Products, Inc.

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN1A} = V_{IN1B} = V_{IN2} = V_{PA_EN} = V_{EN1} = V_{EN2} = 3.6V$, $V_{HP} = 0V$, $V_{REFIN} = 0.9V$ (MAX8805Y/MAX8805Z), $V_{REFIN} = 0.72V$ (MAX8805W/MAX8805X), $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

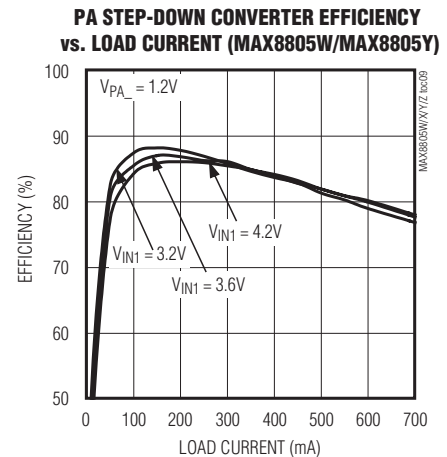
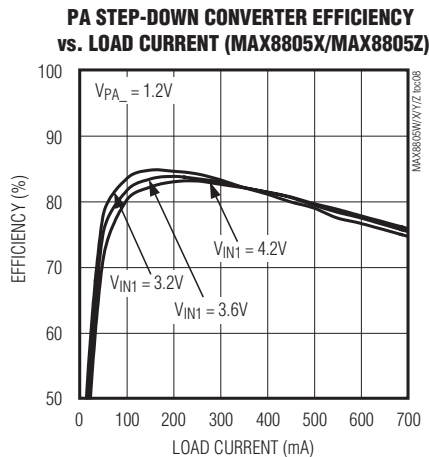
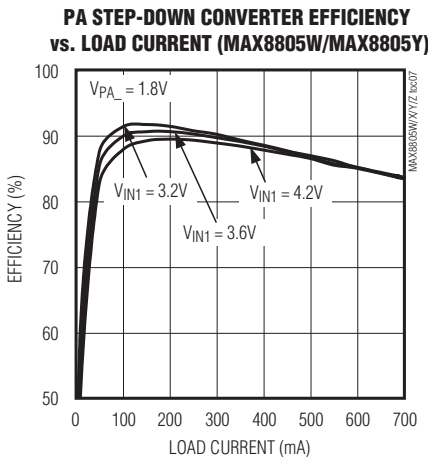
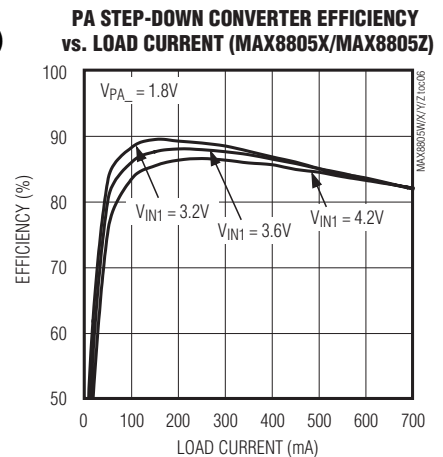
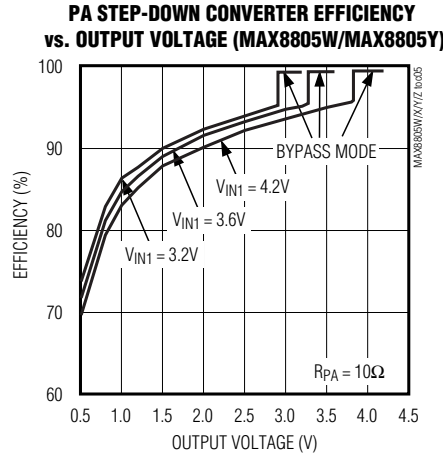
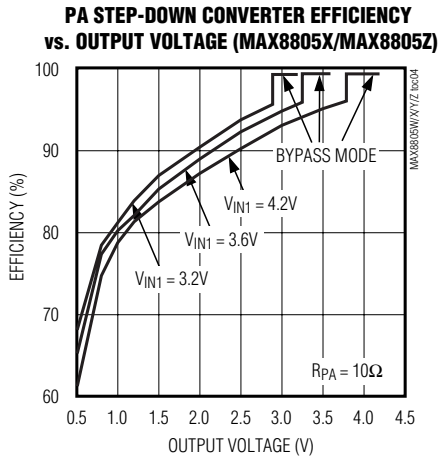
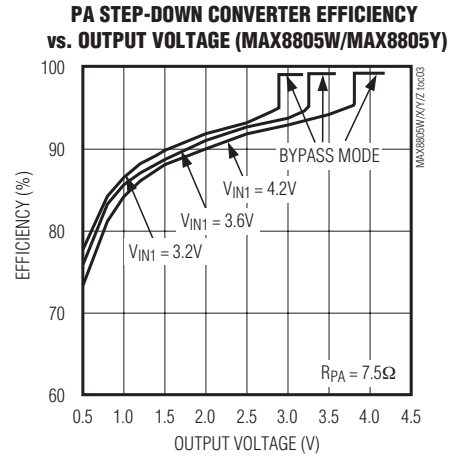
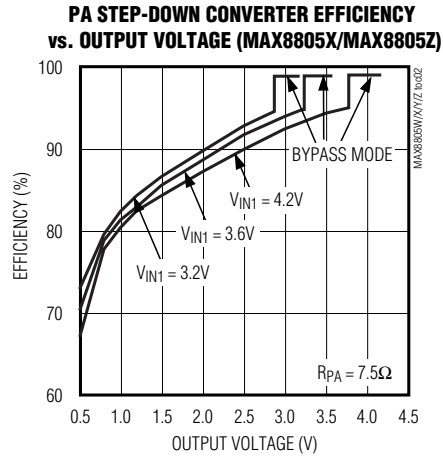
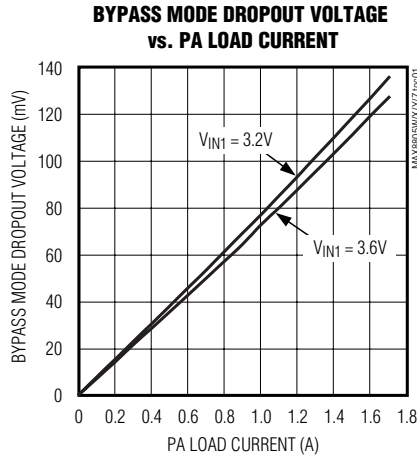
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	
Output Noise	100Hz to 100kHz, C _{LDO1} = 1μF, I _{LDO1} = 30mA		35			μVRMS	
Output Capacitor for Stable Operation	0 < I _{LDO1} < 10mA		100			nF	
	0 < I _{LDO1} < 200mA		1			μF	
Shutdown Output Impedance	V _{EN1} = 0V		1			kΩ	
LDO2							
Output Voltage V _{LDO2}	V _{IN2} = 5.5V, I _{LDO2} = 1mA; V _{IN2} = 3.4V, I _{LDO2} = 100mA	MAX8805_E_EAA+T	1.746	1.8	1.854	V	
		MAX8805_E_EAC+T	2.619	2.7	2.781		
		MAX8805_E_EAD+T	2.716	2.8	2.884		
		MAX8805_E_EBE+T	2.765	2.85	2.936		
		MAX8805_E_EGG+T	2.910	3.0	3.090		
Output Current			200			mA	
Current Limit	V _{LDO2} = 0V		250	550	750	mA	
Dropout Voltage	I _{LDO2} = 100mA, T _A = +25°C		70			200	mV
Line Regulation	V _{IN2} stepped from 3.5V to 5.5V, I _{LDO2} = 100mA		2.4			mV	
Load Regulation	I _{LDO2} stepped from 50μA to 200mA		25			mV	
Power-Supply Rejection ΔV _{LDO2} / ΔV _{IN2}	10Hz to 10kHz, C _{LDO2} = 1μF, I _{LDO2} = 30mA		70			dB	
Output Noise	100Hz to 100kHz, C _{LDO2} = 1μF, I _{LDO2} = 30mA		35			μVRMS	
Output Capacitor for Stable Operation	0μA < I _{LDO2} < 10mA		100			nF	
	0μA < I _{LDO2} < 200mA		1			μF	
Shutdown Output Impedance	V _{EN2} = 0V		1			kΩ	
REFBP							
REFBP Output Voltage	0 ≤ I _{REFBP} ≤ 1μA		1.237	1.250	1.263	V	
REFBP Supply Rejection	V _{IN2} stepped from 2.55V to 5.5V		0.2			5	mV

Note 1: All devices are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range are guaranteed by design.

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Typical Operating Characteristics

($V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V$, $V_{PA_} = 1.2V$, $V_{LDO1} = 2.85V$, $V_{LDO2} = 2.85V$, $R_{PA} = 7.5\Omega$, circuit of Figure 5, $T_A = +25^\circ C$, unless otherwise noted.)

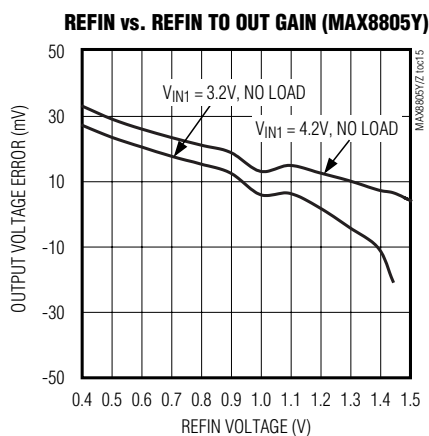
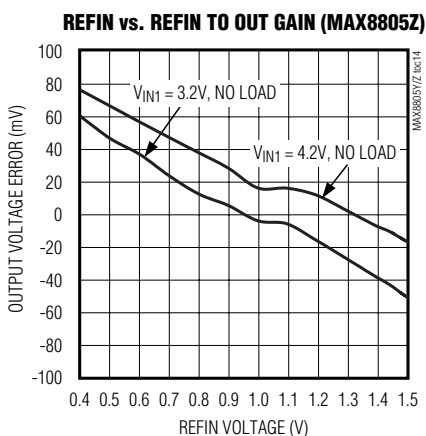
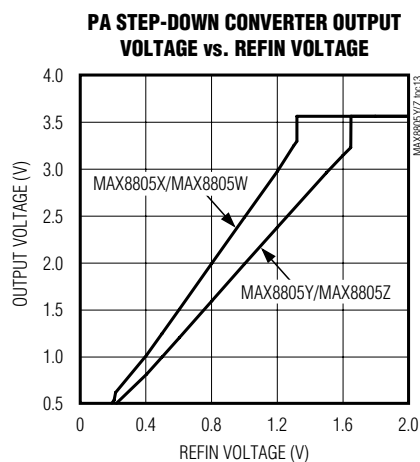
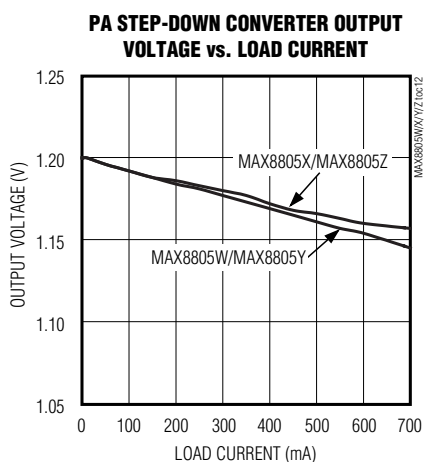
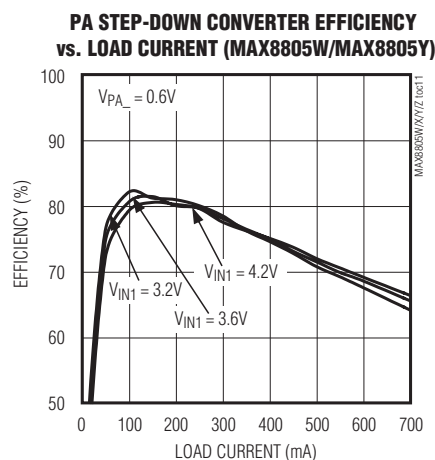
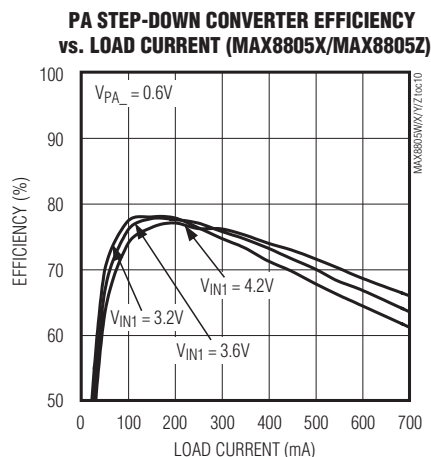


MAX8805W/MAX8805X/MAX8805Y/MAX8805Z

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Typical Operating Characteristics (continued)

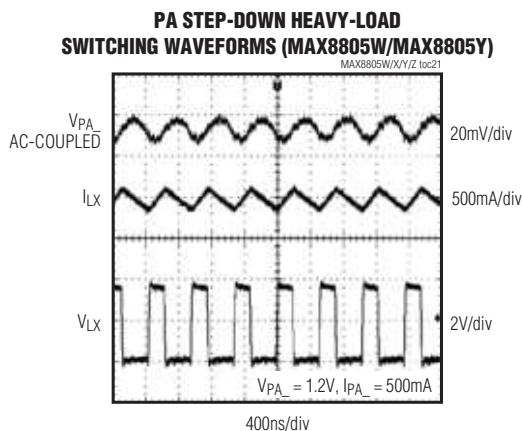
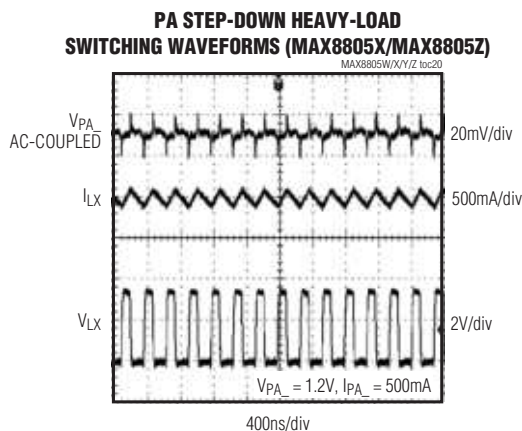
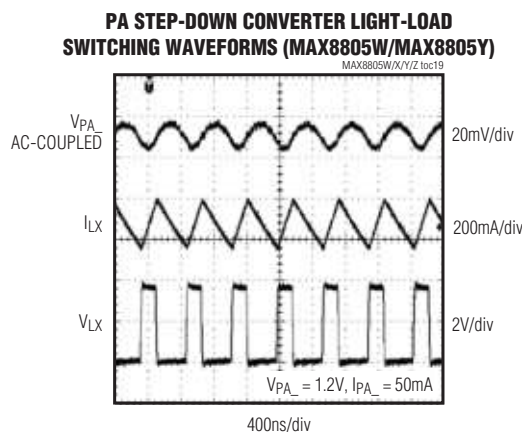
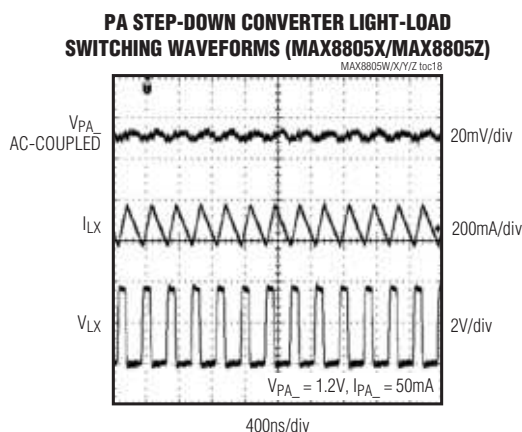
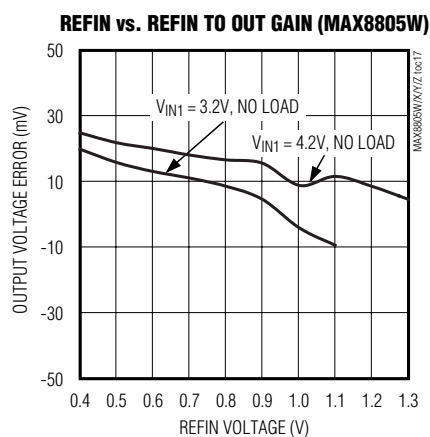
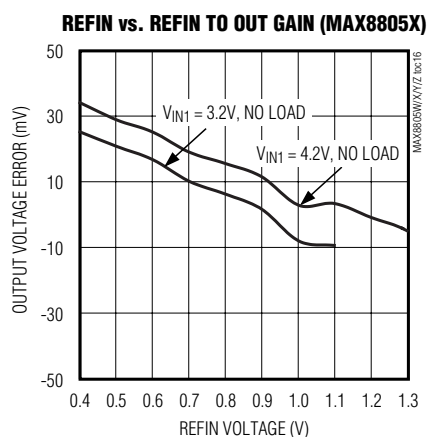
($V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V$, $V_{PA_} = 1.2V$, $V_{LDO1} = 2.85V$, $V_{LDO2} = 2.85V$, $R_{PA} = 7.5\Omega$, circuit of Figure 5, $T_A = +25^\circ C$, unless otherwise noted.)



600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Typical Operating Characteristics (continued)

($V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V$, $V_{PA_} = 1.2V$, $V_{LDO1} = 2.85V$, $V_{LDO2} = 2.85V$, $R_{PA} = 7.5\Omega$, circuit of Figure 5, $T_A = +25^\circ C$, unless otherwise noted.)

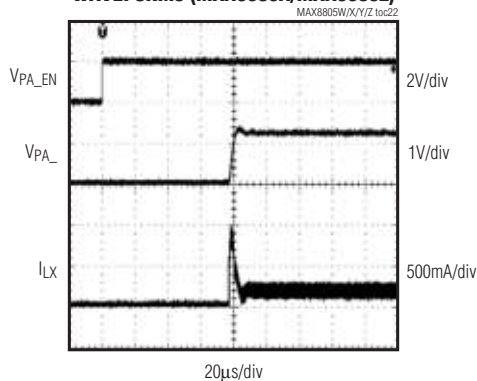


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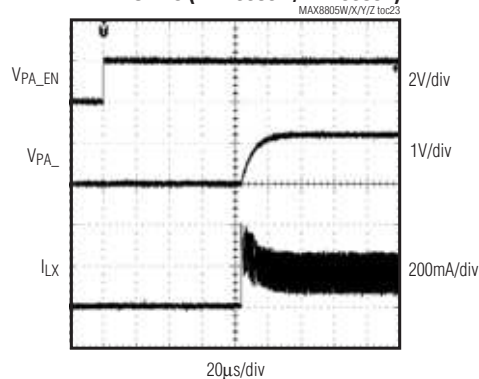
Typical Operating Characteristics (continued)

($V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V$, $V_{PA_} = 1.2V$, $V_{LDO1} = 2.85V$, $V_{LDO2} = 2.85V$, $R_{PA} = 7.5\Omega$, circuit of Figure 5, $T_A = +25^\circ C$, unless otherwise noted.)

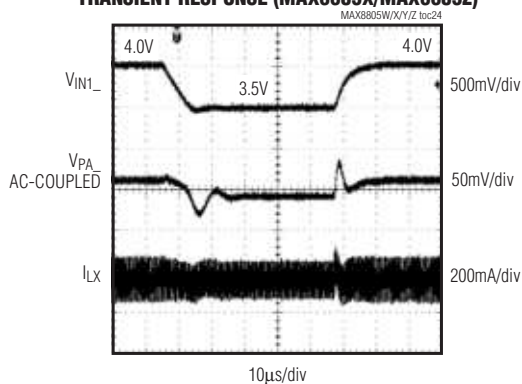
**PA STEP-DOWN SOFT-START
WAVEFORMS (MAX8805X/MAX8805Z)**



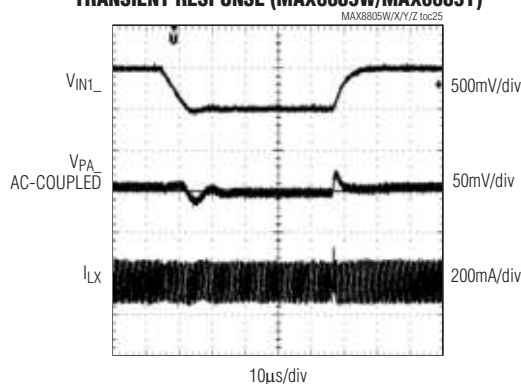
**PA STEP-DOWN SOFT-START
WAVEFORMS (MAX8805W/MAX8805Y)**



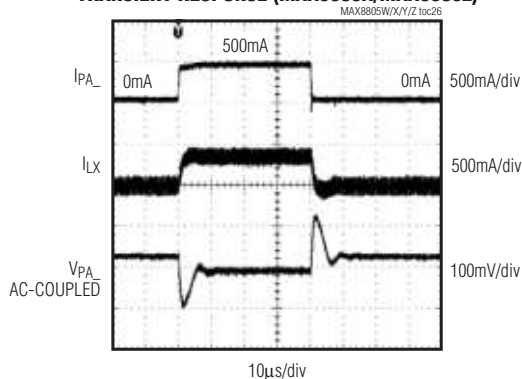
**PA STEP-DOWN CONVERTER LINE
TRANSIENT RESPONSE (MAX8805X/MAX8805Z)**



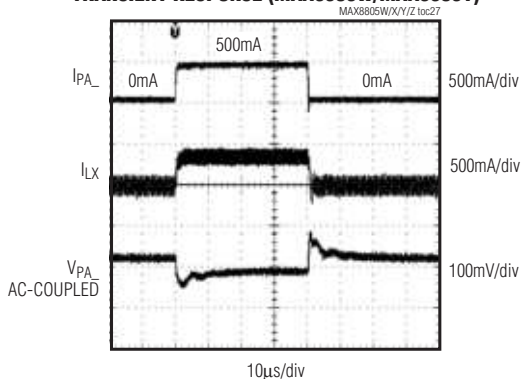
**PA STEP-DOWN CONVERTER LINE
TRANSIENT RESPONSE (MAX8805W/MAX8805Y)**



**PA STEP-DOWN CONVERTER LOAD
TRANSIENT RESPONSE (MAX8805X/MAX8805Z)**



**PA STEP-DOWN CONVERTER LOAD
TRANSIENT RESPONSE (MAX8805W/MAX8805Y)**

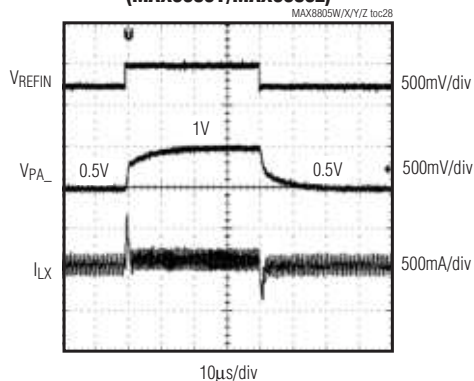


600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

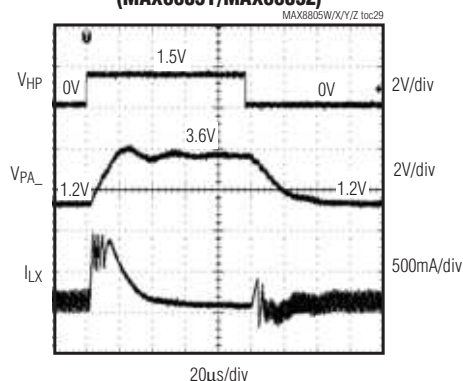
Typical Operating Characteristics (continued)

($V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V$, $V_{PA_} = 1.2V$, $V_{LDO1} = 2.85V$, $V_{LDO2} = 2.85V$, $R_{PA} = 7.5\Omega$, circuit of Figure 5, $T_A = +25^\circ C$, unless otherwise noted.)

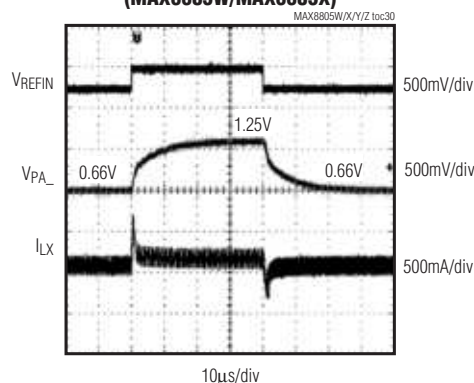
**PA STEP-DOWN CONVERTER OUTPUT
VOLTAGE TRANSIENT RESPONSE
(MAX8805Y/MAX8805Z)**



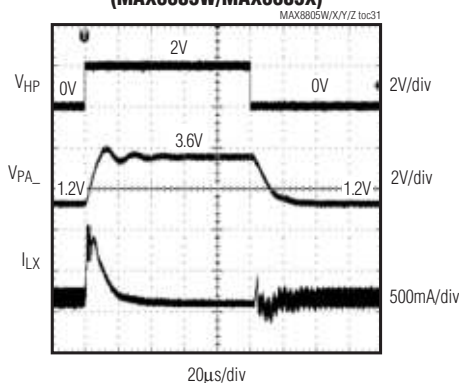
**PA STEP-DOWN CONVERTER FORCED
BYPASS-FET TRANSIENT RESPONSE
(MAX8805Y/MAX8805Z)**



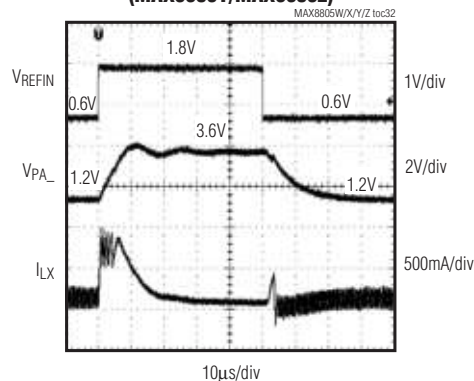
**PA STEP-DOWN CONVERTER OUTPUT
VOLTAGE TRANSIENT RESPONSE
(MAX8805W/MAX8805X)**



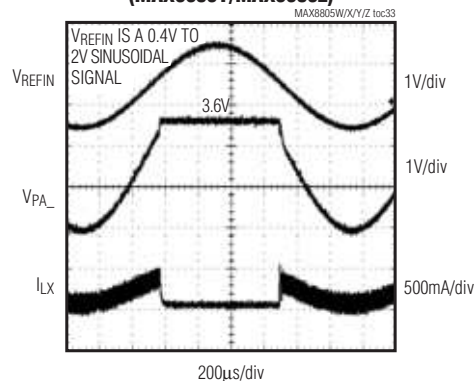
**PA STEP-DOWN CONVERTER
BYPASS-FET TRANSIENT RESPONSE
(MAX8805W/MAX8805X)**



**PA STEP-DOWN CONVERTER AUTOMATIC
BYPASS-FET TRANSIENT RESPONSE
(MAX8805Y/MAX8805Z)**



**PA STEP-DOWN CONVERTER AUTOMATIC
BYPASS-FET TRANSIENT RESPONSE
(MAX8805Y/MAX8805Z)**

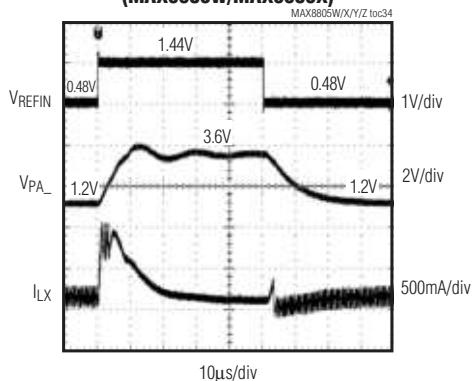


600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

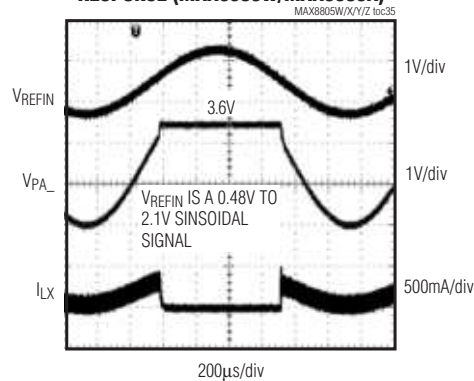
Typical Operating Characteristics (continued)

($V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V$, $V_{PA_} = 1.2V$, $V_{LDO1} = 2.85V$, $V_{LDO2} = 2.85V$, $R_{PA} = 7.5\Omega$, circuit of Figure 5, $T_A = +25^\circ C$, unless otherwise noted.)

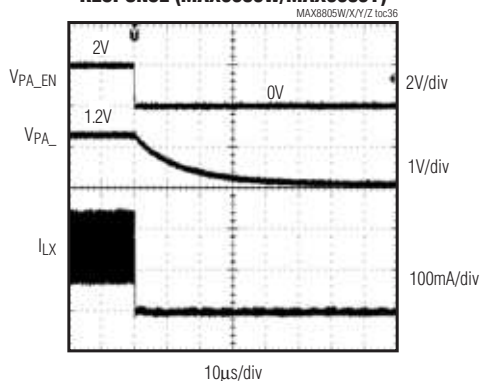
PA STEP-DOWN CONVERTER AUTOMATIC BYPASS-FET TRANSIENT RESPONSE (MAX8805W/MAX8805X)



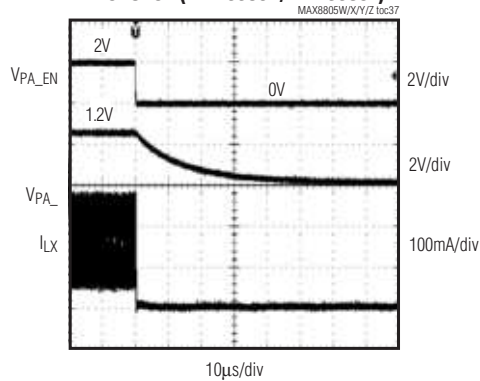
PA STEP-DOWN CONVERTER AUTOMATIC BYPASS-FET TRANSIENT RESPONSE (MAX8805W/MAX8805X)



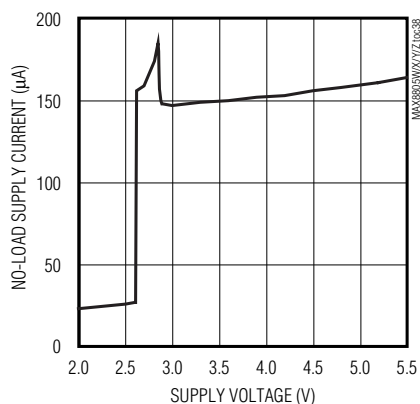
PA STEP-DOWN CONVERTER SHUTDOWN RESPONSE (MAX8805W/MAX8805Y)



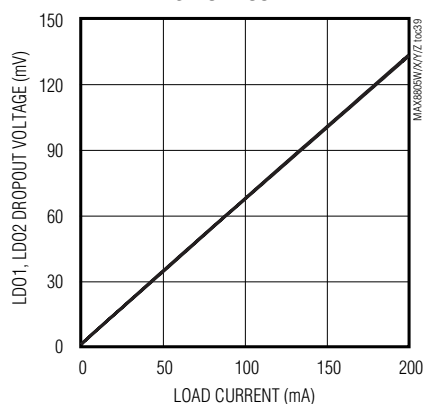
PA STEP-DOWN CONVERTER SHUTDOWN RESPONSE (MAX8805X/MAX8805Z)



LD01, LD02 SUPPLY CURRENT vs. SUPPLY VOLTAGE



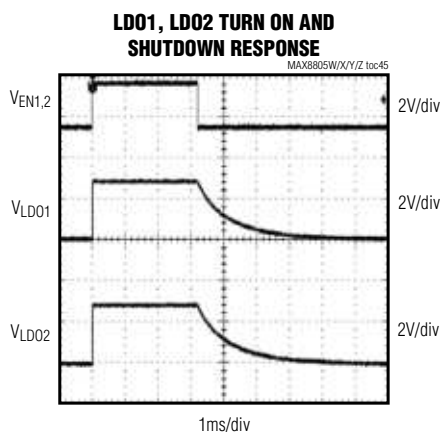
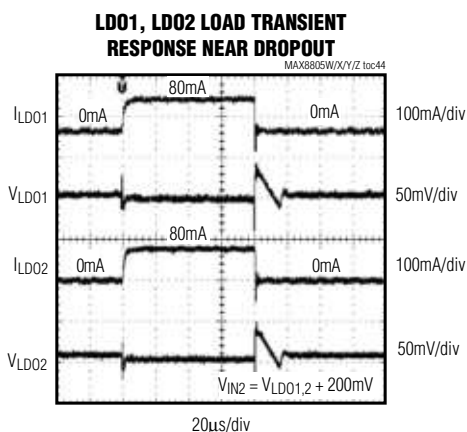
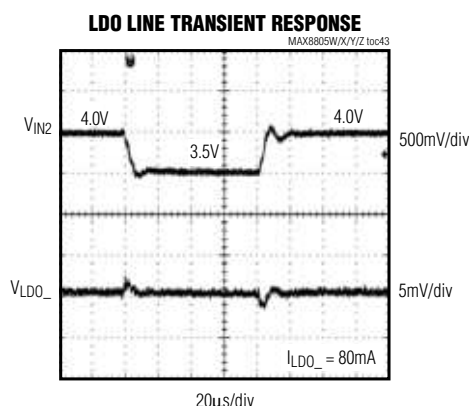
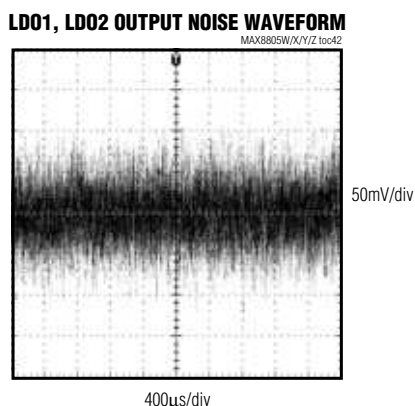
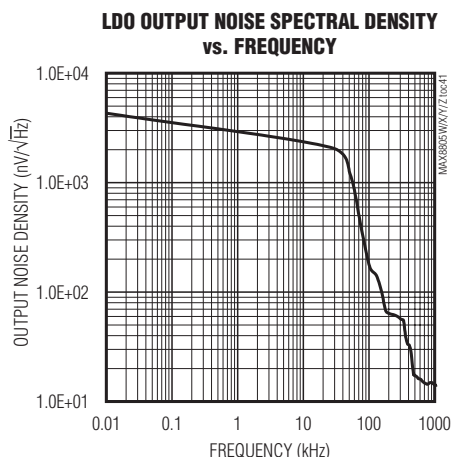
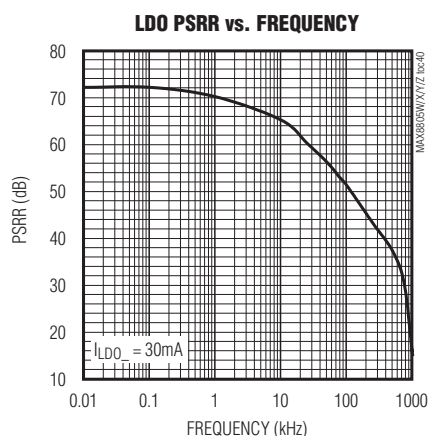
LD01, LD02 DROPOUT VOLTAGE vs. LOAD CURRENT



600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Typical Operating Characteristics (continued)

($V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V$, $V_{PA_} = 1.2V$, $V_{LDO1} = 2.85V$, $V_{LDO2} = 2.85V$, $R_{PA} = 7.5\Omega$, circuit of Figure 5, $T_A = +25^\circ C$, unless otherwise noted.)



600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Pin Description

PIN	NAME	FUNCTION
A1	REFBP	Reference Noise Bypass. Bypass REFBP to AGND with a 0.22 μ F ceramic capacitor to reduce noise on the LDO outputs. REFBP is internally pulled down through a 1k Ω resistor during shutdown.
A2	AGND	Low-Noise Analog Ground
A3	REFIN	DAC-Controlled Input. The output of the PA step-down converter is regulated to 2 x VREFIN for the MAX8805Y/MAX8805Z and 2.5 x VREFIN for the MAX8805W/MAX8805X. When VREFIN reaches 0.465 x VIN2 for the MAX8805Y/MAX8805Z and 0.372 x VIN2 for the MAX8805W/MAX8805X, bypass mode is enabled.
A4	PGND	Power Ground for PA Step-Down Converter
B1	LDO2	200mA LDO Regulator 2 Output. Bypass LDO2 with a 1 μ F ceramic capacitor as close as possible to LDO2 and AGND. LDO2 is internally pulled down through a 1k Ω resistor when this regulator is disabled.
B2	PA_EN	PA Step-Down Converter Enable Input. Connect to IN_ or logic-high for normal operation. Connect to GND or logic-low for shutdown mode.
B3	EN2	LDO2 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
B4	LX	Inductor Connection. Connect an inductor from LX to the output of the PA step-down converter.
C1	IN2	Supply Voltage Input for LDO1, LDO2, and Internal Reference. Connect IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN2 with a 2.2 μ F ceramic capacitor as close as possible to IN2 and AGND. Connect IN2 to the same source as IN1A and IN1B.
C2	HP	High-Power Mode Set Input. Drive HP high to invoke forced bypass mode. Bypass mode connects the input of the PA step-down converter directly to its output through the internal bypass MOSFET. Drive HP low to disable the forced bypass mode.
C3, C4	IN1B, IN1A	Supply Voltage Input for PA Step-Down Converter. Connect IN1_ to a battery or supply voltage from 2.7V to 5.5V. Bypass the connection of IN1_ with a 2.2 μ F ceramic capacitor as close as possible to IN1_, and PGND. IN1A and IN1B are internally connected together. Connect IN1_ to the same source as IN2.
D1	LDO1	200mA LDO Regulator 1 Output. Bypass LDO1 with a 1 μ F ceramic capacitor as close as possible to LDO1 and AGND. LDO1 is internally pulled down through a 1k Ω resistor when this regulator is disabled.
D2	EN1	LDO1 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
D3, D4	PAB, PAA	PA Connection for Bypass Mode. Internally connected to IN1_ using the internal bypass MOSFET during bypass mode. PA_ is connected to the internal feedback network. Bypass PA_ with a 2.2 μ F ceramic capacitor as close as possible to PA_ and PGND.

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

MAX8805W/MAX8805X/MAX8805Y/MAX8805Z

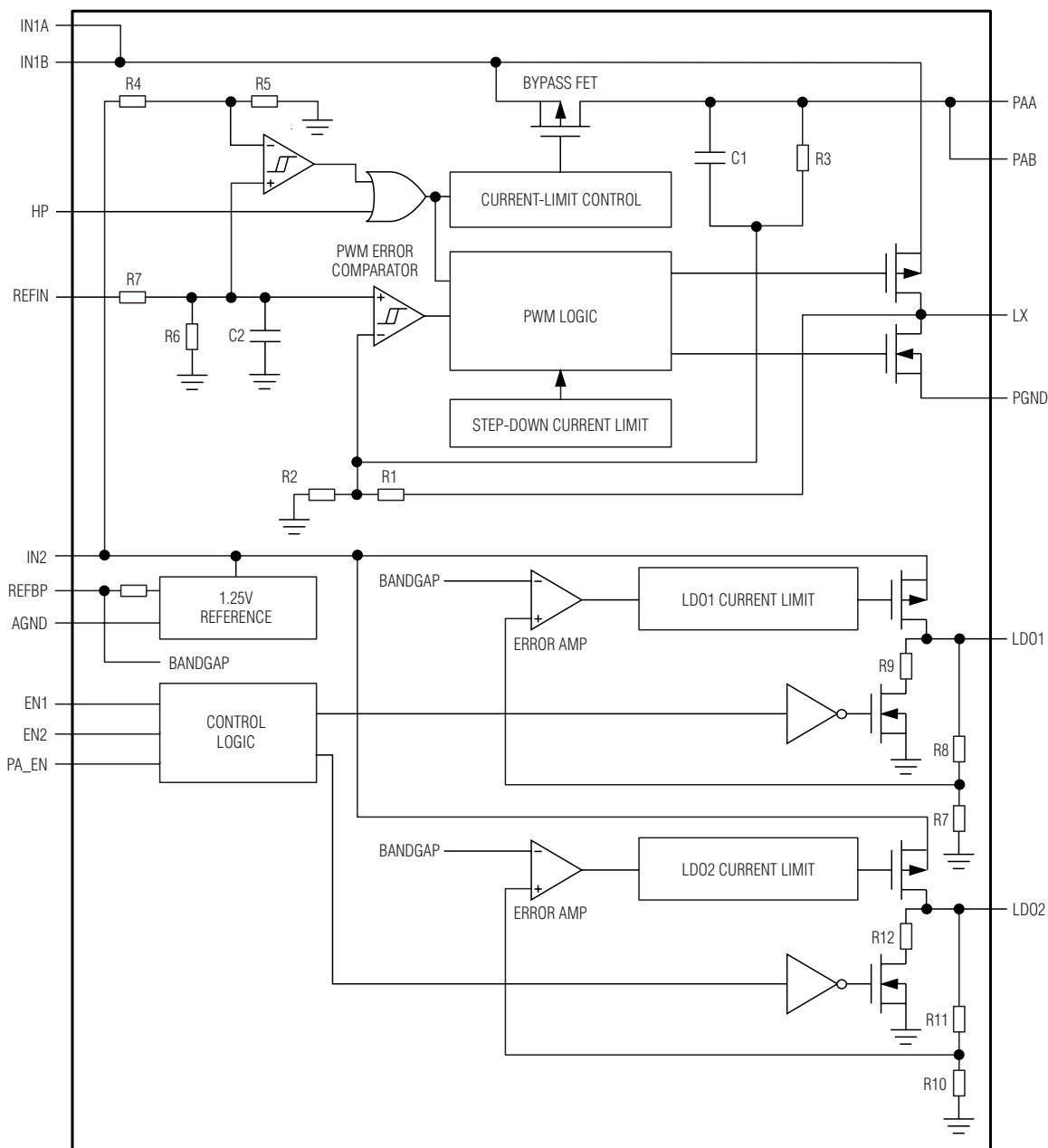


Figure 1. Block Diagram

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Detailed Description

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z are designed to dynamically power the PA in WCDMA and NCDMA handsets. The devices contain a high-frequency, high-efficiency step-down converter, and two LDOs. The MAX8805Y/MAX8805Z step-down converters deliver over 600mA, while the MAX8805W/MAX8805X deliver over 650mA. The hysteretic PWM control scheme provides extremely fast transient response, while 2MHz and 4MHz switching-frequency options allow the trade-off between efficiency and the smallest external components. A 60mΩ bypass FET connects the PA directly to the battery during high-power transmission.

Step-Down Converter Control Scheme

A hysteretic PWM control scheme ensures high efficiency, fast switching, fast transient response, low-output ripple, and physically tiny external components. The control scheme is simple: when the output voltage is below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This high-side switch remains on until the minimum on-time expires and the output voltage is within regulation, or the inductor current is above the current-limit threshold. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls again below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until the high-side switch turns on again. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z step-down converters utilize a unique feedback network. By taking DC feedback from the LX node through R1 in Figure 1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of very small ceramic output capacitors. To improve the load regulation, resistor R3 is included in the feedback. This configuration yields load regulation equal to half of the inductor's series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients or when changing the output voltage from one level to another. However, when calculating the required REFIN voltage, the load regulation should be considered. Because inductor resistance is typically well specified and the typical PA is a resistive load, the MAX8805Y/MAX8805Z V_{REFIN} to V_{OUT} gain is slightly less than 2V/V, and the MAX8805W/MAX8805X V_{REFIN} to V_{OUT} gain is slightly less than 2.5V/V. The output voltage is approximately:

$$V_{OUT} = (REFIN \text{ to } PA_Gain) \times V_{REFIN} - 1/2 \times I_{ESR} \times I_{LOAD}$$

Step-Down Converter Bypass Mode

During high-power transmission, the bypass mode connects IN1A and IN1B directly to PAA and PAB with the internal 60mΩ (typ) bypass FET, while the step-down converter is forced into 100% duty-cycle operation. The low on-resistance in this mode provides low dropout, long battery life, and high output current capability.

Forced and Automatic Bypass Mode

Invoke forced bypass mode by driving HP high or invoke automatic bypass mode by applying a high voltage to REFIN. To prevent excessive output ripple as the step-down converter approaches dropout, the MAX8805Y/MAX8805Z enter bypass mode automatically when $V_{REFIN} > 0.465 \times V_{IN2}$ (see Figure 2) and MAX8805W/MAX8805X enter bypass mode automatically when $V_{REFIN} > 0.372 \times V_{IN2}$. Note that IN2 is used instead of IN1 to prevent switching noise from causing false engagement of automatic bypass mode. For this reason, IN2 must be connected to the same source as IN1.

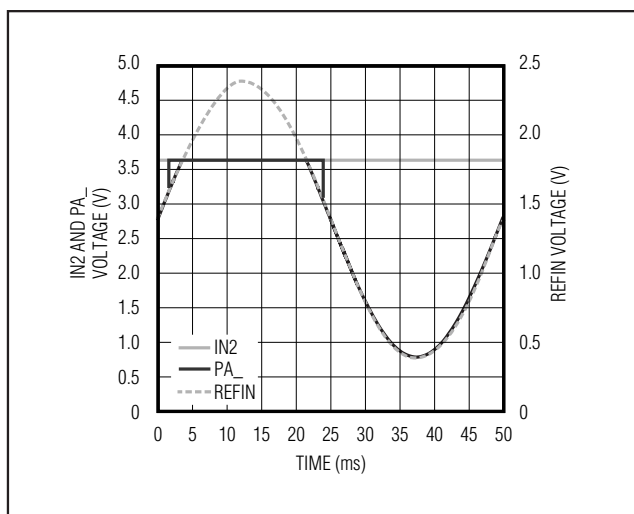


Figure 2. V_{IN2} and $V_{PA_}$ with Automatic Entry/Exit into Bypass Mode (MAX8805Y/MAX8805Z)

Shutdown Mode

Connect PA_EN to GND or logic-low to place the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z PA step-down converter in shutdown mode. In shutdown, the control circuitry, internal switching MOSFET, and synchronous rectifier turn off and LX becomes high impedance. Connect PA_EN to IN1_ or logic-high for normal operation.

Connect EN1 or EN2 to GND or logic-low to place LDO1 or LDO2, respectively, in shutdown mode. In

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

shutdown, the outputs of the LDOs are pulled to ground through an internal 1k Ω resistor.

When the PA step-down and LDOs are all in shutdown, the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z enter a very low power state, where the input current drops to 0.1 μ A (typ).

Step-Down Converter Soft-Start

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z PA step-down converter has internal soft-start circuitry that limits inrush current at startup, reducing transients on the input source. Soft-start is particularly useful for supplies with high output impedance such as Li+ and alkaline cells. See the PA Step-Down Soft-Start Waveforms (MAX8805X/MAX8805Z) and PA Step-Down Soft-Start Waveforms (MAX8805W/MAX8805Y) in the *Typical Operating Characteristics*.

Analog REFIN Control

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z PA step-down converter uses REFIN to set the output voltage. This allows the converter to operate in applications where dynamic voltage control is required.

Thermal Shutdown

Thermal shutdown limits total power dissipation in the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z. If the junction temperature exceeds +160°C, thermal-shutdown circuitry turns off the IC, allowing it to cool. The IC turns on and begins soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

Applications Information

Output Voltages

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z PA step-down converters set the PA_{OUT} output voltage based on the voltage applied to REFIN.

LDO1 and LDO2 output voltages are determined by the part number suffix, as shown in Table 1.

LDO Dropout Voltage

The regulator's minimum input/output differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z LDOs use a p-channel MOSFET pass transistor, their dropout voltages are a function of drain-to-source on-resistance (R_{DS(ON)}) multiplied by the load current (see the *Typical Operating Characteristics*).

Table 1. LDO1 and LDO2 Output Voltage Selection

PART	FREQUENCY (MHz)	LDO1 (V)	LDO2 (V)
MAX8805WE_EAA+T	2	1.80	1.80
MAX8805WE_EAE+T	2	1.80	2.85
MAX8805WE_EEE+T	2	2.85	2.85
MAX8805XE_EAA+T	4	1.80	1.80
MAX8805XE_EAE+T	4	1.80	2.85
MAX8805XE_EEE+T	4	2.85	2.85
MAX8805YE_EAA+T	2	1.80	1.80
MAX8805YE_EAE+T	2	1.80	2.85
MAX8805YE_EEE+T	2	2.85	2.85
MAX8805ZE_EAA+T	4	1.80	1.80
MAX8805ZE_EAE+T	4	1.80	2.85
MAX8805ZE_EEE+T	4	2.85	2.85

Note: Contact the factory for other output-voltage options.

Inductor Selection

The MAX8805W/MAX8805Y operate with a switching frequency of 2MHz and utilize a 2.2 μ H inductor. The MAX8805X/MAX8805Z operate with a switching frequency of 4MHz and utilize a 1 μ H inductor. The higher switching frequency of the MAX8805X/MAX8805Z allow the use of physically smaller inductors at the cost of slightly lower efficiency. The lower switching frequency of the MAX8805W/MAX8805Y results in greater efficiency at the cost of a physically larger inductor. See the *Typical Operating Characteristics* for efficiency graphs for both the MAX8805W/MAX8805Y and MAX8805X/MAX8805Z.

The inductor's DC current rating only needs to match the maximum load of the application because the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z feature zero current overshoot during startup and load transients. For optimum transient response and high efficiency, choose an inductor with DC series resistance in the 50m Ω to 150m Ω range. See Table 2 for suggested inductors and manufacturers.

Output Capacitor Selection

For the PA step-down converter, the output capacitor (C_{PA}) is required to keep the output voltage ripple small and ensure regulation loop stability. C_{PA} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended.

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Table 2. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (μH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS (mm)
Coilcraft	LPO3310	1.0	0.07	1600	3.3 x 3.3 x 1.0 = 11mm ³
		1.5	0.10	1400	
		2.2	0.13	1100	
FDK	MIPF2520	1.0	0.05	1500	2.5 x 2.0 x 1.0 = 5mm ³
		1.5	0.07	1500	
		2.2	0.08	1300	
	MIPS2520	1.3	0.09	1500	2.5 x 2.0 x 1.0 = 5mm ³
		2.0	0.11	1200	
	MIPF2016	1.0	0.11	1100	2.0 x 1.6 x 1.0 = 3.2mm ³
Hitachi	KSLI-252010	1.5	0.115	—	2.5 x 2.0 x 1.0 = 5mm ³
		2.2	0.080		
Murata	LQH32C_53	1.0	0.06	1000	3.2 x 2.5 x 1.7 = 14mm ³
		2.2	0.10	790	
Sumida	CDRH2D09	1.2	0.08	590	3.0 x 3.0 x 1.0 = 9mm ³
		1.5	0.09	520	
		2.2	0.12	440	
Taiyo Yuden	CDRH2D11	1.5	0.05	680	3.2 x 3.2 x 1.2 = 12mm ³
		2.2	0.08	580	
		3.3	0.10	450	
	CB2518T	2.2	0.09	510	2.5 x 1.8 x 2.0 = 9mm ³
		4.7	0.13	340	
TOKO	D3010FB	1.0	0.20	1170	3.0 x 3.0 x 1.0 = 9mm ³
	D2812C	1.2	0.09	860	3.0 x 3.0 x 1.2 = 11mm ³
		2.2	0.15	640	
	D310F	1.5	0.13	1230	3.6 x 3.6 x 1.0 = 13mm ³
		2.2	0.17	1080	
	D312C	1.5	0.10	1290	3.6 x 3.6 x 1.2 = 16mm ³
		2.2	0.12	1140	

due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. A 2.2μF capacitor is recommended for most applications. For optimum load-transient performance and very low output ripple, the output capacitor value can be increased.

For LDO1 and LDO2, the minimum output capacitance required is dependent on the load currents. For loads less than 10mA, it is sufficient to use a 0.1μF capacitor for stable operation over the full temperature range. With rated maximum load currents, a minimum of 1μF is recommended. Reduce output noise and improve load-

transient response, stability, and power-supply rejection by using larger output capacitors.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it is necessary to use 2.2μF or larger to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 1μF is sufficient at all operating temperatures. These regulators are optimized for ceramic capacitors. Tantalum capacitors are not recommended.

Input Capacitor Selection

The input capacitor (C_{IN1}) of the PA converter reduces the current peaks drawn from the battery or input power source and reduces switching noise in the

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

MAX8805W/MAX8805X/MAX8805Y/MAX8805Z. The impedance of C_{IN1} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. A 2.2 μ F capacitor is recommended for most applications. For optimum noise immunity and low input ripple, the input capacitor value can be increased.

For the LDOs, use an input capacitance equal to the value of the sum of the output capacitance of LDO1 and LDO2. Larger input capacitor values and lower ESR provide better noise rejection and line transient response.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use two times the sum of the output capacitor values of LDO1 and LDO2 (or larger) to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, a capacitance equal to the sum is sufficient at all operating temperatures.

Thermal Considerations

In most applications, the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z do not dissipate much heat due to their high efficiency. However, in applications where the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z run at high ambient temperature with heavy loads, the heat dissipated may exceed the maximum junction temperature of the IC. If the junction temperature reaches approximately +160°C, all power switches are turned off and LX and PA_ become high impedance, and LDO1 and LDO2 are pulled down to ground through an internal 1k Ω pulldown resistor.

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipated in the device is:

$$P_{DISS} = P_{PA} \times (1/\eta_{PA} - 1) + I_{LDO1} \times (V_{IN2} - V_{LDO1}) + I_{LDO2} \times (V_{IN2} - V_{LDO2})$$

where η_{PA} is the efficiency of the PA step-down converter and P_{PA} is the output power of the PA step-down converter.

The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A) / \theta_{JA}$$

where $(T_{JMAX} - T_A)$ is the temperature difference between the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z die junction and the surrounding air; θ_{JA} is the thermal resistance of the junction through the PCB, copper traces, and other materials to the surrounding air.

PCB Layout

High switching frequencies and relatively large peak currents make the PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, resulting in a stable and well-regulated output. Connect C_{IN1} close to IN1A/IN1B and PGND. Connect the inductor and output capacitor as close as possible to the IC and keep their traces short, direct, and wide. Keep noisy traces, such as the LX node, as short as possible. Figure 3 illustrates an example PCB layout and routing scheme.

MAX8805W/MAX8805X/MAX8805Y/MAX8805Z

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

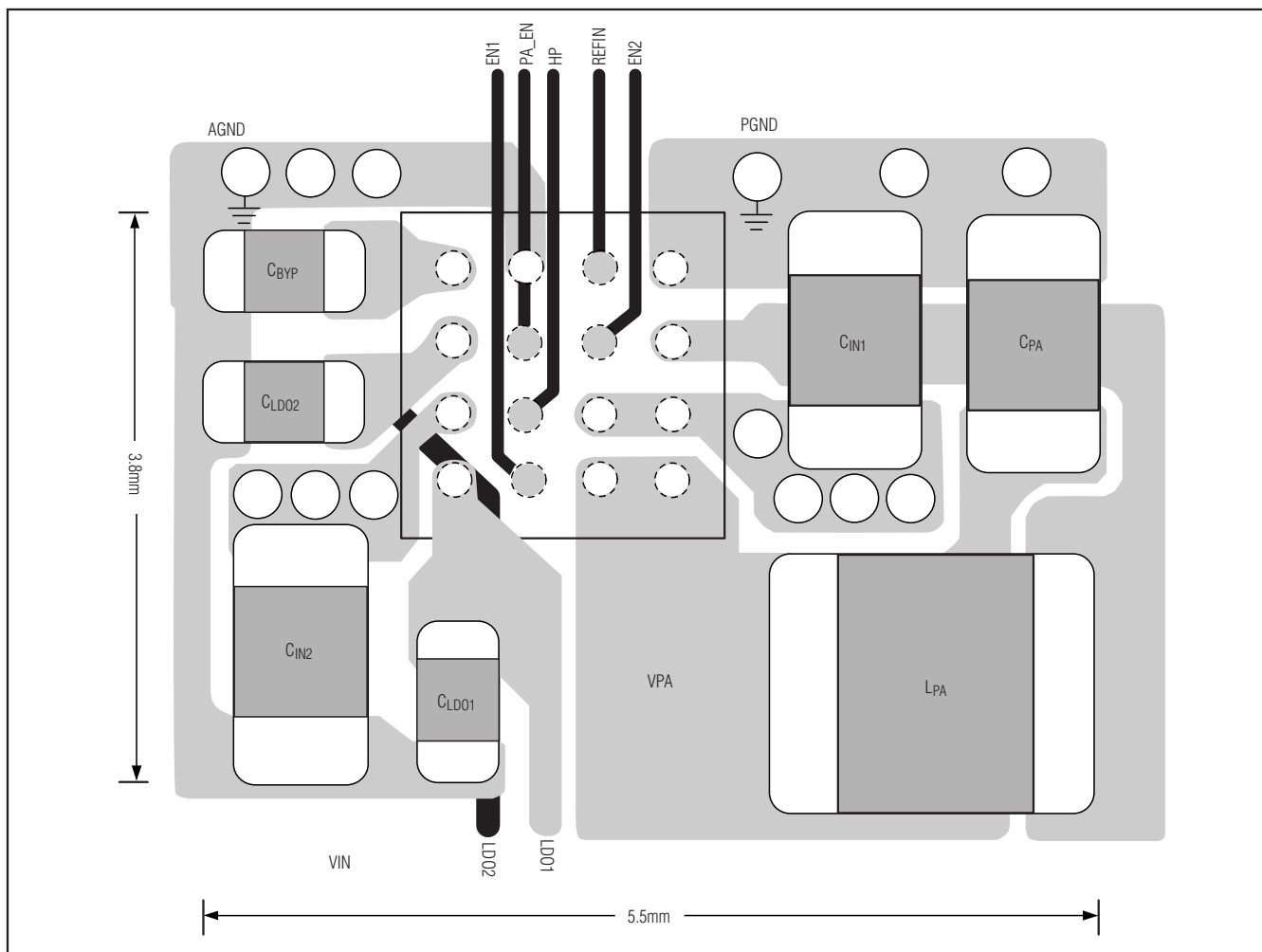


Figure 3. Recommended PCB Layout

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

MAX8805W/MAX8805X/MAX8805Y/MAX8805Z

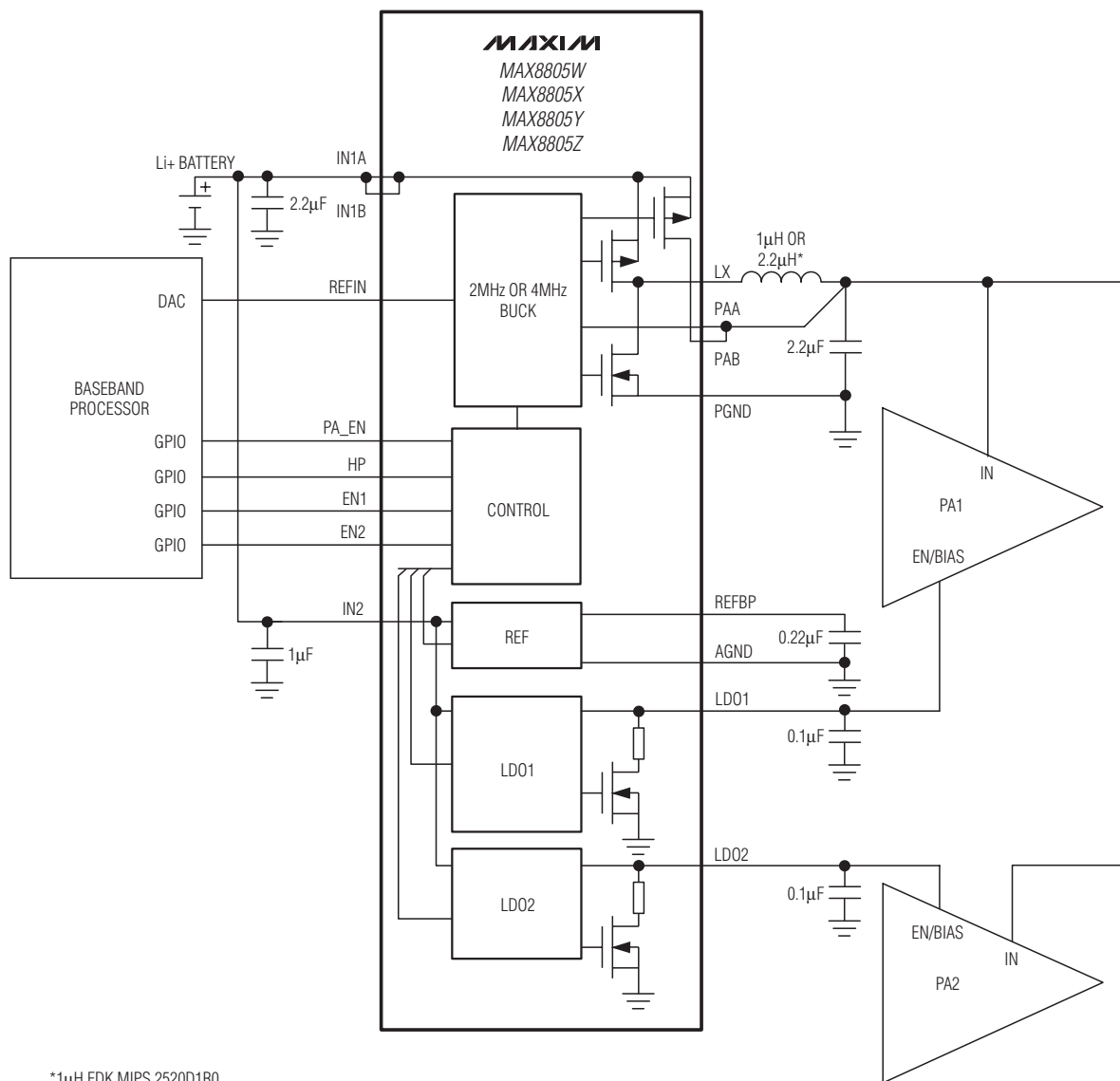
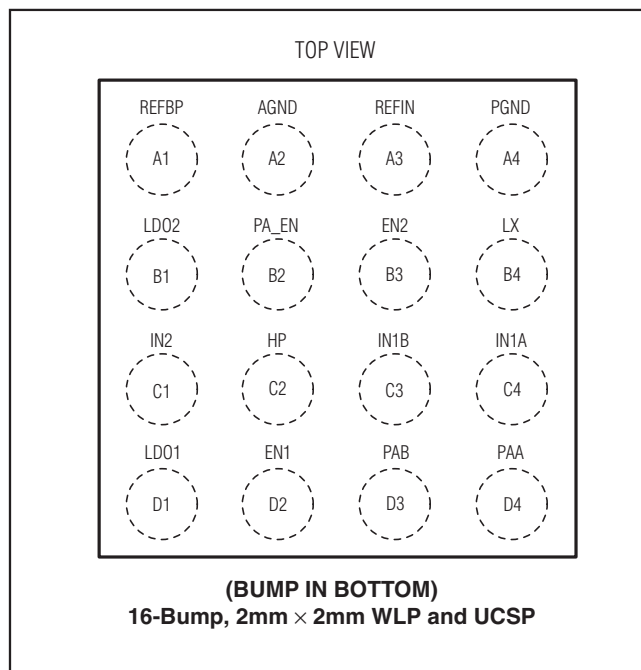


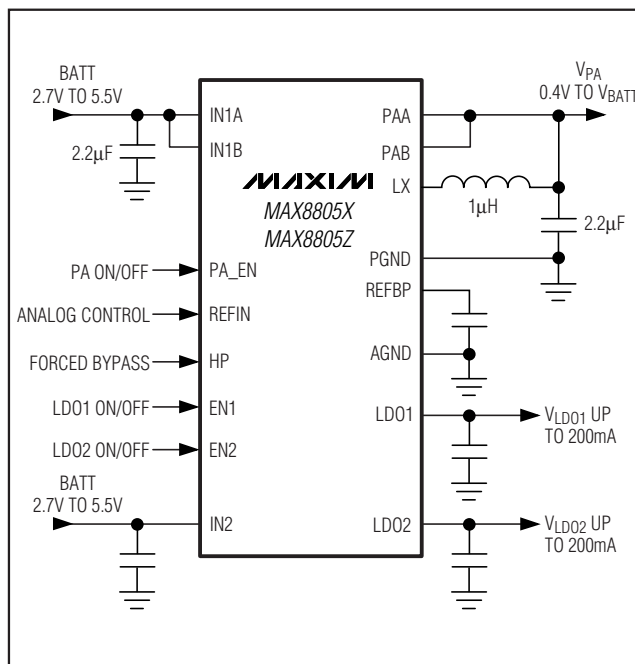
Figure 4. Typical Application Circuit Using LDOs for PA Enable/Bias

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Pin Configuration



Typical Operating Circuit



Ordering Information (continued)

PART	PIN-PACKAGE	SWITCHING FREQUENCY	REFIN TO OUT GAIN
MAX8805WEWExy+T*	16 WLP	2MHz	2.5V/V
MAX8805XEWExy+T*	16 WLP	4MHz	2.5V/V
MAX8805YEWExy+T*	16 WLP	2MHz	2V/V
MAX8805ZEWExy+T*	16 WLP	4MHz	2V/V

+Denotes a lead-free/RoHS-compliant package.

T = Tape and reel.

*xy is the output voltage code (see Table 1).

Note: All devices are specified over the -40°C to +85°C operating temperature range.

Chip Information

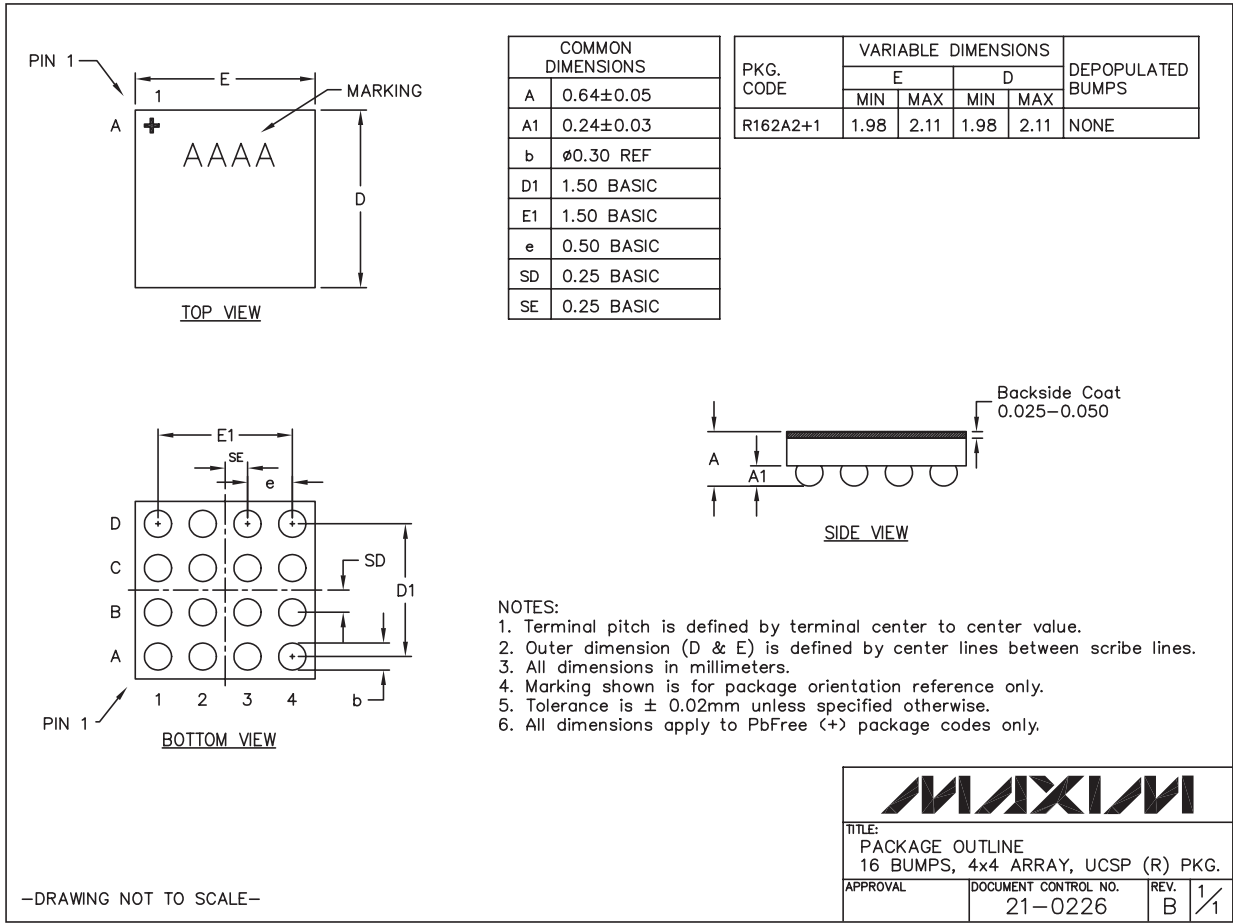
PROCESS: BiCMOS

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 UCSP	R162A2+1	21-0226
16 WLP	W162B2+1	21-0200



MAX8805W/MAX8805X/MAX8805Y/MAX8805Z

TOP VIEW

SIDE VIEW

COMMON DIMENSIONS

COMMON DIMENSIONS	
A	0.64±0.05
A1	0.24±0.03
A2	0.40 REF
A3	0.025 BASIC
b	∅0.31±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

NOTES:

1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front-side finish can be either Black or Clear.

PKG. CODE

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W162B2+1	1.98	2.11	1.98	2.11	NONE
W162C2+1	2.12	2.26	1.99	2.13	NONE
W162D2+1	1.99	2.01	1.99	2.01	B3, C2

—DRAWING NOT TO SCALE—

600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	3/08	Updating package information	21
3	5/08	Corrected maximum range of Y axis for TOC 03	5
4	9/08	Updated EC table, TOC 13, and <i>Voltage-Positioning Load Regulation</i> section	1, 2, 3, 6, 14
5	2/10	Added UCSP package	1-4, 15, 22

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