Dual 4-Stage Binary Ripple Counter

High−Performance Silicon−Gate CMOS

MC74HC393A

The MC74HC393A is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4−bit binary ripple counters with parallel outputs from each counter stage. A ÷ 256 counter can be obtained by cascading the two binary counters.

Internal flip−flops are triggered by high−to−low transitions of the clock input. Reset for the counters is asynchronous and active−high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393A.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 236 FETs or 59 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

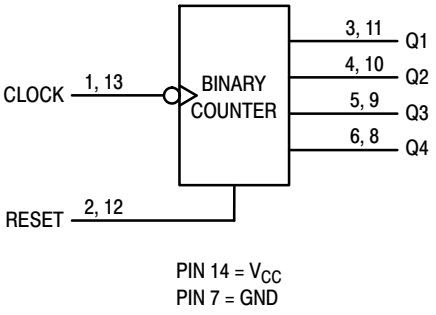
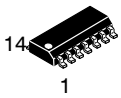
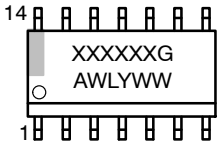


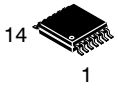
Figure 1. Logic Diagram

MARKING DIAGRAMS

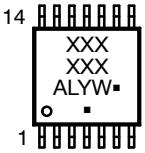


SOIC−14
D SUFFIX
CASE 751A





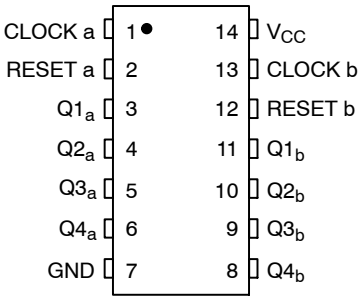
TSSOP−14
DT SUFFIX
CASE 948G



XXX = Specific Device Code
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		
Clock	**Reset**	**Outputs**
X	H	L
H	L	No Change
L	L	No Change
↗	L	No Change
↘	L	Advance to Next State

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		±150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−14 QFN14 TSSOP−14	116 130 150	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−14 QFN14 TSSOP−20	1077 962 833	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 2)	2.0 3.0 4.5 6.0	10 15 30 50	9 14 28 45	8 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q1 (Figures 2 and 3)	2.0 3.0 4.5 6.0	70 40 24 20	80 45 30 26	90 50 36 31	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q2 (Figures 2 and 3)	2.0 3.0 4.5 6.0	100 56 34 20	105 70 45 38	180 100 55 48	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q3 (Figures 2 and 3)	2.0 3.0 4.5 6.0	130 80 44 37	150 105 55 47	180 130 70 58	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q4 (Figures 2 and 3)	2.0 3.0 4.5 6.0	160 110 52 44	250 185 65 55	300 210 82 65	ns
t_{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	80 48 30 26	95 65 38 33	110 75 50 43	ns

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Counter)*	35	pF

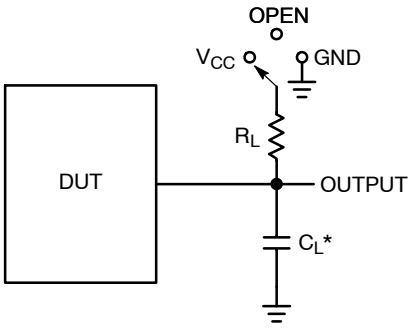
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 4)	2.0 3.0 4.5 6.0	25 15 10 9	30 20 13 11	40 30 15 13	ns
t_w	Minimum Pulse Width, Clock (Figure 3)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
t_w	Minimum Pulse Width, Reset (Figure 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0 3.0 4.5 6.0	1000 600 500 400	1000 600 500 400	1000 600 500 400	ns

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SWITCHING WAVEFORMS



*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 2. Test Circuit

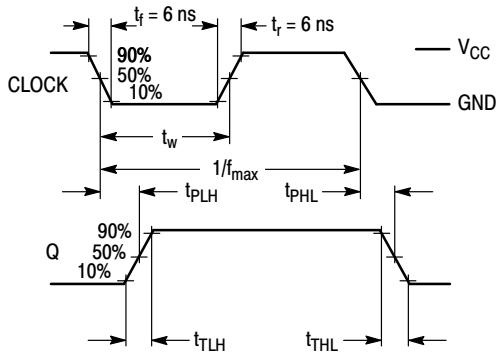


Figure 3.

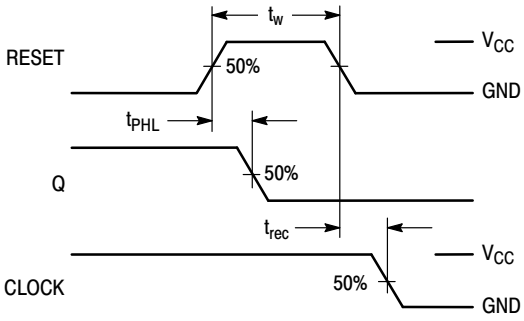


Figure 4.

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PIN DESCRIPTIONS

INPUTS

Clock (Pins 1, 13)

Clock input. The internal flip−flops are toggled and the counter state advances on high−to−low transitions of the clock input.

CONTROL INPUTS

Reset (Pins 2, 12)

Active−high, asynchronous reset. A separate reset is provided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

OUTPUTS

Q1, Q2, Q3, Q4 (Pins 3, 4, 5, 6, 8, 9, 10, 11)

Parallel binary outputs Q4 is the most significant bit.

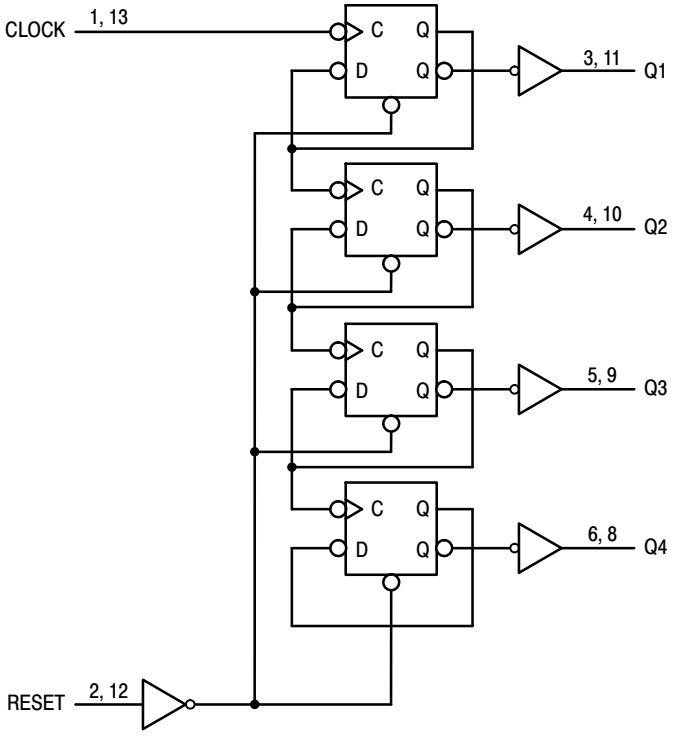


Figure 5. Expanded Logic Diagram

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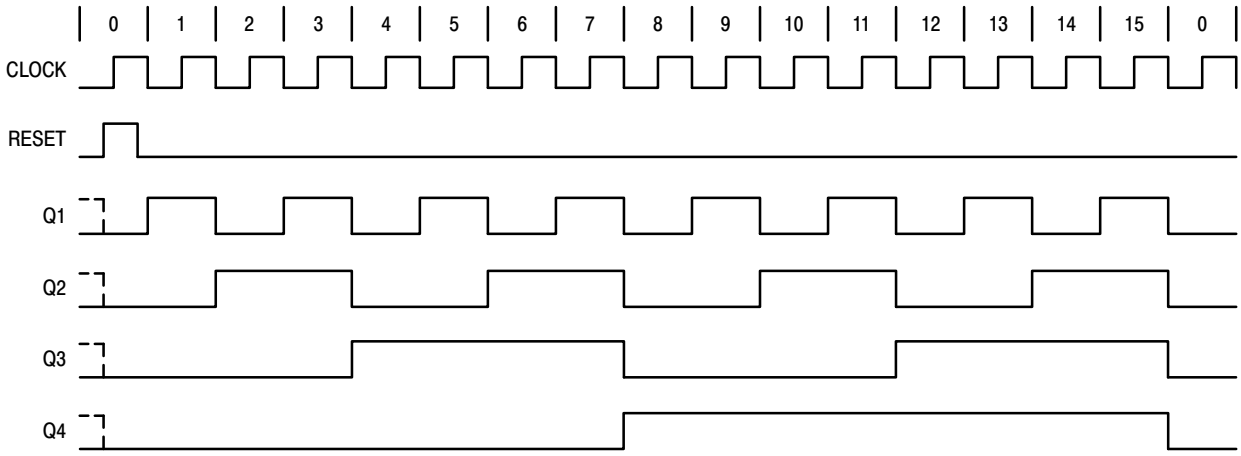


Figure 6. Timing Diagram

COUNT SEQUENCE

Count	Outputs			
	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

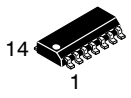
ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC393ADG	HC393AG	SOIC−14	55 Units / Rail
MC74HC393ADR2G	HC393AG	SOIC−14	2500 / Tape & Reel
MC74HC393ADR2G−Q*	HC393AG	SOIC−14	2500 / Tape & Reel
MC74HC393ADTR2G	HC 393A	TSSOP−14	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

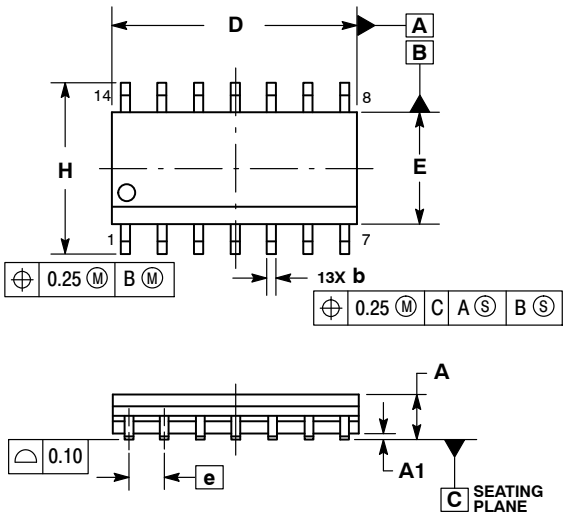
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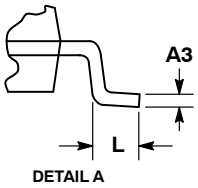


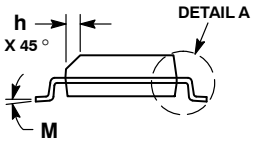
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ISSUE L

DATE 03 FEB 2016



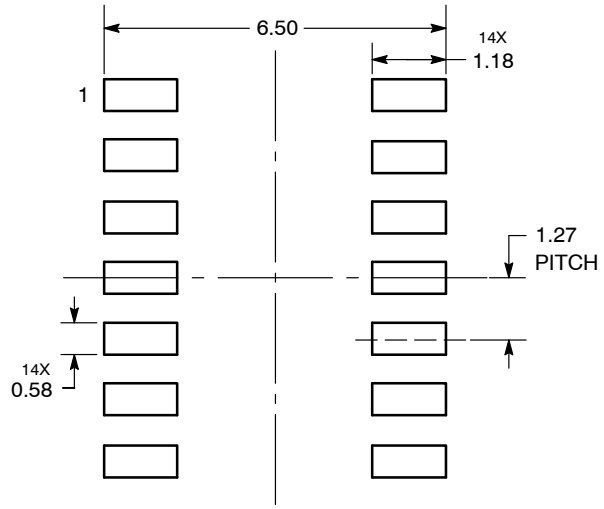




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

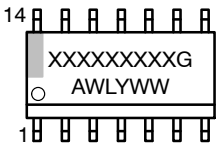
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

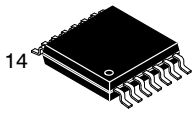
STYLE 6:
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7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
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12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

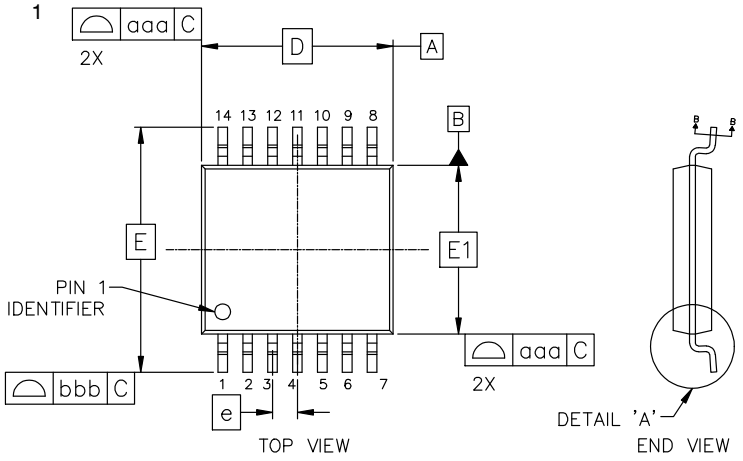
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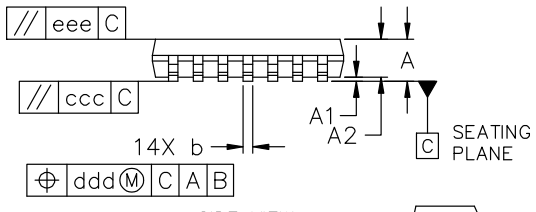
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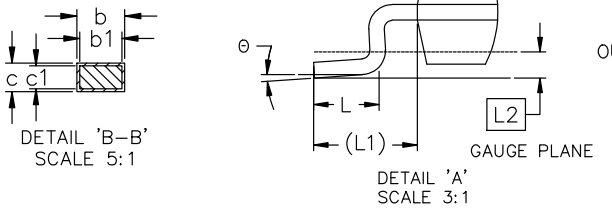


TSSOP−14 5.00x4.40x0.95, 0.65P
CASE 948G
ISSUE D

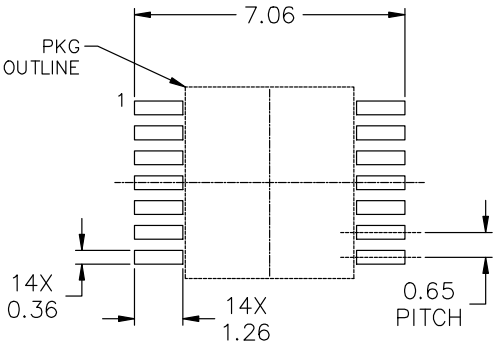
DATE 30 JUN 2026







MILLIMETERS			
DIM	MIN	NOM	MAX
A	−−−	−−−	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.19	0.25	0.30
b1	0.19	0.22	0.25
c	0.09	0.15	0.20
c1	0.09	0.12	0.16
D	5.00 BSC		
E	6.40 BSC		
E1	4.40 BSC		
e	0.65 BSC		
L	0.50	0.63	0.75
L1	1.00 REF		
L2	0.25 BSC		
θ	0°	4°	8°
TOLERANCE FORM & POSITION			
aaa	0.10		
bbb	0.15		
ccc	0.08		
ddd	0.10		
eee	0.10		

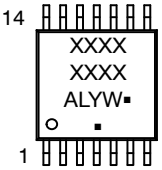


RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D DOES NOT INCLIDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 5.00x4.40x0.95, 0.65P**	**PAGE 1 OF 1**

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