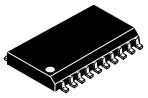
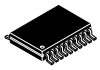
# Low-Voltage CMOS Octal Buffer Flow Through Pinout

## With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

# MC74LCX541

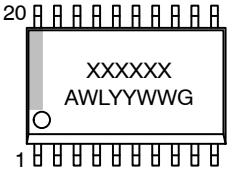


SOIC-20 WB
DW SUFFIX
CASE 751D

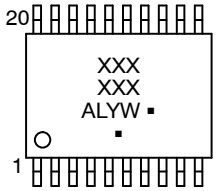


TSSOP-20
DT SUFFIX
CASE 948E

**MARKING DIAGRAM**




SOIC-20 WB




TSSOP-20

| | | |
|---|---|---|
| A | = | Assembly Location |
| L, WL | = | Wafer Lot |
| Y, YY | = | Year |
| W, WW | = | Work Week |
| G or ▪ | = | Pb-Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 8 of this data sheet.

The MC74LCX541 is a high performance, non-inverting octal buffer operating from a 1.65 to 5.5 V supply. This device is similar in function to the MC74LCX244, while providing flow through architecture. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_I$ specification of 5.5 V allows MC74LCX541 inputs to be safely driven from 5 V devices. The MC74LCX541 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs at $V_{CC}$ = 3 V. The Output Enable ($\overline{OE1}$. $\overline{OE2}$) inputs, when HIGH, disables the output by placing them in a HIGH Z condition.

### Features

- Designed for 1.65 to 5.5 V $V_{CC}$ Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$ Specification Guarantees High Impedance When $V_{CC}$ = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability at 3 V
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
  - ♦ Human Body Model > 2000 V
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

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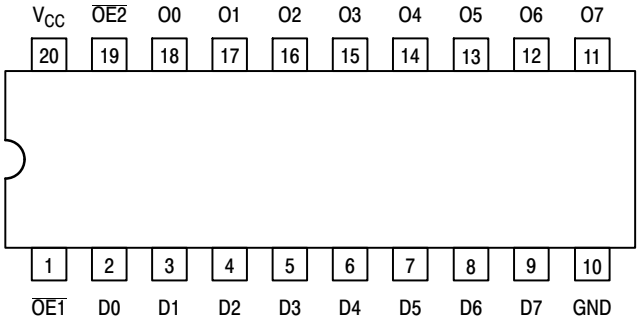



**Figure 1. Pinout: 20-Lead** (Top View)

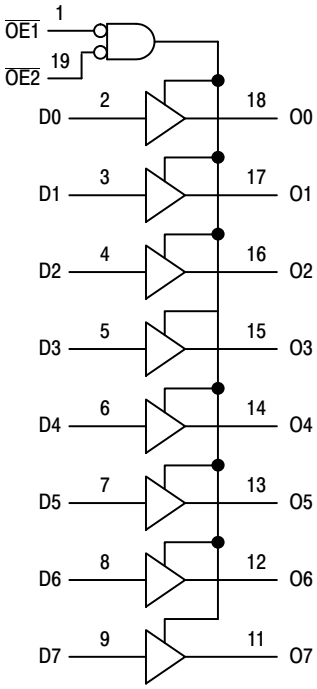



**Figure 2. Logic Diagram**

**PIN NAMES**

| Pin | Function |
|---|---|
| $\overline{OEn}$<br>Dn<br>On | Output Enable Inputs<br>Data Inputs<br>3-State Outputs |

**TRUTH TABLE**

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | Dn | On |
| L | L | L | L |
| L | L | H | H |
| X | H | X | Z |
| H | X | X | Z |

H = High Voltage Level;
L = Low Voltage Level;
Z = High Impedance State;
X = High or Low Voltage Level and Transitions are Acceptable, for $I_{CC}$ reasons, DO NOT FLOAT Inputs



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## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_I$ | DC Input Voltage (Note 1) | | −0.5 to +6.5 | V |
| $V_O$ | DC Output Voltage (Note 1) | Active-Mode (High or Low State) | −0.5 to $V_{CC}$ + 0.5 | V |
| | | Tri-State Mode | −0.5 to +6.5 | |
| | | Power-Down Mode ($V_{CC}$ = 0 V) | −0.5 to +6.5 | |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < GND | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND | −50 | mA |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ or $I_{GND}$ | DC Supply Current per Supply Pin or Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | SOIC-20W | 96 | °C/W |
| | | WQFN20 | 99 | |
| | | QFN20 | 111 | |
| | | TSSOP-20 | 150 | |
| $P_D$ | Power Dissipation in Still Air | SOIC-20W | 1302 | mW |
| | | WQFN20 | 1256 | |
| | | QFN20 | 1127 | |
| | | TSSOP-20 | 833 | |
| MSL | Moisture Sensitivity | SOIC-20W<br>All Other Packages | Level 3<br>Level 1 | – |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | – |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3) | Human Body Model<br>Charged Device Model | > 2000<br>N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_O$ absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.



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## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating | 1.65 | 3.3 | 5.5 | V |
| | | Data Retention Only | 1.5 | 3.3 | 5.5 | |
| $V_I$ | Digital Input Voltage | | 0 | – | 5.5 | V |
| $V_O$ | Output Voltage | Active Mode (High or Low State) | 0 | – | $V_{CC}$ | V |
| | | Tri-State Mode | 0 | – | 5.5 | |
| | | Power Down Mode ($V_{CC}$ = 0 V) | 0 | – | 5.5 | |
| $T_A$ | Operating Free-Air Temperature | | −40 | – | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate | $V_{CC}$ = 1.65 V to 1.95 V | 0 | – | 20 | nS/V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0 | – | 20 | |
| | | $V_I$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V | 0 | – | 10 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0 | – | 5 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | $T_A$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $V_{IH}$ | High-Level Input Voltage | | 1.65 to 1.95 | 0.65 x $V_{CC}$ | | 0.65 x $V_{CC}$ | | V |
| | | | 2.3 to 2.7 | 1.7 | | 1.7 | | |
| | | | 2.7 to 3.6 | 2.0 | | 2.0 | | |
| | | | 4.5 to 5.5 | 0.7 x $V_{CC}$ | | 0.7 x $V_{CC}$ | | |
| $V_{IL}$ | Low-Level Input Voltage | | 1.65 to 1.95 | | 0.35 x $V_{CC}$ | | 0.35 x $V_{CC}$ | V |
| | | | 2.3 to 2.7 | | 0.7 | | 0.7 | |
| | | | 2.7 to 3.6 | | 0.8 | | 0.8 | |
| | | | 4.5 to 5.5 | | 0.3 x $V_{CC}$ | | 0.3 x $V_{CC}$ | |
| $V_{OH}$ | High-Level Output Voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | V |
| | | $I_{OH}$ = −100 μA | 1.65 to 5.5 | $V_{CC}$ − 0.1 | – | $V_{CC}$ − 0.1 | – | |
| | | $I_{OH}$ = −4 mA | 1.65 | 1.2 | – | 1.2 | – | |
| | | $I_{OH}$ = −8 mA | 2.3 | 1.8 | – | 1.8 | – | |
| | | $I_{OH}$ = −12 mA | 2.7 | 2.2 | – | 2.2 | – | |
| | | $I_{OH}$ = −16 mA | 3.0 | 2.4 | – | 2.4 | – | |
| | | $I_{OH}$ = −24 mA | 3.0 | 2.2 | – | 2.2 | – | |
| | | $I_{OH}$ = −32 mA | 4.5 | 3.8 | | 3.8 | | |
| $V_{OL}$ | Low-Level Output Voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | V |
| | | $I_{OL}$ = 100 μA | 1.65 to 5.5 | – | 0.1 | – | 0.1 | |
| | | $I_{OL}$ = 4 mA | 1.65 | – | 0.45 | – | 0.45 | |
| | | $I_{OL}$ = 8 mA | 2.3 | – | 0.6 | – | 0.6 | |
| | | $I_{OL}$ = 12 mA | 2.7 | – | 0.4 | – | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3.0 | – | 0.4 | – | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | – | 0.55 | – | 0.55 | |
| | | $I_{OL}$ = 32 mA | 4.5 | | 0.6 | | 0.6 | |
| $I_I$ | Input Leakage Current | $V_I$ = 0 to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |



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## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | $T_A$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $I_{OZ}$ | 3-State Output Leakage Current | $V_I = V_{IH}$ or $V_{IL}$, $V_O$ = 0 V to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_I$ = 5.5 V or $V_O$ = 5.5 V | 0 | – | 10 | – | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_I$ = 5.5 V or GND | 3.6 | – | 10 | – | 10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC}$ – 0.6 V | 2.3 to 3.6 | – | 500 | – | 500 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These values of $V_I$ are used to test DC electrical characteristics only.

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | $T_A$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, D to O | See Figures 3 and 4 | 1.65 to 1.95 | – | 10.3 | – | 10.3 | ns |
| | | | 2.3 to 2.7 | – | 7.8 | – | 7.8 | |
| | | | 2.7 | – | 7.5 | – | 7.5 | |
| | | | 3.0 to 3.6 | – | 6.5 | – | 6.5 | |
| | | | 4.5 to 5.5 | – | 5.9 | – | 5.9 | |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time,OE to $\overline{OE}$ to O | See Figures 3 and 4 | 1.65 to 1.95 | – | 13.0 | – | 13.0 | ns |
| | | | 2.3 to 2.7 | – | 10.5 | – | 10.5 | |
| | | | 2.7 | – | 9.5 | – | 9.5 | |
| | | | 3.0 to 3.6 | – | 8.5 | – | 8.5 | |
| | | | 4.5 to 5.5 | – | 7.3 | – | 7.3 | |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time, $\overline{OE}$ to O | See Figures 3 and 4 | 1.65 to 1.95 | – | 11.0 | – | 11.0 | ns |
| | | | 2.3 to 2.7 | – | 9.0 | – | 9.0 | |
| | | | 2.7 | – | 8.5 | – | 8.5 | |
| | | | 3.0 to 3.6 | – | 7.5 | – | 7.5 | |
| | | | 4.5 to 5.5 | – | 6.5 | – | 6.5 | |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew (Note 5) | | 1.65 to 1.95 | – | – | – | – | ns |
| | | | 2.3 to 2.7 | – | – | – | – | |
| | | | 2.7 | – | – | – | – | |
| | | | 3.0 to 3.6 | – | 1.0 | – | 1.0 | |

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$); parameter guaranteed by design.



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## DYNAMIC SWITCHING CHARACTERISTICS

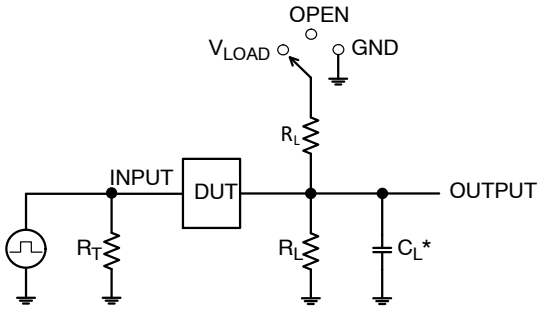
| Symbol | Characteristic | Condition | $T_A$ = +25 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 7) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V | | 0.8 | | V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 7) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V | | 0.8 | | V |

7. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typ | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | 10 MHz, $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 25 | pF |

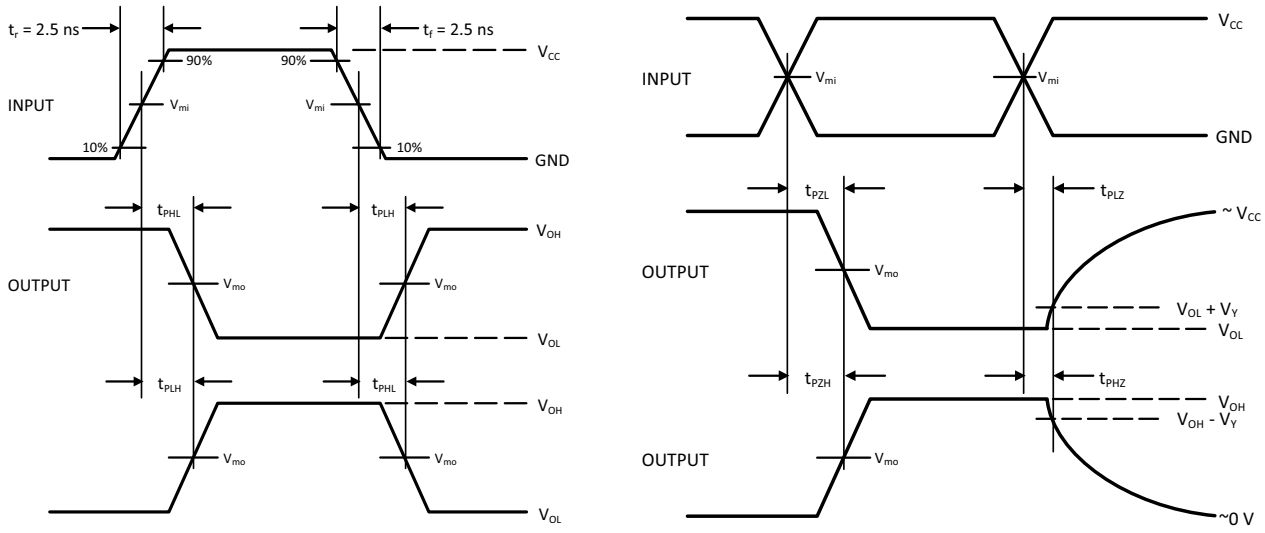

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| Test | Switch Position |
|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}$ / $t_{PZH}$ | GND |

$C_L$ includes probe and jig capacitance
$R_T$ is $Z_{OUT}$ of pulse generator (typically 50 Ω)
f = 1 MHz

**Figure 3. Test Circuit**




| $V_{CC}$, V | $R_L$, Ω | $C_L$, pF | $V_{LOAD}$ | $V_{mi}$, V | $V_{mo}$, V | $V_Y$, V |
|---|---|---|---|---|---|---|
| 1.65 to 1.95 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 2.3 to 2.7 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 2.7 | 500 | 50 | 6 V | 1.5 | $V_{CC}$/2 | 0.3 |
| 3.0 to 3.6 | 500 | 50 | 6 V | 1.5 | $V_{CC}$/2 | 0.3 |
| 4.5 to 4.5 | 500 | 50 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.3 |

**Figure 4. Switching Waveforms**



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## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MC74LCX541DWR2G | LCX541 | SOIC-20<br>(Pb-Free) | 1000 / Tape & Reel |
| MC74LCX541DWG | LCX541 | SOIC-20<br>(Pb-Free) | 38 Units / Rail |
| MC74LCX541DTG | LCX<br>541 | TSSOP-20<br>(Pb-Free) | 75 Units / Rail |
| MC74LCX541DTR2G | LCX<br>541 | TSSOP-20<br>(Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

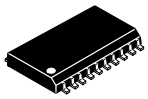
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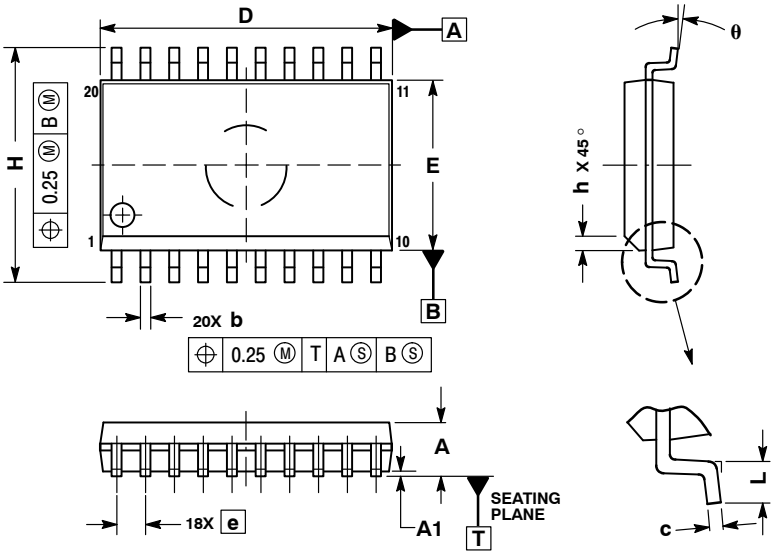
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**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



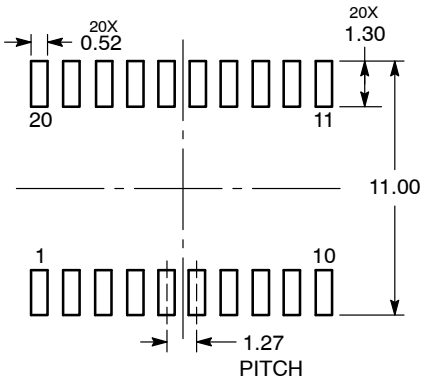
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

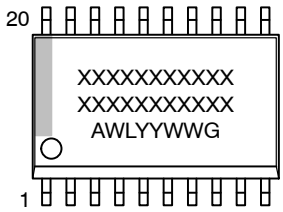
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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