# Low-Voltage CMOS Unbuffered Hex Inverter
## With 5 V-Tolerant Inputs

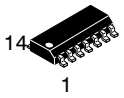
# MC74LCXU04

The MC74LCXU04 is a high performance unbuffered hex inverter operating from a 1.65 to 5.5 V supply. (High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance.) A $V_I$ specification of 5.5 V allows MC74LCXU04 inputs to be safely driven from 5 V devices.

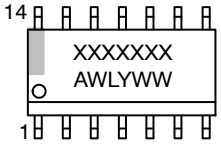
### Features

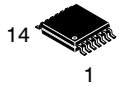
- Designed for 1.65 to 5.5 V $V_{CC}$ Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- Near Zero Static Supply Current (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
  - Human Body Model >2000 V
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

**MARKING DIAGRAMS**

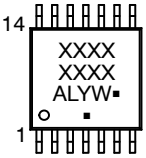



**SOIC–14**
**D SUFFIX**
**CASE 751A**




**TSSOP–14**
**DT SUFFIX**
**CASE 948G**




| | |
|---|---|
| XXXXXX | = Specific Device Code |
| A | = Assembly Location |
| L, WL | = Wafer Lot |
| Y, YY | = Year |
| W, WW | = Work Week |
| G or ▪ | = Pb–Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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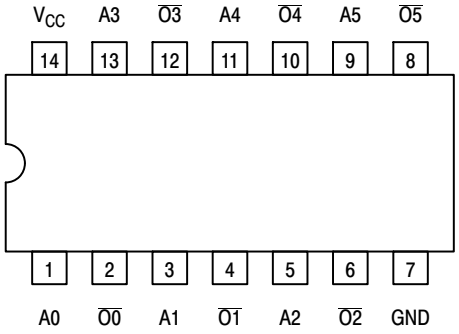



**Figure 1. Pinout: 14−Lead (Top View)**

**PIN NAMES**

| Pins | Function |
|---|---|
| An | Data Inputs |
| $\overline{On}$ | Outputs |

**TRUTH TABLE**

| An | $\overline{On}$ |
|---|---|
| L | H |
| H | L |

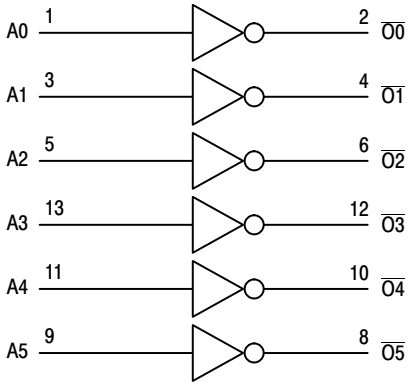



**Figure 2. Logic Diagram**

**MAXIMUM RATINGS**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_I$ | DC Input Voltage (Note 1) | | −0.5 to +6.5 | V |
| $V_O$ | DC Output Voltage (Note 1) | | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | $V_I$ < GND | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_O$ > $V_{CC}$, $V_O$ < GND | ±50 | mA |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ or $I_{GND}$ | DC Supply Current per Supply Pin or Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 1) | SOIC−14<br>TSSOP−14 | 116<br>150 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 125 °C | SOIC−14<br>TSSOP−14 | 1077<br>833 | mW |
| MSL | Moisture Sensitivity | | Level 1 | − |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | − |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3) | Human Body Model<br>Charged Device Model | >4000<br>>2000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_O$ absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.



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## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating<br>Data Retention Only | 1.65<br>1.5 | 3.3<br>3.3 | 5.5<br>5.5 | V |
| $V_I$ | Digital Input Voltage | | 0 | – | 5.5 | V |
| $V_O$ | Output Voltage | | 0 | – | $V_{CC}$ | V |
| $T_A$ | Operating Free−Air Temperature | | −40 | – | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate | $V_{CC}$ = 1.65 V to 1.95 V<br>$V_{CC}$ = 2.3 V to 2.7 V<br>$V_{IN}$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V<br>$V_{CC}$ = 4.5 V to 5.5 V | 0<br>0<br>0<br>0 | –<br>–<br>–<br>– | 20<br>20<br>10<br>5 | nS/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | $T_A$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 1.65 | 1.2 | – | 1.2 | – | V |
| | | | 2.3 | 1.7 | – | 1.7 | – | |
| | | | 2.7 | 2.1 | – | 2.1 | – | |
| | | | 3.0 | 2.2 | – | 2.2 | – | |
| | | | 3.6 | 2.7 | – | 2.7 | – | |
| | | | 4.5 | 3.4 | – | 3.4 | – | |
| $V_{IL}$ | LOW Level Input Voltage | | 1.65 | – | 0.4 | – | 0.4 | V |
| | | | 2.3 | – | 0.6 | – | 0.6 | |
| | | | 2.7 | – | 0.7 | – | 0.7 | |
| | | | 3.0 | – | 0.8 | – | 0.8 | |
| | | | 3.6 | – | 0.9 | – | 0.9 | |
| | | | 4.5 | – | 1.1 | – | 1.1 | |
| $V_{OH}$ | High−Level Output Voltage | $V_I$ = GND<br>$I_{OH}$ = −100 μA<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA<br>$I_{OH}$ = −12 mA<br>$I_{OH}$ = −18 mA<br>$I_{OH}$ = −24 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>4.5 | <br>$V_{CC}$ − 0.2<br>1.29<br>1.8<br>2.2<br>2.4<br>3.7 | <br>–<br>–<br>–<br>–<br>–<br>– | <br>$V_{CC}$ − 0.2<br>1.29<br>1.8<br>2.2<br>2.4<br>3.7 | <br>–<br>–<br>–<br>–<br>–<br>– | V |
| $V_{OL}$ | Low−Level Output Voltage | $V_I$ = $V_{CC}$<br>$I_{OL}$ = 100 μA<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA<br>$I_{OL}$ = 12 mA<br>$I_{OL}$ = 18 mA<br>$I_{OL}$ = 24 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>4.5 | <br>–<br>–<br>–<br>–<br>–<br>– | <br>0.2<br>0.36<br>0.6<br>0.4<br>0.5<br>0.55 | <br>–<br>–<br>–<br>–<br>–<br>– | <br>0.3<br>0.36<br>0.6<br>0.4<br>0.55<br>0.55 | V |
| $I_I$ | Input Leakage Current | $V_I$ = 0 to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_I$ = 5.5 V | 0 | – | 10 | – | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_I$ = 5.5 V or GND | 3.6 | – | 10 | – | 10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH}$ = $V_{CC}$ − 0.6 V | 2.3 to 3.6 | – | 500 | – | 500 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | $T_A$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, Input to Output | See Figures 3 and 4 | 1.65 to 1.95 | – | 4.6 | – | 4.6 | ns |
| | | | 2.3 to 2.7 | – | 4.3 | – | 4.3 | |
| | | | 2.7 | – | 4.5 | – | 4.5 | |
| | | | 3.0 to 3.6 | – | 3.6 | – | 3.6 | |
| | | | 4.5 to 5.5 | – | 3.3 | – | 3.3 | |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew | | 1.65 to 1.95 | – | – | – | – | ns |
| | | | 2.3 to 2.7 | – | – | – | – | |
| | | | 2.7 | – | – | – | – | |
| | | | 3.0 to 3.6 | – | 1.0 | – | 1.0 | |
| | | | 4.5 to 5.5 | – | – | – | – | |

5. These AC parameters are preliminary and may be modified.
6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW ($t_{OSHL}$) or LOW−to−HIGH ($t_{OSLH}$); parameter guaranteed by design.

## DYNAMIC SWITCHING CHARACTERISTICS

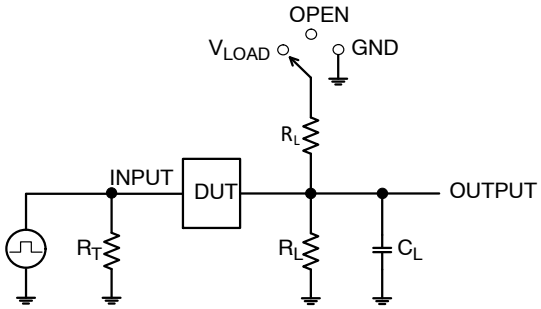
| Symbol | Characteristic | Condition | $T_A$ = +25 °C | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 7) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | 0.8<br>0.6 | | V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 7) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | −0.8<br>−0.6 | | V |

7. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | 10 MHz, $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 25 | pF |

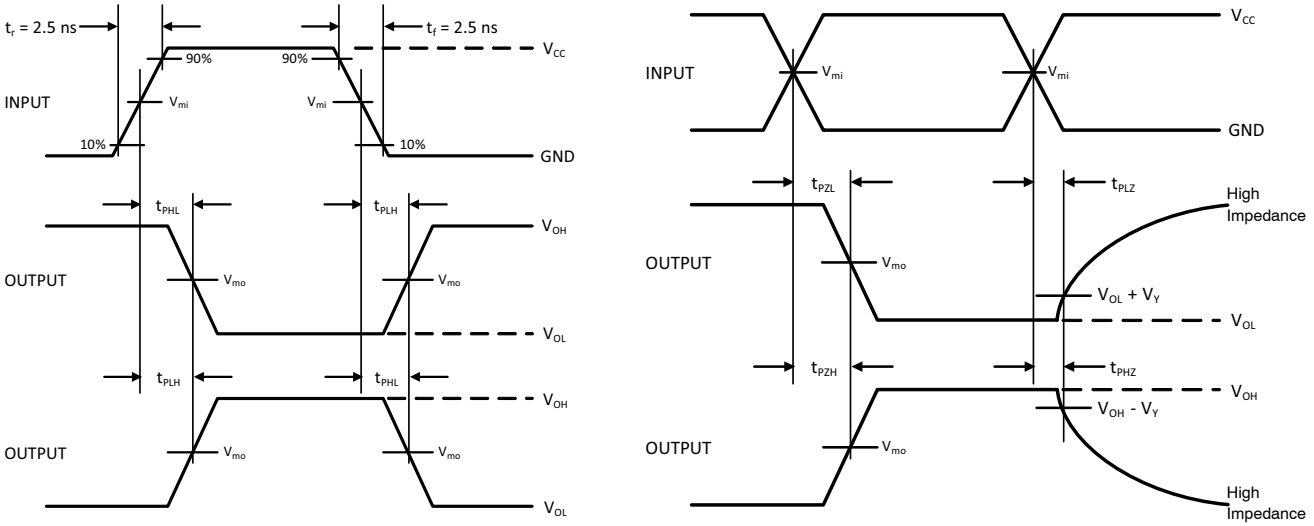

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| Test | Switch Position |
|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}$ / $t_{PZH}$ | GND |

$C_L$ includes probe and jig capacitance
$R_T$ is $Z_{OUT}$ of pulse generator (typically 50 Ω)
f = 1 MHz, tw = 500 ns

**Figure 3. Test Circuit**




| $V_{CC}$, V | $R_L$, Ω | $C_L$, pF | $V_{LOAD}$ | $V_m$, V | $V_Y$, V |
|---|---|---|---|---|---|
| 1.65 to 1.95 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | 0.15 |
| 2.3 to 2.7 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | 0.15 |
| 2.7 | 500 | 50 | 6 V | 1.5 | 0.3 |
| 3.0 to 3.6 | 500 | 50 | 6 V | 1.5 | 0.3 |
| 4.5 to 5.5 | 500 | 50 | 2 x $V_{CC}$ | $V_{CC}$/2 | 0.3 |

**Figure 4. Switching Waveforms**

## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MC74LCXU04DG | LCXU04G | SOIC−14 (Pb−Free) | 55 Units / Rail |
| MC74LCXU04DR2G | LCXU04G | SOIC−14 (Pb−Free) | 2500 Tape & Reel |
| MC74LCXU04DTR2G | LCX U04 | TSSOP−14 (Pb−Free) | 2500 Tape & Reel |
| MC74LCXU04DTR2G−Q* | LCX U04 | TSSOP−14 (Pb−Free) | 2500 Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



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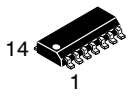
## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 13 | Updated ESD Withstand Voltage values. | 4/20/2026 |
| 14 | Added MC74LCXU04DTR2G−Q OPN to order table. | 8/5/2026 |

* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.



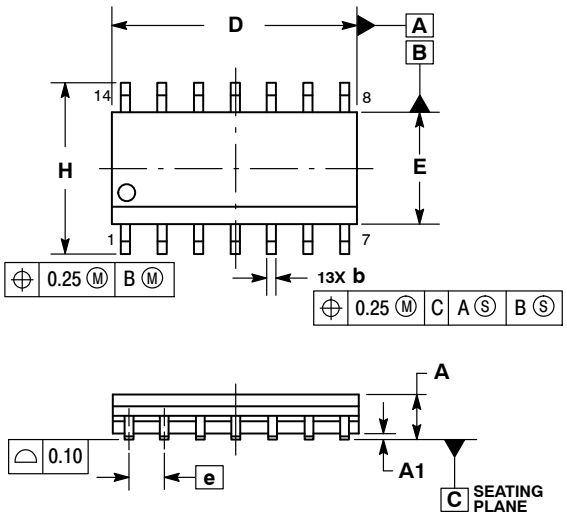
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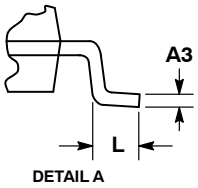


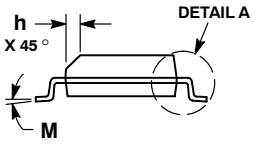

**SCALE 1:1**

**SOIC−14 NB**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



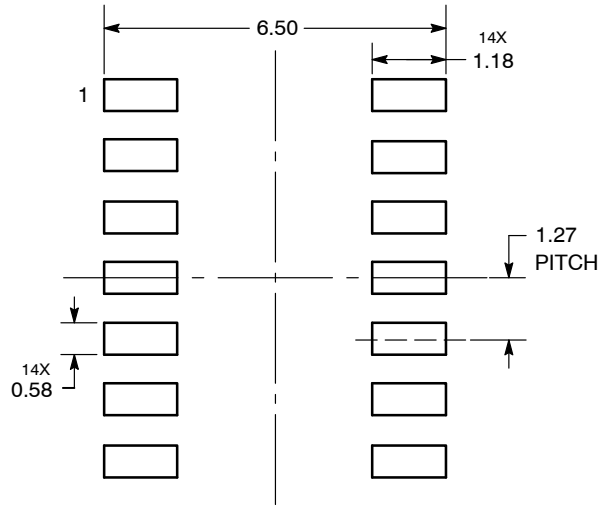




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |

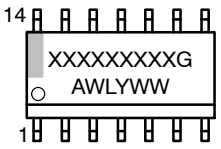
## SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **SOIC−14 NB** | | **PAGE 1 OF 2** |

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**SOIC−14**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

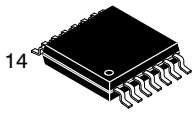
STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE



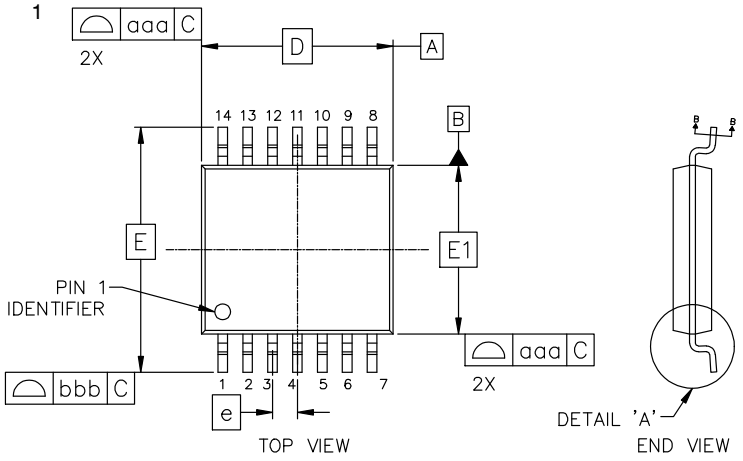

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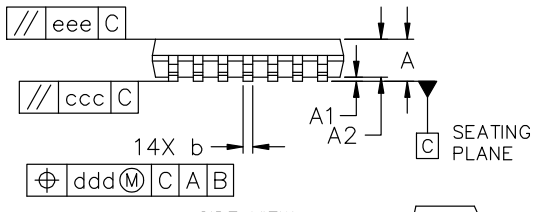
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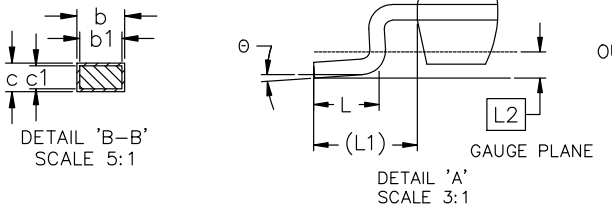


**TSSOP−14 5.00x4.40x0.95, 0.65P**
CASE 948G
ISSUE D

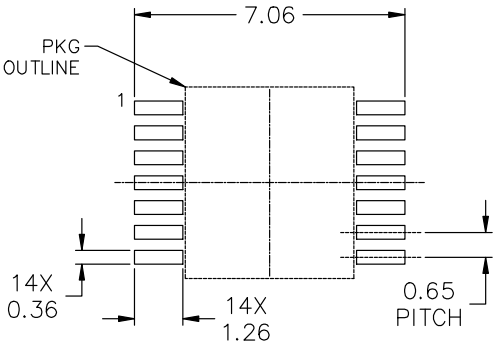
DATE 30 JUN 2026




| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | −−− | −−− | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.85 | 0.95 | 1.05 |
| b | 0.19 | 0.25 | 0.30 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.09 | 0.15 | 0.20 |
| c1 | 0.09 | 0.12 | 0.16 |
| D | 5.00 BSC | | |
| E | 6.40 BSC | | |
| E1 | 4.40 BSC | | |
| e | 0.65 BSC | | |
| L | 0.50 | 0.63 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 BSC | | |
| θ | 0° | 4° | 8° |
| TOLERANCE FORM & POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.15 | | |
| ccc | 0.08 | | |
| ddd | 0.10 | | |
| eee | 0.10 | | |

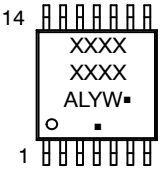



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D DOES NOT INCLIDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

**GENERIC MARKING DIAGRAM***




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TSSOP−14 5.00x4.40x0.95, 0.65P** | **PAGE 1 OF 1** |

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