# Integrated Relay, Inductive Load Driver

## MDC3105

**Relay, Inductive Load Driver**

This device is intended to replace an array of three to six discrete components with an integrated SMT part. It is available in a SOT−23 package. It can be used to switch 3 to 6 Vdc inductive loads such as relays, solenoids, incandescent lamps, and small DC motors without the need of a free−wheeling diode.

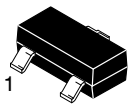
### Features

- Provides a Robust Driver Interface between DC Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays from a 3.0 V to 5.0 V Rail
- Capable of Driving Relay Coils Rated up to 2.5 W at 5.0 V
- Features Low Input Drive Current and Good Back−to−Front Transient Isolation
- Internal Zener Eliminates Need for Free−Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter System Operation
- Guaranteed Off State with No Input Connection
- Supports Large Systems with Minimal Off−State Leakage
- ESD Resistant in Accordance with the Class 1C Human Body Model
- Low Sat Voltage Reduces System Current Drain by Allowing Use of Higher Resistance Relay Coils
- These Devices are Pb−Free and Halide Free

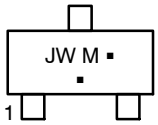
### Applications

- **Telecom:** Line Cards, Modems, Answering Machines, FAX Machines, Feature Phone Electronic Hook Switch
- **Computer and Office:** Photocopiers, Printers, Desktop Computers
- **Consumer:** TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders, TV Set Top Boxes
- **Industrial:** Small Appliances, White Goods, Security Systems, Automated Test Equipment, Garage Door Openers
- **Automotive:** 5.0 V Driven Relays, Motor Controls, Power Latches, Lamp Drivers

### MARKING DIAGRAMS



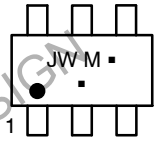

**SOT−23**
**CASE 318**
**STYLE 6**







**SC−74**
**CASE 318F**
**STYLE 8**




JW = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

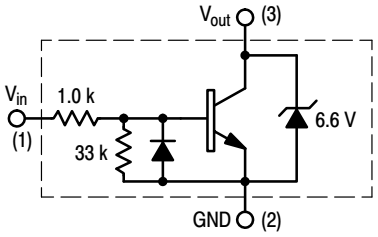
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

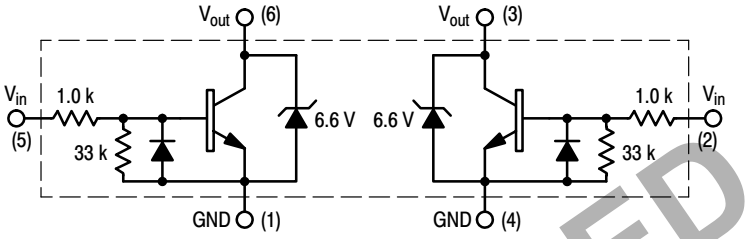
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## INTERNAL CIRCUIT DIAGRAMS




CASE 318




CASE 318F

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$ | 6.0 | Vdc |
| Input Voltage | | $V_{in(fwd)}$ | 6.0 | Vdc |
| Reverse Input Voltage | | $V_{in(rev)}$ | −0.5 | Vdc |
| Repetitive Pulse Zener Energy Limit (Duty Cycle ≤ 0.01%) | SOT−23 | Ezpk | 50 | mJ |
| Output Sink Current − Continuous | | $I_O$ | 500 | mA |
| Junction Temperature | | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | | $T_{stg}$ | −65 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS**

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Total Device Power Dissipation (Note 1)<br>Derate above 25°C | SOT−23 | $P_D$ | 225<br>1.8 | mW<br>mW/°C |
| Total Device Power Dissipation (Note 1)<br>Derate above 25°C | SC−74 | $P_D$ | 380<br>1.5 | mW<br>mW/°C |
| Thermal Resistance Junction−to−Ambient | SOT−23<br>SC−74 | $R_{\theta JA}$ | 556<br>329 | °C/W |

1. FR−5 PCB of 1″ x 0.75″ x 0.062″, $T_A$ = 25°C.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Output Zener Breakdown Voltage<br>(@ IT = 10 mA Pulse) | $V_{(BRout)}$<br>$V_{(-BRout)}$ | 6.2<br>– | 6.6<br>−0.7 | 7.0<br>– | V<br>V |
| Output Leakage Current @ 0 Input Voltage<br>($V_O$ = 5.5 Vdc, $V_{in}$ = O.C., $T_A$ = 25°C)<br>($V_O$ = 5.5 Vdc, $V_{in}$ = O.C., $T_A$ = 85°C) | $I_{OO}$ | <br>–<br>– | <br>–<br>– | <br>0.1<br>30 | μA |
| Guaranteed “OFF” State Input Voltage ($I_O \leq$ 100 μA) | $V_{in(off)}$ | – | – | 0.4 | V |
| **ON CHARACTERISTICS** | | | | | |
| Input Bias Current ($H_{FE}$ Limited)<br>($I_O$ = 250 mA, $V_O$ = 0.25 Vdc) | $I_{in}$ | – | 0.8 | 1.6 | mAdc |
| Output Saturation Voltage<br>($I_O$ = 250 mA, $I_{in}$ = 1.5 mA) | $V_{O(sat)}$ | – | 0.12 | 0.16 | Vdc |
| Output Sink Current – Continuous<br>($V_{CE}$ = 0.25 Vdc, $I_{in}$ = 1.5 mA) | $I_{O(on)}$ | 250 | 400 | – | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL APPLICATION−DEPENDENT SWITCHING PERFORMANCE

**SWITCHING CHARACTERISTICS**

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Propagation Delay Times: | | | | | nS |
| High to Low Propagation Delay; Figure 1 (5.0 V 74HC04) | $t_{PHL}$ | – | 55 | – | |
| Low to High Propagation Delay; Figure 1 (5.0 V 74HC04) | $t_{PLH}$ | – | 430 | – | |
| High to Low Propagation Delay; Figures 1, 13 (3.0 V 74HC04) | $t_{PHL}$ | – | 85 | – | |
| Low to High Propagation Delay; Figures 1, 13 (3.0 V 74HC04) | $t_{PLH}$ | – | 315 | – | |
| High to Low Propagation Delay; Figures 1, 14 (5.0 V 74LS04) | $t_{PHL}$ | – | 55 | – | |
| Low to High Propagation Delay; Figures 1, 14 (5.0 V 74LS04) | $t_{PLH}$ | – | 2.4 | – | μS |
| Transition Times: | | | | | nS |
| Fall Time; Figure 1 (5.0 V 74HC04) | $t_f$ | – | 45 | – | |
| Rise Time; Figure 1 (5.0 V 74HC04) | $t_r$ | – | 160 | – | |
| Fall Time; Figures 1, 13 (3.0 V 74HC04) | $t_f$ | – | 70 | – | |
| Rise Time; Figures 1, 13 (3.0 V 74HC04) | $t_r$ | – | 195 | – | |
| Fall Time; Figures 1, 14 (5.0 V 74LS04) | $t_f$ | – | 45 | – | |
| Rise Time; Figures 1, 14 (5.0 V 74LS04) | $t_r$ | – | 2.4 | – | μS |

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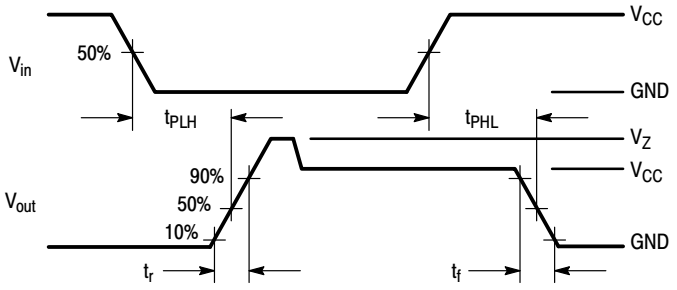



**Figure 1. Switching Waveforms**

## TYPICAL PERFORMANCE CHARACTERISTICS

(ON CHARACTERISTICS)

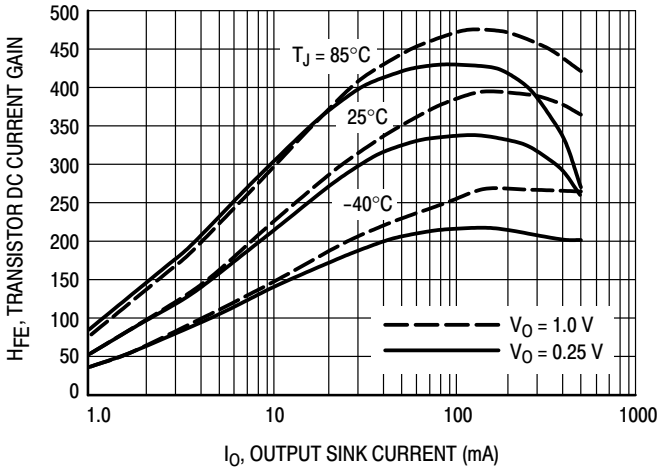



**Figure 2. Transistor DC Current Gain**

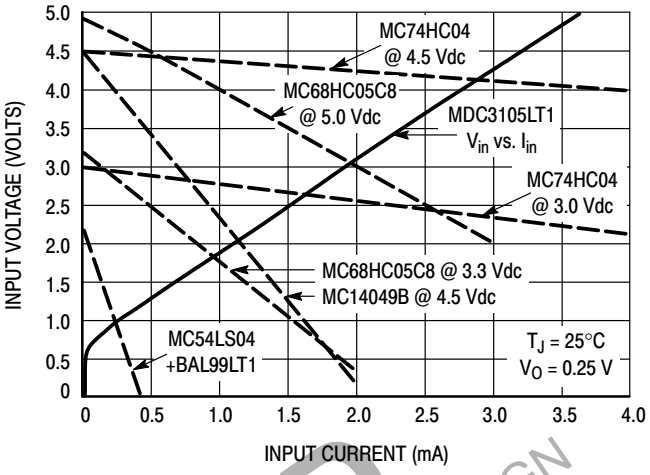



**Figure 3. Input V−I Requirement Compared to Possible Source Logic Outputs**

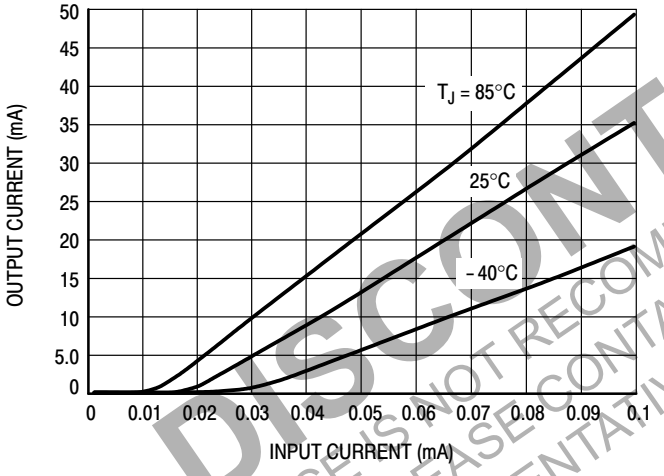



**Figure 4. Threshold Effects**

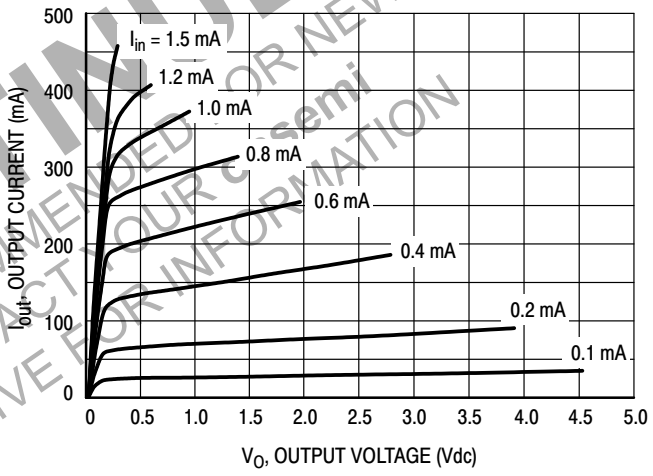



**Figure 5. Transistor Output V−I Characteristic**

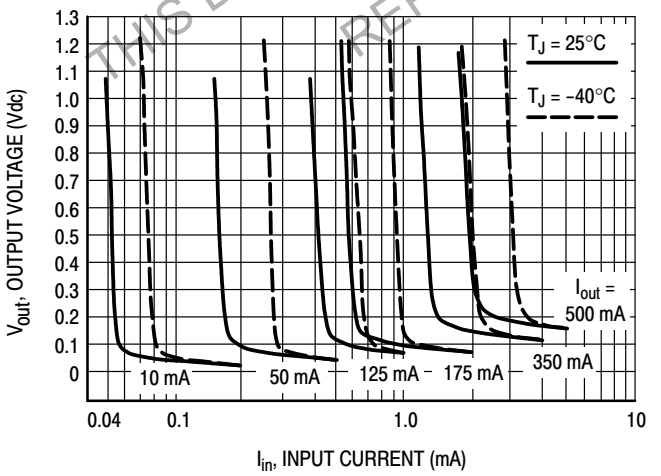



**Figure 6. Output Saturation Voltage versus $I_{out}/I_{in}$**

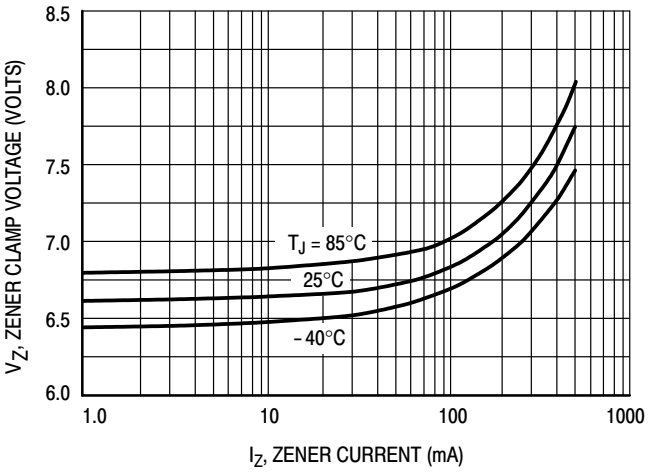



**Figure 7. Zener Clamp Voltage versus Zener Current**

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## TYPICAL PERFORMANCE CHARACTERISTICS

(OFF CHARACTERISTICS)

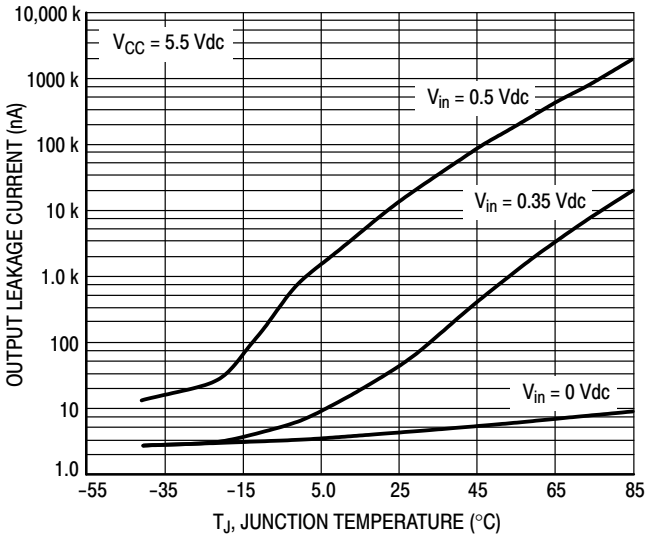



**Figure 8. Output Leakage Current versus Temperature**

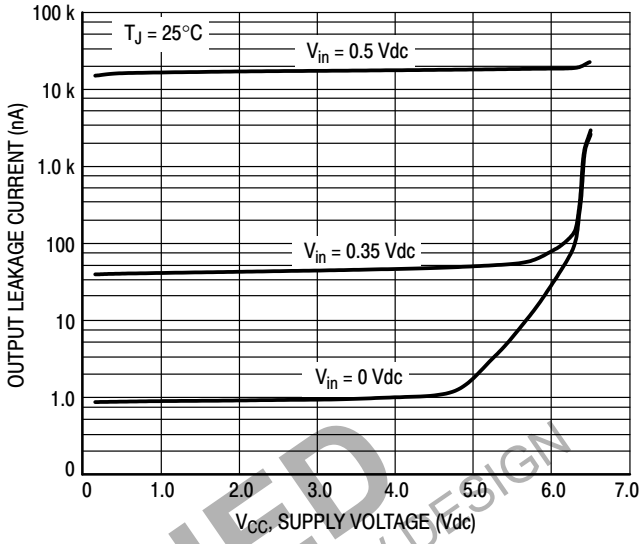



**Figure 9. Output Leakage Current versus Supply Voltage**

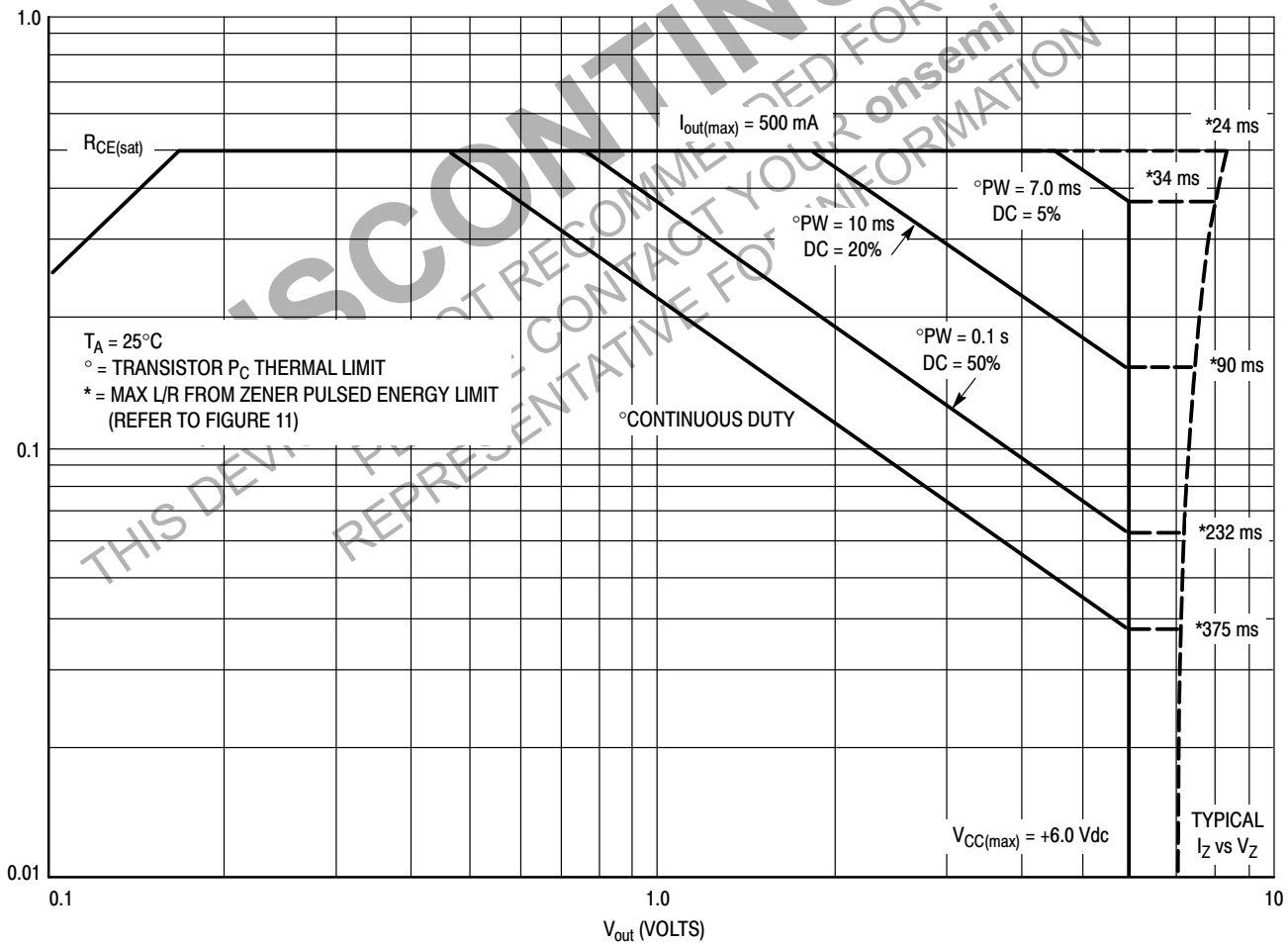



**Figure 10. Safe Operating Area for MDC3105LT1**

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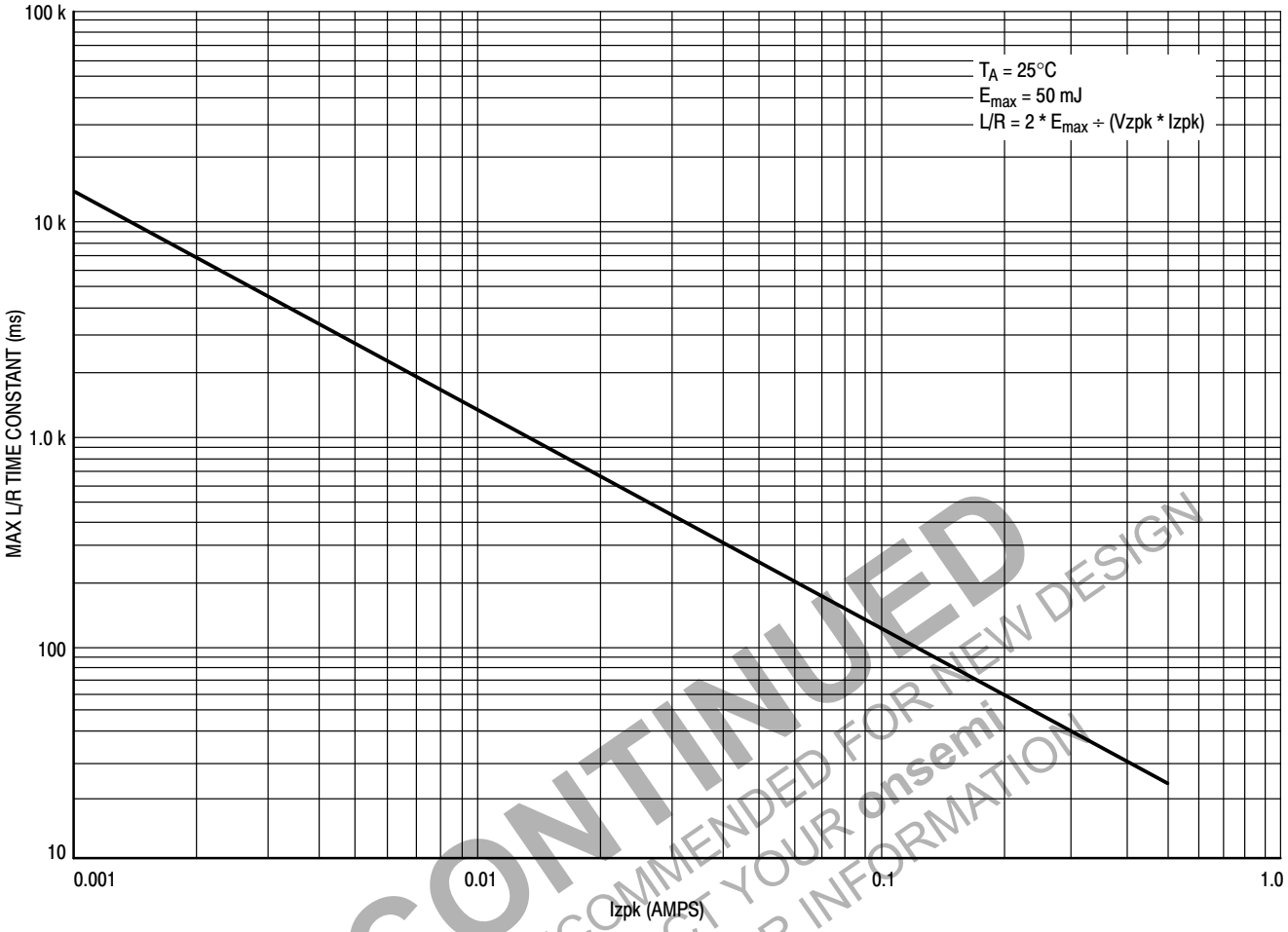



**Figure 11. Zener Repetitive Pulse Energy Limit on L/R Time Constant for MDC3105LT1**

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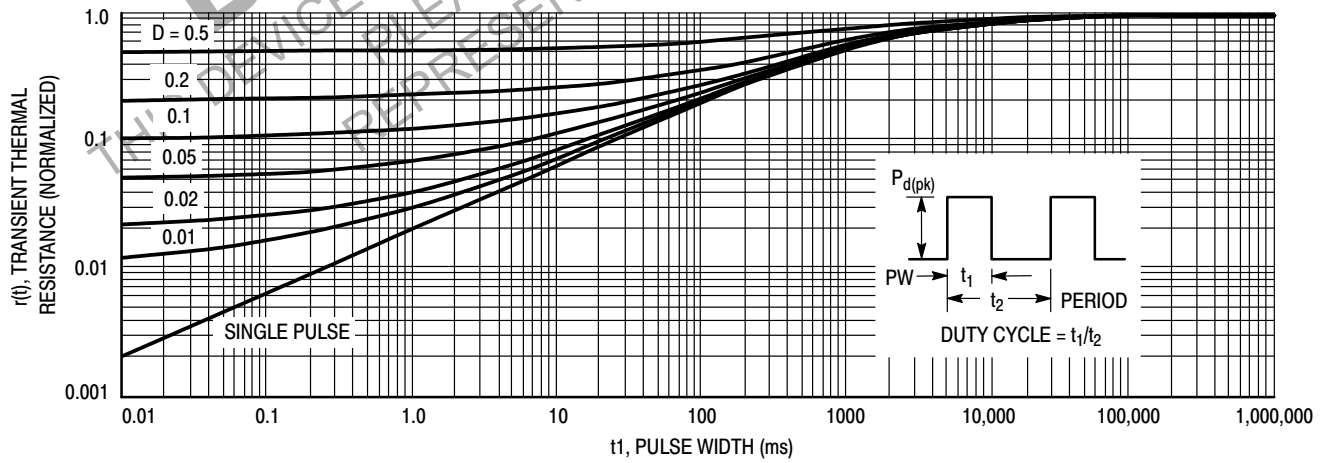



**Figure 12. Transient Thermal Response for MDC3105LT1**

### Using TTR Designing for Pulsed Operation

For a repetitive pulse operating condition, time averaging allows one to increase a device's peak power dissipation rating above the average rating by dividing by the duty cycle of the repetitive pulse train. Thus, a continuous rating of 200 mW of dissipation is increased to 1.0 W peak for a 20% duty cycle pulse train. However, this only holds true for pulse widths which are short compared to the thermal time

constant of the semiconductor device to which they are applied.

For pulse widths which are significant compared to the thermal time constant of the device, the peak operating condition begins to look more like a continuous duty operating condition over the time duration of the pulse. In these cases, the peak power dissipation rating cannot be merely time averaged by dividing the continuous power rating by the duty cycle of the pulse train. Instead, the average power rating can only be scaled up a reduced amount in accordance with the device's transient thermal response, so that the device's max junction temperature is not exceeded.

Figure 12 of the MDC3105 data sheet plots its transient thermal resistance, r(t) as a function of pulse width in ms for various pulse train duty cycles as well as for a single pulse and illustrates this effect. For short pulse widths near the left side of the chart, r(t), the factor, by which the continuous duty thermal resistance is multiplied to determine how much the peak power rating can be increased above the average power rating, approaches the duty cycle of the pulse train, which is the expected value. However, as the pulse width is increased, that factor eventually approaches 1.0 for all duty cycles indicating that the pulse width is sufficiently long to appear as a continuous duty condition to this device. For the MDC3105LT1, this pulse width is about 100 seconds. At this and larger pulse widths, the peak power dissipation capability is the same as the continuous duty power capability.

To use Figure 12 to determine the peak power rating for a specific application, enter the chart with the worst case pulse condition, that is the max pulse width and max duty cycle and determine the worst case r(t) for your application. Then calculate the peak power dissipation allowed by using the equation,

$$Pd(pk) = (T_{Jmax} - T_{Amax}) \div (R_{\theta JA} * r(t))$$

$$Pd(pk) = (150°C - T_{Amax}) \div (556°C/W * r(t))$$

Thus for a 20% duty cycle and a PW = 40 ms, Figure 12 yields r(t) = 0.3 and when entered in the above equation, the max allowable Pd(pk) = 390 mW for a max $T_A$ = 85°C.

Also note that these calculations assume a rectangular pulse shape for which the rise and fall times are insignificant compared to the pulse width. If this is not the case in a specific application, then the $V_O$ and $I_O$ waveforms should be multiplied together and the resulting power waveform integrated to find the total dissipation across the device. This then would be the number that has to be less than or equal to the Pd(pk) calculated above. A circuit simulator having a waveform calculator may prove very useful for this purpose.

### Notes on SOA and Time Constant Limitations

Figure 10 is the Safe Operating Area (SOA) for the MDC3105. Device instantaneous operation should never be pushed beyond these limits. It shows the SOA for the Transistor "ON" condition as well as the SOA for the Zener during the turn−off transient. The max current is limited by the Izpk capability of the Zener as well as the transistor in addition to the max input current through the resistor. It should not be exceeded at any temperature. The BJT power dissipation limits are shown for various pulse widths and duty cycles at an ambient temperature of 25°C. The voltage limit is the max $V_{CC}$ that can be applied to the device. When the input to the device is switched off, the BJT "ON" current is instantaneously dumped into the Zener diode where it begins its exponential decay. The Zener clamp voltage is a function of that BJT current level as can be seen by the bowing of the $V_Z$ versus $I_Z$ curve at the higher currents. In addition to the Zener's current limit impacting this device's 500 mA max rating, the clamping diode also has a peak energy limit as well. This energy limit was measured using a rectangular pulse and then translated to an exponential equivalent using the 2:1 relationship between the L/R time constant of an exponential pulse and the pulse width of a rectangular pulse having equal energy content. These L/R time constant limits in ms appear along the $V_Z$ versus $I_Z$ curve for the various values of $I_Z$ at which the Pd lines intersect the $V_{CC}$ limit. The L/R time constant for a given load should not exceed these limits at their respective currents. Precise L/R limits on Zener energy at intermediate current levels can be obtained from Figure 11.

### Designing with this Data Sheet

1. Determine the maximum inductive load current (at max $V_{CC}$, min coil resistance and usually minimum temperature) that the MDC3105 will have to drive and make sure it is less than the max rated current.
2. For pulsed operation, use the Transient Thermal Response of Figure 12 and the instructions with it to determine the maximum limit on transistor power dissipation for the desired duty cycle and temperature range.
3. Use Figures 10 and 11 with the SOA notes above to insure that instantaneous operation does not push the device beyond the limits of the SOA plot.

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4. While keeping any $V_{O(sat)}$ requirements in mind, determine the max input current needed to achieve that output current from Figures 2 and 6.
5. For levels of input current below 100 μA, use the input threshold curves of Figure 4 to verify that there will be adequate input current available to turn on the MDC3105 at all temperatures.
6. For levels of input current above 100 μA, enter Figure 3 using that max input current and determine the input voltage required to drive the MDC3105 from the solid $V_{in}$ versus $I_{in}$ line. Select a suitable drive source family from those whose dotted lines cross the solid input characteristic line to the right of the $I_{in}$, $V_{in}$ point.
7. Using the max output current calculated in step 1, check Figure 7 to insure that the range of Zener clamp voltage over temperature will satisfy all system and EMI requirements.
8. Using Figures 8 and 9, insure that “OFF” state leakage over temperature and voltage extremes does not violate any system requirements.
9. Review circuit operation and insure none of the device max ratings are being exceeded.

## APPLICATIONS DIAGRAMS

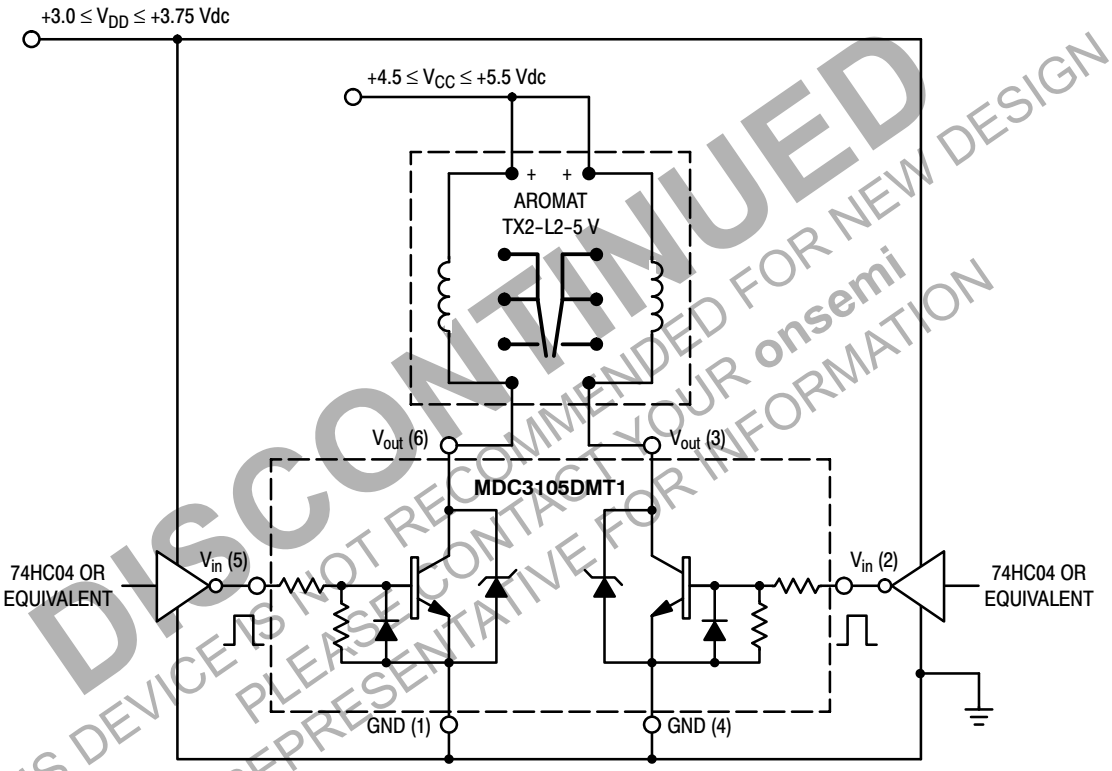



**Figure 13. A 200 mW, 5.0 V Dual Coil Latching Relay Application with 3.0 V−HCMOS Level Translating Interface**

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**Max Continuous Current Calculation**

for TX2−5V Relay, R1 = 178 Ω Nominal @ $R_A$ = 25°C

Assuming ±10% Make Tolerance,
R1 = 178 Ω * 0.9 = 160 Ω Min @ $T_A$ = 25°C

$T_C$ for Annealed Copper Wire is 0.4%/°C

R1 = 160 Ω * [1+(0.004) * (−40°−25°)] = 118 Ω Min @ −40°C

$I_O$ Max = (5.5 V Max − 0.25V) /118 Ω = 45 mA

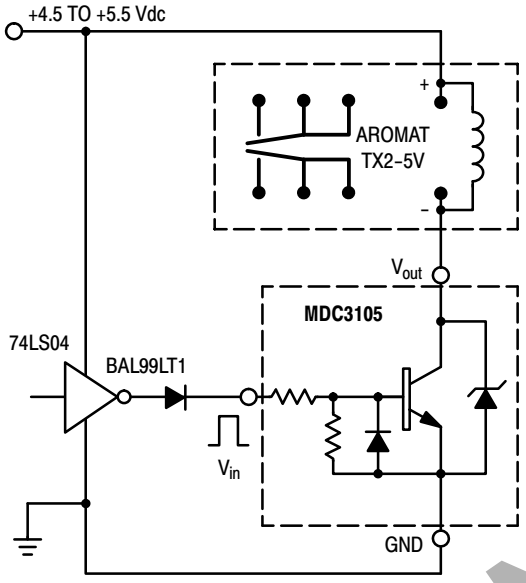



**Figure 14. A 140 mW, 5.0 V Relay with TTL Interface**

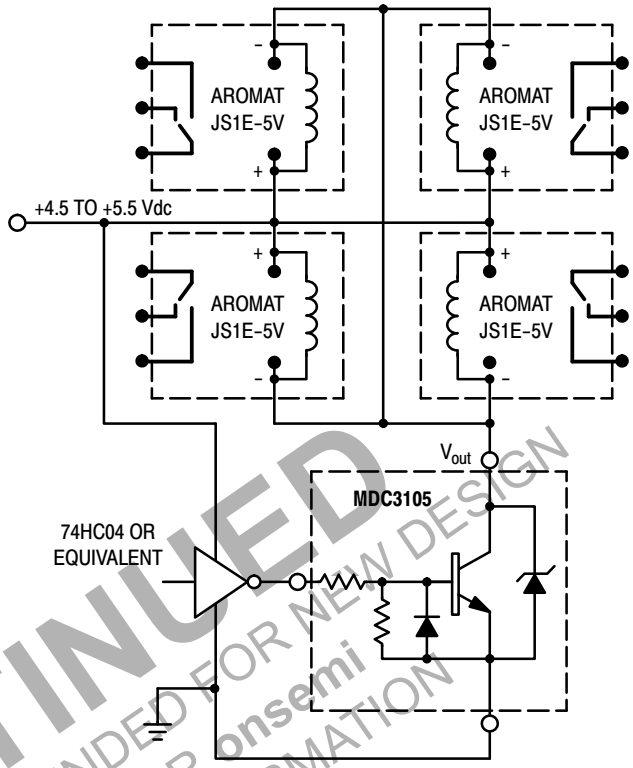



**Figure 15. A Quad 5.0 V, 360 mW Coil Relay Bank**

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## TYPICAL OPERATING WAVEFORMS

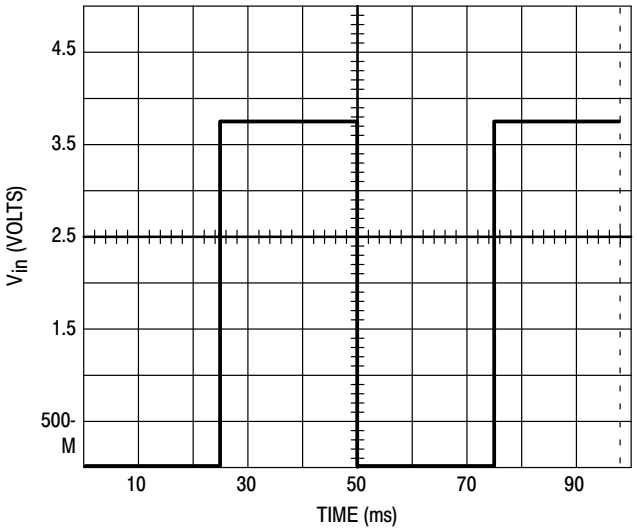



**Figure 16. 20 Hz Square Wave Input**

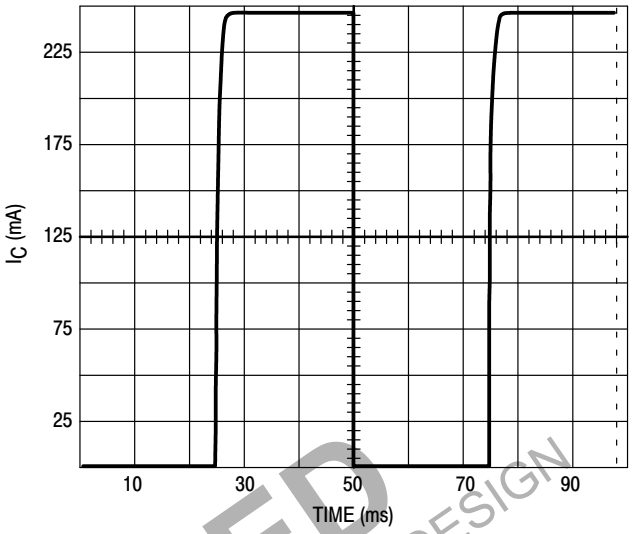



**Figure 17. 20 Hz Square Wave Response**

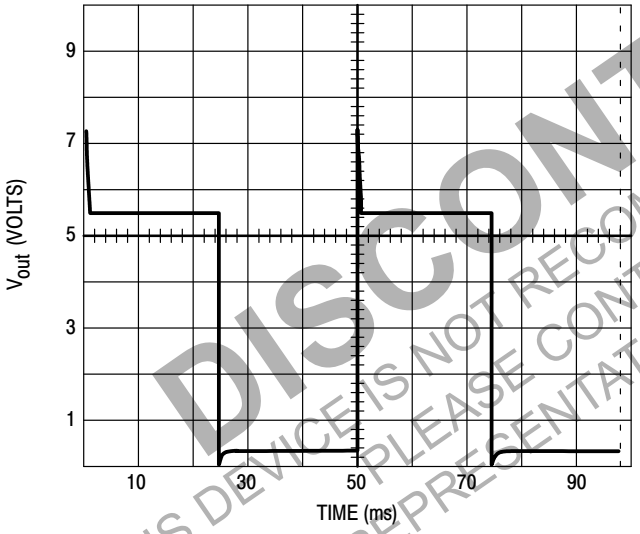



**Figure 18. 20 Hz Square Wave Response**

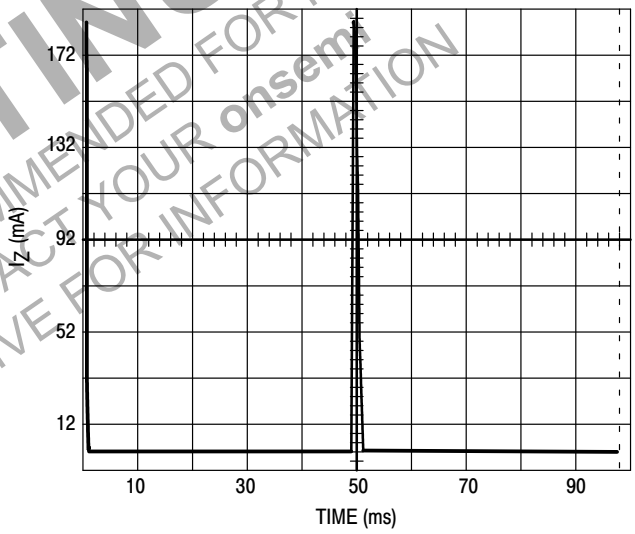



**Figure 19. 20 Hz Square Wave Response**

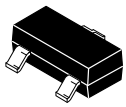
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### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MDC3105LT1G | SOT−23<br>(Pb−Free) | 3000 / Tape & Reel |
| MDC3105DMT1G | SC−74<br>(Pb−Free) | |

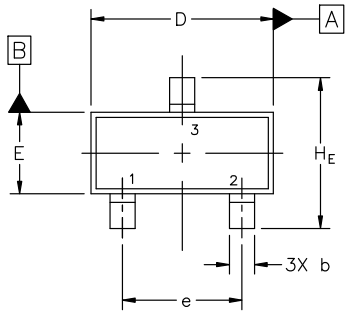
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



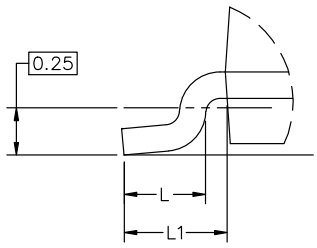
**SCALE 4:1**

**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**
CASE 318
ISSUE AU

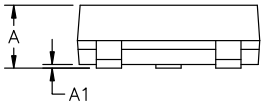
DATE 14 AUG 2024



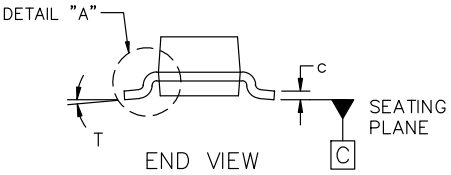

TOP VIEW




DETAIL "A"
Scale 3:1




SIDE VIEW

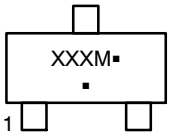



END VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 |
| A1 | 0.01 | 0.06 | 0.10 |
| b | 0.37 | 0.44 | 0.50 |
| c | 0.08 | 0.14 | 0.20 |
| D | 2.80 | 2.90 | 3.04 |
| E | 1.20 | 1.30 | 1.40 |
| e | 1.78 | 1.90 | 2.04 |
| L | 0.30 | 0.43 | 0.55 |
| L1 | 0.35 | 0.54 | 0.69 |
| $H_E$ | 2.10 | 2.40 | 2.64 |
| T | 0° | −−− | 10° |

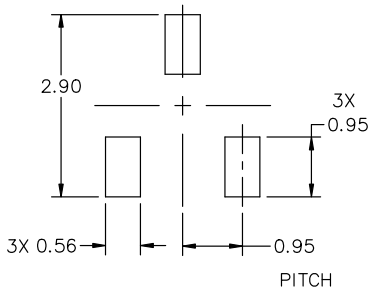
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

**GENERIC**
**MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **SOT−23 (TO−236) 2.90x1.30x1.00 1.90P** | | **PAGE 1 OF 2** |

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**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

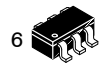
STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE




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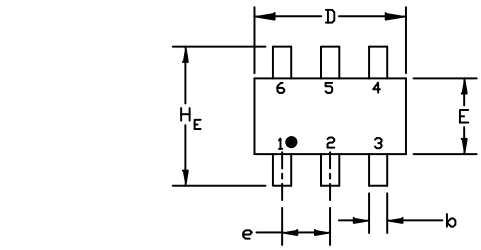
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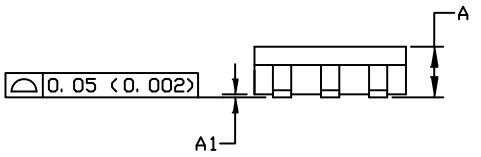
**SCALE 2:1**

**SC−74**
CASE 318F
ISSUE P

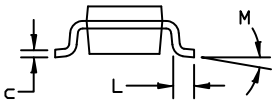
DATE 07 OCT 2021




TOP VIEW




SIDE VIEW

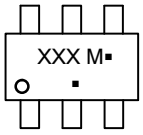



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 | 0.035 | 0.039 | 0.043 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.25 | 0.37 | 0.50 | 0.010 | 0.015 | 0.020 |
| c | 0.10 | 0.18 | 0.26 | 0.004 | 0.007 | 0.010 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 1.30 | 1.50 | 1.70 | 0.051 | 0.059 | 0.067 |
| e | 0.85 | 0.95 | 1.05 | 0.034 | 0.037 | 0.041 |
| $H_E$ | 2.50 | 2.75 | 3.00 | 0.099 | 0.108 | 0.118 |
| L | 0.20 | 0.40 | 0.60 | 0.008 | 0.016 | 0.024 |
| M | 0° | --- | 10° | 0° | --- | 10° |

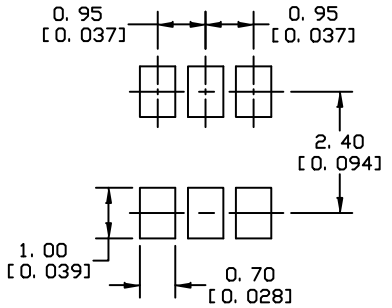
## GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.




* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

| | | |
|---|---|---|
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