# MGM12P Wireless Gecko Multi-Protocol Module Data Sheet

The Silicon Labs Wireless Gecko Module (MGM12P) is a fully-integrated, certified module, enabling rapid development of wireless mesh networking solutions.

Based on the Silicon Labs EFR32MG12 Wireless Gecko SoC, the MGM12P combines an energy- efficient, multi-protocol wireless SoC with a proven RF/antenna design and industry leading wireless software stacks. This integration accelerates time-to-market and saves months of engineering effort and development costs.

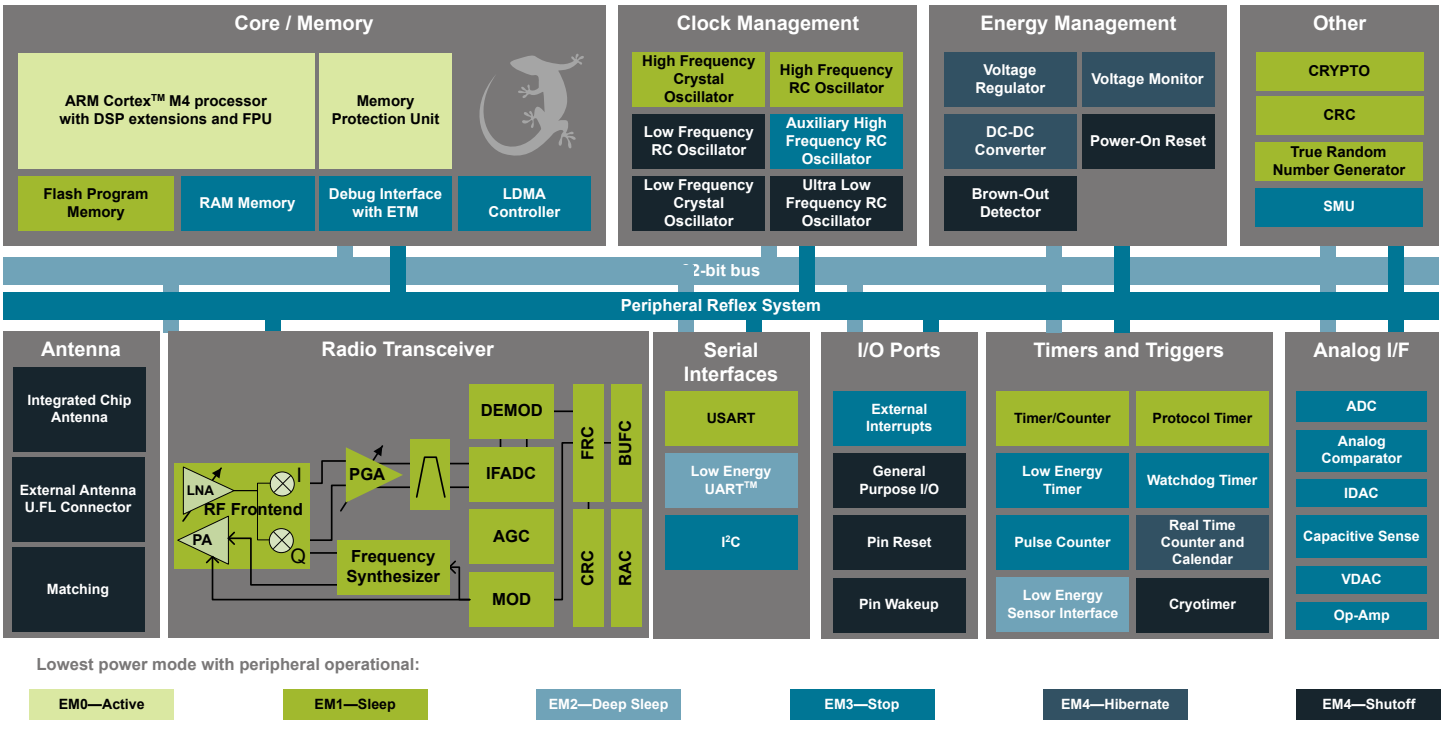
In addition, common software and development tools enable seamless migration from a module to discrete SoC-based design when the time is right.

MGM12P can be used in a wide variety of applications:

- IoT Multi-Protocol Devices
- Connected Home
- Lighting
- Health and Wellness
- Metering
- Building Automation and Security

**KEY FEATURES**

- 32-bit ARM® Cortex®-M4 core at 38.4 MHz maximum operating frequency
- 1 MB of flash and 256 kB of RAM
- ZigBee, Thread, BLE, and multi-protocol support
- Pin-compatible with MGM111 module
- 12-channel Peripheral Reflex System, Low-Energy Sensor Interface & Multi-channel Capacitive Sense Interface
- Integrated PA with up to +17 dBm transmit power
- Robust peripheral set and up to 25 GPIO




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# 1. Feature List

The MGM12P highlighted features are listed below.

- **Low Power Wireless System-on-Chip**.
  - High Performance 32-bit ARM Cortex®-M4 core at 38.4 MHz with DSP instruction and floating-point unit for efficient signal processing
  - 1024 kB flash program memory
  - 256 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to +17 dBm
- **Low Energy Consumption**
  - 10.3 mA RX current at 2.4 GHz (1 Mbps GFSK)
  - 10.8 mA RX current at 2.4 GHz (250 kbps O-QPSK DSSS)
  - 10 mA TX current @ 0 dBm output power at 2.4 GHz
  - 70 µA/MHz in Active Mode (EM0)
  - 2.62 µA EM2 DeepSleep current (256 kB RAM retention and RTCC running from LFXO)
- **High Receiver Performance**
  - -102 dBm sensitivity @ 250 kbps O-QPSK DSSS
  - -105.7 dBm sensitivity @ 250 kbps O-QPSK DSSS (MGM12P22 and MGM12P32)
  - -94.4 dBm sensitivity @ 1Mbps 2GFSK
  - -100.3 dBm sensitivity @ 1Mbps 2GFSK (MGM12P22 and MGM12P32)
- **Supported Modulation Format**
  - Shaped OQPSK
  - 2-FSK / 4-FSK with fully configurable shaping
- **Supported Protocols:**
  - Bluetooth® Low Energy (Bluetooth 5)
  - zigbee
  - Thread
- **Support for Internet Security**
  - General Purpose CRC
  - True Random Number Generator
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2×Analog Comparator (ACMP)
  - 2×Digital to Analog Converter (VDAC)
  - 3×Operational Amplifier (Opamp)
  - Digital to Analog Current Converter (IDAC)
  - Low-Energy Sensor Interface (LESENSE)
  - Multi-channel Capacitive Sense Interface (CSEN)
  - Up to 25 pins connected to analog channels (APORT) shared between analog peripherals
  - Up to 25 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2×16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 2×32-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 3×16-bit Pulse Counter with asynchronous operation
  - 2×Watchdog Timer with dedicated RC oscillator
  - 4×Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/$I^2S$)
  - Low Energy UART (LEUART™)
  - 2×$I^2C$ interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - -40 °C to 85 °C
- **WxLxH:** 12.9 x 17.8 x 2.3 mm

## 2. Ordering Information

| Ordering Code | Description | Max TX Power | Sensitivity (O-QPSK) | Antenna | Packaging | Production Status |
|---|---|---|---|---|---|---|
| MGM12P32F1024GA-V4 | Multi-protocol Module | +17 dBm | -105.7 dBm | Integrated chip antenna | Cut Tape (100 pcs) | Full Production (certified) |
| MGM12P32F1024GA-V4R | Multi-protocol Module | +17 dBm | -105.7 dBm | Integrated chip antenna | Reel (1000 pcs) | Full Production (certified) |
| MGM12P32F1024GE-V4 | Multi-protocol Module | +17 dBm | -105.7 dBm | External (U.FL) | Cut Tape (100 pcs) | Full Production (certified) |
| MGM12P32F1024GE-V4R | Multi-protocol Module | +17 dBm | -105.7 dBm | External (U.FL) | Reel (1000 pcs) | Full Production (certified) |
| MGM12P22F1024GA-V4 | Multi-protocol Module | +10 dBm | -105.7 dBm | Integrated chip antenna | Cut Tape (100 pcs) | Full Production (certified) |
| MGM12P22F1024GA-V4R | Multi-protocol Module | +10 dBm | -105.7 dBm | Integrated chip antenna | Reel (1000 pcs) | Full Production (certified) |
| MGM12P22F1024GE-V4 | Multi-protocol Module | +10 dBm | -105.7 dBm | External (U.FL) | Cut Tape (100 pcs) | Full Production (certified) |
| MGM12P22F1024GE-V4R | Multi-protocol Module | +10 dBm | -105.7 dBm | External (U.FL) | Reel (1000 pcs) | Full Production (certified) |
| MGM12P02F1024GA-V4 | Multi-protocol Module | +10 dBm | -102 dBm | Integrated chip antenna | Cut Tape (100 pcs) | Full Production (certified) |
| MGM12P02F1024GA-V4R | Multi-protocol Module | +10 dBm | -102 dBm | Integrated chip antenna | Reel (1000 pcs) | Full Production (certified) |
| MGM12P02F1024GE-V4 | Multi-protocol Module | +10 dBm | -102 dBm | External (U.FL) | Cut Tape (100 pcs) | Full Production (certified) |
| MGM12P02F1024GE-V4R | Multi-protocol Module | +10 dBm | -102 dBm | External (U.FL) | Reel (1000 pcs) | Full Production (certified) |
| SLWRB4304A | MGM12P Radio Board[2] | +17 dBm | -105.7 dBm | Integrated chip antenna | Single Unit | Development Board |

**Note:**

1. IAR license required for zigbee and Thread software development.
2. Requires Mesh Networking kit SLWSTK6000A or SLWSTK6000B

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# 3. System Overview

## 3.1 Introduction

This section provides a brief overview of the MGM12P module architecture including both MCU and RF sub-systems. A detailed functional description of the EFR32MG12 SoC used inside the module is available in the *EFR32MG12 Wireless Gecko Data Sheet* and *EFR32xG12 Wireless Gecko Reference Manual*. A block diagram of the EFR32MG12 SoC is shown in the figure below.

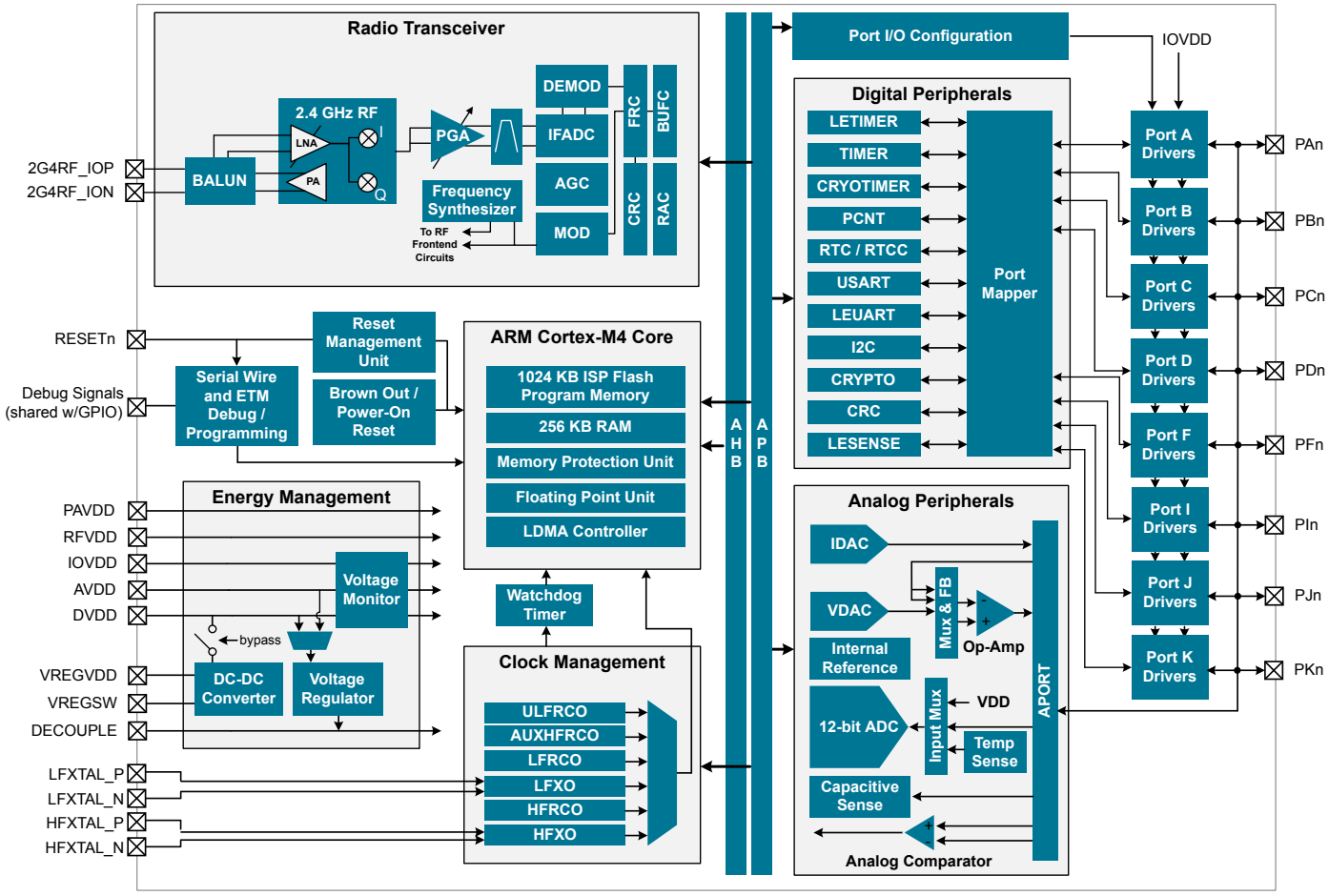



**Figure 3.1. Detailed EFR32MG12 Block Diagram**

## 3.2 Radio

The MGM12P modules feature a highly configurable radio transceiver that supports a wide range of wireless protocols including zigbee, Thread, and Bluetooth Low Energy.

### 3.2.1 Antenna Interface

The MGM12P module family includes options for either a high-performance, integrated chip-antenna (MGM12P-GA) or external antenna (MGM12P-GE) via a U.FL connector. The table below includes performance specifications for the integrated chip antenna.

**Table 3.1. Antenna Efficiency and Peak Gain (MGM12P)**

| Parameter | With optimal layout | Note |
|---|---|---|
| Efficiency | -1.5 dB to -3 dB | Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to the Layout Guidelines Chapter for PCB layout and antenna integration guidelines for optimal performance. Typical efficiency gain is expected to be between -3.5 dB and -5 dB. |
| Peak gain | 1.0 dBi | |

### 3.2.2 Packet and State Trace

The MGM12P Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

### 3.2.3 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

### 3.3 Power

The MGM12P has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

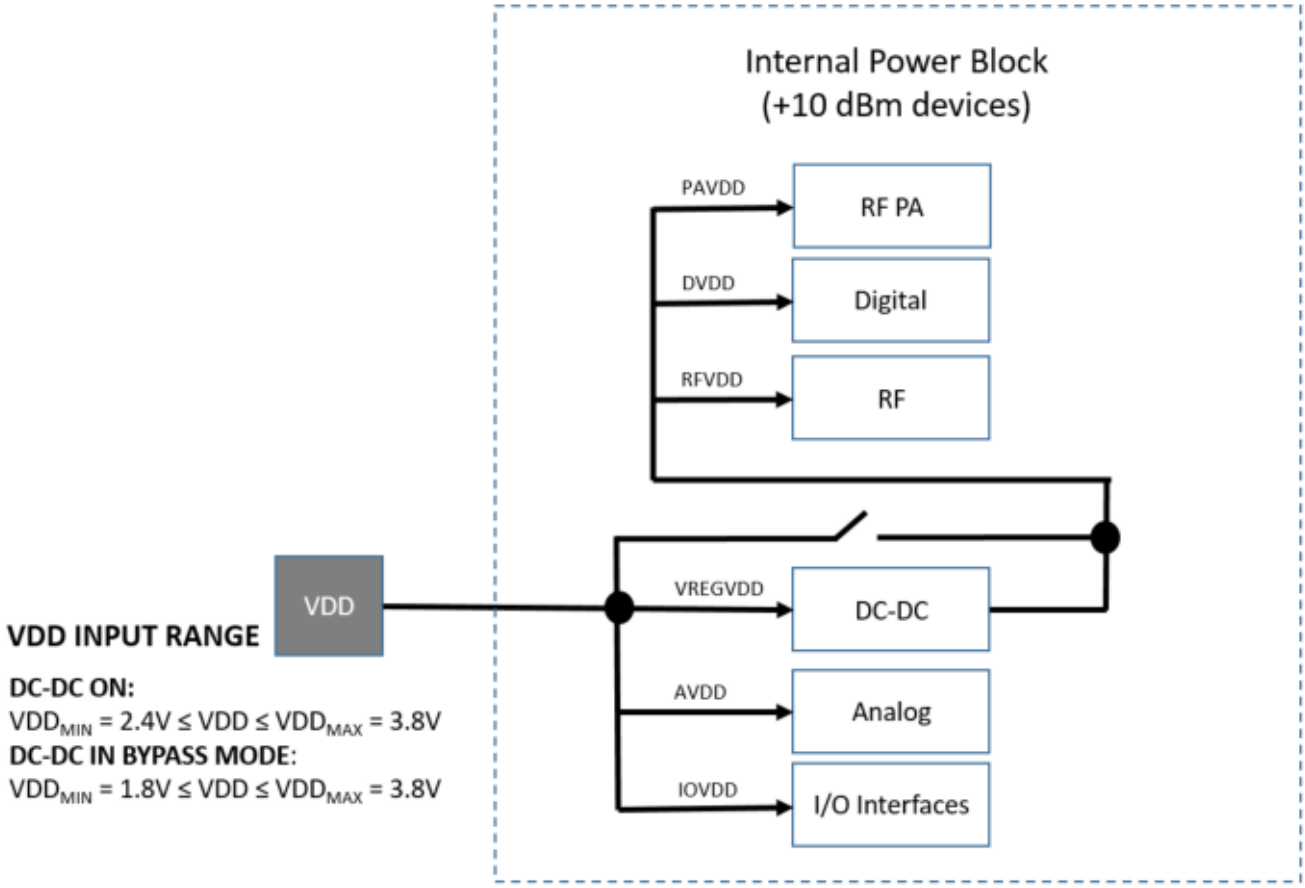



**Figure 3.2. MGM12P Power Block for Modules (+10 dBm)**

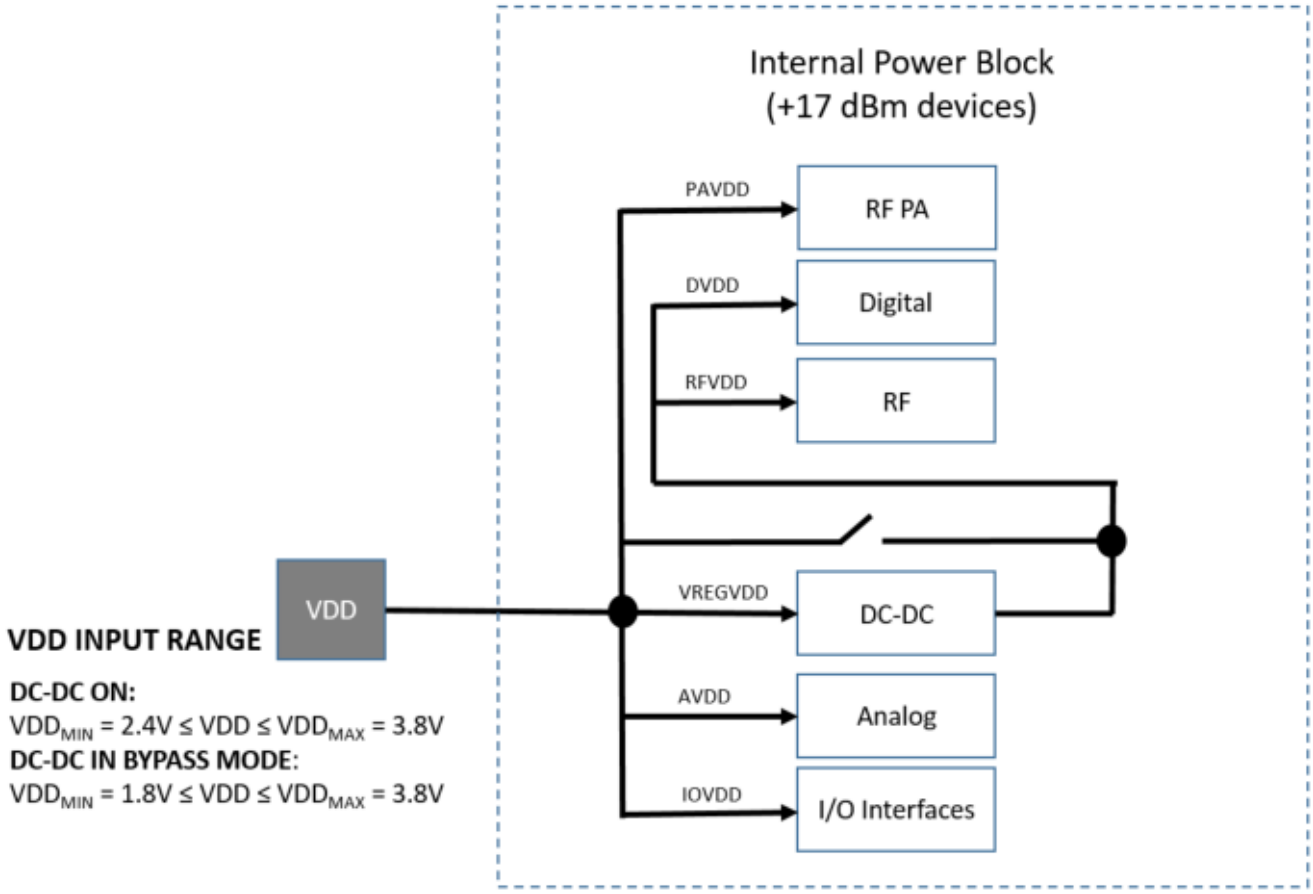



**Figure 3.3. MGM12P Power Block for Modules (+17 dBm)**

### 3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

### 3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2, and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

### 3.3.3 Power Domains

The MGM12P has two peripheral power domains for operation in EM2 and lower. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

**Table 3.2. Peripheral Power Subdomains**

| Peripheral Power Domain 1 | Peripheral Power Domain 2 |
|---|---|
| ACMP0 | ACMP1 |
| PCNT0 | PCNT1 |
| ADC0 | PCNT2 |
| LETIMER0 | CSEN |
| LESENSE | DAC0 |
| APORT | LEUART0 |
| - | I2C0 |
| - | I2C1 |
| - | IDAC |

## 3.4 General Purpose Input/Output (GPIO)

MGM12P has 25 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

## 3.5 Clocking

### 3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the MGM12P. Individual enabling and disabling of clocks to all peripheral modules is perfomed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

### 3.5.2 Internal Oscillators

The MGM12P fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HFXO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

## 3.6 Counters/Timers and PWM

### 3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

### 3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

### 3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

### 3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

### 3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

### 3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

### 3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

## 3.7 Communications and Other Digital Peripherals

### 3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- $I^2S$

### 3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

### 3.7.3 Inter-Integrated Circuit Interface ($I^2C$)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$ bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the $I^2C$ module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

### 3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement.

Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

### 3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

## 3.8 Security Features

### 3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

### 3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

### 3.8.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

**Note:** TRNG operation is only supported at VSCALE2. TRNG cannot be used at VSCALE0.

### 3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

## 3.9 Analog

### 3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

### 3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

### 3.9.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

### 3.9.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

### 3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

### 3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

## 3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the MGM12P. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

## 3.11 Core and Memory

### 3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 1024 KB flash program memory
- 256 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

### 3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

### 3.12 Memory Map

The MGM12P memory map is shown in the figures below.

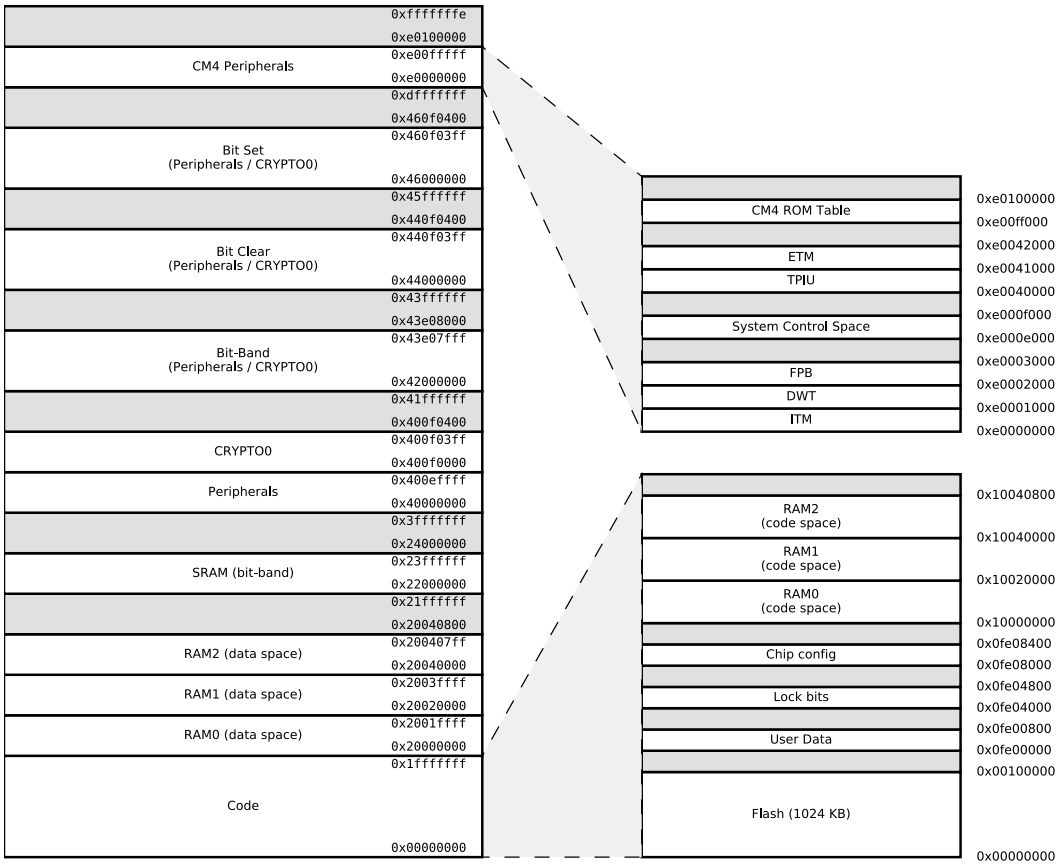



**Figure 3.4. MGM12P Memory Map — Core Peripherals and Code Space**

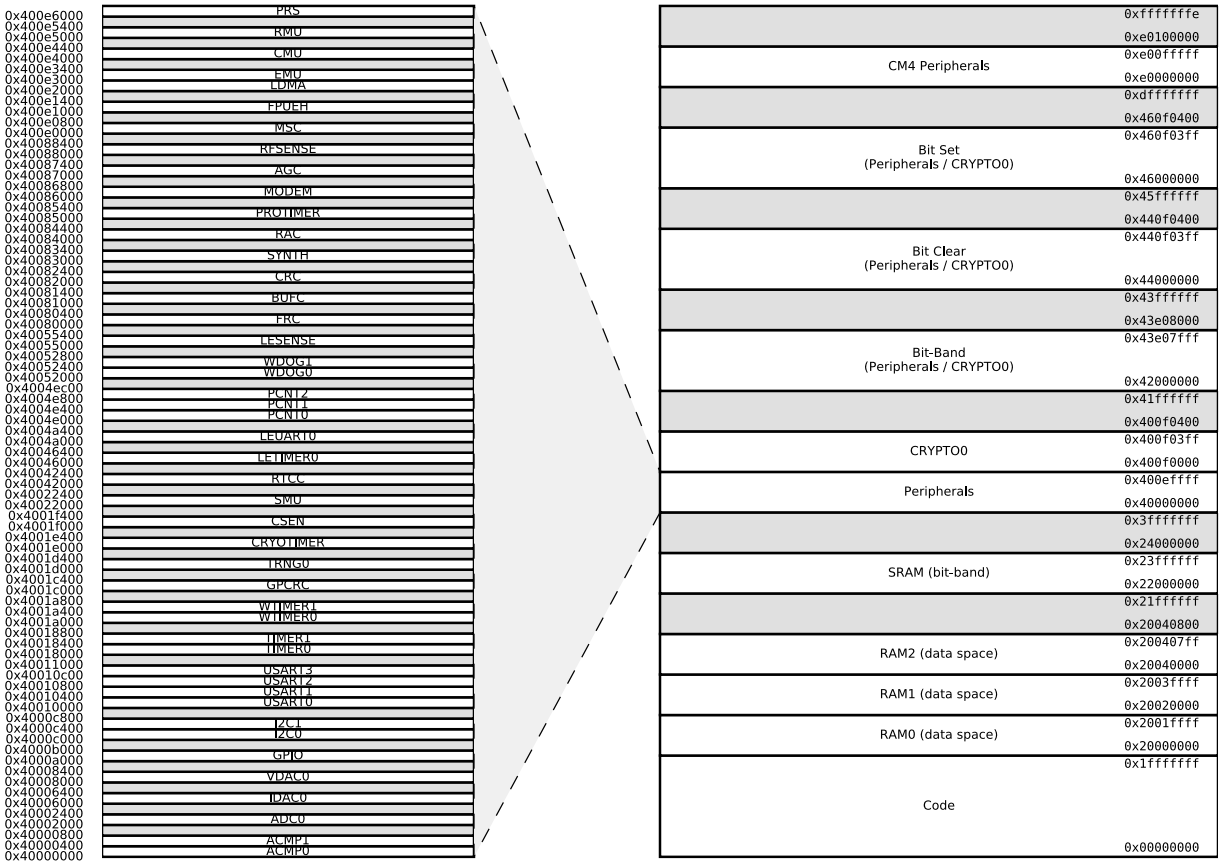



**Figure 3.5. MGM12P Memory Map — Peripherals**

### 3.13 Configuration Summary

The features of the MGM12P are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

**Table 3.3. Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| USART0 | IrDA SmartCard | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | IrDA $I^2S$ SmartCard | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | IrDA SmartCard | US2_TX, US2_RX, US2_CLK, US2_CS |
| USART3 | IrDA $I^2S$ SmartCard | US3_TX, US3_RX, US3_CLK, US3_CS |
| TIMER0 | with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | - | TIM1_CC[3:0] |
| WTIMER0 | with DTI | WTIM0_CC[2:0], WTIM0_CDTI[2:0] |
| WTIMER1 | - | WTIM1_CC[3:0] |

# 4. Electrical Specifications

## 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}$=25 °C and $V_{DD}$= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to Figure 3.2 MGM12P Power Block for Modules (+10 dBm) on page 9 and Figure 3.3 MGM12P Power Block for Modules (+17 dBm) on page 10 to see the relation between the modules external VDD pin and internal voltage supplies. The module has only one external power supply input (VDD).

Refer to 4.1.2 General Operating Conditions for more details about operational supply and temperature limits.

### 4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -40 | — | 85 | °C |
| Voltage on any supply pin | $V_{DDMAX}$ | | -0.3 | — | 3.8 | V |
| Voltage ramp rate on any supply pin | $V_{DDRAMPMAX}$ | | — | — | 1 | V / µs |
| DC Voltage on any over-voltage tolerant GPIO pin[1] | $V_{DIGPIN}$ | | -0.3 | — | Min of 5.25 and IOVDD +2 | V |
| | | | -0.3 | — | IOVDD+0.3 | V |
| Input RF level | $P_{RFMAX2G4}$ | | — | — | -2 | dBm |
| Current per I/O pin | $I_{IOMAX}$ | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | $I_{IOALLMAX}$ | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |

**Note:**
1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

### 4.1.2 General Operating Conditions

**Table 4.2. General Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Ambient temperature range | $T_A$ | -G temperature grade | -40 | 25 | 85 | °C |
| VDD supply voltage [1] | $V_{VDD}$ | DCDC in regulation | 2.4 | 3.3 | 3.8 | V |
| | | DCDC in bypass 50mA load | 1.8 | 3.3 | 3.8 | V |
| Core Clock Frequency | $f_{CORE}$ | FWAIT = 1, VSCALE2 | — | — | 40 | MHz |
| | | FWAIT = 0, VSCALE0 | — | — | 20 | MHz |

**Note:**

1. The minimum voltage required in bypass mode is calculated using $R_{BYP}$ from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD_min}+I_{LOAD} * R_{BYP_max}$.

### 4.1.3 DC-DC Converter

**Table 4.3. DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{DCDC_I}$ | Bypass mode, $I_{DCDC_LOAD}$ = 50 mA | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | Low noise (LN) mode, 1.8 V output, $I_{DCDC_LOAD}$ = 100 mA, or Low power (LP) mode, 1.8 V output, $I_{DCDC_LOAD}$ = 10 mA | 2.4 | — | $V_{VREGVDD_MAX}$ | V |
| | | Low noise (LN) mode, 1.8 V output, $I_{DCDC_LOAD}$ = 200 mA | 2.6 | — | $V_{VREGVDD_MAX}$ | V |
| Output voltage programmable range[1] | $V_{DCDC_O}$ | | 1.8 | — | $V_{VREGVDD}$ | V |
| Max load current | $I_{LOAD_MAX}$ | Low noise (LN) mode, Medium Drive[2] | — | — | 100 | mA |
| | | Low noise (LN) mode, Light Drive[2] | — | — | 50 | mA |
| | | Low power (LP) mode, LPCMPBIASEMxx[3] = 0 | — | — | 75 | µA |
| | | Low power (LP) mode, LPCMPBIASEMxx[3] = 3 | — | — | 10 | mA |

**Note:**

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VDD}$
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. In EMU_DCDCMISCCTRL register

### 4.1.4 Current Consumption

#### 4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3 V, DC-DC enabled. $T_{OP}$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at $T_{OP}$ = 25 °C.

**Table 4.4. Current Consumption 3.3 V using DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]. | $I_{ACTIVE_DCM}$ | 38.4 MHz crystal, CPU running while loop from flash[4] | — | 88 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 70 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 70 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 85 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 77 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 636 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1]. | $I_{ACTIVE_CCM}$ | 38.4 MHz crystal, CPU running while loop from flash[4] | — | 98 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 81 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 82 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 95 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 95 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1155 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1]. | $I_{ACTIVE_CCM_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 101 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1155 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]. | $I_{EM1_DCM}$ | 38.4 MHz crystal[4] | — | 59 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 41 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 48 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 610 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2]. | $I_{EM1_DCM_VS}$ | 19 MHz HFRCO | — | 52 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 587 | — | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, with votage scaling enabled, DCDC in LP mode. [3] | $I_{EM2_VS}$ | Full 256 kB RAM retention and RTCC running from LFXO | — | 2.62 | — | µA |
| Current consumption in EM3 mode, with voltage scaling enabled. | $I_{EM3_VS}$ | Full 256 kB RAM retention and CRYOTIMER running from ULFRCO | — | 2.33 | — | µA |
| Current consumption in EM4H mode, with voltage scaling enabled. | $I_{EM4H_VS}$ | 128 byte RAM retention, RTCC running from LFXO | — | 1.21 | — | µA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.91 | — | µA |
| | | 128 byte RAM retention, no RTCC | — | 0.91 | — | µA |
| Current consumption in EM4S mode | $I_{EM4S}$ | No RAM retention, no RTCC | — | 0.58 | — | µA |

**Note:**

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. CMU_HFXOCTRL_LOWPOWER=0.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

#### 4.1.4.2 Current Consumption Using Radio 3.3 V with DC-DC

Unless otherwise indicated, typical conditions are: VDD = 3.3 V, DC-DC enabled. $T_{OP}$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at $T_{OP}$ = 25 °C.

**Table 4.5. Current Consumption Using Radio 3.3 V with DC-DC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled).<br>LNA in bypass. | $I_{RX_ACTIVE}$ | 1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4 | — | 10.3 | — | mA |
| | | 2 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4 | — | 11.5 | — | mA |
| | | 802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3 | — | 10.8 | — | mA |
| Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)<br>LNA in bypass. | $I_{RX_LISTEN}$ | 1 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling | — | 11.6 | — | mA |
| | | 2 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling | — | 12.6 | — | mA |
| | | 802.15.4, F = 2.4 GHz, No radio clock prescaling | — | 12.3 | — | mA |
| Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)<br>LNA in bypass. | $I_{TX}$ | F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 1 (MGM12P02) | — | 10 | — | mA |
| | | F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 1 (MGM12P22) | — | 15.8 | — | |
| | | F = 2.4 GHz, CW, 8 dBm output power (MGM12P02) | — | 27.1 | — | mA |
| | | F = 2.4 GHz, CW, 8 dBm output power (MGM12P22) | — | 31.8 | — | mA |
| | | F = 2.4 GHz, CW, 10.0 dBm output power (MGM12P02) | — | 35.4 | — | mA |
| | | F = 2.4 GHz, CW, 10.0 dBm output power (MGM12P22) | — | 39.2 | — | mA |
| | | F = 2.4 GHz, CW, 17.0 dBm output power, PAVDD connected directly to VDD (MGM12P32) | — | 121 | — | mA |

### 4.1.5 Wake Up Times

**Table 4.6. Wake Up Times**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Wake up time from EM1 | $t_{EM1_WU}$ | | — | 3 | — | AHB Clocks |
| Wake up from EM2 | $t_{EM2_WU}$ | Code execution from flash | — | 10.1 | — | µs |
| | | Code execution from RAM | — | 3.2 | — | µs |
| Wake up from EM3 | $t_{EM3_WU}$ | Code execution from flash | — | 10.1 | — | µs |
| | | Code execution from RAM | — | 3.2 | — | µs |
| Wake up from EM4H[1] | $t_{EM4H_WU}$ | Executing from flash | — | 80 | — | µs |
| Wake up from EM4S[1] | $t_{EM4S_WU}$ | Executing from flash | — | 291 | — | µs |
| Time from release of reset source to first instruction execution | $t_{RESET}$ | Soft Pin Reset released | — | 43 | — | µs |
| | | Any other reset released | — | 350 | — | µs |
| Power mode scaling time | $t_{SCALE}$ | VSCALE0 to VSCALE2, HFCLK = 19 MHz[2] [3] | — | 31.8 | — | µs |
| | | VSCALE2 to VSCALE0, HFCLK = 19 MHz[4] | — | 4.3 | — | µs |

**Note:**

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.
3. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/µs for approximately 20 µs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
4. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.

### 4.1.6 Brown Out Detector (BOD)

**Table 4.7. Brown Out Detector (BOD)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DVDD BOD threshold | $V_{DVDDBOD}$ | DVDD rising | — | — | 1.62 | V |
| | | DVDD falling (EM0/EM1) | 1.35 | — | — | V |
| | | DVDD falling (EM2/EM3) | 1.3 | — | — | V |
| DVDD BOD hysteresis | $V_{DVDDBOD_HYST}$ | | — | 18 | — | mV |
| DVDD BOD response time | $t_{DVDDBOD_DELAY}$ | Supply drops at 0.1V/µs rate | — | 2.4 | — | µs |
| AVDD BOD threshold | $V_{AVDDBOD}$ | AVDD rising | — | — | 1.8 | V |
| | | AVDD falling (EM0/EM1) | 1.62 | — | — | V |
| | | AVDD falling (EM2/EM3) | 1.53 | — | — | V |
| AVDD BOD hysteresis | $V_{AVDDBOD_HYST}$ | | — | 20 | — | mV |
| AVDD BOD response time | $t_{AVDDBOD_DELAY}$ | Supply drops at 0.1V/µs rate | — | 2.4 | — | µs |
| EM4 BOD threshold | $V_{EM4DBOD}$ | AVDD rising | — | — | 1.7 | V |
| | | AVDD falling | 1.45 | — | — | V |
| EM4 BOD hysteresis | $V_{EM4BOD_HYST}$ | | — | 25 | — | mV |
| EM4 BOD response time | $t_{EM4BOD_DELAY}$ | Supply drops at 0.1V/µs rate | — | 300 | — | µs |

### 4.1.7 Frequency Synthesizer

**Table 4.8. Frequency Synthesizer**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF Synthesizer Frequency range | $f_{RANGE}$ | 2400 - 2483.5 MHz | 2400 | — | 2483.5 | MHz |
| LO tuning frequency resolution with 38.4 MHz crystal | $f_{RES}$ | 2400 - 2483.5 MHz | — | — | 73 | Hz |
| Frequency deviation resolution with 38.4 MHz crystal | $df_{RES}$ | 2400 - 2483.5 MHz | — | — | 73 | Hz |
| Maximum frequency deviation with 38.4 MHz crystal | $df_{MAX}$ | 2400 - 2483.5 MHz | — | — | 1677 | kHz |

### 4.1.8 2.4 GHz RF Transceiver Characteristics

#### 4.1.8.1 RF Transmitter General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_{OP}$ = 25 °C, VDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

**Table 4.9. RF Transmitter General Characteristics for 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum TX power[1] | $POUT_{MAX}$ | 17 dBm-rated part numbers. PAVDD connected directly to VDD[2] (MGM12P32) | — | 17 | — | dBm |
| | | 10 dBm-rated part numbers (MGM12P02 & MGM12P22) | — | 10 | — | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | CW | | -30 | — | dBm |
| Output power step size | $POUT_{STEP}$ | -5 dBm< Output power < 0 dBm | — | 1 | — | dB |
| | | 0 dBm < output power < $POUT_{MAX}$ | — | 0.5 | — | dB |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 1.8 V < $V_{VREGVDD}$ < 3.8 V, PAVDD connected directly to VDD, for output power > 10 dBm. | — | 5.7 | — | dB |
| | | 1.8 V < $V_{VREGVDD}$ < 3.8 V using DC-DC converter | — | 3.4 | — | dB |
| Output power variation vs temperature at $POUT_{MAX}$ | $POUT_{VAR_T}$ | From -40 to +85 °C, PAVDD connected to DC-DC output | — | 1.5 | — | dB |
| | | From -40 to +85 °C, PAVDD connected to VDD | — | 1.5 | — | dB |
| Output power variation vs RF frequency at $POUT_{MAX}$ | $POUT_{VAR_F}$ | Over RF tuning frequency range | — | 0.2 | — | dB |
| RF tuning frequency range | $F_{RANGE}$ | | 2400 | — | 2483.5 | MHz |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. For Bluetooth, the Maximum TX power on Channel 2456 is limited to +15 dBm to comply with In-band Spurious emissions.

#### 4.1.8.2 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_{OP}$ = 25 °C, VDD = 3.3 V, DC-DC enabled. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

**Table 4.10. RF Receiver General Characteristics for 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 2400 | — | 2483.5 | MHz |
| Receive mode maximum spurious emission | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -57 | — | dBm |
| | | 1 GHz to 12 GHz | — | -47 | — | dBm |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216 MHz to 960 MHz, Conducted Measurement | — | -55.2 | — | dBm |
| | | Above 960 MHz, Conducted Measurement | — | -47.2 | — | dBm |

#### 4.1.8.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V, DC-DC enabled. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz.

**Table 4.11. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sensitivity, 0.1% BER | SENS | Signal is reference signal[1]. Using DC-DC converter. (MGM12P02) | — | -94.4 | — | dBm |
| | | With non-ideal signal. Using DC-DC converter. (MGM12P02) | — | -94.3 | — | dBm |
| | | Signal is reference signal.[1] Using DC-DC converter.<br>(MGM12P22 & MGM12P32) | — | -100.3 | — | dBm |
| | | With non-ideal signal. Using DC-DC converter. (MGM12P22 & MGM12P32) | — | -100.1 | — | dBm |

**Note:**

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9, Packet length = 37 bytes; interferer data = PRBS15; frequency accuracy better than 1 ppm.

#### 4.1.8.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V, DC-DC enabled. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz.1

**Table 4.12. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sensitivity, 0.1% BER | SENS | Signal is reference signal[1]. Using DC-DC converter. | — | -91 | — | dBm |
| | | With non-ideal signal. Using DC-DC converter. (MGM12P02) | — | -90.8 | — | dBm |
| | | Signal is reference signal.[1] Using DC-DC converter.<br>(MGM12P22 & MGM12P32) | — | -97 | — | dBm |
| | | With non-ideal signal. Using DC-DC converter. (MGM12P22 & MGM12P32) | — | -96.7 | — | dBm |

**Note:**

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 2 Mbps, desired data = PRBS9, Packet length = 37 bytes; interferer data = PRBS15; frequency accuracy better than 1 ppm.

#### 4.1.8.5 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_{OP}$ = 25 °C, VDD = 3.3 V, DC-DC enabled. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

**Table 4.13. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sensitivity, 1% PER | SENS | Signal is reference signal.[1] Using DC-DC converter. | — | -102 | — | dBm |
| | | Signal is reference signal. Using DC-DC converter.<br>(MGM12P22 & MGM12P32) | — | -105.7 | — | dBm |

**Note:**

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s, Packet length = 20 bytes.

### 4.1.9 Current Consumption

#### 4.1.9.1 Low-Frequency Crystal Oscillator (LFXO)

**Table 4.14. Low-Frequency Crystal Oscillator (LFXO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal Frequency | $f_{LFXO}$ | | — | 32.768 | — | kHz |
| Crystal Frequency Tolerance | | | -100 | | +100 | ppm |

#### 4.1.9.2 High-Frequency Crystal Oscillator (HFXO)

**Table 4.15. High-Frequency Crystal Oscillator (HFXO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal Frequency | $f_{HFXO}$ | | | 38.4 | | MHz |
| Frequency Tolerance for the crystal | $FT_{HFXO}$ | | -40 | — | 40 | ppm |

#### 4.1.9.3 Low-Frequency RC Oscillator (LFRCO)

**Table 4.16. Low-Frequency RC Oscillator (LFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{LFRCO}$ | ENVREF[1] = 1 | 31.3 | 32.768 | 33.6 | kHz |
| | | ENVREF[1] = 0 | 31.3 | 32.768 | 33.4 | kHz |
| Startup time | $t_{LFRCO}$ | | — | 500 | — | µs |
| Current consumption [2] | $I_{LFRCO}$ | ENVREF = 1 in CMU_LFRCOCTRL | — | 370 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 520 | — | nA |

**Note:**
1. In CMU_LFRCOCTRL register.
2. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.

#### 4.1.9.4 High-Frequency RC Oscillator (HFRCO)

**Table 4.17. High-Frequency RC Oscillator (HFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency accuracy | $f_{HFRCO_ACC}$ | At production calibrated frequencies, across supply voltage and temperature | -2.5 | — | 2.5 | % |
| Start-up time | $t_{HFRCO}$ | $f_{HFRCO} \geq 19$ MHz | — | 300 | — | ns |
| | | $4 < f_{HFRCO} < 19$ MHz | — | 1 | — | µs |
| | | $f_{HFRCO} \leq 4$ MHz | — | 2.5 | — | µs |
| Current consumption on all supplies | $I_{HFRCO}$ | $f_{HFRCO} = 38$ MHz | — | 244 | 265 | µA |
| | | $f_{HFRCO} = 32$ MHz | — | 204 | 222 | µA |
| | | $f_{HFRCO} = 26$ MHz | — | 173 | 188 | µA |
| | | $f_{HFRCO} = 19$ MHz | — | 143 | 156 | µA |
| | | $f_{HFRCO} = 16$ MHz | — | 123 | 136 | µA |
| | | $f_{HFRCO} = 13$ MHz | — | 110 | 124 | µA |
| | | $f_{HFRCO} = 7$ MHz | — | 85 | 94 | µA |
| | | $f_{HFRCO} = 4$ MHz | — | 32 | 37 | µA |
| | | $f_{HFRCO} = 2$ MHz | — | 28 | 34 | µA |
| | | $f_{HFRCO} = 1$ MHz | — | 26 | 31 | µA |
| Coarse trim step size (% of period) | $SS_{HFRCO_COARSE}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{HFRCO_FINE}$ | | — | 0.1 | — | % |
| Period jitter | $PJ_{HFRCO}$ | | — | 0.2 | — | % RMS |

#### 4.1.9.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

**Table 4.18. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency accuracy | $f_{AUXHFRCO_ACC}$ | At production calibrated frequencies, across supply voltage and temperature | -3 | — | 3 | % |
| Start-up time | $t_{AUXHFRCO}$ | $f_{AUXHFRCO} \geq 19$ MHz | — | 400 | — | ns |
| | | $4 < f_{AUXHFRCO} < 19$ MHz | — | 1.4 | — | µs |
| | | $f_{AUXHFRCO} \leq 4$ MHz | — | 2.5 | — | µs |
| Current consumption on all supplies | $I_{AUXHFRCO}$ | $f_{AUXHFRCO}$ = 38 MHz | — | 193 | 213 | µA |
| | | $f_{AUXHFRCO}$ = 32 MHz | — | 157 | 175 | µA |
| | | $f_{AUXHFRCO}$ = 26 MHz | — | 135 | 151 | µA |
| | | $f_{AUXHFRCO}$ = 19 MHz | — | 108 | 122 | µA |
| | | $f_{AUXHFRCO}$ = 16 MHz | — | 100 | 113 | µA |
| | | $f_{AUXHFRCO}$ = 13 MHz | — | 77 | 88 | µA |
| | | $f_{AUXHFRCO}$ = 7 MHz | — | 53 | 63 | µA |
| | | $f_{AUXHFRCO}$ = 4 MHz | — | 29 | 36 | µA |
| | | $f_{AUXHFRCO}$ = 2 MHz | — | 28 | 34 | µA |
| | | $f_{AUXHFRCO}$ = 1 MHz | — | 27 | 31 | µA |
| Coarse trim step size (% of period) | $SS_{AUXHFRCO_COARSE}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{AUXHFRCO_FINE}$ | | — | 0.1 | — | % |
| Period jitter | $PJ_{AUXHFRCO}$ | | — | 0.2 | — | % RMS |

#### 4.1.9.6 Ultra-low Frequency RC Oscillator (ULFRCO)

**Table 4.19. Ultra-low Frequency RC Oscillator (ULFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{ULFRCO}$ | | 0.95 | 1 | 1.07 | kHz |

### 4.1.10 Flash Memory Characteristics[1]

**Table 4.20. Flash Memory Characteristics[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash erase cycles before failure | $EC_{FLASH}$ | | 10000 | — | — | cycles |
| Flash data retention | $RET_{FLASH}$ | | 10 | — | — | years |
| Word (32-bit) programming time | $t_{W_PROG}$ | Burst write, 128 words, average time per word | 20 | 24.4 | 30 | µs |
| | | Single word | 60 | 68.4 | 80 | µs |
| Page erase time[2] | $t_{PERASE}$ | | 20 | 26.4 | 35 | ms |
| Mass erase time[3] | $t_{MERASE}$ | | 20 | 26.5 | 35 | ms |
| Device erase time[4] [5] | $t_{DERASE}$ | | — | 82 | 100 | ms |
| Erase current[6] | $I_{ERASE}$ | Page Erase | — | — | 1.6 | mA |
| Write current[6] | $I_{WRITE}$ | | — | — | 3.8 | mA |
| Supply voltage during flash erase and write | $V_{FLASH}$ | | 1.62 | — | 3.6 | V |

**Note:**

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
3. Mass erase is issued by the CPU and erases all flash.
4. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
5. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
6. Measured at 25 °C.

### 4.1.11 General-Purpose I/O (GPIO)

**Table 4.21. General-Purpose I/O (GPIO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input low voltage[1] | $V_{IL}$ | GPIO pins | — | — | IOVDD*0.3 | V |
| | | RESETn | — | — | AVDD*0.3 | V |
| Input high voltage[1] | $V_{IH}$ | GPIO pins | IOVDD*0.7 | — | — | V |
| | | RESETn | AVDD*0.7 | — | — | V |
| Output high voltage relative to IOVDD | $V_{OH}$ | Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[2] = WEAK | IOVDD*0.8 | — | — | V |
| | | Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[2] = WEAK | IOVDD*0.6 | — | — | V |
| | | Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[2] = STRONG | IOVDD*0.8 | — | — | V |
| | | Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[2] = STRONG | IOVDD*0.6 | — | — | V |
| Output low voltage relative to IOVDD | $V_{OL}$ | Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[2] = WEAK | — | — | IOVDD*0.2 | V |
| | | Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[2] = WEAK | — | — | IOVDD*0.4 | V |
| | | Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[2] = STRONG | — | — | IOVDD*0.2 | V |
| | | Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[2] = STRONG | — | — | IOVDD*0.4 | V |
| Input leakage current | $I_{IOLEAK}$ | All GPIO except LFXO pins, GPIO ≤ IOVDD | — | 0.1 | 30 | nA |
| | | LFXO Pins, GPIO ≤ IOVDD | — | 0.1 | 50 | nA |
| Input leakage current on 5VTOL pads above IOVDD | $I_{5VTOLLEAK}$ | IOVDD < GPIO ≤ IOVDD + 2 V | — | 3.3 | 15 | µA |
| I/O pin pull-up/pull-down resistor[3] | $R_{PUD}$ | | 30 | 40 | 65 | kΩ |
| Pulse width of pulses removed by the glitch suppression filter | $t_{IOGLITCH}$ | | 15 | 25 | 45 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output fall time, From 70% to 30% of $V_{IO}$ | $t_{IOOF}$ | $C_L$ = 50 pF, DRIVESTRENGTH[2] = STRONG, SLEWRATE[2] = 0x6 | — | 1.8 | — | ns |
| | | $C_L$ = 50 pF, DRIVESTRENGTH[2] = WEAK, SLEWRATE[2] = 0x6 | — | 4.5 | — | ns |
| Output rise time, From 30% to 70% of $V_{IO}$ | $t_{IOOR}$ | $C_L$ = 50 pF, DRIVESTRENGTH[2] = STRONG, SLEWRATE = 0x6[2] | — | 2.2 | — | ns |
| | | $C_L$ = 50 pF, DRIVESTRENGTH[2] = WEAK, SLEWRATE[2] = 0x6 | — | 7.4 | — | ns |
| RESETn low time to ensure pin reset | $T_{RESET}$ | | 100 | — | — | ns |

**Note:**

1. GPIO input threshold are proportional to the IOVDD supply, except for RESETn which is proportional to AVDD.
2. In GPIO_Pn_CTRL register.
3. GPIO pull-ups are referenced to the IOVDD supply, except for RESETn, which connects to AVDD.

### 4.1.12 Voltage Monitor (VMON)

**Table 4.22. Voltage Monitor (VMON)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply current (including I_SENSE) | $I_{VMON}$ | In EM0 or EM1, 1 active channel | — | 6.3 | 10 | µA |
| | | In EM0 or EM1, All channels active | — | 12.5 | 17 | µA |
| | | In EM2, EM3 or EM4, 1 channel active and above threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 1 channel active and below threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, All channels active and above threshold | — | 99 | — | nA |
| | | In EM2, EM3 or EM4, All channels active and below threshold | — | 99 | — | nA |
| Loading of monitored supply | $I_{SENSE}$ | In EM0 or EM1 | — | 2 | — | µA |
| | | In EM2, EM3 or EM4 | — | 2 | — | nA |
| Threshold range | $V_{VMON_RANGE}$ | | 1.62 | — | 3.4 | V |
| Threshold step size | $N_{VMON_STESP}$ | Coarse | — | 200 | — | mV |
| | | Fine | — | 20 | — | mV |
| Response time | $t_{VMON_RES}$ | Supply drops at 1V/µs rate | — | 460 | — | ns |
| Hysteresis | $V_{VMON_HYST}$ | | — | 26 | — | mV |

### 4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

**Table 4.23. Analog to Digital Converter (ADC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resolution | $V_{RESOLUTION}$ | | 6 | — | 12 | Bits |
| Input voltage range[1] | $V_{ADCIN}$ | Single ended | — | — | $V_{FS}$ | V |
| | | Differential | $-V_{FS}/2$ | — | $V_{FS}/2$ | V |
| Input range of external reference voltage, single ended and differential | $V_{ADCREFIN_P}$ | | 1 | — | $V_{AVDD}$ | V |
| Power supply rejection[2] | $PSRR_{ADC}$ | At DC | — | 80 | — | dB |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | At DC | — | 80 | — | dB |
| Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE[3] = KEEPADCWARM | $I_{ADC_CONTINUOUS_LP}$ | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4] | — | 270 | 315 | µA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [4] | — | 125 | — | µA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [4] | — | 80 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[3] = NORMAL | $I_{ADC_NORMAL_LP}$ | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4] | — | 45 | — | µA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [4] | — | 8 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[3] = KEEPINSTANDBY or KEEPINSLOWACC | $I_{ADC_STANDBY_LP}$ | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4] | — | 105 | — | µA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [4] | — | 70 | — | µA |
| Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE[3] = KEEPADCWARM | $I_{ADC_CONTINUOUS_HP}$ | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4] | — | 325 | — | µA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [4] | — | 175 | — | µA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [4] | — | 125 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[3] = NORMAL | $I_{ADC_NORMAL_HP}$ | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4] | — | 85 | — | µA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [4] | — | 16 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[3] = KEEPINSTANDBY or KEEPINSLOWACC | $I_{ADC_STANDBY_HP}$ | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4] | — | 160 | — | µA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [4] | — | 125 | — | µA |
| Current from HFPERCLK | $I_{ADC_CLK}$ | HFPERCLK = 16 MHz | — | 160 | — | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ADC clock frequency | $f_{ADCCLK}$ | | — | — | 16 | MHz |
| Throughput rate | $f_{ADCRATE}$ | | — | — | 1 | Msps |
| Conversion time[5] | $t_{ADCCONV}$ | 6 bit | — | 7 | — | cycles |
| | | 8 bit | — | 9 | — | cycles |
| | | 12 bit | — | 13 | — | cycles |
| Startup time of reference generator and ADC core | $t_{ADCSTART}$ | WARMUPMODE[3] = NORMAL | — | — | 5 | µs |
| | | WARMUPMODE[3] = KEEPIN-STANDBY | — | — | 2 | µs |
| | | WARMUPMODE[3] = KEEPINSLO-WACC | — | — | 1 | µs |
| SNDR at 1Msps and $f_{IN}$ = 10kHz | $SNDR_{ADC}$ | Internal reference[6], differential measurement | 58 | 67 | — | dB |
| | | External reference[7], differential measurement | — | 68 | — | dB |
| Spurious-free dynamic range (SFDR) | $SFDR_{ADC}$ | 1 MSamples/s, 10 kHz full-scale sine wave | — | 75 | — | dB |
| Differential non-linearity (DNL) | $DNL_{ADC}$ | 12 bit resolution, No missing co-des | -1 | — | 2 | LSB |
| Integral non-linearity (INL), End point method | $INL_{ADC}$ | 12 bit resolution | -6 | — | 6 | LSB |
| Offset error | $V_{ADCOFFSETERR}$ | | -3 | 0 | 3 | LSB |
| Gain error in ADC | $V_{ADCGAIN}$ | Using internal reference | — | -0.2 | 3.5 | % |
| | | Using external reference | — | -1 | — | % |
| Temperature sensor slope | $V_{TS_SLOPE}$ | | — | -1.84 | — | mV/°C |

**Note:**

1. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_CTRL register.
4. In ADCn_BIASPROG register.
5. Derived from ADCCLK.
6. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.
7. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.

### 4.1.14 Analog Comparator (ACMP)

**Table 4.24. Analog Comparator (ACMP)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ACMPIN}$ | ACMPVDD = ACMPn_CTRL_PWRSEL [1] | — | — | $V_{ACMPVDD}$ | V |
| Supply voltage | $V_{ACMPVDD}$ | BIASPROG[2] ≤ 0x10 or FULLBIAS[2] = 0 | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | 0x10 < BIASPROG[2] ≤ 0x20 and FULLBIAS[2] = 1 | 2.1 | — | $V_{VREGVDD_MAX}$ | V |
| Active current not including voltage reference[3] | $I_{ACMP}$ | BIASPROG[2] = 0x10, FULLBIAS[2] = 0 | — | 306 | — | nA |
| | | BIASPROG[2] = 0x02, FULLBIAS[2] = 1 | — | 6.5 | — | µA |
| | | BIASPROG[2] = 0x20, FULLBIAS[2] = 1 | — | 75 | 92 | µA |
| Current consumption of internal voltage reference[3] | $I_{ACMPREF}$ | VLP selected as input using 2.5 V Reference / 4 (0.625 V) | — | 50 | — | nA |
| | | VLP selected as input using VDD | — | 20 | — | nA |
| | | VBDIV selected as input using 1.25 V reference / 1 | — | 4.1 | — | µA |
| | | VADIV selected as input using VDD/1 | — | 2.4 | — | µA |
| Hysteresis ($V_{CM}$ = 1.25 V, BIASPROG[2] = 0x10, FULLBIAS[2] = 1) | $V_{ACMPHYST}$ | HYSTSEL[4] = HYST0 | -3 | 0 | 3 | mV |
| | | HYSTSEL[4] = HYST1 | 5 | 18 | 27 | mV |
| | | HYSTSEL[4] = HYST2 | 12 | 33 | 50 | mV |
| | | HYSTSEL[4] = HYST3 | 17 | 46 | 67 | mV |
| | | HYSTSEL[4] = HYST4 | 23 | 57 | 86 | mV |
| | | HYSTSEL[4] = HYST5 | 26 | 68 | 104 | mV |
| | | HYSTSEL[4] = HYST6 | 30 | 79 | 130 | mV |
| | | HYSTSEL[4] = HYST7 | 34 | 90 | 150 | mV |
| | | HYSTSEL[4] = HYST8 | -3 | 0 | 3 | mV |
| | | HYSTSEL[4] = HYST9 | -27 | -18 | -5 | mV |
| | | HYSTSEL[4] = HYST10 | -50 | -33 | -12 | mV |
| | | HYSTSEL[4] = HYST11 | -67 | -45 | -17 | mV |
| | | HYSTSEL[4] = HYST12 | -86 | -57 | -23 | mV |
| | | HYSTSEL[4] = HYST13 | -104 | -67 | -26 | mV |
| | | HYSTSEL[4] = HYST14 | -130 | -78 | -30 | mV |
| | | HYSTSEL[4] = HYST15 | -155 | -88 | -34 | mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Comparator delay[5] | $t_{ACMPDELAY}$ | BIASPROG[2] = 0x10, FULLBIAS[2] = 0 | — | 3.7 | — | µs |
| | | BIASPROG[2] = 0x02, FULLBIAS[2] = 1 | — | 360 | — | ns |
| | | BIASPROG[2] = 0x20, FULLBIAS[2] = 1 | — | 35 | — | ns |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG[2] =0x10, FULLBIAS[2] = 1 | -35 | — | 35 | mV |
| Reference voltage | $V_{ACMPREF}$ | Internal 1.25 V reference | 1 | 1.25 | 1.47 | V |
| | | Internal 2.5 V reference | 2 | 2.5 | 2.8 | V |
| Capacitive sense internal resistance | $R_{CSRES}$ | CSRESSEL[6] = 0 | — | infinite | — | kΩ |
| | | CSRESSEL[6] = 1 | — | 15 | — | kΩ |
| | | CSRESSEL[6] = 2 | — | 27 | — | kΩ |
| | | CSRESSEL[6] = 3 | — | 39 | — | kΩ |
| | | CSRESSEL[6] = 4 | — | 51 | — | kΩ |
| | | CSRESSEL[6] = 5 | — | 100 | — | kΩ |
| | | CSRESSEL[6] = 6 | — | 162 | — | kΩ |
| | | CSRESSEL[6] = 7 | — | 235 | — | kΩ |

**Note:**

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. In ACMPn_CTRL register.
3. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
4. In ACMPn_HYSTERESIS registers.
5. ± 100 mV differential drive.
6. In ACMPn_INPUTSEL register.

### 4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

**Table 4.25. Digital to Analog Converter (VDAC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{DACOUT}$ | Single-Ended | 0 | — | $V_{VREF}$ | V |
| | | Differential[1] | $-V_{VREF}$ | — | $V_{VREF}$ | V |
| Current consumption including references (2 channels)[2] | $I_{DAC}$ | 500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4 | — | 396 | — | µA |
| | | 44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4 | — | 72 | — | µA |
| | | 200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, REFSEL = 4, SETTLETIME = 0x02, WARMUPTIME = 0x0A | — | 1.2 | — | µA |
| Current from HFPERCLK[3] | $I_{DAC_CLK}$ | | — | 5.8 | — | µA/MHz |
| Sample rate | $SR_{DAC}$ | | — | — | 500 | ksps |
| DAC clock frequency | $f_{DAC}$ | | — | — | 1 | MHz |
| Conversion time | $t_{DACCONV}$ | $f_{DAC}$ = 1MHz | 2 | — | — | µs |
| Settling time | $t_{DACSETTLE}$ | 50% fs step settling to 5 LSB | — | 2.5 | — | µs |
| Startup time | $t_{DACSTARTUP}$ | Enable to 90% fs output, settling to 10 LSB | — | — | 12 | µs |
| Output impedance | $R_{OUT}$ | DRIVESTRENGTH = 2, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -8 mA < $I_{OUT}$ < 8 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -400 µA < $I_{OUT}$ < 400 µA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 2, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -2 mA < $I_{OUT}$ < 2 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -100 µA < $I_{OUT}$ < 100 µA, Full supply range | — | 2 | — | Ω |
| Power supply rejection ratio[4] | PSRR | Vout = 50% fs. DC | — | 65.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz | $SNDR_{DAC}$ | 500 ksps, single-ended, internal 1.25V reference | — | 60.4 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 61.6 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 64.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 63.3 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 64.4 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 65.8 | — | dB |
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz | $SNDR_{DAC_BAND}$ | 500 ksps, single-ended, internal 1.25V reference | — | 65.3 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 66.7 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 70.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 67.8 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 69.0 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 68.5 | — | dB |
| Total harmonic distortion | THD | | — | 70.2 | — | dB |
| Differential non-linearity[5] | $DNL_{DAC}$ | | -0.99 | — | 1 | LSB |
| Intergral non-linearity | $INL_{DAC}$ | | -4 | — | 4 | LSB |
| Offset error[6] | $V_{OFFSET}$ | T = 25 °C | -8 | — | 8 | mV |
| | | Across operating temperature range | -25 | — | 25 | mV |
| Gain error[6] | $V_{GAIN}$ | T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -2.5 | — | 2.5 | % |
| | | T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5) | -5 | — | 5 | % |
| | | T = 25 °C, External reference (REFSEL = VDD or EXT) | -1.8 | — | 1.8 | % |
| | | Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -3.5 | — | 3.5 | % |
| | | Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5) | -7.5 | — | 7.5 | % |
| | | Across operating temperature range, External reference (REFSEL = VDD or EXT) | -2.0 | — | 2.0 | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External load capactiance, OUTSCALE=0 | $C_{LOAD}$ | | — | — | 75 | pF |

**Note:**

1. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
2. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
3. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC peripheral is enabled in the CMU.
4. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.

### 4.1.16 Current Digital to Analog Converter (IDAC)

**Table 4.26. Current Digital to Analog Converter (IDAC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Number of ranges | $N_{IDAC_RANGES}$ | | — | 4 | — | ranges |
| Output current | $I_{IDAC_OUT}$ | RANGESEL[1] = RANGE0 | 0.05 | — | 1.6 | µA |
| | | RANGESEL[1] = RANGE1 | 1.6 | — | 4.7 | µA |
| | | RANGESEL[1] = RANGE2 | 0.5 | — | 16 | µA |
| | | RANGESEL[1] = RANGE3 | 2 | — | 64 | µA |
| Linear steps within each range | $N_{IDAC_STEPS}$ | | — | 32 | — | steps |
| Step size | $SS_{IDAC}$ | RANGESEL[1] = RANGE0 | — | 50 | — | nA |
| | | RANGESEL[1] = RANGE1 | — | 100 | — | nA |
| | | RANGESEL[1] = RANGE2 | — | 500 | — | nA |
| | | RANGESEL[1] = RANGE3 | — | 2 | — | µA |
| Total accuracy, STEPSEL[1] = 0x10 | $ACC_{IDAC}$ | EM0 or EM1, AVDD=3.3 V, T = 25 °C | -3 | — | 3 | % |
| | | EM0 or EM1, Across operating temperature range | -18 | — | 22 | % |
| | | EM2 or EM3, Source mode, RANGESEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C | — | -2 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C | — | -1.7 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.8 | — | % |
| | | EM2 or EM3, Source mode, RANGESEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C | — | -0.7 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C | — | -0.6 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGESEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| Start up time | $t_{IDAC_SU}$ | Output within 1% of steady state value | — | 5 | — | µs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Settling time, (output settled within 1% of steady state value), | $t_{IDAC_SETTLE}$ | Range setting is changed | — | 5 | — | µs |
| | | Step value is changed | — | 1 | — | µs |
| Current consumption[2] | $I_{IDAC}$ | EM0 or EM1 Source mode, excluding output current, Across operating temperature range | — | 11 | 18 | µA |
| | | EM0 or EM1 Sink mode, excluding output current, Across operating temperature range | — | 13 | 21 | µA |
| | | EM2 or EM3 Source mode, excluding output current, T = 25 °C | — | 0.023 | — | µA |
| | | EM2 or EM3 Sink mode, excluding output current, T = 25 °C | — | 0.041 | — | µA |
| | | EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C | — | 11 | — | µA |
| | | EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C | — | 13 | — | µA |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | $I_{COMP_SRC}$ | RANGESEL[1] = RANGE0, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-100 mV) | — | 0.11 | — | % |
| | | RANGESEL[1] = RANGE1, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-100 mV) | — | 0.06 | — | % |
| | | RANGESEL[1] = RANGE2, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-150 mV) | — | 0.04 | — | % |
| | | RANGESEL[1] = RANGE3, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-250 mV) | — | 0.03 | — | % |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD | $I_{COMP_SINK}$ | RANGESEL[1] = RANGE0, output voltage = 100 mV | — | 0.12 | — | % |
| | | RANGESEL[1] = RANGE1, output voltage = 100 mV | — | 0.05 | — | % |
| | | RANGESEL[1] = RANGE2, output voltage = 150 mV | — | 0.04 | — | % |
| | | RANGESEL[1] = RANGE3, output voltage = 250 mV | — | 0.03 | — | % |

**Note:**

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

### 4.1.17 Capacitive Sense (CSEN)

**Table 4.27. Capacitive Sense (CSEN)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single conversion time (1x accumulation) | $t_{CNV}$ | 12-bit SAR Conversions | — | 20.2 | — | µs |
| | | 16-bit SAR Conversions | — | 26.4 | — | µs |
| | | Delta Modulation Conversion (single comparison) | — | 1.55 | — | µs |
| Maximum external capacitive load | $C_{EXTMAX}$ | IREFPROG=7 (Gain = 1x), including routing parasitics | — | 68 | — | pF |
| | | IREFPROG=0 (Gain = 10x), including routing parasitics | — | 680 | — | pF |
| Maximum external series impedance | $R_{EXTMAX}$ | | — | 1 | — | kΩ |
| Supply current, EM2 bonded conversions, WARMUPMODE=NORMAL, WARMUPCNT=0 | $I_{CSEN_BOND}$ | 12-bit SAR conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 326 | — | nA |
| | | Delta Modulation conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 226 | — | nA |
| | | 12-bit SAR conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 33 | — | nA |
| | | Delta Modulation conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 25 | — | nA |
| Supply current, EM2 scan conversions, WARMUPMODE=NORMAL, WARMUPCNT=0 | $I_{CSEN_EM2}$ | 12-bit SAR conversions, 20 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan[1] | — | 690 | — | nA |
| | | Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan[1] | — | 515 | — | nA |
| | | 12-bit SAR conversions, 200 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan[1] | — | 79 | — | nA |
| | | Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan[1] | — | 57 | — | nA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply current, continuous conversions, WARMUPMODE=KEEPCSENWARM | $I_{CSEN_ACTIVE}$ | SAR or Delta Modulation conversions of 33 pF capacitor, IREFPROG=0 (Gain = 10x), always on | — | 90.5 | — | µA |
| HFPERCLK supply current | $I_{CSEN_HFPERCLK}$ | Current contribution from HFPERCLK when clock to CSEN block is enabled. | — | 2.25 | — | µA/MHz |

**Note:**

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the peripheral is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

### 4.1.18 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAINOUTEN = 1, $C_{LOAD}$ = 75 pF with OUTSCALE = 0, or $C_{LOAD}$ = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes[1] [2].

**Table 4.28. Operational Amplifier (OPAMP)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (from AVDD) | $V_{OPA}$ | HCMDIS = 0, Rail-to-rail input range | 2 | — | 3.8 | V |
| | | HCMDIS = 1 | 1.62 | — | 3.8 | V |
| Input voltage | $V_{IN}$ | HCMDIS = 0, Rail-to-rail input range | $V_{VSS}$ | — | $V_{OPA}$ | V |
| | | HCMDIS = 1 | $V_{VSS}$ | — | $V_{OPA}$-1.2 | V |
| Input impedance | $R_{IN}$ | | 100 | — | — | MΩ |
| Output voltage | $V_{OUT}$ | | $V_{VSS}$ | — | $V_{OPA}$ | V |
| Load capacitance[3] | $C_{LOAD}$ | OUTSCALE = 0 | — | — | 75 | pF |
| | | OUTSCALE = 1 | — | — | 37.5 | pF |
| Output impedance | $R_{OUT}$ | DRIVESTRENGTH = 2 or 3, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -8 mA < $I_{OUT}$ < 8 mA, Buffer connection, Full supply range | — | 0.25 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -400 µA < $I_{OUT}$ < 400 µA, Buffer connection, Full supply range | — | 0.6 | — | Ω |
| | | DRIVESTRENGTH = 2 or 3, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -2 mA < $I_{OUT}$ < 2 mA, Buffer connection, Full supply range | — | 0.4 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -100 µA < $I_{OUT}$ < 100 µA, Buffer connection, Full supply range | — | 1 | — | Ω |
| Internal closed-loop gain | $G_{CL}$ | Buffer connection | 0.99 | 1 | 1.01 | - |
| | | 3x Gain connection | 2.93 | 2.99 | 3.05 | - |
| | | 16x Gain connection | 15.07 | 15.7 | 16.33 | - |
| Active current[4] | $I_{OPA}$ | DRIVESTRENGTH = 3, OUTSCALE = 0 | — | 580 | — | µA |
| | | DRIVESTRENGTH = 2, OUTSCALE = 0 | — | 176 | — | µA |
| | | DRIVESTRENGTH = 1, OUTSCALE = 0 | — | 13 | — | µA |
| | | DRIVESTRENGTH = 0, OUTSCALE = 0 | — | 4.7 | — | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Open-loop gain | $G_{OL}$ | DRIVESTRENGTH = 3 | — | 135 | — | dB |
| | | DRIVESTRENGTH = 2 | — | 137 | — | dB |
| | | DRIVESTRENGTH = 1 | — | 121 | — | dB |
| | | DRIVESTRENGTH = 0 | — | 109 | — | dB |
| Loop unit-gain frequency[5] | UGF | DRIVESTRENGTH = 3, Buffer connection | — | 3.38 | — | MHz |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 0.9 | — | MHz |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 132 | — | kHz |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 34 | — | kHz |
| | | DRIVESTRENGTH = 3, 3x Gain connection | — | 2.57 | — | MHz |
| | | DRIVESTRENGTH = 2, 3x Gain connection | — | 0.71 | — | MHz |
| | | DRIVESTRENGTH = 1, 3x Gain connection | — | 113 | — | kHz |
| | | DRIVESTRENGTH = 0, 3x Gain connection | — | 28 | — | kHz |
| Phase margin | PM | DRIVESTRENGTH = 3, Buffer connection | — | 67 | — | ° |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 69 | — | ° |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 63 | — | ° |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 68 | — | ° |
| Output voltage noise | $N_{OUT}$ | DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz | — | 146 | — | µVrms |
| | | DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz | — | 163 | — | µVrms |
| | | DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz | — | 170 | — | µVrms |
| | | DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz | — | 176 | — | µVrms |
| | | DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz | — | 313 | — | µVrms |
| | | DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz | — | 271 | — | µVrms |
| | | DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz | — | 247 | — | µVrms |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz | — | 245 | — | µVrms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Slew rate[6] | SR | DRIVESTRENGTH = 3, INCBW=1[7] | — | 4.7 | — | V/µs |
| | | DRIVESTRENGTH = 3, INCBW=0 | — | 1.5 | — | V/µs |
| | | DRIVESTRENGTH = 2, INCBW=1[7] | — | 1.27 | — | V/µs |
| | | DRIVESTRENGTH = 2, INCBW=0 | — | 0.42 | — | V/µs |
| | | DRIVESTRENGTH = 1, INCBW=1[7] | — | 0.17 | — | V/µs |
| | | DRIVESTRENGTH = 1, INCBW=0 | — | 0.058 | — | V/µs |
| | | DRIVESTRENGTH = 0, INCBW=1[7] | — | 0.044 | — | V/µs |
| | | DRIVESTRENGTH = 0, INCBW=0 | — | 0.015 | — | V/µs |
| Startup time[8] | $T_{START}$ | DRIVESTRENGTH = 2 | — | — | 12 | µs |
| Input offset voltage | $V_{OSI}$ | DRIVESTRENGTH = 2 or 3, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 1 or 0, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 2 or 3, across operating temperature range | -12 | — | 12 | mV |
| | | DRIVESTRENGTH = 1 or 0, across operating temperature range | -30 | — | 30 | mV |
| DC power supply rejection ratio[9] | $PSRR_{DC}$ | Input referred | — | 70 | — | dB |
| DC common-mode rejection ratio[9] | $CMRR_{DC}$ | Input referred | — | 70 | — | dB |
| Total harmonic distortion | $THD_{OPA}$ | DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, $V_{OUT}$ = 0.1 V to $V_{OPA}$ - 0.1 V | — | 90 | — | dB |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, $V_{OUT}$ = 0.1 V to $V_{OPA}$ - 0.1 V | — | 90 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{INPUT}$ = 0.5 V, $V_{OUTPUT}$ = 0.5 V.
2. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{INPUT}$ = 0.5 V, $V_{OUTPUT}$ = 1.5 V. Nominal voltage gain is 3.
3. If the maximum $C_{LOAD}$ is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
6. Step between 0.2V and $V_{OPA}$-0.2V, 10%-90% rising/falling range.
7. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
8. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
9. When HCMDIS=1 and input common mode transitions the region from $V_{OPA}$-1.4V to $V_{OPA}$-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

### 4.1.19 Pulse Counter (PCNT)

**Table 4.29. Pulse Counter (PCNT)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input frequency | $F_{IN}$ | Asynchronous Single and Quadrature Modes | — | — | 20 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |

### 4.1.20 Analog Port (APORT)

**Table 4.30. Analog Port (APORT)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply current[1] [2] | $I_{APORT}$ | Operation in EM0/EM1 | — | 7 | — | µA |
| | | Operation in EM2/EM3 | — | 67 | — | nA |

**Note:**

1. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported peripheral currents. Additional peripherals requesting access to APORT do not incur further current.
2. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.

### 4.1.21 I2C

#### 4.1.21.1 I2C Standard-mode (Sm)[1]

**Table 4.31. I2C Standard-mode (Sm)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 100 | kHz |
| SCL clock low time | $t_{LOW}$ | | 4.7 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 4 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 250 | — | — | ns |
| SDA hold time[3] | $t_{HD_DAT}$ | | 100 | — | 3450 | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 4.7 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD_STA}$ | | 4 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 4 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 4.7 | — | — | µs |

**Note:**
1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD_DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

#### 4.1.21.2 I2C Fast-mode (Fm)[1]

**Table 4.32. I2C Fast-mode (Fm)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 400 | kHz |
| SCL clock low time | $t_{LOW}$ | | 1.3 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.6 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 100 | — | — | ns |
| SDA hold time[3] | $t_{HD_DAT}$ | | 100 | — | 900 | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 0.6 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD_STA}$ | | 0.6 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 0.6 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 1.3 | — | — | µs |

**Note:**

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

#### 4.1.21.3 I2C Fast-mode Plus (Fm+)[1]

**Table 4.33. I2C Fast-mode Plus (Fm+)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 1000 | kHz |
| SCL clock low time | $t_{LOW}$ | | 0.5 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.26 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 50 | — | — | ns |
| SDA hold time | $t_{HD_DAT}$ | | 100 | — | — | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 0.26 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD_STA}$ | | 0.26 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 0.26 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 0.5 | — | — | µs |

**Note:**
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

### 4.1.22 USART SPI

#### SPI Master Timing

**Table 4.34. SPI Master Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period [1] [2] [3] | $t_{SCLK}$ | | 2 * $t_{HFPERCLK}$ | — | — | ns |
| CS to MOSI [1] [2] | $t_{CS_MO}$ | | -14.5 | — | 13.5 | ns |
| SCLK to MOSI [1] [2] | $t_{SCLK_MO}$ | | -8.5 | — | 8 | ns |
| MISO setup time [1] [2] | $t_{SU_MI}$ | IOVDD = 1.62 V | 92 | — | — | ns |
| | | IOVDD = 3.0 V | 42 | — | — | ns |
| MISO hold time [1] [2] | $t_{H_MI}$ | | -10 | — | — | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

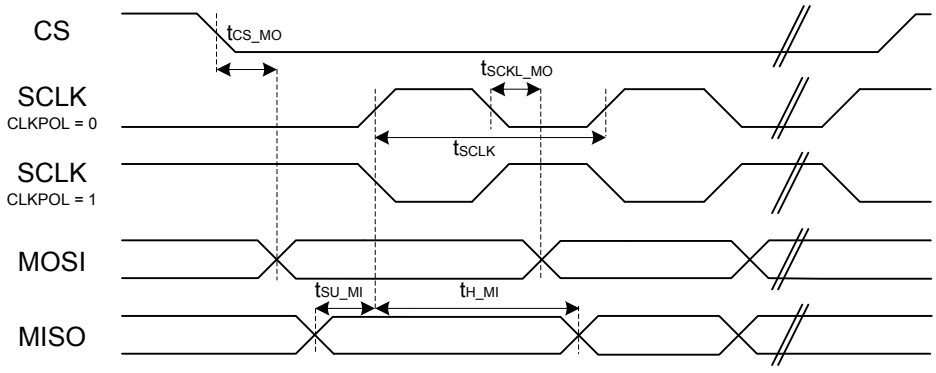



**Figure 4.1. SPI Master Timing Diagram (SMSDELAY = 0)**

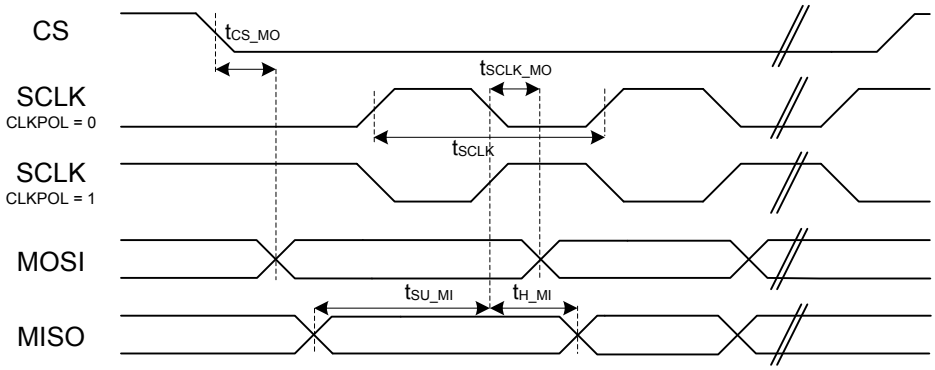



**Figure 4.2. SPI Master Timing Diagram (SMSDELAY = 1)**

### SPI Slave Timing

**Table 4.35. SPI Slave Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period [1] [2] [3] | $t_{SCLK}$ | | 6 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK high time[1] [2] [3] | $t_{SCLK_HI}$ | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK low time[1] [2] [3] | $t_{SCLK_LO}$ | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| CS active to MISO [1] [2] | $t_{CS_ACT_MI}$ | | 4 | — | 70 | ns |
| CS disable to MISO [1] [2] | $t_{CS_DIS_MI}$ | | 4 | — | 50 | ns |
| MOSI setup time [1] [2] | $t_{SU_MO}$ | | 8 | — | — | ns |
| MOSI hold time [1] [2] [3] | $t_{H_MO}$ | | 7 | — | — | ns |
| SCLK to MISO [1] [2] [3] | $t_{SCLK_MI}$ | | 10 + 1.5 * $t_{HFPERCLK}$ | — | 65 + 2.5 * $t_{HFPERCLK}$ | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

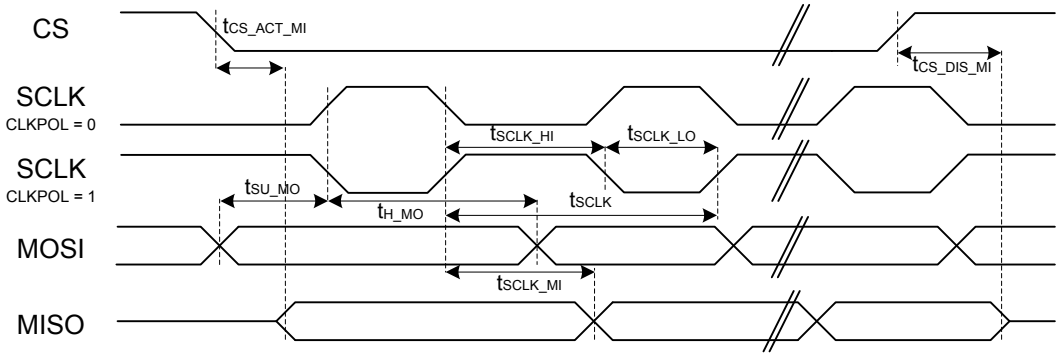



**Figure 4.3. SPI Slave Timing Diagram**

# 5. Typical Connection Diagrams

## 5.1 Network Co-Processor (NCP) Application with UART Host

The MGM12P can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug, and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

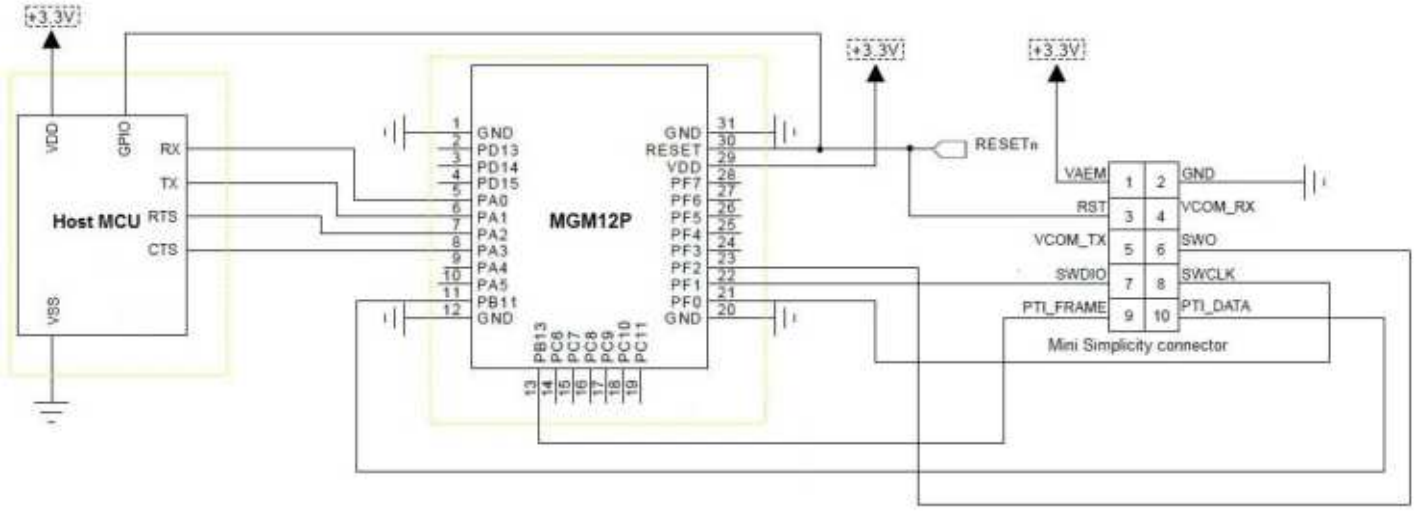



**Figure 5.1. Connection Diagram: UART NCP Configuration**

## 5.2 Network Co-Processor (NCP) Application with SPI Host

The MGM12P can be controlled over the SPI interface as a peripheral to an external host processor. Typical power supply, programming/debug and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

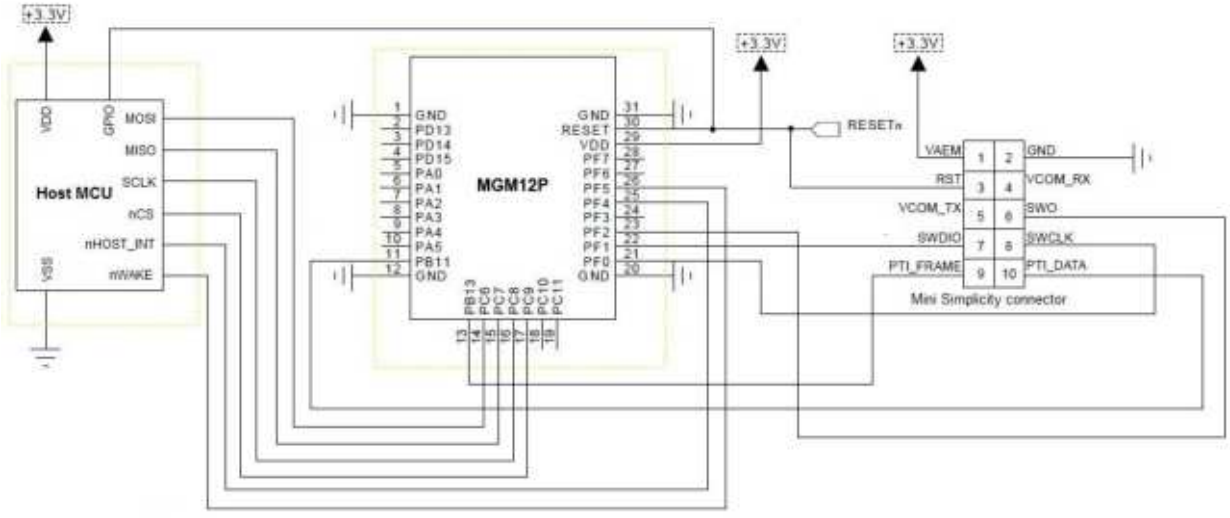



**Figure 5.2. Connection Diagram: SPI NCP Configuration**

### 5.3 SoC Application

The MGM12P can be used in a standalone SoC configuration with no external host processor. Typical power supply and programming/debug connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

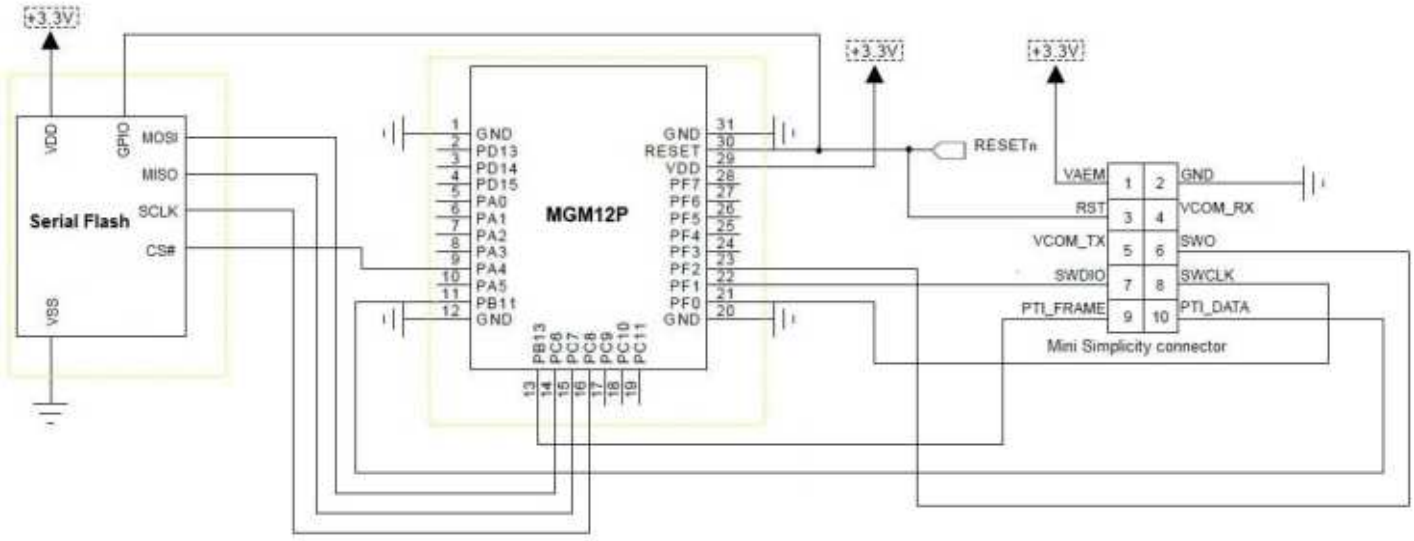



**Figure 5.3. Connection Diagram: SoC Configuration**

# 6. Layout Guidelines

For optimal performance of the MGM12P (with integrated antenna), please follow the PCB layout guidelines and ground plane recommendations indicated in this section.

## 6.1 Module Placement and Application PCB Layout Guidelines

- Place the module at the edge of the PCB, as shown in the figure below.
- Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna (shown in the figure below).
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Do not place plastic or any other dielectric material in touch with the antenna.

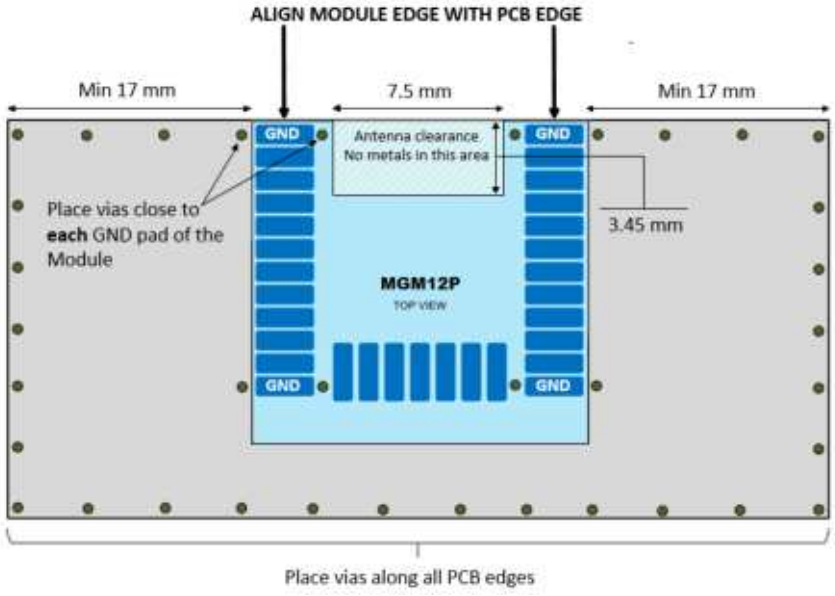



**Figure 6.1. Recommended Application PCB Layout for MGM12P with Integrated Antenna**

The layouts in the next figure will result in severely degraded RF-performance.

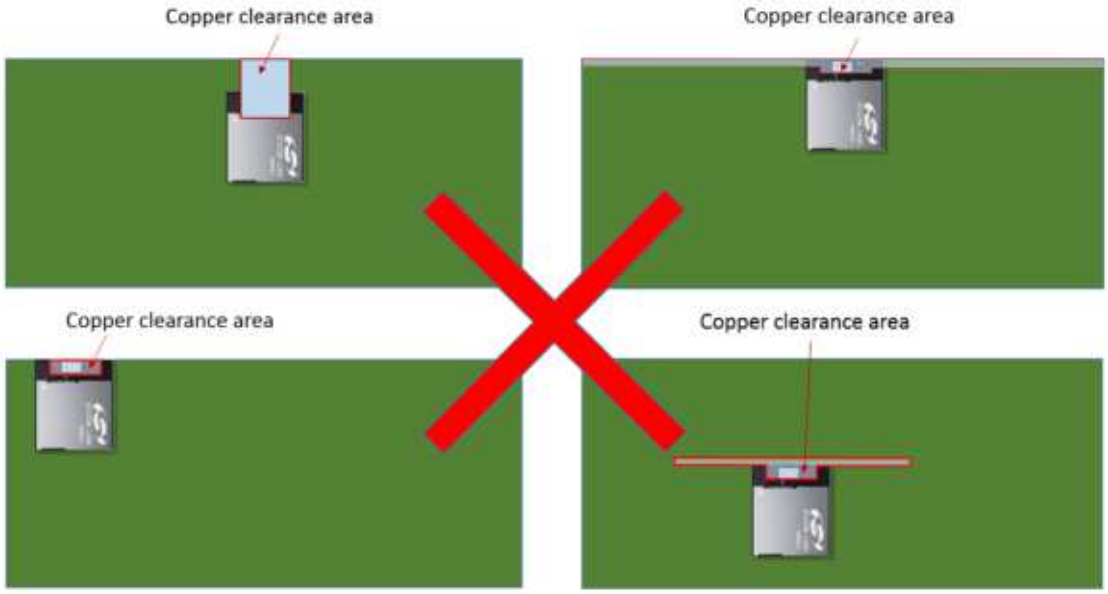



**Figure 6.2. Non-optimal Module Placements for MGM12P with Integrated Antenna**

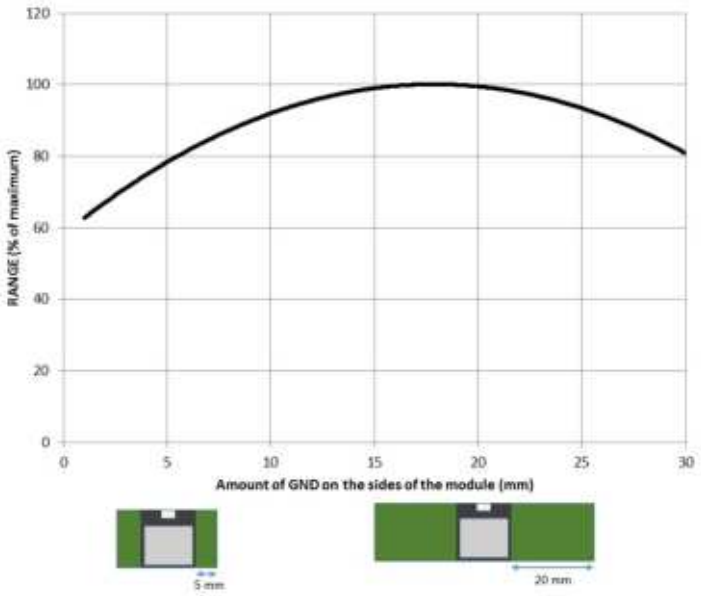



**Figure 6.3. Impact of GND Plane Size vs. Range for MGM12P**

### 6.2 Effect of Plastic and Metal Materials

Do not place plastic or any other dielectric material in closs proximity to the antenna.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

### 6.3 Locating the Module Close to Human Body

Placing the module in touch or very close to the human body will negatively impact antenna efficiency and reduce range.

### 6.4 2D Radiation Pattern Plots

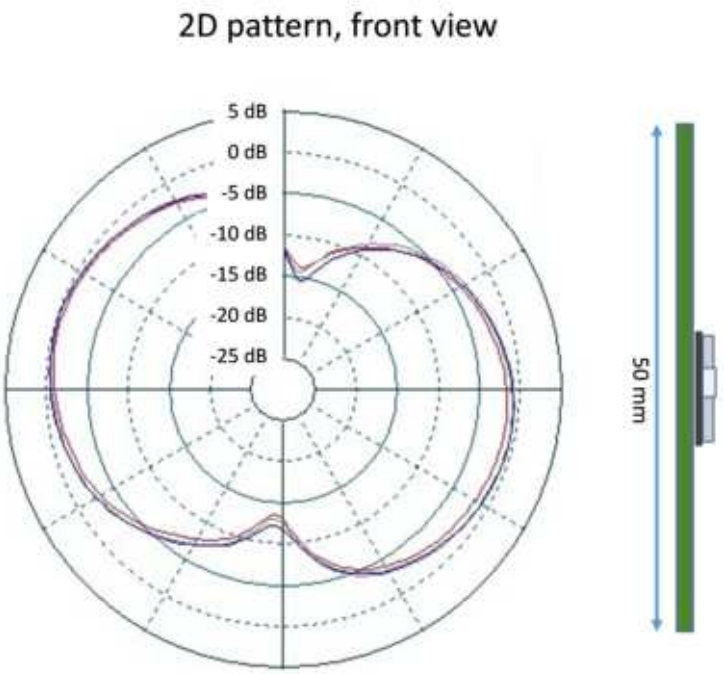



**Figure 6.4. Typical 2D Radiation Pattern – Front View**

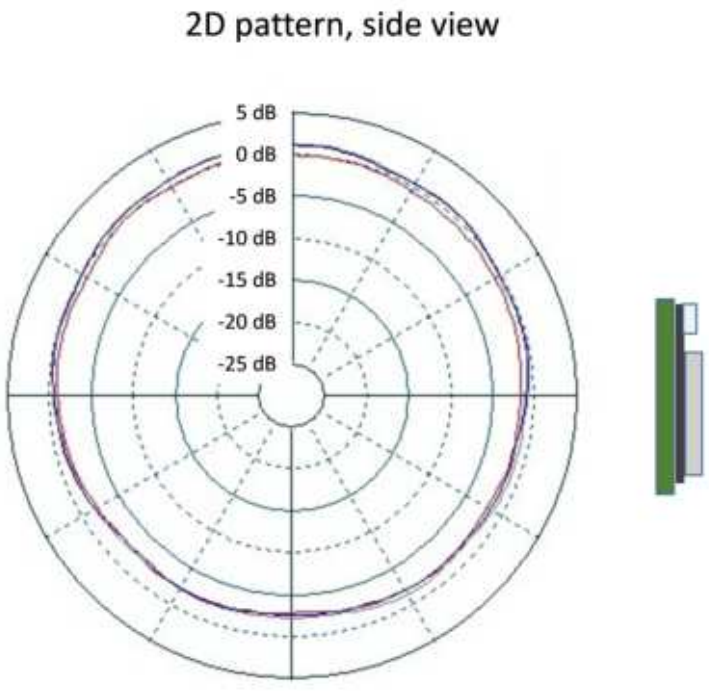



**Figure 6.5. Typical 2D Radiation Pattern – Side View**

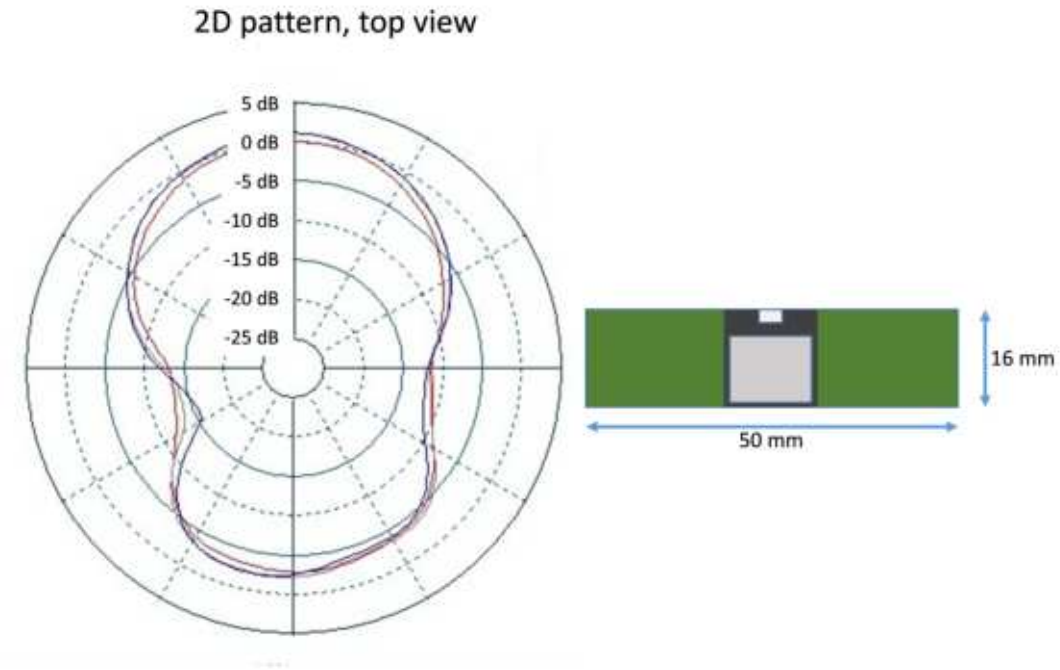



**Figure 6.6. Typical 2D Radiation Pattern – Top View**

# 7. Hardware Design Guidelines

The MGM12P is an easy-to-use module with regard to hardware application design but certain design guidelines must be followed to guarantee optimal performance. These guidelines are listed in the next sub-sections.

## 7.1 Power Supply Requirements

Coin cell batteries cannot withstand high peak currents (e.g. higher than 15 mA). If the peak current exceeds 15 mA it's recommended to place 47 - 100 µF capacitor in parallel with the coin cell battery to improve the battery life time. Notice that the total current consumption of your application is a combination of the radio, peripherals and MCU current consumption so you must take all of these into account. MGM12P should be powered by a unipolar supply voltage with nominal value of 3.3 V.

## 7.2 Reset Functions

The MGM12P can be reset by three different methods: by pulling the RESET line low, by the internal watchdog timer or software command. The reset state in MGM12P does not provide any power saving functionality and thus is not recommended as a means to conserve power. MGM12P has an internal system power-up reset function. The RESET pin includes an on-chip pull-up resistor and can therefore be left unconnected if no external reset switch or source is needed.

## 7.3 Debug and Firmware Updates

This section contains information on debug and firmware update methods. For additional information, refer to the following application note: AN958: Debugging and Programming Interfaces for Custom Designs.

### 7.3.1 Programming and Debug Connections

It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes. The following table lists the required pins for JTAG connection and SWD connections.

The debug pins have pull-down and pull-up enabled by default, so leaving them enabled may increase current consumption if left connected to supply or ground. If enabling the JTAG pins the module must be power cycled to enable a SWD debug session.

**Table 7.1. JTAG Pads**

| PAD NAME | PAD NUMBER | JTAG SIGNAL NAME | SWD SIGNAL NAME | COMMENTS |
|---|---|---|---|---|
| PF3 | 24 | TDI | N/A | This pin is disabled after reset. Once enabled the pin has a built-in pull-up. |
| PF2 | 23 | TDO | N/A | This pin is disabled after reset |
| PF1 | 22 | TMS | SWDIO | Pin is enabled after reset and has a built-in pull-up |
| PF0 | 21 | TCK | SWCLK | Pin is enabled after reset and has a built-in pull-down |

### 7.3.2 Packet Trace Interface (PTI)

The MGM12P integrates a true PHY-level PTI with the MAC, allowing complete, non-intrusive capture of all packets to and from the EFR32 Wireless STK development tools.

# 8. Pin Definitions

## 8.1 Pin Definitions

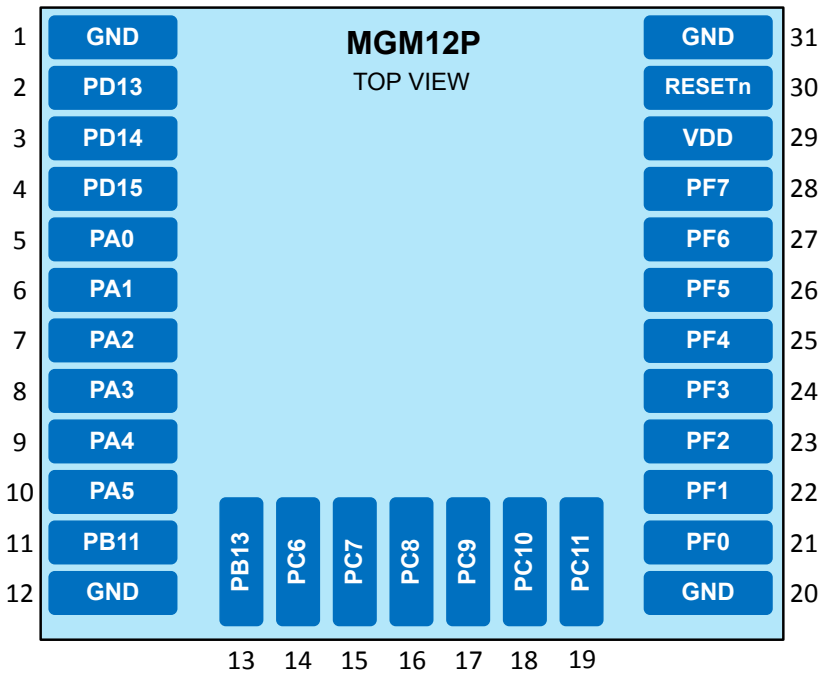



**Figure 8.1. MGM12P Pinout**

**Table 8.1. MGM12P Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| GND | 1<br>12<br>20<br>31 | Ground | PD13 | 2 | GPIO |
| PD14 | 3 | GPIO | PD15 | 4 | GPIO |
| PA0 | 5 | GPIO | PA1 | 6 | GPIO |
| PA2 | 7 | GPIO | PA3 | 8 | GPIO |
| PA4 | 9 | GPIO | PA5 | 10 | GPIO (5V) |
| PB11 | 11 | GPIO | PB13 | 13 | GPIO |
| PC6 | 14 | GPIO (5V) | PC7 | 15 | GPIO (5V) |
| PC8 | 16 | GPIO (5V) | PC9 | 17 | GPIO (5V) |
| PC10 | 18 | GPIO (5V) | PC11 | 19 | GPIO (5V) |
| PF0 | 21 | GPIO (5V) | PF1 | 22 | GPIO (5V) |
| PF2 | 23 | GPIO (5V) | PF3 | 24 | GPIO (5V) |
| PF4 | 25 | GPIO (5V) | PF5 | 26 | GPIO (5V) |
| PF6 | 27 | GPIO (5V) | PF7 | 28 | GPIO (5V) |
| VDD | 29 | Module Power Supply | RESETn | 30 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

### 8.1.1 GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port are indicated by a number from 15 down to 0.

**Table 8.2. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Port A** | - | - | - | - | - | - | - | - | - | - | PA5 (5V) | PA4 | PA3 | PA2 | PA1 | PA0 |
| **Port B** | | | PB13 | | PB11 | - | - | - | - | - | - | - | - | - | - | - |
| **Port C** | - | - | - | - | PC11 (5V) | PC10 (5V) | PC9 (5V) | PC8 (5V) | PC7 (5V) | PC6 (5V) | - | - | - | - | - | - |
| **Port D** | PD15 | PD14 | PD13 | | | | - | - | - | - | - | - | - | - | - | - |
| **Port E** | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| **Port F** | - | - | - | - | - | - | - | - | PF7 (5V) | PF6 (5V) | PF5 (5V) | PF4 (5V) | PF3 (5V) | PF2 (5V) | PF1 (5V) | PF0 (5V) |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

### 8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 8.3. Alternate Functionality Overview**

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| ACMP0_O | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Analog comparator ACMP0, digital output. |
| ACMP1_O | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Analog comparator ACMP1, digital output. |
| ADC0_EXTN | 0: PA0 | | | | | | | | Analog to digital converter ADC0 external reference input negative pin. |
| ADC0_EXTP | 0: PA1 | | | | | | | | Analog to digital converter ADC0 external reference input positive pin. |
| CMU_CLK0 | 0: PA1<br><br>2: PC6<br>3: PC11 | <br>5: PD14<br>6: PF2<br>7: PF7 | | | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | 0: PA0<br><br>2: PC7<br>3: PC10 | <br>5: PD15<br>6: PF3<br>7: PF6 | | | | | | | Clock Management Unit, clock output number 1. |
| CMU_CLKI0 | 0: PB13<br>1: PF7<br>2: PC6 | 4: PA5 | | | | | | | Clock Management Unit, clock output number I0. |
| DBG_SWCLKTCK | 0: PF0 | | | | | | | | Debug-interface Serial Wire clock input and JTAG Test Clock.<br><br>Note that this function is enabled to the pin out of reset, and has a built-in pull down. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| DBG_SWDIOTMS | 0: PF1 | | | | | | | | Debug-interface Serial Wire data input / output and JTAG Test Mode Select.<br><br>Note that this function is enabled to the pin out of reset, and has a built-in pull up. |
| DBG_SWO | 0: PF2<br>1: PB13<br>2: PD15<br>3: PC11 | | | | | | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| DBG_TDI | 0: PF3 | | | | | | | | Debug-interface JTAG Test Data In.<br><br>Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active. |
| DBG_TDO | 0: PF2 | | | | | | | | Debug-interface JTAG Test Data Out.<br><br>Note that this function becomes available after the first valid JTAG command is received. |
| ETM_TCLK | 1: PA5<br><br>3: PC6 | | | | | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | 3: PC7 | | | | | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | 3: PC8 | | | | | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | 3: PC9 | | | | | | | | Embedded Trace Module ETM data 2. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| ETM_TD3 | 3: PC10 | | | | | | | | Embedded Trace Module ETM data 3. |
| FRC_DCLK | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Frame Controller, Data Sniffer Clock. |
| FRC_DFRAME | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>6: PB13 | 9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11 | 19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | Frame Controller, Data Sniffer Frame active |
| FRC_DOUT | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>7: PB13 | 10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Frame Controller, Data Sniffer Output. |
| GPIO_EM4WU0 | 0: PF2 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | 0: PF7 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | 0: PD14 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU8 | 0: PA3 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU9 | 0: PB13 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU12 | 0: PC10 | | | | | | | | Pin can be used to wake the system up from EM4 |
| I2C0_SCL | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>7: PB13 | 10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | I2C0 Serial Data input / output. |
| I2C1_SCL | | | | | 18: PC10<br>19: PC11 | | | | I2C1 Serial Clock Line input / output. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| I2C1_SDA | | | | | 19: PC10 | 20: PC11 | | | I2C1 Serial Data input / output. |
| LES_CH5 | 0: PD13 | | | | | | | | LESENSE channel 5. |
| LES_CH6 | 0: PD14 | | | | | | | | LESENSE channel 6. |
| LES_CH7 | 0: PD15 | | | | | | | | LESENSE channel 7. |
| LES_CH8 | 0: PA0 | | | | | | | | LESENSE channel 8. |
| LES_CH9 | 0: PA1 | | | | | | | | LESENSE channel 9. |
| LES_CH10 | 0: PA2 | | | | | | | | LESENSE channel 10. |
| LES_CH11 | 0: PA3 | | | | | | | | LESENSE channel 11. |
| LES_CH12 | 0: PA4 | | | | | | | | LESENSE channel 12. |
| LES_CH13 | 0: PA5 | | | | | | | | LESENSE channel 13. |
| LETIM0_OUT0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | LEUART0 Receive input. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| LEU0_TX | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| MODEM_ANT0 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | <br>5: PB13 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | <br><br>18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | MODEM antenna control output 0, used for antenna diversity. |
| MODEM_ANT1 | 0: PA4<br>1: PA5<br>2: PB11 | 4: PB13<br><br><br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11 | <br><br>17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | MODEM antenna control output 1, used for antenna diversity. |
| MODEM_DCLK | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | MODEM data clock out. |
| MODEM_DIN | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | MODEM data in. |
| MODEM_DOUT | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br><br>6: PB13 | <br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11 | <br><br><br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | MODEM data out. |
| OPA0_N | 0: PA4 | | | | | | | | Operational Amplifier 0 external negative input. |
| OPA0_P | 0: PA2 | | | | | | | | Operational Amplifier 0 external positive input. |
| OPA1_N | 0: PD15 | | | | | | | | Operational Amplifier 1 external negative input. |
| OPA1_P | 0: PD13 | | | | | | | | Operational Amplifier 1 external positive input. |
| OPA2_N | 0: PB13 | | | | | | | | Operational Amplifier 2 external negative input. |
| OPA2_P | 0: PB11 | | | | | | | | Operational Amplifier 2 external positive input. |
| PCNT0_S0IN | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Pulse Counter PCNT0 input number 0. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PCNT0_S1IN | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | | | | | <br><br>19: PF6 | 20: PF7 | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | | | | | <br><br>18: PF6<br>19: PF7 | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | | | | | <br><br>19: PC10 | 20: PC11 | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | | | | | <br><br>18: PC10<br>19: PC11 | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | 0: PF0<br>1: PF1<br>2: PF2<br>3: PF3 | 4: PF4<br>5: PF5<br>6: PF6<br>7: PF7 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | 0: PF1<br>1: PF2<br>2: PF3<br>3: PF4 | 4: PF5<br>5: PF6<br>6: PF7<br>7: PF0 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | 0: PF2<br>1: PF3<br>2: PF4<br>3: PF5 | 4: PF6<br>5: PF7<br>6: PF0<br>7: PF1 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | 0: PF3<br>1: PF4<br>2: PF5<br>3: PF6 | 4: PF7<br>5: PF0<br>6: PF1<br>7: PF2 | | 12: PD13<br>13: PD14<br>14: PD15 | | | | | Peripheral Reflex System PRS, channel 3. |
| PRS_CH4 | | 4: PD13<br>5: PD14<br>6: PD15 | | | | | | | Peripheral Reflex System PRS, channel 4. |
| PRS_CH5 | <br><br>3: PD13 | 4: PD14<br>5: PD15 | | | | | | | Peripheral Reflex System PRS, channel 5. |
| PRS_CH6 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13 | <br><br>15: PD13 | 16: PD14<br>17: PD15 | | | | Peripheral Reflex System PRS, channel 6. |
| PRS_CH7 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PA0 | | | | | | Peripheral Reflex System PRS, channel 7. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PRS_CH8 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br><br>6: PB13 | <br>9: PA0<br>10: PA1 | | | | | | Peripheral Reflex System PRS, channel 8. |
| PRS_CH9 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | <br>5: PB13 | 8: PA0<br>9: PA1<br>10: PA2<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | | | | Peripheral Reflex System PRS, channel 9. |
| PRS_CH10 | 0: PC6<br>1: PC7<br>2: PC8<br>3: PC9 | 4: PC10<br>5: PC11 | | | | | | | Peripheral Reflex System PRS, channel 10. |
| PRS_CH11 | 0: PC7<br>1: PC8<br>2: PC9<br>3: PC10 | 4: PC11<br>5: PC6 | | | | | | | Peripheral Reflex System PRS, channel 11. |
| TIM0_CC0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br><br>6: PB13 | <br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11 | <br><br><br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | <br>5: PB13 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | <br><br>18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1 | 0: PA4<br>1: PA5<br>2: PB11 | 4: PB13<br><br><br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11 | <br><br>17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | 0: PA5<br>1: PB11<br><br>3: PB13 | <br><br>6: PC6<br>7: PC7 | 8: PC8<br>9: PC9<br>10: PC10<br>11: PC11 | | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3<br>23: PF4 | 24: PF5<br>25: PF6<br>26: PF7<br>27: PA0 | 28: PA1<br>29: PA2<br>30: PA3<br>31: PA4 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br><br>6: PB13 | <br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11 | <br><br><br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | Timer 1 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| TIM1_CC3 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 5: PB13 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | 18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | Timer 1 Capture Compare input / output channel 3. |
| US0_CLK | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>6: PB13 | 9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11 | 19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | USART0 clock input / output. |
| US0_CS | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 5: PB13 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | 18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | USART0 chip select input / output. |
| US0_CTS | 0: PA4<br>1: PA5<br>2: PB11 | 4: PB13<br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11 | 17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | USART0 Clear To Send hardware flow control input. |
| US0_RTS | 0: PA5<br>1: PB11<br>3: PB13 | 6: PC6<br>7: PC7 | 8: PC8<br>9: PC9<br>10: PC10<br>11: PC11 | | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3<br>23: PF4 | 24: PF5<br>25: PF6<br>26: PF7<br>27: PA0 | 28: PA1<br>29: PA2<br>30: PA3<br>31: PA4 | USART0 Request To Send hardware flow control output. |
| US0_RX | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>7: PB13 | 10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>6: PB13 | 9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11 | 19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | USART1 clock input / output. |
| US1_CS | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 5: PB13 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | 18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | USART1 chip select input / output. |
| US1_CTS | 0: PA4<br>1: PA5<br>2: PB11 | 4: PB13<br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11 | 17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | USART1 Clear To Send hardware flow control input. |
| US1_RTS | 0: PA5<br>1: PB11<br>3: PB13 | 6: PC6<br>7: PC7 | 8: PC8<br>9: PC9<br>10: PC10<br>11: PC11 | | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3<br>23: PF4 | 24: PF5<br>25: PF6<br>26: PF7<br>27: PA0 | 28: PA1<br>29: PA2<br>30: PA3<br>31: PA4 | USART1 Request To Send hardware flow control output. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US1_RX | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br><br>7: PB13 | <br><br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | USART1 Asynchronous Receive.<br><br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11 | 8: PB13<br><br><br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | <br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.<br><br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | | | | 12: PF0<br>13: PF1<br>14: PF3<br>15: PF4 | 16: PF5<br>17: PF6<br>18: PF7 | | | 30: PA5 | USART2 clock input / output. |
| US2_CS | | | <br><br>11: PF0 | 12: PF1<br>13: PF3<br>14: PF4<br>15: PF5 | 16: PF6<br>17: PF7 | | | 29: PA5 | USART2 chip select input / output. |
| US2_CTS | | | <br><br>10: PF0<br>11: PF1 | 12: PF3<br>13: PF4<br>14: PF5<br>15: PF6 | 16: PF7 | | | 28: PA5 | USART2 Clear To Send hardware flow control input. |
| US2_RTS | | | <br>9: PF0<br>10: PF1<br>11: PF3 | 12: PF4<br>13: PF5<br>14: PF6<br>15: PF7 | | | <br><br>27: PA5 | | USART2 Request To Send hardware flow control output. |
| US2_RX | | | | <br>13: PF0<br>14: PF1<br>15: PF3 | 16: PF4<br>17: PF5<br>18: PF6<br>19: PF7 | | | <br><br>31: PA5 | USART2 Asynchronous Receive.<br><br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | 0: PA5 | | | <br><br>14: PF0<br>15: PF1 | 16: PF3<br>17: PF4<br>18: PF5<br>19: PF6 | 20: PF7 | | | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication.<br><br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| US3_CLK | <br><br>3: PD13 | 4: PD14<br>5: PD15 | | 13: PB11 | | | | | USART3 clock input / output. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US3_CS | 2: PD13<br>3: PD14 | 4: PD15 | | 12: PB11 | | | | | USART3 chip select input / output. |
| US3_CTS | 1: PD13<br>2: PD14<br>3: PD15 | | 11: PB11 | | | | | | USART3 Clear To Send hardware flow control input. |
| US3_RTS | 0: PD13<br>1: PD14<br>2: PD15 | | 10: PB11 | | | | | | USART3 Request To Send hardware flow control output. |
| US3_RX | | 4: PD13<br>5: PD14<br>6: PD15 | | 14: PB11 | | | | | USART3 Asynchronous Receive.<br>USART3 Synchronous mode Master Input / Slave Output (MISO). |
| US3_TX | | 5: PD13<br>6: PD14<br>7: PD15 | | 15: PB11 | | | | | USART3 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART3 Synchronous mode Master Output / Slave Input (MOSI). |
| VDAC0_EXT | 0: PA1 | | | | | | | | Digital to analog converter VDAC0 external reference input pin. |
| VDAC0_OUT0 / OPA0_OUT | 0: PA3 | | | | | | | | Digital to Analog Converter DAC0 output channel number 0. |
| VDAC0_OUT0ALT / OPA0_OUTALT | 0: PA5<br>1: PD13<br>2: PD15 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 0. |
| VDAC0_OUT1 / OPA1_OUT | 0: PD14 | | | | | | | | Digital to Analog Converter DAC0 output channel number 1. |
| VDAC0_OUT1ALT / OPA1_OUTALT | 1: PA2<br>2: PA4 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 1. |
| WTIM0_CC0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5 | | 15: PB11 | 17: PB13 | | 26: PC6<br>27: PC7 | 28: PC8<br>29: PC9<br>30: PC10<br>31: PC11 | Wide timer 0 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| WTIM0_CC1 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | | | 13: PB11<br><br>15: PB13 | | | 24: PC6<br>25: PC7<br>26: PC8<br>27: PC9 | 28: PC10<br>29: PC11 | Wide timer 0 Capture Compare input / output channel 1. |
| WTIM0_CC2 | 0: PA4<br>1: PA5 | | 11: PB11 | 13: PB13 | | 22: PC6<br>23: PC7 | 24: PC8<br>25: PC9<br>26: PC10<br>27: PC11 | | Wide timer 0 Capture Compare input / output channel 2. |
| WTIM0_CDTI0 | | 7: PB11 | 9: PB13 | | 18: PC6<br>19: PC7 | 20: PC8<br>21: PC9<br>22: PC10<br>23: PC11 | | 29: PD13<br>30: PD14<br>31: PD15 | Wide timer 0 Complimentary Dead Time Insertion channel 0. |
| WTIM0_CDTI1 | | 5: PB11<br><br>7: PB13 | | | 16: PC6<br>17: PC7<br>18: PC8<br>19: PC9 | 20: PC10<br>21: PC11 | 27: PD13 | 28: PD14<br>29: PD15<br>30: PF0<br>31: PF1 | Wide timer 0 Complimentary Dead Time Insertion channel 1. |
| WTIM0_CDTI2 | 3: PB11 | 5: PB13 | | 14: PC6<br>15: PC7 | 16: PC8<br>17: PC9<br>18: PC10<br>19: PC11 | | 25: PD13<br>26: PD14<br>27: PD15 | 28: PF0<br>29: PF1<br>30: PF2<br>31: PF3 | Wide timer 0 Complimentary Dead Time Insertion channel 2. |
| WTIM1_CC0 | 1: PB13 | | 10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Wide timer 1 Capture Compare input / output channel 0. |
| WTIM1_CC1 | | | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | 19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7 | Wide timer 1 Capture Compare input / output channel 1. |
| WTIM1_CC2 | | 6: PC6<br>7: PC7 | 8: PC8<br>9: PC9<br>10: PC10<br>11: PC11 | | 17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | | Wide timer 1 Capture Compare input / output channel 2. |
| WTIM1_CC3 | | 4: PC6<br>5: PC7<br>6: PC8<br>7: PC9 | 8: PC10<br>9: PC11 | 15: PD13 | 16: PD14<br>17: PD15<br>18: PF0<br>19: PF1 | 20: PF2<br>21: PF3<br>22: PF4<br>23: PF5 | 24: PF6<br>25: PF7 | | Wide timer 1 Capture Compare input / output channel 3. |

### 8.3 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 8.2 APORT Connection Diagram on page 77 Shows the APORT routing for this device family. A complete description of APORT functionality can be found in the Reference Manual. The APORT information in this section is reflective of the IC used in the modules. Not all ports are available on the modules. The module pins available correspond with the pin names in this section.

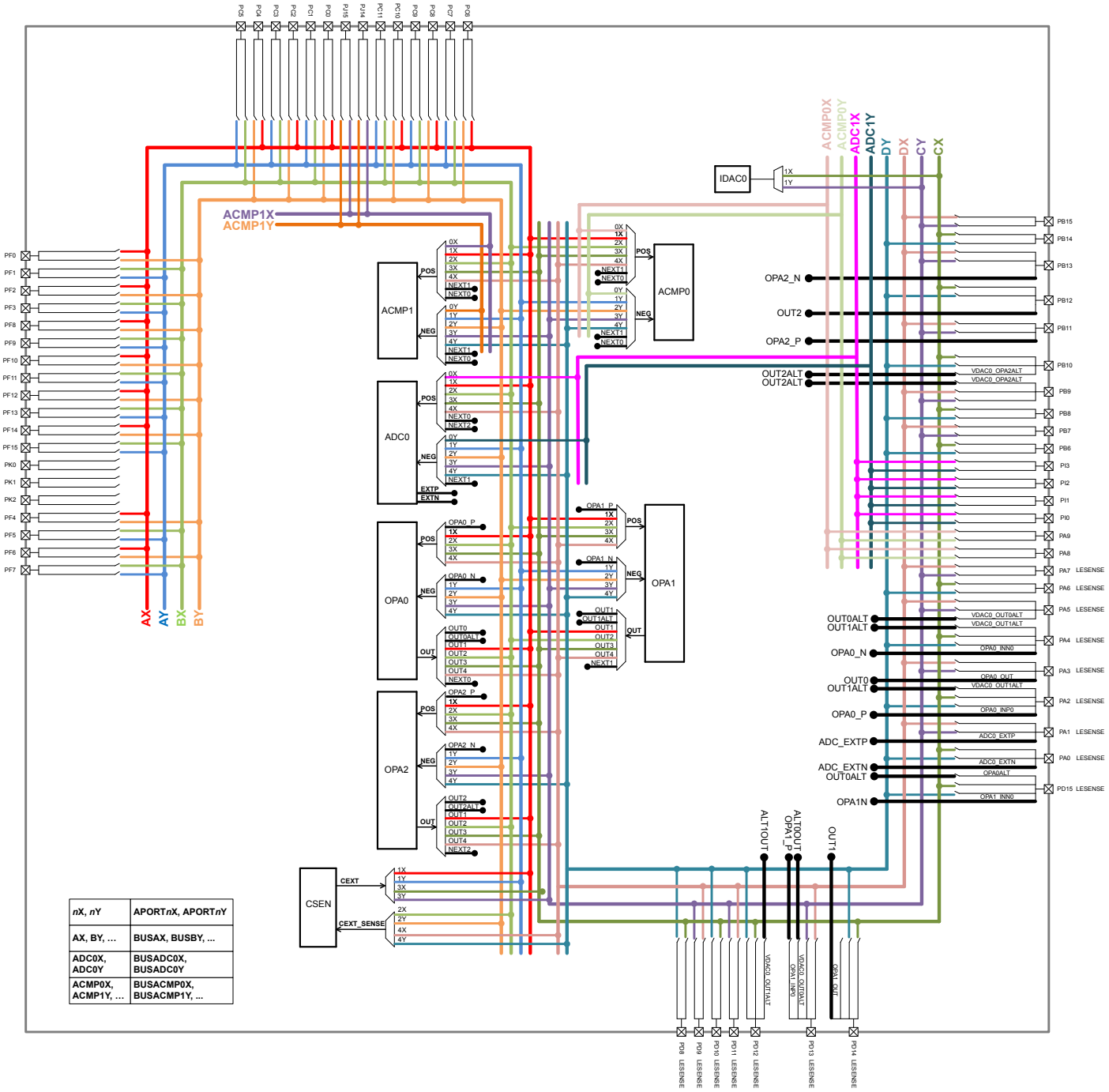



**Figure 8.2. APORT Connection Diagram**

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

**Table 8.4. ACMP0 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT0X | BUSACMP0X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PA9 | PA8 |
| APORT0Y | BUSACMP0Y | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PA9 | PA8 |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |

**Table 8.5. ACMP1 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT0X | BUSACMP1X | | | | | | | | | | | | | | | | | | | | | | | | | PJ15 | PJ14 | | | | | | |
| APORT0Y | BUSACMP1Y | | | | | | | | | | | | | | | | | | | | | | | | | PJ15 | PJ14 | | | | | | |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |

**Table 8.6. ADC0 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT0X | BUSADC0X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PI3 | PI2 | PI1 | PI0 |
| APORT0Y | BUSADC0Y | | | | | | | | | | | | | | | | | | | | | | | | | | | | | PI3 | PI2 | PI1 | PI0 |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |

**Table 8.7. CSEN Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CEXT** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| **CEXT_SENSE** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |

**Table 8.8. IDAC0 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT1X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| APORT1Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |

**Table 8.9. VDAC0 / OPA Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OPA0_N** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| **OPA0_P** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 | |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OPA1_N** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| **OPA1_P** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| **OPA2_N** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OPA2_OUT** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| **OPA2_P** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT2X | BUSBX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT3X | BUSCX | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| **VDAC0_OUT0 / OPA0_OUT** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **VDAC0_OUT1 / OPA1_OUT** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | PC5 | | PC3 | | PC1 | |
| APORT2Y | BUSBY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | PC4 | | PC2 | | PC0 |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | PB9 | | PB7 | | | | | | | | PA7 | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | PD9 | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | PB10 | | PB8 | | PB6 | | | | | | | | PA6 | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | PD8 |

# 9. Package Specifications

## 9.1 MGM12P Package Outline

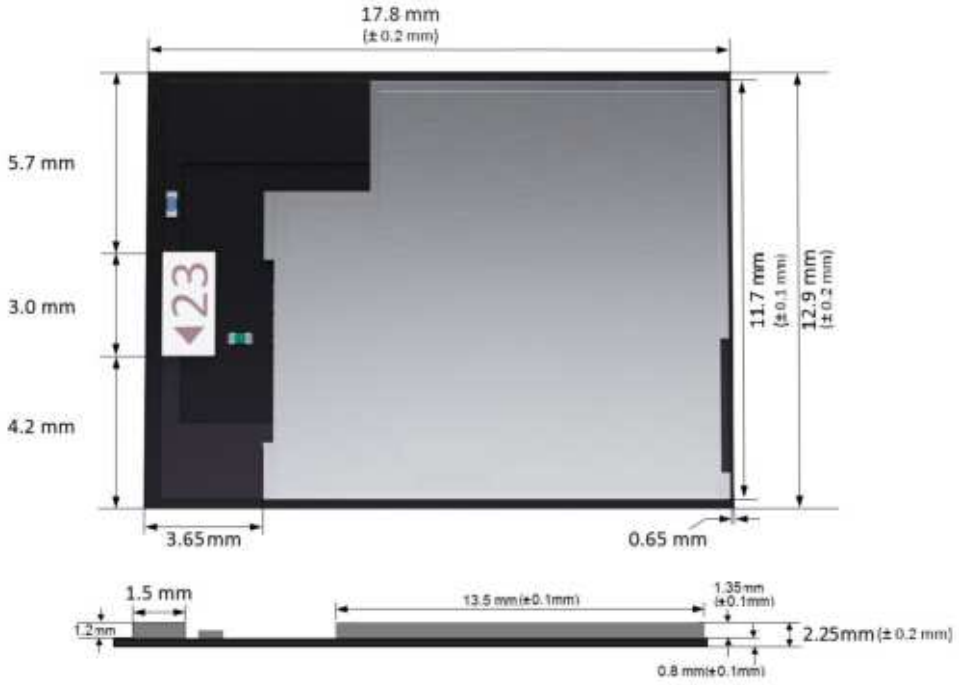



**Figure 9.1. Top View and Side View with Antenna Option**

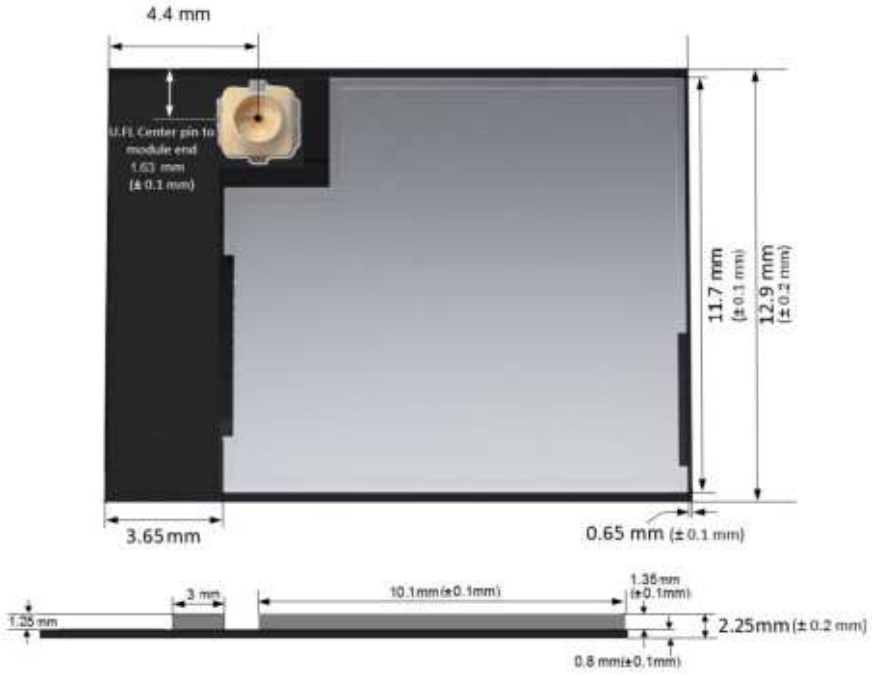



**Figure 9.2. Top View and Side View with U.FL Option**

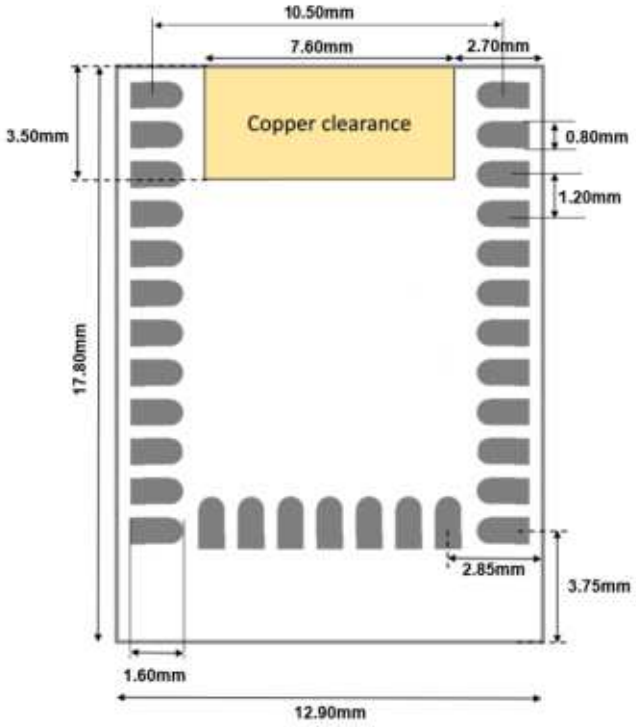



**Figure 9.3. Bottom View**

### 9.2 MGM12P Recommended PCB Land Pattern

The figure below shows the recommended land pattern. The antenna clearance section is not required for the MGM12P module version with the U.FL connector.

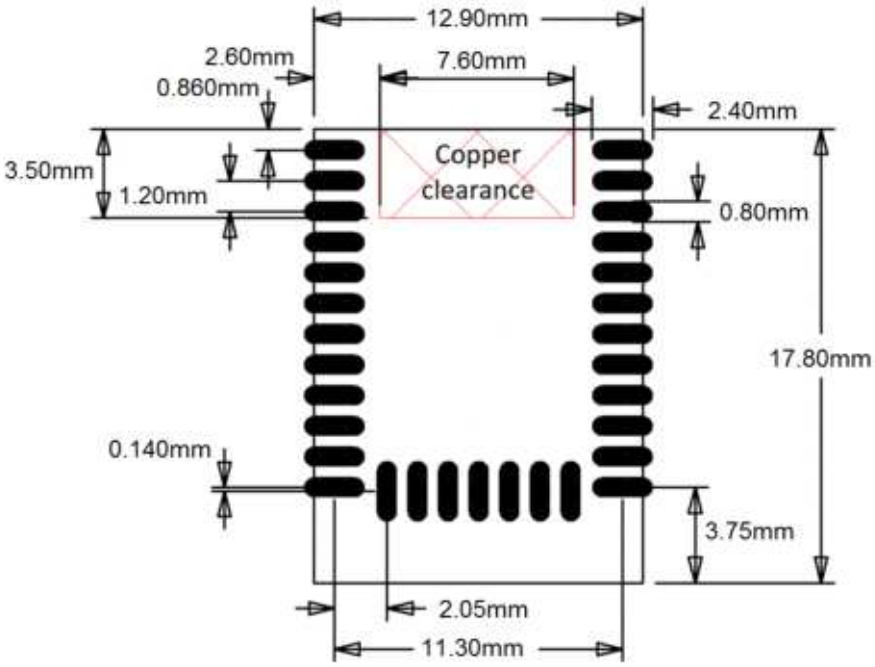



**Figure 9.4. MGM12P Recommended PCB Land Pattern**

### 9.3 MGM12P Package Marking

The figure below shows the Module markings printed on the RF-shield.

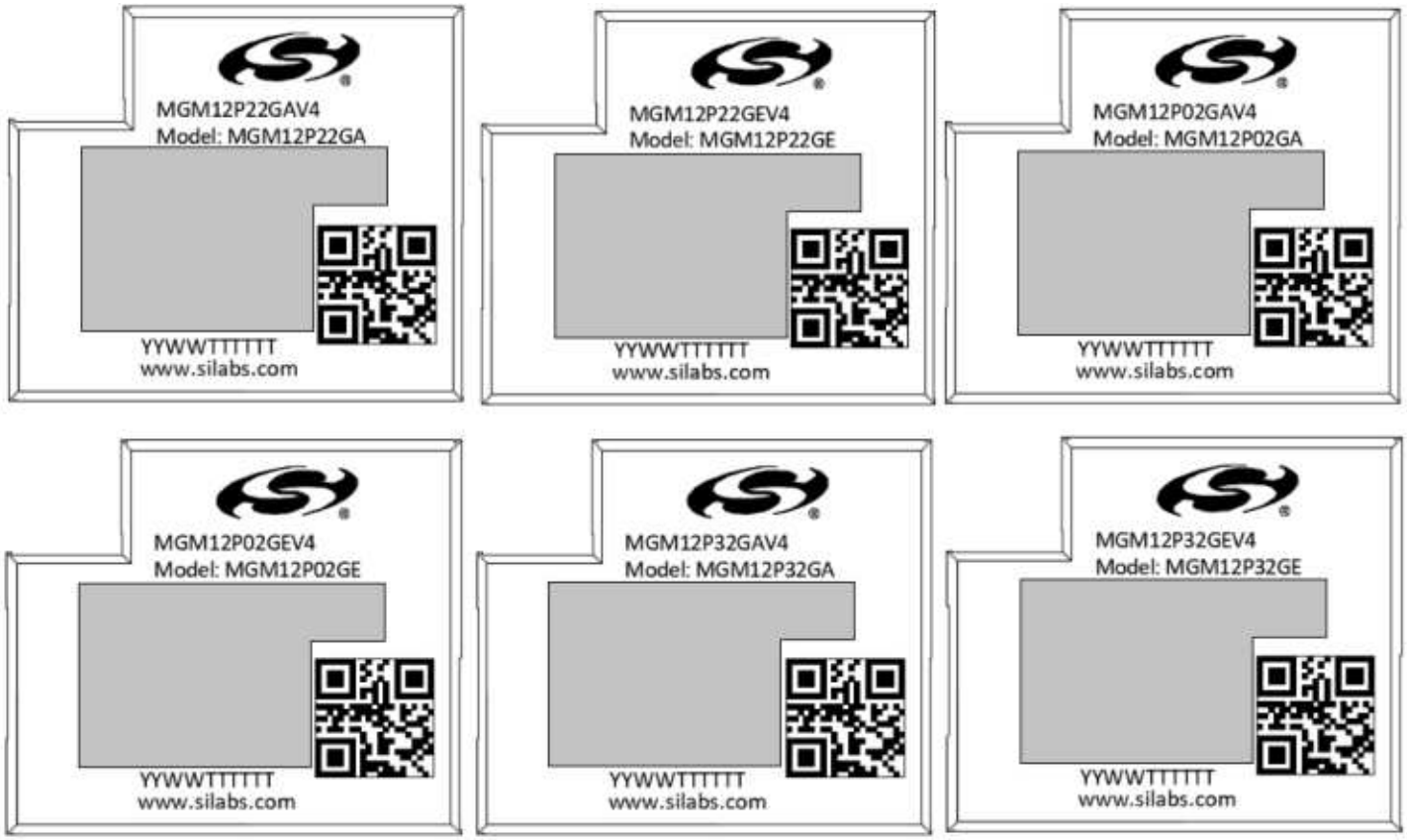



**Figure 9.5. MGM12P Package Marking**

**Mark Description**

The package marking consists of:

- MGM12Pxxxxxx - Part number designation
- Model: MGM12Pxxxx – Model number designation
- QR Code: YYWWMMABCDE
  - YY – The last 2 digits of the assembly year
  - WW – The 2 digit work week when the device was assembled
  - MMABCDE – Silicon Labs unit code
- Trace Code: YYWWTTTTTT
  - YY – The last 2 digits of the assembly year
  - WW – The 2 digit work week when the device was assembled
  - TTTTTT – A trace or manufacturing code. The first letter is the device revision
- Certification marks such as the CE logo, FCC and IC IDs, etc. will be engraved on the grayed out area or printed on the back side of the module, according to regulatory body requirements

# 10. Soldering Recommendations

It is recommended that final PCB assembly of this product follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

**CLASS 1 General Electronic Products**

Includes products suitable for applications where the major requirement is function of the completed assembly.

**CLASS 2 Dedicated Service Electronic Products**

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

**CLASS 3 High Performance/Harsh Environment Electronic Products**

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

# 11. Tape and Reel Specifications

## 11.1 Tape and Reel Specification

This section contains information regarding the tape and reel packaging for the MGM12P Wireless Gecko Module.

## 11.2 Reel Material and Dimensions

- Reel material: Polystyrene (PS)
- Reel diameter: 13 inches (330 mm)
- Number of modules per reel: 1000 pcs
- Disk deformation, folding whitening and mold imperfections: Not allowed
- Disk set: consists of two 13 inch (330 mm) rotary round disks and one central axis (100 mm)
- Antistatic treatment: Required
- Surface resistivity: 104 - 109 Ω/sq.

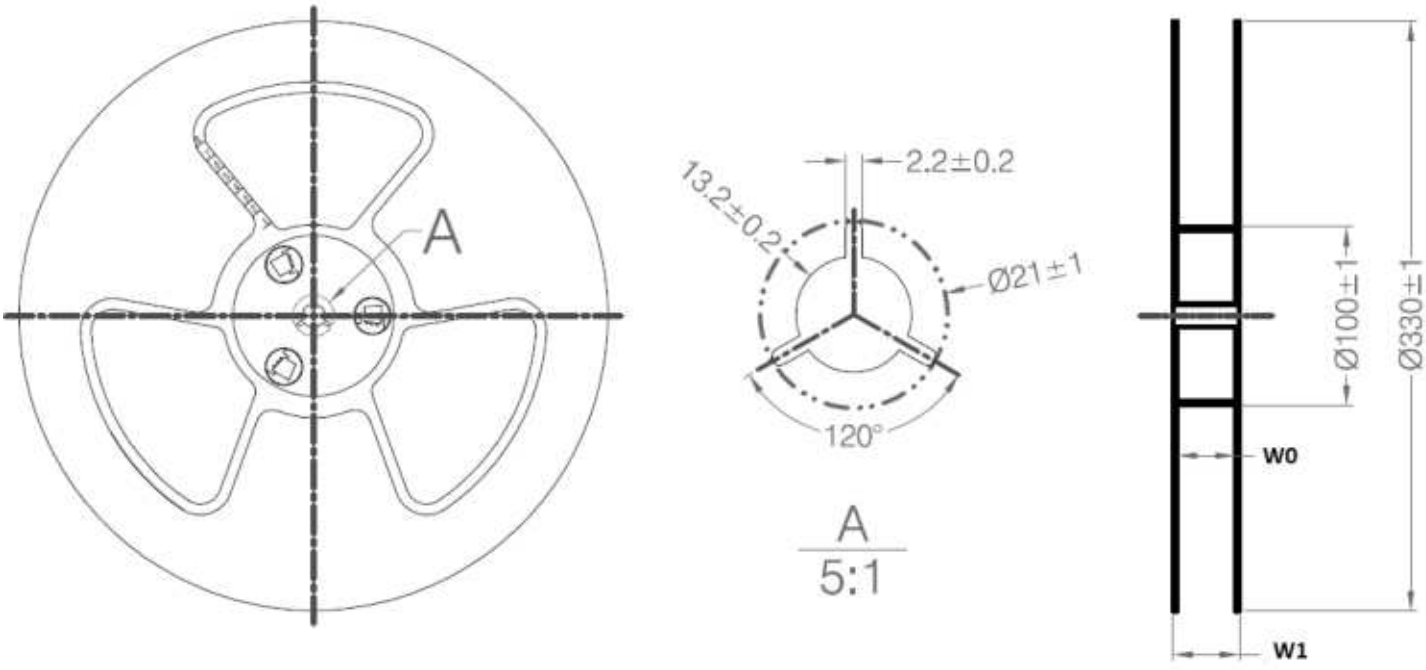



**Figure 11.1. Reel Dimension — Side View**

| Symbol | Dimensions [mm] |
|---|---|
| W0 | 44.0 +0.5/-.0.0 |
| W1 | 48.0 |

### 11.3 Module Orientation and Tap

The user direction of feed, start and end of tape on reel and orientation of the Modules on the tape are shown in the figures below.

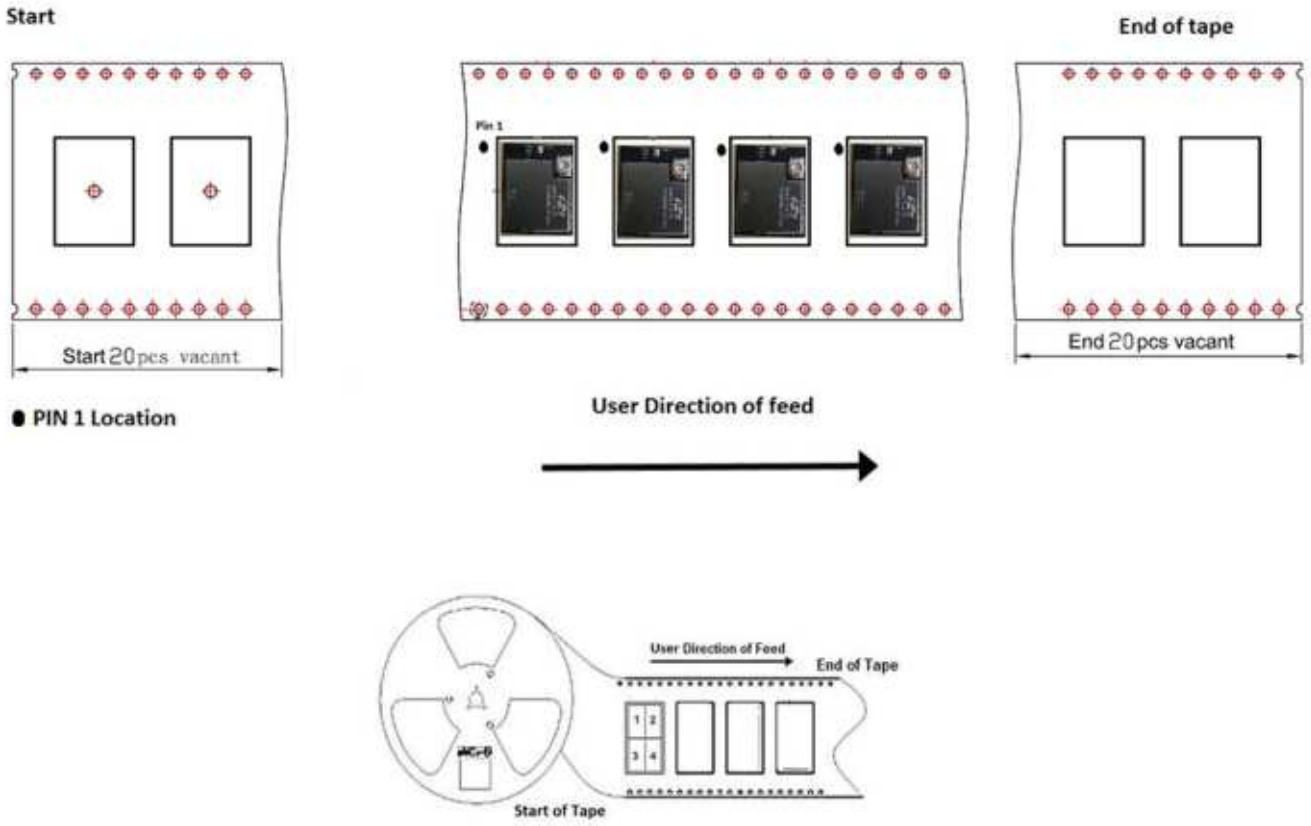



**Figure 11.2. Module Orientation and Feed Direction**

### 11.4 Carrier Tape and Cover Tape Information

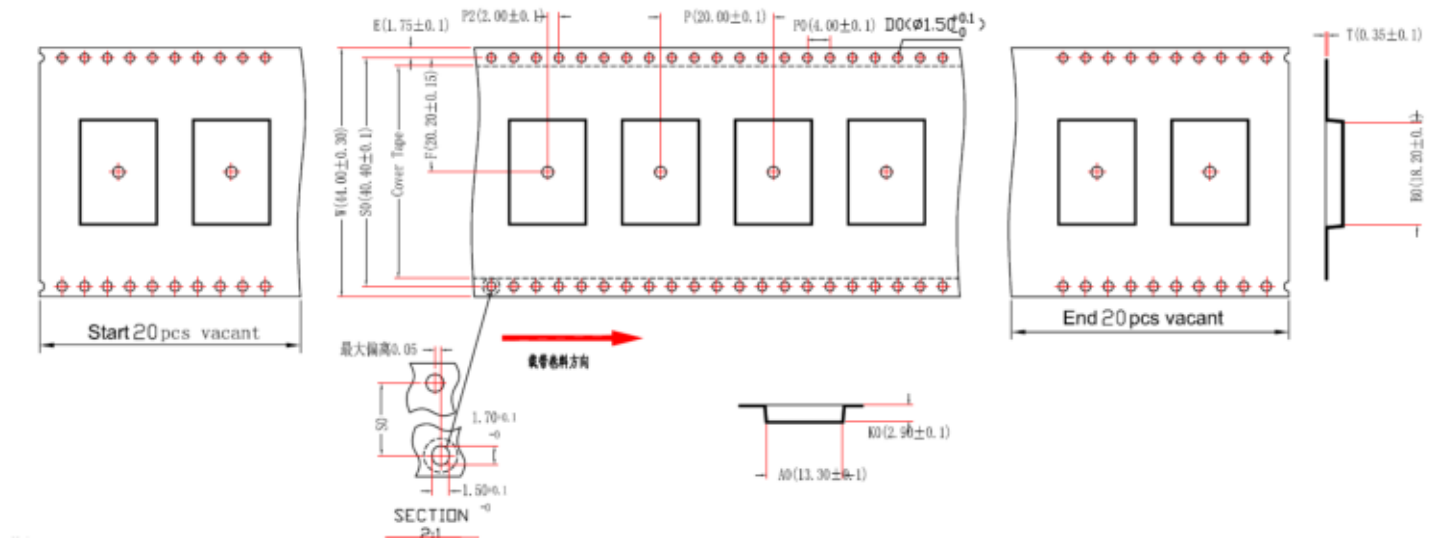



**Figure 11.3. Carrier Tape Information**

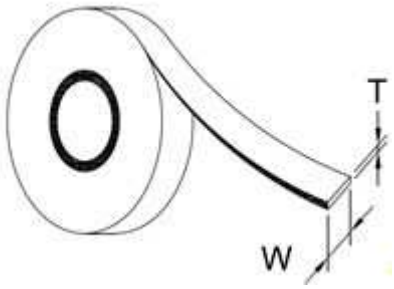



**Figure 11.4. Cover Tape Information**

| Symbol | Dimensions [mm] |
|---|---|
| Thickness (T) | 0.055 +0.005/-0.003 |
| Width (W) | 37.50 +0.30/-0.10 |

# 12. Certifications

## 12.1 CE and UKCA - EU and UK

The MGM12P(MGM12P02 and MGM12P22) modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating a MGM12P(MGM12P02 and MGM12P22) module will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their end-products as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

The modules are entitled to carry the CE and UKCA Marks, and a formal Declaration of Conformity (DoC) is available at the product web page which is reachable starting from https://www.silabs.com/.

## 12.2 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user’s authority to operate the equipment.

**FCC RF Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

**OEM Responsibilities to comply with FCC Regulations**

OEM integrator is responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

- With MGM12P22GA, MGM12P22GE, MGM12P02GA and MGM12P02GE the antenna(s) must be installed such that a minimum separation distance of 6.7mm is maintained between the radiator (antenna) and all persons at all times.
- With MGM12P32GA and MGM12P32GE the antenna(s) must be installed such that a minimum separation distance of 39mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

**IMPORTANT NOTE:** In the event that the above conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

**End Product Labeling**

The variants of MGM12P Modules are labeled with their own FCC IDs. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final product must be labeled in a visible area with the following

**MODELS MGM12P02GE and MGM12P02GA:**

"**Contains Transmitter Module FCC ID: QOQMGM12P0**"

or

"**Contains FCC ID: QOQMGM12P0**

**MODELS MGM12P22GE and MGM12P22GA:**

"**Contains Transmitter Module FCC ID: QOQMGM12P2**"

or

"**Contains FCC ID: QOQMGM12P2**

**MODELS MGM12P32GE and MGM12P32GA:**

"**Contains Transmitter Module FCC ID: QOQMGM12P3**"

or

"**Contains FCC ID: QOQMGM12P3**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

### 12.3 ISEDC

This radio transmitter (IC: 5123A-MGM12P) has been approved by Industry Canada to operate with the embedded chip antenna and a standard 2.14 dBi dipole antenna. Other antenna types are strictly prohibited for use with this device.

This device complies with Industry Canada's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

**RF Exposure Statemment**

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

MGM12P22GA, MGM12P22GE, MGM12P02GA and MGM12P02GE modules meets the given requirements when the minimum separation distance to human body is 20 mm.

MGM12P32GA and MGM12P32GA modules meets the given requirements when the minimum separation distance to human body is 35 mm.

RF exposure or SAR evaluation is not required when the separation distance is same or more than stated above. If the separation distance is less than stated above the OEM integrator is responsible for evaluating the SAR.

**OEM Responsibilities to comply with IC Regulations**

The MGM12P module has been certified for integration into products only by OEM integrators under the following conditions:

- The antenna(s) must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**IMPORTANT NOTE**: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the ISEDC authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate ISEDC authorization.

**End Product Labeling**

The MGM12P modules are labeled with their own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**MODELS MGM12P02GE and MGM12P02GA:**

"**Contains Transmitter Module IC: 5123A-MGM12P0**"

or

"**Contains IC: 5123A-MGM12P0**

**MODELS MGM12P22GE and MGM12P22GA:**

"**Contains Transmitter Module IC: 5123A-MGM12P2**"

or

"**Contains IC: 5123A-MGM12P2**

**MODELS MGM12P32GE and MGM12P32GA:**

"**Contains Transmitter Module IC: 5123A-MGM12P3**"

or

"**Contains IC: 5123A-MGM12P3"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product

**ISEDC (Français)**

Industrie Canada a approuvé l'utilisation de cet émetteur radio (IC: 5123A-MGM12P) en conjonction avec des antennes de type dipolaire à 2.14dBi ou des antennes embarquées, intégrée au produit.

L'utilisation de tout autre type d'antenne avec ce composant est proscrite.

Ce composant est conforme aux normes RSS, exonérées de licence d'Industrie Canada. Son mode de fonctionnement est soumis aux deux conditions suivantes :

1. Ce composant ne doit pas générer d'interférences
2. Ce composant doit pouvoir est soumis à tout type de perturbation y compris celle pouvant nuire à son bon fonctionnement.

**Déclaration d'exposition RF**

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 5.

Les modules MGM12P22GA, MGM12P22GE, MGM12P02GA et MGM12P02GE répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 20 mm.

Les modules MGM12P32GA et MGM12P32GA répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 35 mm.

La déclaration d'exposition RF ou l'évaluation SAR n'est pas nécessaire lorsque la distance de séparation est identique ou supérieure à celle indiquée ci-dessus.

Si la distance de séparation est inférieure à celle mentionnées plus haut, il incombe à l'intégrateur OEM de procédé à une évaluation SAR.

**Responsabilités des OEM pour une mise en conformité avec le Règlement du Circuit Intégré**

Le module MGM12P a été approuvé pour l'intégration dans des produits finaux exclusivement réalisés par des OEM sous les conditions suivantes:

- L'antenne (s) doit être installée de sorte qu'une distance de séparation minimale indiquée ci-dessus soit maintenue entre le radiateur (antenne) et toutes les personnes avoisinante, ce à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner avec une autre antenne ou un autre transmetteur que celle indiquée plus haut.

Tant que les deux conditions ci-dessus sont respectées, il n'est pas nécessaire de tester ce transmetteur de façon plus poussée. Cependant, il incombe à l'intégrateur OEM de s'assurer de la bonne conformité du produit fini avec les autres normes auxquelles il pourrait être soumis de fait de l'utilisation de ce module (par exemple, les émissions des périphériques numériques, les exigences de périphériques PC, etc.).

**REMARQUE IMPORTANTE**: dans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou co-implantation avec un autre émetteur), l'autorisation ISEDC n'est plus considérée comme valide et le numéro d'identification ID IC ne peut pas être apposé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera responsable de la réévaluation du produit final (y compris le transmetteur) et de l'obtention d'une autorisation ISEDC distincte.

**Étiquetage des produits finis**

Les modules MGM12P sont étiquetés avec leur propre ID IC. Si l'ID IC n'est pas visible lorsque le module est intégré au sein d'un autre produit, cet autre produit dans lequel le module est installé devra porter une étiquette faisant apparaitre les référence du module intégré. Dans un tel cas, sur le produit final doit se trouver une étiquette aisément lisible sur laquelle figurent les informations suivantes :

**MODÈLES MGM12P02GE et MGM12P02GA:**

**"Contient le module transmetteur : 5123A-MGM12P0"**

ou

**"Contient le circuit: 5123A-MGM12P0**

**MODÈLES MGM12P22GE et MGM12P22GA:**

**"Contient le module transmetteur: 5123A-MGM12P2"**

ou

**"Contient IC: 5123A-MGM12P2**

**MODÈLES MGM12P32GE et MGM12P32GA:**

**"Contient le module émetteur IC: 5123A-MGM12P3"**

ou

**"Contient IC: 5123A-MGM12P3"**

L'intégrateur OEM doit être conscient qu'il ne doit pas fournir, dans le manuel d'utilisation, d'informations relatives à la façon d'installer ou de d'enlever ce module RF ainsi que sur la procédure à suivre pour modifier les paramètres liés à la radio.

# 13. Revision History

### Revision 1.5

October, 2022

- Added timing specifications for RESETn low time and clarified $V_{IL}$ and $V_{IH}$ logic levels for RESETn pins in Table 4.21 General-Purpose I/O (GPIO) on page 32.
- Removed BIASPROG = 1, FULLBIAS = 0 specifications from Table 4.24 Analog Comparator (ACMP) on page 37.
- Updated Hysteresis max values in Table 4.24 Analog Comparator (ACMP) on page 37.
- Added Figure 4.2 SPI Master Timing Diagram (SMSDELAY = 1) on page 54.
- Updated 9.3 MGM12P Package Marking.
- Updated 12.1 CE and UKCA - EU and UK.
- Removed all references to RFSENSE.
- Removed references to BOOT_TX and BOOT_RX.

### Revision 1.4

February, 2020

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated 3.6.4 Low Energy Timer (LETIMER) lowest energy mode.
- Added a Note about the operating voltage in 3.8.3 True Random Number Generator (TRNG).
- Corrected the Input RF level from +10dBm to -2dBm in Table 4.1. Absolute Maximum Ratings.
- Updated the module dimensions and tolerances in Figure 9.1 Top View and Side View with Antenna Option on page 86 and Figure 9.2 Top View and Side View with U.FL Option on page 86.
- Renamed the figures in 9.1 MGM12P Package Outline.
- Renamed section 9.1 from MGM12P Dimensions to 9.1 MGM12P Package Outline.
- Removed MGM12P Module Footprint section and added Figure 9.3 Bottom View on page 87 to 9.1 MGM12P Package Outline.

### Revision 1.3

May, 2019

- Updated Section 2. Ordering Information
- Updated Table 4.30 Analog Port (APORT) on page 49 Analog Port (APORT) Operation in EM2/EM3 (Typ: 67 nA)
- Updated Section 9.3 MGM12P Package Marking
- Updated 1 Mbps Bluetooth Sensitivity values in Table 4.11 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate on page 26
- Added Bluetooth sensitivity values with non-ideal signals to Table 4.11 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate on page 26 and Table 4.12 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate on page 27
- Added Chapter 10. Soldering Recommendations

### Revision 1.2

January, 2019

- Updated Section 2. Ordering Information.
- Updated Section 9.1 MGM12P Package Outline
- Updated Section 9.3 MGM12P Package Marking.
- Updated Section 12.1 CE and UKCA - EU and UK.

### Revision 1.1

April, 2018

- Updated Section 2. Ordering Information.
- Updated Section Table 3.1 Antenna Efficiency and Peak Gain (MGM12P) on page 7.
- Updated Section 4.1.8 2.4 GHz RF Transceiver Characteristics

**Revision 1.0**

- Minor Updates

**Revision 0.2**

- Initial Publication

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