# MIC2174/MIC2174C

## Synchronous Buck Controller Featuring Adaptive On-Time Control 40V Input, 300kHz

## Hyper Speed Control™ Family

## General Description

The Micrel MIC2174/MIC2174C is a fixed-frequency, synchronous buck controller featuring adaptive on-time control. The MIC2174/MIC2174C operates over an input supply range of 3V to 40V at a fixed switching frequency of 300kHz and is capable of driving 25A of output current. The output voltage is adjustable down to 0.8V.

A unique Hyper Speed Control™ architecture allows for ultra-fast transient response while reducing the output capacitance. It also makes ultra-fast transient response while reducing the output capacitance and also allows for extremely low duty-cycle operation. The MIC2174 / MIC2174C utilizes an adaptive $T_{ON}$ ripple controlled architecture. A UVLO is provided to ensure proper operation under power-sag conditions to prevent the external power MOSFET from overheating. A soft-start is provided to reduce inrush current. Foldback current limit and "hiccup" mode short-circuit protection ensure FET and load protection.

The MIC2174/MIC2174C is available in a 10-pin MSOP (MAX1954A-compatible) package with an operating junction temperature range from –40°C to +125°C.

All support documentation can be found on Micrel's web site at: www.micrel.com.

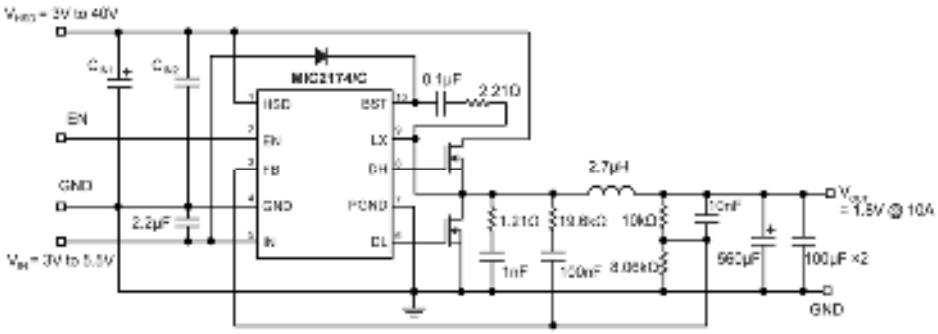
## Features

- Hyper Speed Control™ architecture enables:
  - High delta V operation ($V_{HSD}$ = 40V and $V_{OUT}$ = 0.8V)
  - Smaller output capacitors than competitors
- 3V to 40V input voltage
- Any Capacitor™ stable
  - Zero ESR to high ESR
- 300kHz switching frequency
- Adjustable output from 0.8V to 5.5V ($V_{HSD}$ ≤ 28V)
- Adjustable output from 0.8V to 3.6V ($V_{HSD}$ > 28V)
- ±1% FB accuracy (MIC2174)
- ±3% FB accuracy (MIC2174C)
- Up to 94% efficiency
- Foldback current limit and "hiccup" mode short-circuit protection
- Thermal shutdown
- Safe start-up into pre-biased loads
- –40°C to +125°C junction temperature range

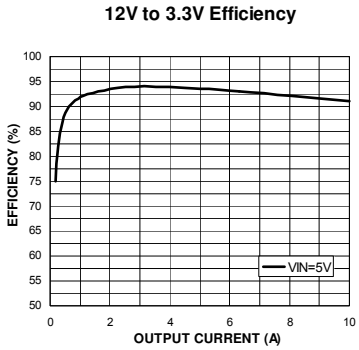
## Applications

- Telecom Networking
- Industrial Equipment
- Distributed DC power systems

## Typical Application




**Synchronous Buck Controller Featuring Adaptive On-Time Control**

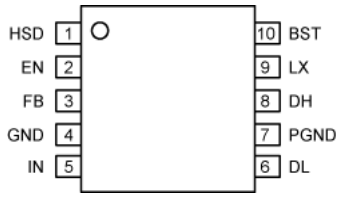



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## Ordering Information

| Part Number | Voltage | Accuracy | Switching Frequency | Junction Temperature Range | Package | Lead Finish |
|---|---|---|---|---|---|---|
| MIC2174-1YMM | Adj. | ±1% | 300kHz | –40° to +125°C | 10-Pin MSOP | Pb-Free |
| MIC2174C-1YMM | Adj. | ±3% | 270kHz | –40° to +125°C | 10-Pin MSOP | Pb-Free |

## Pin Configuration




**10-Pin MSOP (MM)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | HSD | High-Side N-MOSFET Drain Connection (input): Power to the drain of the external high-side N-channel MOSFET. The HSD operating voltage range is from 3V to 40V. Input capacitors between HSD and the power ground (PGND) are required. |
| 2 | EN | Enable (input): A logic level control of the output. The EN pin is CMOS-compatible. Logic high or floating = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 0.8mA). |
| 3 | FB | Feedback (input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. |
| 4 | GND | Signal ground. GND is the ground path for the device input voltage $V_{IN}$ and the control circuitry. The loop for the signal ground should be separate from the power ground (PGND) loop. |
| 5 | IN | Input Voltage (input): Power to the internal reference and control sections of the MIC2174/MIC2174C. The IN operating voltage range is from 3V to 5.5V. A 2.2µF ceramic capacitors from IN to GND are recommended for clean operation. $V_{IN}$ must be powered up no earlier than $V_{HSD}$ to make the soft-start function behavior correctly. |
| 6 | DL | Low-Side Drive (output): High-current driver output for external low-side MOSFET. The DL driving voltage swings from ground to IN. |
| 7 | PGND | Power Ground. PGND is the ground path for the MIC2174/MIC2174C buck converter power stage. The PGND pin connects to the sources of low-side N-Channel MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal ground (GND) loop. |
| 8 | DH | High-Side Drive (output): High-current driver output for external high-side MOSFET. The DH driving voltage is floating on the switch node voltage (LX). It swings from ground to $V_{IN}$ minus the diode drop. Adding a small resistor between DH pin and the gate of the high-side N-channel MOSFETs can slow down the turn-on and turn-off time of the MOSFETs. |

## Pin Description (Continued)

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 9 | LX | Switch Node and Current Sense input: High current output driver return. The LX pin connects directly to the switch node. Due to the high speed switching on this pin, the LX pin should be routed away from sensitive nodes.<br>LX pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to LX using a Kelvin connection. |
| 10 | BST | Boost (output): Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the IN pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the LX pin. Adding a small resistor in series with the boost capacitor can slow down the turn-on time of high-side N-Channel MOSFETs. |

## Absolute Maximum Ratings[1]

IN, FB, EN to GND ..... –0.3V to +6V
BST to LX ..... –0.3V to +6V
BST to GND ..... –0.3V to +46V
DH to LX ..... –0.3V to ($V_{BST}$ + 0.3V)
DL, COMP to GND ..... –0.3V to ($V_{IN}$ + 0.3V)
HSD to GND ..... –0.3V to 42V
PGND to GND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature ($T_S$) ..... –65°C to +150°C
Lead Temperature (soldering, 10sec) ..... 260°C

## Operating Ratings[2]

Input Voltage ($V_{IN}$) ..... 3.0V to 5.5V
Supply Voltage ($V_{HSD}$) ..... 3.0V to 40V
Junction Temperature ($T_J$) ..... –40°C to +125°C
Junction Thermal Resistance
MSOP ($\theta_{JA}$) ..... 130.5°C/W
Continuous Power Dissipation ($T_A$ = 70°C) ..... 421mW
(derate 5.6mW/°C above 70°C)

.

## Electrical Characteristics[4]

$V_{BST} - V_{LX}$ = 5V; $T_A$ = 25°C, unless noted. **Bold** values indicate –40°C ≤ $T_J$ ≤ +125°C.

| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **General** | | | | | |
| Operating Input Voltage ($V_{IN}$) [5] | | **3.0** | | **5.5** | V |
| HSD Voltage Range ($V_{HSD}$) | | **3.0** | | **40** | V |
| Quiescent Supply Current | ($V_{FB}$ = 1.5V, output switching but excluding external MOSFET gate current) | | 1.4 | **3.0** | mA |
| Standby Supply Current | $V_{IN}$ = $V_{BST}$ = 5.5V, $V_{HSD}$ = 40V, LX = unconnected, EN = GND [6] | | 0.8 | **2** | mA |
| Undervoltage Lockout Trip Level | | **2.4** | 2.7 | **3** | V |
| UVLO Hysteresis | | | 50 | | mV |
| **DC-DC Controller** | | | | | |
| Output-Voltage Adjust Range ($V_{OUT}$) | 3.0V ≤ $V_{HSD}$ ≤ 28V | **0.8** | | **5.5** | V |
| | 28V < $V_{HSD}$ ≤ 40V | **0.8** | | **3.6** | |
| **Error Amplifier** | | | | | |
| FB Regulation Voltage | 0°C ≤ $T_J$ ≤ 85°C (MIC2174) | **-1** | | **1** | % |
| | –40°C ≤ $T_J$ ≤ 125°C (MIC2174) | **-2** | | **2** | |
| | $T_J$ = 25°C (MIC2174C) | -3 | | 3 | |
| FB Input Leakage Current | | | 5 | **500** | nA |
| Current-Limit Threshold | $V_{FB}$ = 0.8V (MIC2174) | **103** | 130 | **162** | mV |
| | $V_{FB}$ = 0V (MIC2174) | **19** | 48 | **77** | |
| | $V_{FB}$ = 0.8V(MIC2174C) | **95** | 130 | **170** | |
| | $V_{FB}$ = 0V (MIC2174C) | **15** | 48 | **80** | |

**Notes:**

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.
5. The application is fully functional at low IN (supply of the control section) if the external MOSFETs have enough low voltage $V_{TH}$.
6. The current will come only from the internal 100kΩ pull-up resistor sitting on the EN Input and tied to IN.

## Electrical Characteristics[4]

$V_{BST} - V_{LX}$ = 5V; $T_A$ = 25°C, unless noted. **Bold** values indicate –40°C ≤ $T_J$ ≤ +125°C.

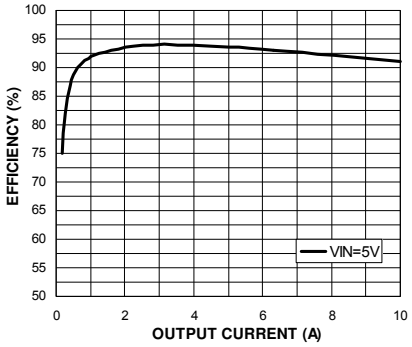
| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Soft-Start** | | | | | |
| Soft-Start Period | | | 6 | | ms |
| **Oscillator** | | | | | |
| Switching Frequency | MIC2174 | **0.225** | 0.3 | **0.375** | MHz |
| | MIC2174C | **0.202** | 0.27 | **0.338** | |
| Maximum Duty Cycle | Measured at DH [7] | | 87 | | % |
| | MIC2174C | | 87 | | |
| Minimum Duty Cycle | Measured at DH, $V_{FB}$ = 1V | | 0 | | % |
| **FET Drives** | | | | | |
| DH, DL Output Low Voltage | $I_{SINK}$ = 10mA | | | **0.1** | V |
| DH, DL Output High Voltage | $I_{SOURCE}$ = 10mA | $V_{IN}$-0.1V or $V_{BST}$-0.1V | | | V |
| DH On-Resistance, High State | | | 2.1 | **3.3** | Ω |
| DH On-Resistance, Low State | | | 1.8 | **3.3** | Ω |
| DL On-Resistance, High State | | | 1.8 | **3.3** | Ω |
| DL On-Resistance, Low State | | | 1.2 | **2.3** | Ω |
| LX Leakage Current | $V_{LX}$ = 40V, $V_{IN}$ = 5.5V,$V_{BST}$ = 45.5V | | | **55** | µA |
| HSD Leakage Current | $V_{LX}$ = 40V, $V_{IN}$ = 5.5V,$V_{BST}$ = 45.5V | | | **21** | µA |
| **Thermal Protection** | | | | | |
| Over-Temperature Shutdown | | | 155 | | °C |
| Over-Temperature Shutdown Hysteresis | | | 10 | | °C |
| **Shutdown Control** | | | | | |
| EN Logic Level Low | 3V < $V_{IN}$ <5.5V | **0.4** | 0.8 | | V |
| EN Logic Level High | 3V < $V_{IN}$ <5.5V | | 0.9 | **1.2** | V |
| EN Pull-Up Current | | | 50 | | µA |

**Note:**

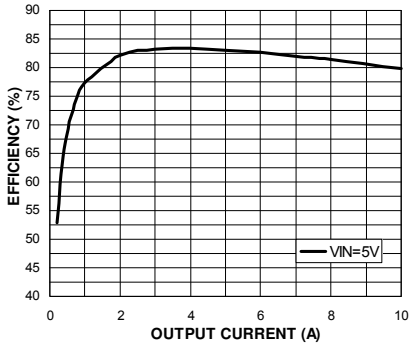
7. The maximum duty cycle is limited by the fixed mandatory off time $T_{OFF}$ of typical 363ns.

## Typical Characteristics

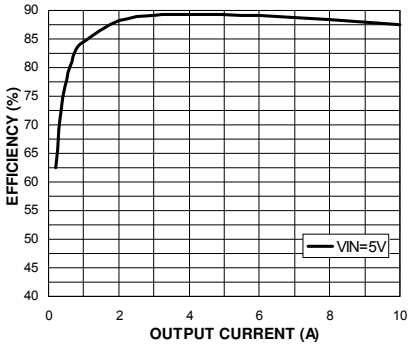
**12V to 3.3V Efficiency**



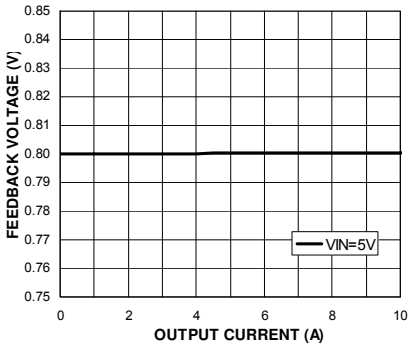

**24V to 1.8V Efficiency**



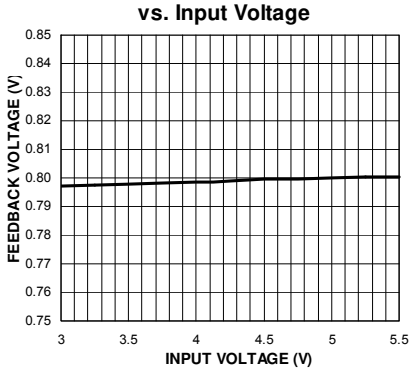

**24V to 3.3V Efficiency**



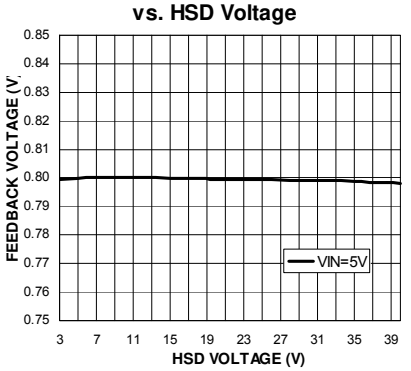

**Feedback Voltage vs. Load**



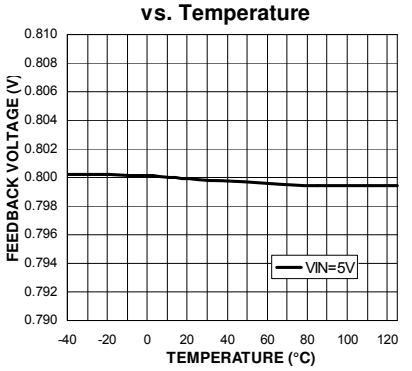

**Feedback Voltage vs. Input Voltage**



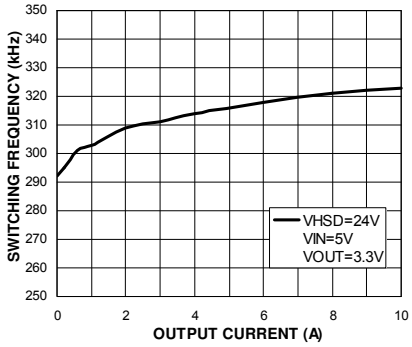

**Feedback Voltage vs. HSD Voltage**



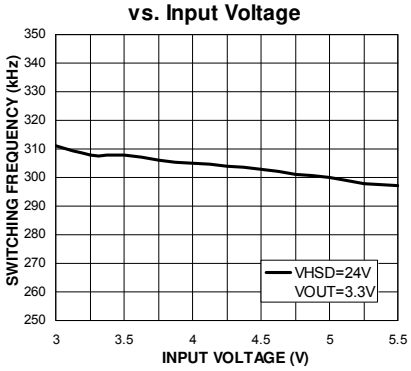

**Feedback Voltage vs. Temperature**



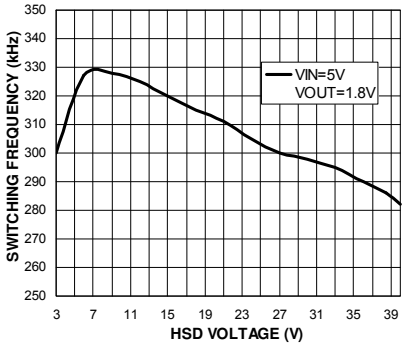

**Switching Frequency vs. Load**



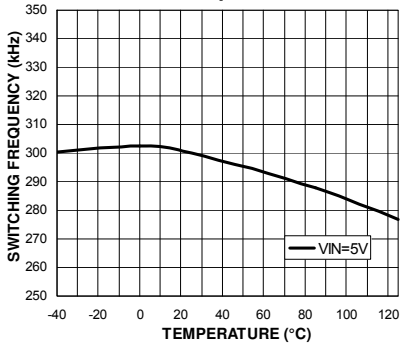

**Switching Frequency vs. Input Voltage**



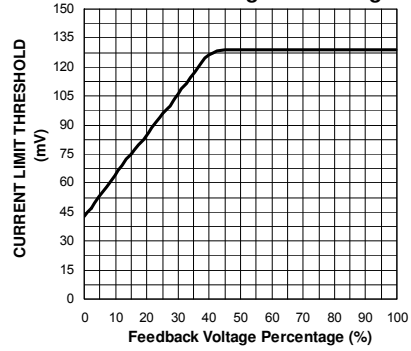

**Switching Frequency vs. HSD Voltage**




**Switching Frequency vs. Temperature**

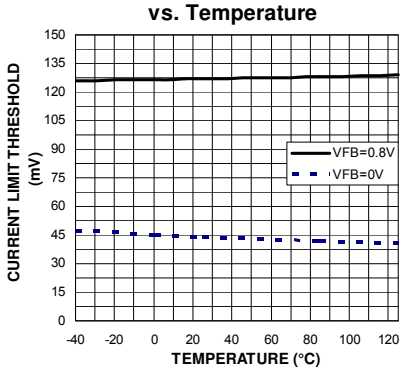



**Current Limit Threshold vs. Feedback Voltage Percentage**

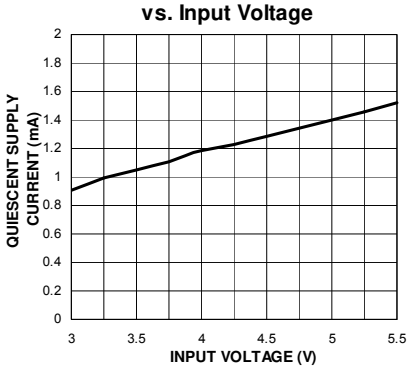


## Typical Characteristics (Continued)

**Current Limit Threshold vs. Temperature**

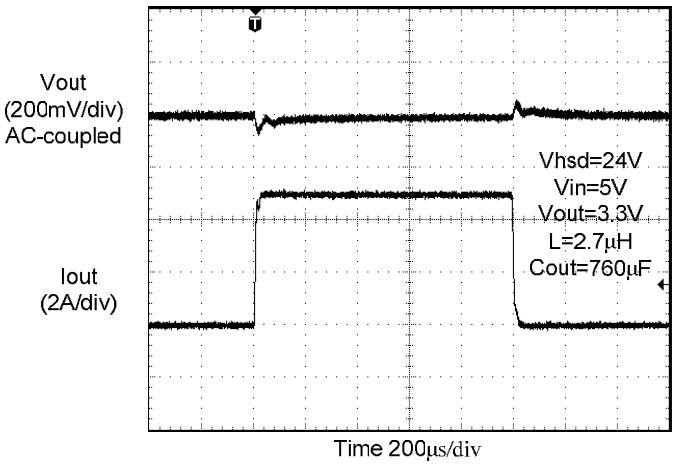



**Quiescent Supply Current vs. Input Voltage**

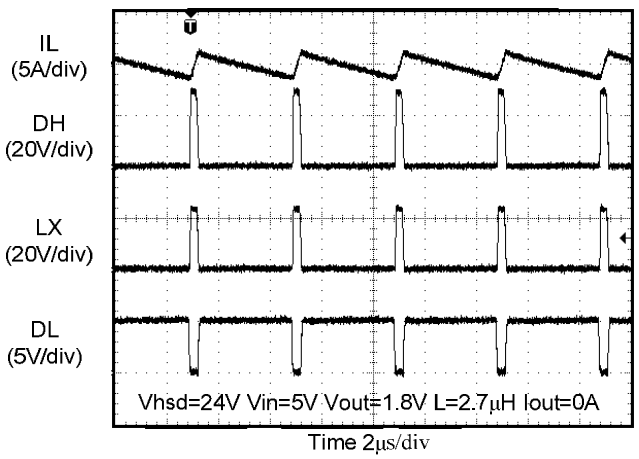


## Functional Characteristics

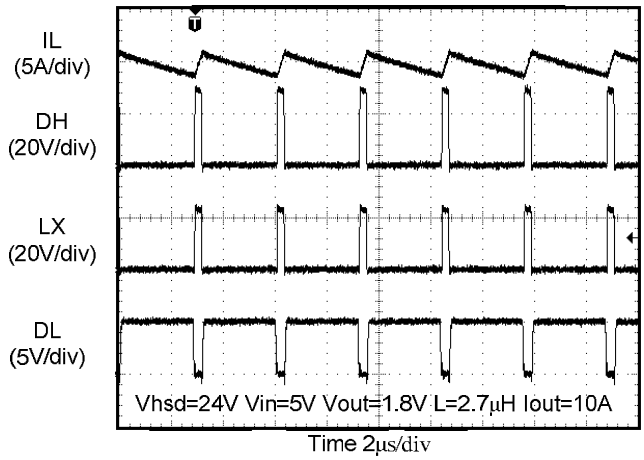
**Load Transient**



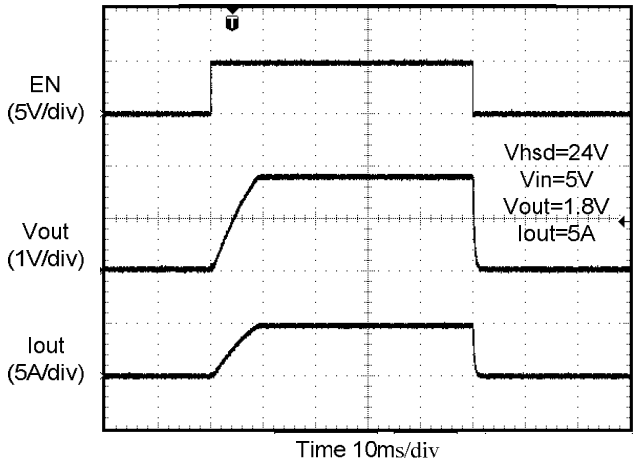

**Switching Waveform (No Load)**




**Switching Waveform (Heavy Load)**

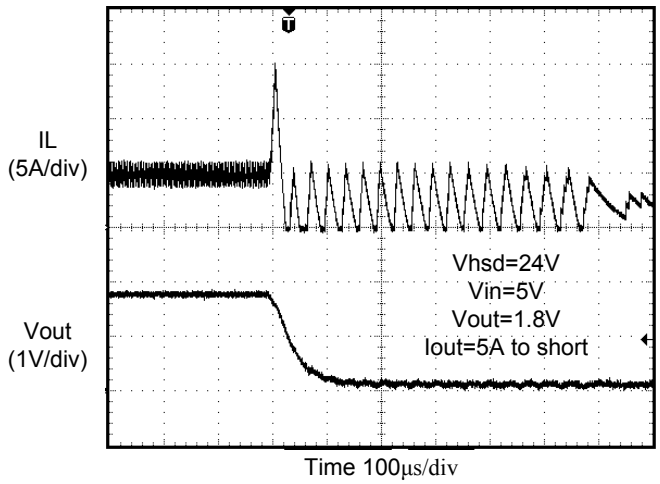



**Power-Up/Power-Down**

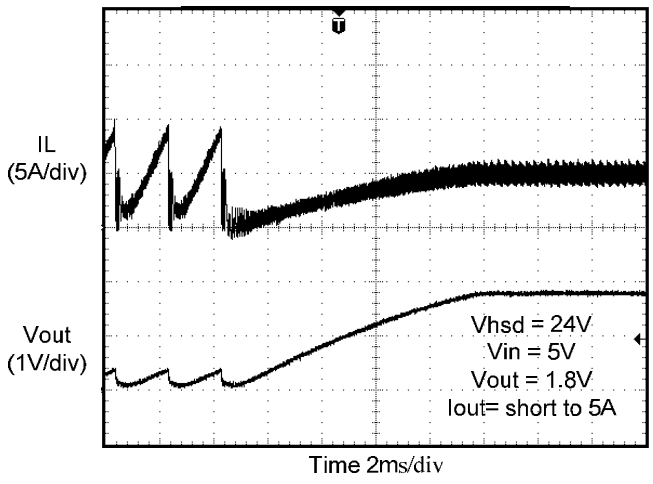


## Functional Characteristics (Continued)

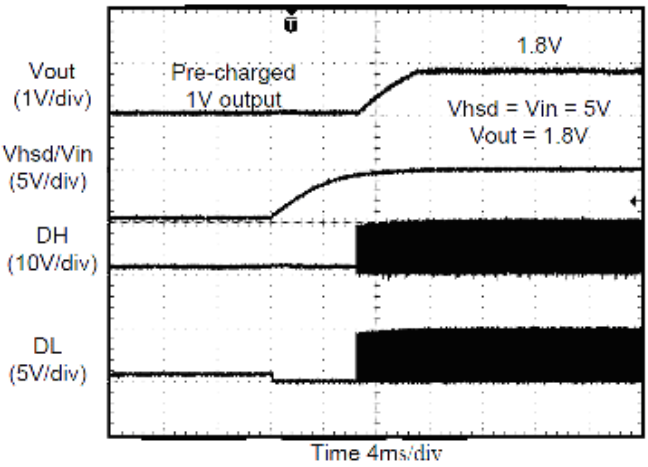
**Short Circuit**



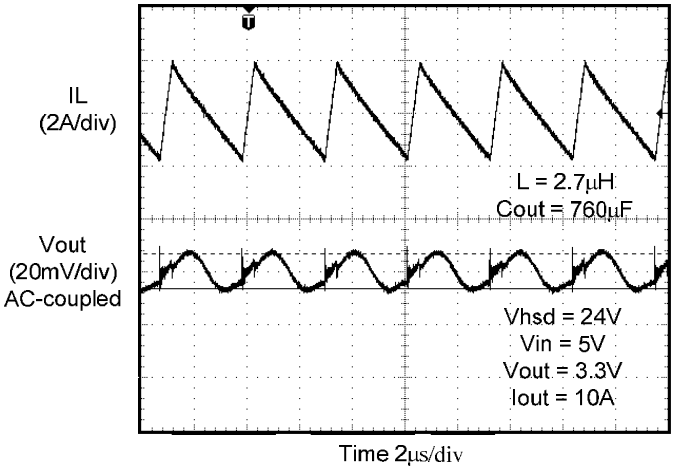

**Short Circuit Recovery**




**Start-up with Prebias Vout**




**Output Voltage Ripple**



## Functional Diagram

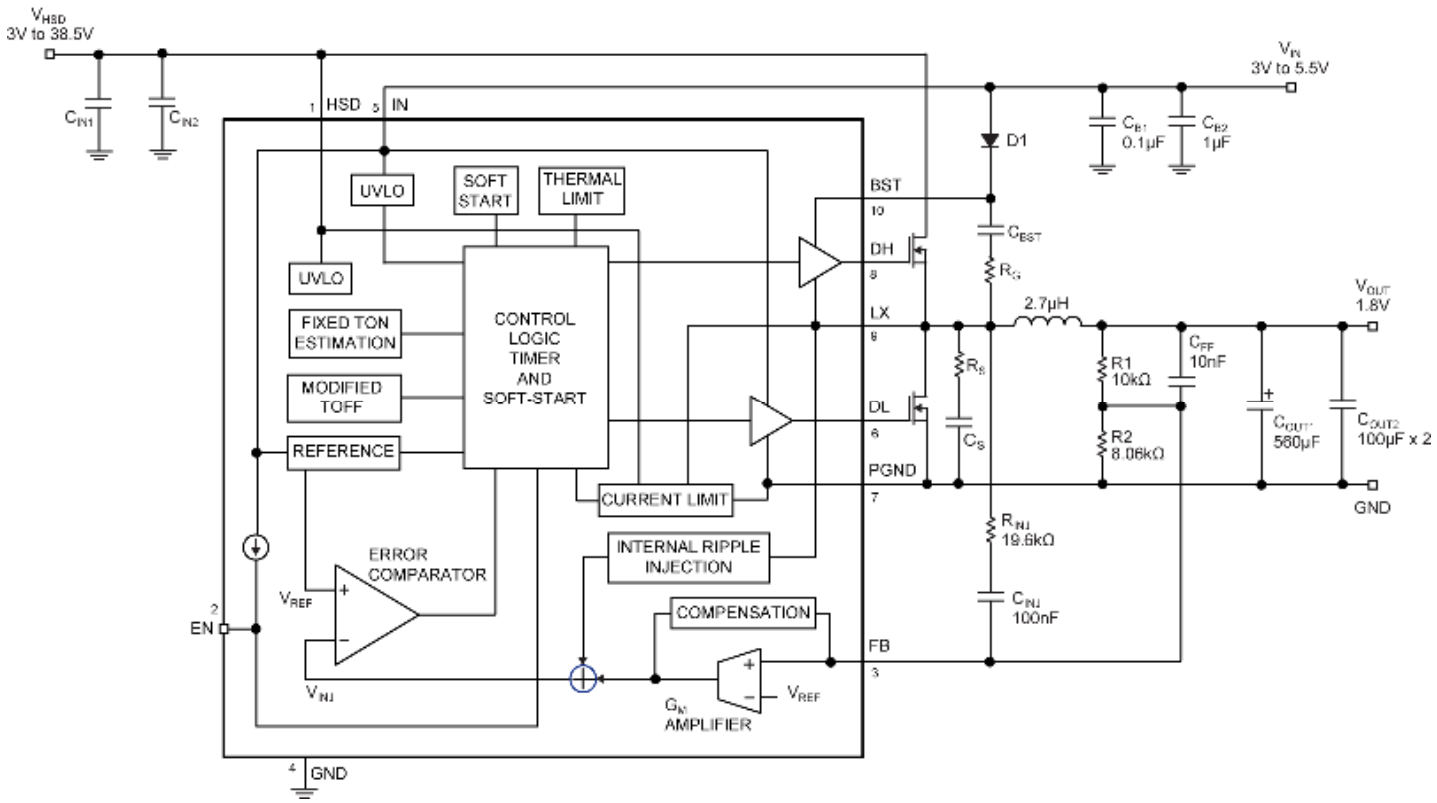



**Figure 1. MIC2174/MIC2174C Block Diagram**

## Functional Description

The MIC2174/MIC2174C is an adaptive on-time synchronous buck controller built for low cost and high performance. It is designed for a wide input voltage range from 3V to 40V and for high output power buck converters. An estimated-ON-time method is applied in MIC2174/MIC2174C to obtain a constant switching frequency and to simplify the control compensation. The over-current protection is implemented without the use of an external sense resistor. It includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

### Theory of Operation

The MIC2174/MIC2174C is an adaptive on-time synchronous buck controller. Further, Figure 1 illustrates the block diagram for the control loop. The output voltage variation will be sensed by the MIC2174/MIC2174C feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage $V_{REF}$ at the error comparator through a low gain transconductance (gm) amplifier, which improves the MIC2174/MIC2174C converter output voltage regulation. If the FB voltage decreases and the output of the gm amplifier is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period, where in DH pin is logic high and DL pin is logic low. The ON-time period length is predetermined by the "FIXED $T_{ON}$ ESTIMATION" circuitry:

$$T_{ON(estimated)} = \frac{V_{OUT}}{V_{HSD} \times 300kHz} \quad (1)$$

where $V_{OUT}$ is the output voltage, $V_{HSD}$ is the power stage input voltage.

After an ON-time period, the MIC2174/MIC2174C goes into the OFF-time period. This is when the DH pin is logic low and DL pin is logic high. The OFF-time period length depends upon the FB voltage in most cases. When the FB voltage decreases and the output of the gm amplifier is below 0.8V, then the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the FB voltage is less than the minimum OFF time $T_{OFF(min)}$, which is about 363ns typical, then the MIC2174/MIC2174C control logic will apply the $T_{OFF(min)}$ instead. $T_{OFF(min)}$ is required to maintain enough energy in the Boost capacitor ($C_{BST}$) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 363ns $T_{OFF(min)}$:

$$Dmax = \frac{T_S - T_{OFF(min)}}{T_S} = 1 - \frac{363ns}{T_S}$$

where Ts = 1/300kHz = 3.33µs. It is not recommended to use MIC2174/MIC2174C with a OFF-time close to $T_{OFF(min)}$ during steady-state operation. Also, as $V_{OUT}$ increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the MIC2174 should be limited to 5.5V for up to 28V $V_{HSD}$ and 3.6V for $V_{HSD}$ higher than 28V. If a higher output voltage is required, use the MIC2176 instead. Please refer to "Setting Output Voltage" subsection in "Application Information" for more details.

The power stage input voltage $V_{HSD}$ is fed into the Fixed $T_{ON}$ Estimation block through a 6:1 divider and 5V voltage clamper. Therefore, if the $V_{HSD}$ is higher than 30V, then the Fixed $T_{ON}$ Estimation block uses 30V to estimate $T_{ON}$ instead of the real $V_{HSD}$. As a result, the switching frequency will be less than 300kHz:

$$f_{SW(VHDS>30V)} = \frac{30V}{V_{HSD}} \times 300kHz \quad (2)$$

The estimated ON-time method results in a constant 300kHz switching frequency up to 30V $V_{HSD}$. The actual ON-time varies with the different rising and falling times of the external MOSFETs. Therefore, the type of the external MOSFETs, the output load current, and the control circuitry power supply $V_{IN}$ will modify the actual ON-time and the switching frequency. Also, the minimum $T_{ON}$ results in a lower switching frequency in high $V_{HSD}$ and low $V_{OUT}$ applications, such as 36V to 1.0V. The minimum $T_{ON}$ measured on the MIC2174/MIC2174C evaluation board with Si7148DP MOSFETs is about 184ns. During the load transient, the switching frequency is changed due to the varying OFF time.

To illustrate the control loop, the steady-state scenario and the load transient scenario are analyzed. For easy analysis, the gain of the gm amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the FB voltage. Figure 2 shows the MIC2174/MIC2174C control loop timing during steady-state operation. During steady-state, the gm amplifier senses the FB voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the estimation. The ending of OFF-time is controlled by the FB voltage. At the valley of

the FB voltage ripple, which occurs when $V_{FB}$ falls below $V_{REF}$, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

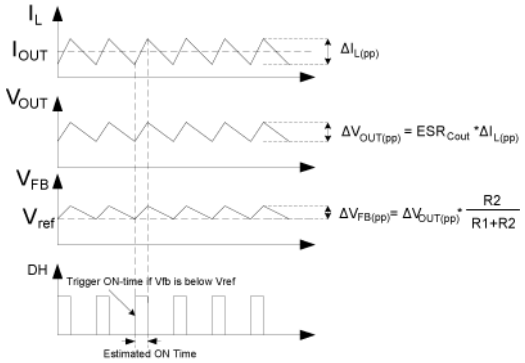



**Figure 2. MIC2174/MIC2174C Control Loop Timing**

Figure 3 shows the load transient operation of the MIC2174/MIC2174C converter. The output voltage drops due to the sudden load increase, which causes the FB voltage to be less than $V_{REF}$. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $T_{OFF(min)}$ is generated to charge $C_{BST}$ since the FB voltage is still below $V_{REF}$. Then, the next ON-time period is triggered due to the low FB voltage. Therefore, the switching frequency changes during the load transient. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC2174/MIC2174C converter.

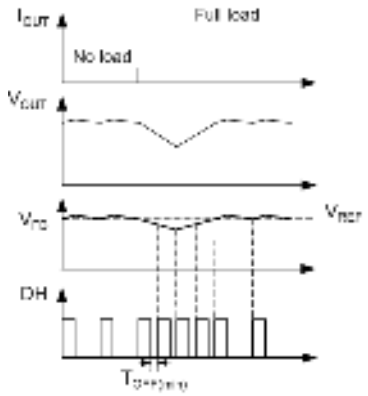



**Figure 3. MIC2174/MIC2174C Load-Transient Response**

Unlike in current-mode control, the MIC2174/MIC2174C uses the output voltage ripple, which is proportional to the inductor current ripple if the ESR of the output capacitor is large enough, to trigger an ON-time period. The MIC2174/MIC2174C predetermined ON-time control loop has the advantage of constant ON-time mode control that eliminates the need for the slope compensation.

The MIC2174/MIC2174C has its own stability concern; the FB voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the gm amplifier and the error comparator. The recommended FB voltage ripple is 20mV~100mV. If a low ESR output capacitor is selected, then the FB voltage ripple may be too small to be sensed by the gm amplifier and the error comparator. Also, the output voltage ripple and the FB voltage ripple are not in phase with the inductor current ripple if the ESR of the output capacitor is very low. Therefore, the ripple injection is required for a low ESR output capacitor. Please refer to "Ripple Injection" subsection in "Application Information" for more details about the ripple injection.

### Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC2174/MIC2174C implements an internal digital soft-start by making the 0.8V reference voltage $V_{REF}$ ramp from 0 to 100% in about 6ms with a 9.7mV step. Therefore, the output voltage is controlled to increase slowly by a stair-case $V_{REF}$ ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. $V_{IN}$ must be powered up no earlier than $V_{HSD}$ to make the soft-start function behavior correctly.

### Current Limit

The MIC2174/MIC2174C uses the $R_{DS(ON)}$ of the low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC2174/MIC2174C converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage is compared with a current-limit threshold voltage $V_{CL}$ after a blanking time of 150ns. If the sensed voltage is over $V_{CL}$, which is 130mV typical at 0.8V feedback voltage, then the MIC2174/MIC2174C turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called "hiccup mode" and its purpose is to protect the downstream load in case of a hard short. The current limit threshold $V_{CL}$ has a fold back characteristic related to the FB voltage. Please refer to the "Typical Characteristics" for the curve of $V_{CL}$ vs. FB voltage.

The circuit in Figure 4 illustrates the MIC2174/MIC2174C current limiting circuit.

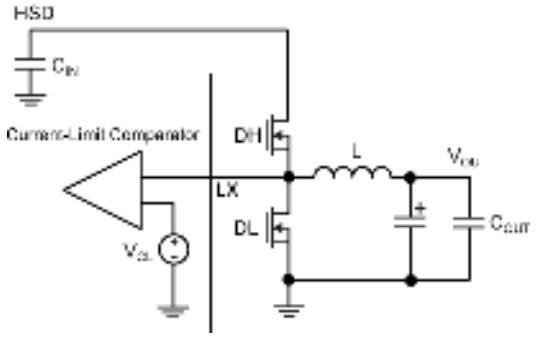



**Figure 4. MIC2174/MIC2174C Current Limiting Circuit**

Using the typical $V_{CL}$ value of 130mV, the current limit value is roughly estimated as:

$$I_{CL} \approx \frac{130mV}{R_{DS(ON)}}$$

For designs where the current ripple is significant compared to the load current $I_{OUT}$, or for low duty cycle operation, calculating the current limit $I_{CL}$ should take into account that one is sensing the peak inductor current and that there is a blanking delay of approximately 150ns.

$$I_{CL} = \frac{130mV}{R_{DS(ON)}} + \frac{V_{OUT} \times t_{DLY}}{L} - \frac{\Delta I_{L(pp)}}{2} \quad (3)$$

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (1-D)}{f_{SW} \times L} \quad (4)$$

where:

$V_{OUT}$ = The output voltage

$t_{DLY}$ = Current limit blanking time, 150ns typical

$\Delta I_{L(pp)}$ = Inductor current ripple peak-to-peak value

D = Duty Cycle

$f_{SW}$ = Switching frequency

The MOSFET $R_{DS(ON)}$ varies 30 to 40% with temperature. Therefore, it is recommended to add 50% margin to $I_{CL}$ in the above equation to avoid false current limiting due to an increased MOSFET junction temperature rise. It is also recommended to connect the LX pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

**MOSFET Gate Drive**

The MIC2174/MIC2174C high-side drive circuit is designed to switch an N-Channel MOSFET. The block diagram of Figure 1 shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and $C_{BST}$. This circuit supplies energy to the high-side drive circuit. Capacitor $C_{BST}$ is charged, while the low-side MOSFET is on, and the voltage on the LX pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from $C_{BST}$ is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the LX pin increases to approximately $V_{HSD}$. Diode D1 is reversed biased and $C_{BST}$ floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. ΔBST = 10mA x 3.33µs/0.1µF = 333mV. When the low-side MOSFET is turned back on, $C_{BST}$ is recharged through D1. A small resistor $R_G$, which is in series with $C_{BST}$, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the supply voltage $V_{IN}$. The nominal low-side gate drive voltage is $V_{IN}$ and the nominal high-side gate drive voltage is approximately $V_{IN} – V_{DIODE}$, where $V_{DIODE}$ is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

## Application Information

### MOSFET Selection

The MIC2174/MIC2174C controller works from input voltages of 3V to 40V and has an external 3V to 5.5V $V_{IN}$ to provide power to turn the external N-Channel power MOSFETs for the high- and low-side switches. For applications where $V_{IN}$ < 5V, it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for $V_{GS}$ of 2.5V. For applications when $V_{IN}$ > 5V; logic-level MOSFETs, whose operation is specified at $V_{GS}$ = 4.5V must be used.

There are differing criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles, such as a 12V to 1.8V conversion. In such an application, the high-side MOSFET is required to switch as quickly as possible to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty cycle approaches 50%, the current carrying capability of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current limit. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions ($V_{DS}$ and $V_{GS}$). The gate charge is supplied by the MIC2174/MIC2174C gate-drive circuit. At 300kHz switching frequency and above, the gate charge can be a significant source of power dissipation in the MIC2174/MIC2174C. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[high\text{-}side]}(avg) = Q_G \times f_{SW} \quad (5)$$

where:

$I_{G[high\text{-}side]}(avg)$ = Average high-side MOSFET gate current

$Q_G$ = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for $V_{GS} = V_{IN}$.

$f_{SW}$ = Switching Frequency (300kHz)

The low-side MOSFET is turned on and off at $V_{DS}$ = 0 because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using $C_{ISS}$ at $V_{DS}$ = 0 instead of gate charge.

For the low-side MOSFET:

$$I_{G[low\text{-}side]}(avg) = C_{ISS} \times V_{GS} \times f_{SW} \quad (6)$$

Since the current from the gate drive comes from the $V_{IN}$, the power dissipated in the MIC2174/MIC2174C due to gate drive is:

$$P_{GATEDRIVE} = V_{IN} \times (I_{G[high\text{-}side]}(avg) + I_{G[low\text{-}side]}(avg)) \quad (7)$$

A convenient figure of merit for switching MOSFETs is the on resistance times the total gate charge $R_{DS(ON)} \times Q_G$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2174/MIC2174C. Also, the $R_{DS(ON)}$ of the low-side MOSFET will determine the current limit value. Please refer to "Current Limit" subsection in "Functional Description" for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage $V_{HSD}$. A safety factor of 20% should be added to the $V_{DS}$(max) of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses during the period of time when the MOSFETs turn on and off ($P_{AC}$):

$$P_{SW} = P_{CONDUCTION} + P_{AC} \quad (8)$$

$$P_{CONDUCTION} = I_{SW(RMS)}^2 \times R_{DS(ON)} \quad (9)$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)} \quad (10)$$

where:

$R_{DS(ON)}$ = on-resistance of the MOSFET switch

D = Duty Cycle = $V_{OUT} / V_{HSD}$

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{IN} + C_{OSS} \times V_{HSD}}{I_G} \quad (11)$$

where:

$C_{ISS}$ and $C_{OSS}$ are measured at $V_{DS}$ = 0

$I_G$ = gate-drive current

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{HSD} + V_D) \times I_{PK} \times t_T \times f_{SW} \quad (12)$$

where:

$t_T$ = Switching transition time

$V_D$ = Body diode drop (0.5V)

$f_{SW}$ = Switching Frequency (300kHz)

The high-side MOSFET switching losses increase with the input voltage $V_{HSD}$ due to the longer turn-on time and turn-off time. The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

**Inductor Selection**

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by Equation 13:

$$L = \frac{V_{OUT} \times (V_{HSD(max)} - V_{OUT})}{V_{HSD(max)} \times f_{sw} \times 20\% \times I_{OUT(max)}} \quad (13)$$

where:

$f_{SW}$ = switching frequency, 300 kHz

20% = ratio of AC ripple current to DC output current

$V_{HSD(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{HSD(max)} - V_{OUT})}{V_{HSD(max)} \times f_{sw} \times L} \quad (14)$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \quad (15)$$

The RMS inductor current is used to calculate the $I^2R$ losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(PP)}^2}{12}} \quad (16)$$

Maximizing efficiency requires both the proper selection of core material and the minimizing of winding resistance. The high frequency operation of the MIC2174/MIC2174C requires the use of ferrite materials for all but the most cost sensitive applications.

Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 17:

$$P_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING} \quad (17)$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$P_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \quad (18)$$

where:

$T_H$ = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

**Output Capacitor Selection**

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAPS. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad (19)$$

where:

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \quad (20)$$

where:

D = duty cycle

$C_{OUT}$ = output capacitance value

$f_{SW}$ = switching frequency

As described in the "Theory of Operation" subsection in *Functional Description*, the MIC2174/MIC2174C requires at least 20mV peak-to-peak ripple at the FB pin to make the gm amplifier and the error comparator to behavior properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor $C_{OUT}$ should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough FB voltage ripple. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated below:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad (21)$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^2 \times ESR_{C_{OUT}} \quad (22)$$

**Input Capacitor Selection**

The input capacitor for the power stage input $V_{HSD}$ should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(pk)} \times ESR_{CIN} \quad (23)$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{CIN(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1-D)} \quad (24)$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN} \quad (25)$$

**External Schottky Diode (Optional)**

An external freewheeling diode, which is not necessary, is used to keep the inductor current flow continuous while both MOSFETs are turned off. This dead-time prevents current from flowing unimpeded through both MOSFETs and is typically 30ns. The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

$$I_{D(avg)} = I_{OUT} \times 2 \times 30ns \times f_{SW} \quad (26)$$

The reverse voltage requirement of the diode is:

$$V_{DIODE(rrm)} = V_{HSD}$$

The power dissipated by the Schottky diode is:

$$P_{DIODE} = I_{D(avg)} \times V_F \quad (27)$$

where, $V_F$ = forward voltage at the peak diode current.

The external Schottky diode is not necessary for the circuit operation since the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease the high frequency noise. If the MOSFET body diode is used, then it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending upon the circuit components and operating conditions, an external Schottky diode will give a 1/2% to 1% improvement in efficiency.

### Snubber Design

A snubber is used to damp out high frequency ringing caused by parasitic inductance and capacitance in the buck converter circuit. Figure 5 shows a simplified schematic of the buck converter. Stray capacitance consists mostly of the two MOSFETs' output capacitance ($C_{OSS}$). The stray inductance consists mostly package inductance and trace inductance. The arrows show the resonant current path when the high side MOSFET turns on. This ringing causes stress on the semiconductors in the circuit as well as increased EMI.

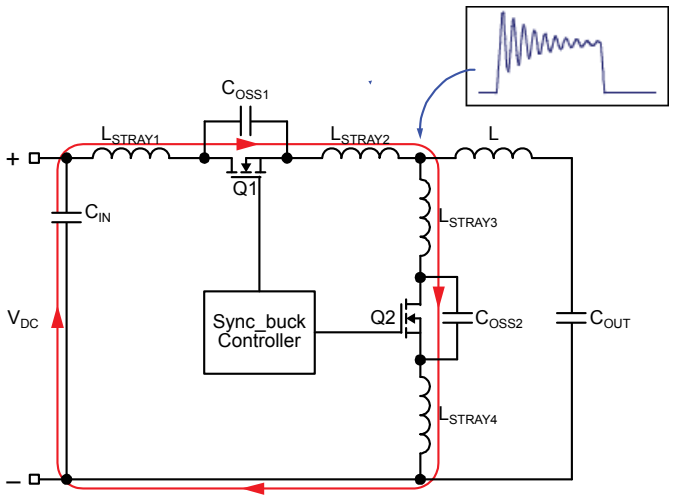



**Figure 5. Output Parasitics**

One method of reducing the ringing is to use a resistor and capacitor to lower the Q of the resonant circuit, as shown in Figure 6. Capacitor $C_S$ is used to block DC and minimize the power dissipation in the resistor. This capacitor value should be between two and ten times the parasitic capacitance of the MOSFET $C_{OSS}$. A capacitor that is too small will have high impedance and prevent the resistor from damping the ringing. A capacitor that is too large causes unnecessary power dissipation in the resistor, which lowers efficiency.

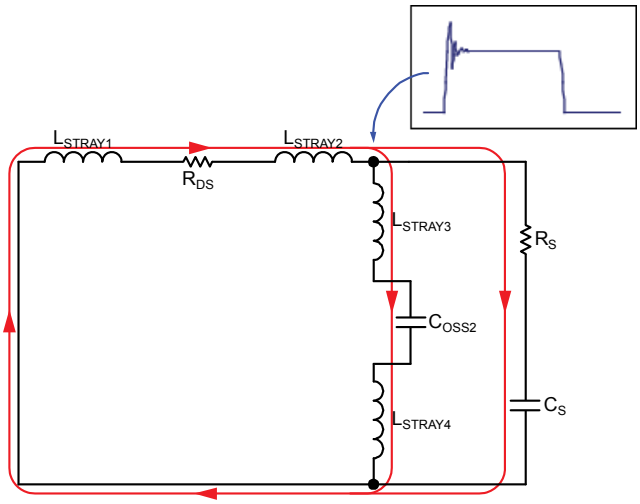



**Figure 6. Snubber Circuit**

The snubber components should be placed as close as possible to the low-side MOSFET and/or external Schottky diode since it contributes to most of the stray capacitance. Placing the snubber too far from the FET or using trace that is too long or thin will add inductance to the snubber and diminishes its effectiveness.

A proper snubber design requires the parasitic inductance and capacitance be known. A method of determining these values and calculating the damping resistor value is outlined below.

1. Measure the ringing frequency at the switch node which is determined by parasitic $L_P$ and $C_P$. Define this frequency as $f_1$.
2. Add a capacitor $C_S$ (such as two times as big as the $C_{OSS}$ of the FET) from the switch node-to-ground and measure the new ringing frequency. Define this new (lower) frequency as $f_2$. $L_P$ and $C_P$ can now be solved using the values of $f_1$, $f_2$ and $C_S$.
3. Add a resistor $R_S$ in series with $C_S$ to generate critical damping.

**Step 1:** First measure the ringing frequency on the switch node voltage when the high-side MOSFET turns on. This ringing is characterized by the equation:

$$f_1 = \frac{1}{2\pi\sqrt{L_P \times C_P}} \quad (28)$$

where $C_P$ and $L_P$ are the parasitic capacitance and inductance.

**Step 2:** Add a capacitor, $C_S$, in parallel with the synchronous MOSFET, Q2. The capacitor value should be approximately two times the $C_{OSS}$ of Q2. Measure the frequency of the switch node ringing, $f_2$:

$$f_2 = \frac{1}{2\pi\sqrt{Lp \times (Cs + Cp)}} \quad (29)$$

Define f' as:

$$f' = \frac{f_1}{f_2}$$

Combining the equations for $f_1$, $f_2$ and f' to derive $C_P$, the parasitic capacitance:

$$C_P = \frac{C_S}{(f')^2 - 1} \quad (30)$$

$L_P$ is solved by re-arranging the equation for $f_1$:

$$L_P = \frac{1}{(2\pi)^2 \times C_P \times (f_1)^2} \quad (31)$$

**Step 3:** Calculate the damping resistor.

Critical damping occurs at Q = 1:

$$Q = R_S \times \sqrt{\frac{C_P}{L_P}} = 1 \quad (32)$$

Solving for $R_S$

$$R_S = \sqrt{\frac{L_P}{C_p}} \quad (33)$$

Figure 6 shows the snubber in the circuit and the damped switch node waveform. The snubber capacitor, $C_S$, is charged and discharged each switching cycle. The energy stored in $C_S$ is dissipated by the snubber resistor, $R_S$, two times per switching period. This power is calculated in Equation 34:

$$P_{SNUBBER} = f_{SW} \times C_S \times V_{IN}^2 \quad (34)$$

**Ripple Injection**

The $V_{FB}$ ripple required for proper operation of the MIC2174/MIC2174C gm amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V output, the output voltage ripple is only 10mV to 20mV, and the FB voltage ripple is less than 20mV. If the FB voltage ripple is so small that the gm amplifier and error comparator can't sense it, then the MIC2174/MIC2174C will lose control and the output voltage will not be regulated. In order to have some amount of $V_{FB}$ voltage ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the FB voltage ripple:

1. Enough ripple at the FB voltage due to the large ESR of the output capacitors.

As shown in Figure 7a, the converter is stable without any ripple injection. The FB voltage ripple is:

$$\Delta V_{FB(pp)} = \frac{R2}{R1 + R2} \times ESR_{C_{OUT}} \times \Delta I_{L(pp)} \quad (35)$$

where $\Delta I_{L(pp)}$ is the peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at the FB voltage due to the small ESR of the output capacitors.

   The output voltage ripple is fed into the FB pin through a feedforward capacitor $C_{ff}$ in this situation, as shown in Figure 7b. The typical $C_{ff}$ value is between 1nF and 100nF. With the feedforward capacitor, the FB voltage ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \quad (36)$$

3. Virtually no ripple at the FB pin voltage is due to the very low ESR of the output capacitors.

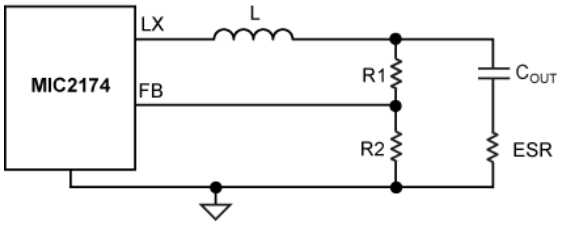



**Figure 7a. Enough Ripple at FB**

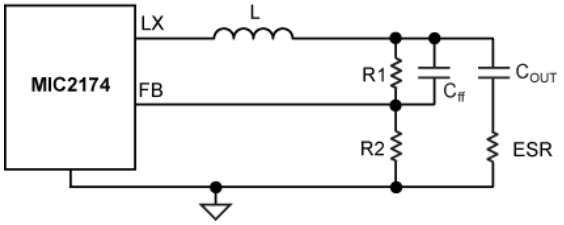



**Figure 7b. Inadequate Ripple at FB**

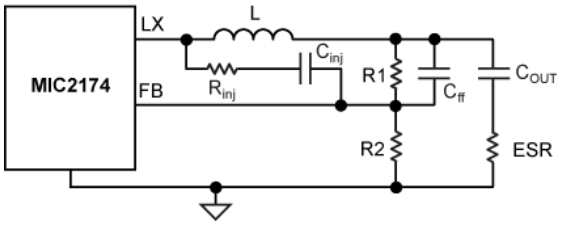



**Figure 7c. Invisible Ripple at FB**

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node LX via a resistor $R_{inj}$ and a capacitor $C_{inj}$, as shown in Figure 7c. The injected ripple is:

$$\Delta V_{FB(pp)} = V_{HSD} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \quad (37)$$

$$K_{div} = \frac{R1//R2}{R_{inj} + R1//R2} \quad (38)$$

where

$V_{HSD}$ = Power stage input voltage at HSD pin

D = Duty Cycle

$f_{SW}$ = switching frequency

$\tau = (R1//R2//R_{inj}) \times C_{ff}$

In the equations (37) and (38), it is assumed that the time constant associated with $C_{ff}$ must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a $C_{ff}$ of 1nF to 100nF can easily satisfy the large time constant consumption. Also, a 100nF injection capacitor $C_{inj}$ is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

***Step 1.*** Select $C_{ff}$ to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of $C_{ff}$ is 1nF to 100nF if R1 and R2 are in kΩ range.

***Step 2.*** Select $R_{inj}$ according to the expected feedback voltage ripple. According to Equation 37:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{HSD}} \times \frac{f_{SW} \times \tau}{D \times (1-D)} \quad (39)$$

Then the value of Rinj is obtained as:

$$R_{inj} = (R1//R2) \times \left(\frac{1}{K_{div}} - 1\right) \quad (40)$$

***Step 3.*** Select $C_{inj}$ as 100nF, which could be considered as short for a wide range of the frequencies.

**Setting Output Voltage**

The MIC2174/MIC2174C requires two resistors to set the output voltage as shown in Figure 8.

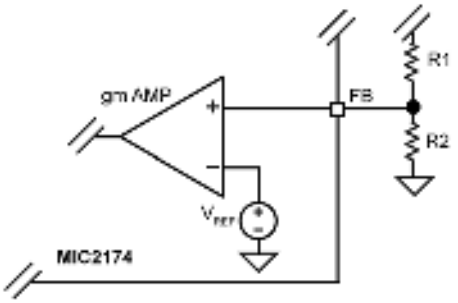



**Figure 8. Voltage-Divider Configuration**

The output voltage is determined by the equation:

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (41)$$

where, $V_{REF}$ = 0.8V. A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads.

Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}} \quad (42)$$

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC2174, as shown in Figure 9. The inverting input voltage $V_{INJ}$ is clamped to 1.2V. For applications with high $V_{HSD}$ and high $V_{OUT}$, the swing of $V_{INJ}$ will be clamped. The clamped $V_{INJ}$ reduces the line regulation because it is reflected back as a DC error on the FB terminal. Therefore, the maximum output voltage of MIC2174 should be limited to 5.5V for up to 28V $V_{HSD}$ and 3.6V for $V_{HSD}$ higher than 28V. If a higher output voltage is required, use the MIC2176 instead.

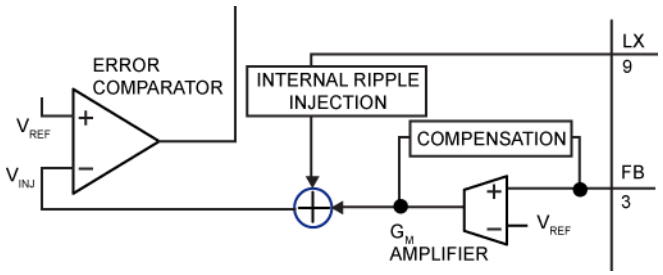



**Figure 9. Internal Ripple Injection**

## PCB Layout Guidelines

**Warning!!! To minimize EMI and output noise, follow these layout recommendations.**

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2174/MIC2174C converter.

**IC**

- The 2.2µF ceramic capacitor, which connects to the $V_{IN}$ terminal, must be located right at the IC. The $V_{IN}$ terminal is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the IN and PGND pins.
- Place the IC and MOSFETs close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

**Input Capacitor**

- Place the HSD input capacitor next.
- Place the HSD input capacitors on the same side of the board and as close to the MOSFETs as possible.
- Keep both the HSD and PGND connections short.
- Place several vias to the ground plane close to the HSD input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.
- An additional Tantalum or Electrolytic bypass input capacitor of 22µF or higher is required at the input power connection.

**Inductor**

- Keep the inductor connection to the switch node (LX) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (LX) away from the feedback (FB) pin.
- The LX pin should be connected directly to the drain of the low-side MOSFET to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

**Output Capacitor**

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

**Schottky Diode (Optional)**

- Place the Schottky diode on the same side of the board as the MOSFETs and HSD input capacitor.
- The connection from the Schottky diode’s Anode to the input capacitors ground terminal must be as short as possible.
- The diode’s cathode connection to the switch node (LX) must be keep as short as possible.

**RC Snubber**

- Place the RC snubber on the same side of the board and as close to the MOSFETs as possible.

**MOSFETs**

- Low-side MOSFET gate drive trace (DL pin to MOSFET gate pin) must be short and routed over a ground plane. The ground plane should be the connection between the MOSFET source and PGND.
- Chose a low-side MOSFET with a high $C_{GS}/C_{GD}$ ratio and a low internal gate resistance to minimize the effect of dv/dt inducted turn-on.
- Do not put a resistor between the LSD output and the gate.
- Use a 4.5V $V_{GS}$ rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than 4.5V $V_{GS}$ should not be used.

## Evaluation Board Schematics

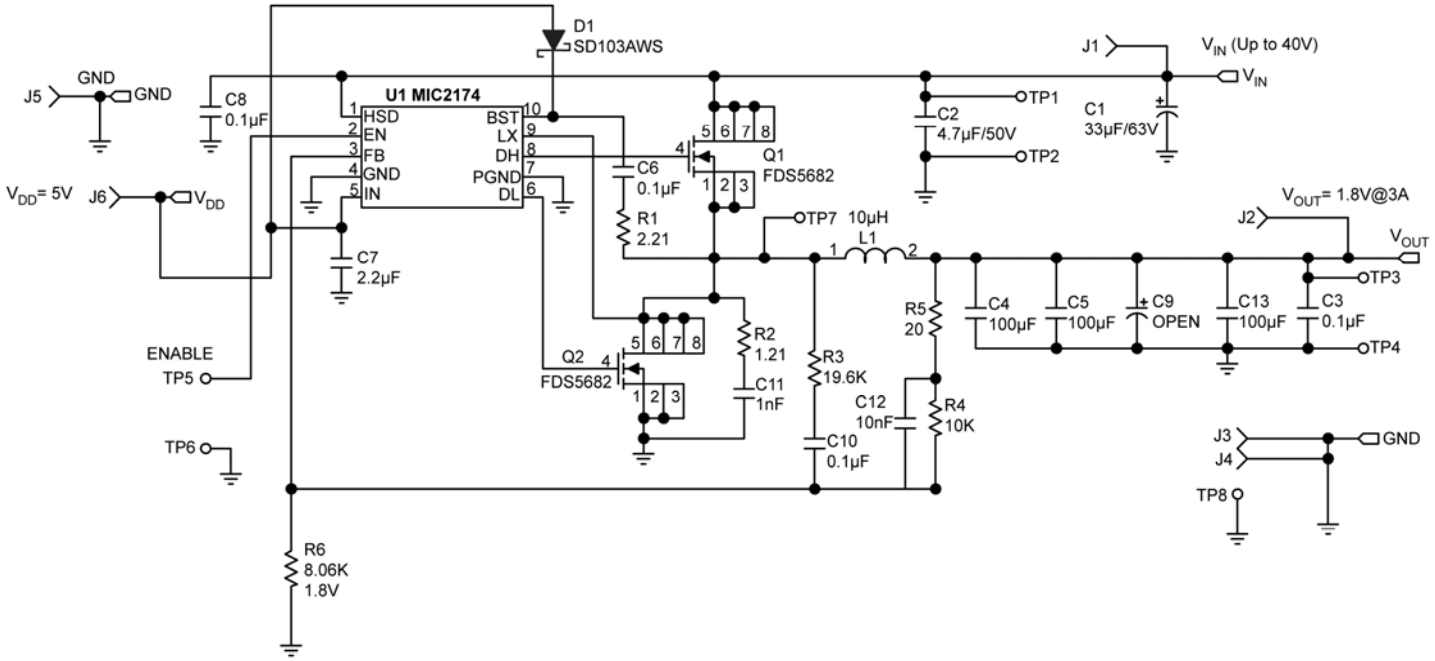



**Figure 10. Schematic of MIC2174/MIC2174C Evaluation Board**

## Bill of Materials

| Item | Part Number | Manufacturer | Description | Qty. |
|---|---|---|---|---|
| C1 | B41112A8336M | EPCOS[1] | 33µF Aluminum Capacitor, SMD, 63V | 1 |
| C2 | 12105C475KAZ2A | AVX[2] | 4.7µF Ceramic Capacitor, X7R, Size 1210, 50V | 1 |
| | GRM32ER71H475KA88L | Murata[3] | | |
| C4, C5, C13 | 12106D107MAT2A | AVX | 100µF Ceramic Capacitor, X5R, Size 1210, 6.3V | 3 |
| | GRM32ER60J107ME20L | Murata | | |
| C3, C6, C8, C10 | 06035C104KAT2A | AVX | 0.1µF Ceramic Capacitor, X7R, Size 0603, 50V | 4 |
| | GRM188R71H104KA93D | Murata | | |
| | C1608X7R1H104K | TDK[4] | | |
| C7 | 0805ZC225MAT2A | AVX | 2.2µF Ceramic Capacitor, X7R, Size 0805, 10V | 1 |
| | GRM21BR71A225KA01L | Murata | | |
| | C2012X7R1A225K | TDK | | |
| C11 | 06035C102KAT2A | AVX | 1nF Ceramic Capacitor, X7R, Size 0603, 50V | 1 |
| | GRM188R71H102KA01D | Murata | | |
| | C1608X7R1H102K | TDK | | |
| C12 | 06035C103KAZ2A | AVX | 10nF Ceramic Capacitor, X7R, Size 0603, 50V | 1 |
| | GRM188R71H103K | Murata | | |
| | C1608X7R1H103K | TDK | | |
| D1 | SD103AWS-7 | Diodes Inc[5] | Small Signal Schottky Diode | 1 |
| | SD103AWS | Vishay[6] | | |
| L1 | CDRH104RNP-100 | Sumida[7] | 10µH Inductor, 3.8A Saturation Current | 1 |
| Q1, Q2 | FDS5682 | Fairchild[8] | 60V 7.5A N-Channel MOSFET 26.5mΩ Rds(on) @ 4.5V | 2 |
| R1 | CRCW06032R21FKEA | Vishay Dale | 2.21Ω Resistor, Size 0603, 1% | 1 |
| R2 | CRCW06031R21FKEA | Vishay Dale | 1.21Ω Resistor, Size 0603, 1% | 1 |
| R3 | CRCW060319K6FKEA | Vishay Dale | 19.6kΩ Resistor, Size 0603, 1% | 1 |
| R4 | CRCW060310K0FKEA | Vishay Dale | 10kΩ Resistor, Size 0603, 1% | 1 |
| R5 | CRCW06030000Z0EA | Vishay Dale | 0Ω Resistor, Size 0603, 1% | 1 |
| R6 | CRCW06038K06FKEA | Vishay Dale | 8.06kΩ Resistor, Size 0603, 1% | 1 |
| **U1** | **MIC2174YMM** | **Micrel. Inc.[9]** | **300kHz Buck Controller** | **1** |

**Notes:**

1. EPCOS: www.epcos.com.
2. AVX: www.avx.com.
3. Murata: www.murata.com.
4. TDK: www.tdk.com.
5. Diodes Inc: www.diodes.com.
6. Vishay: www.vishay.com.
7. Sumida: www.sumida.com.
8. Fairchild: www.fairchildsemi.com
9. **Micrel, Inc.: www.micrel.com.**

## PCB Layout

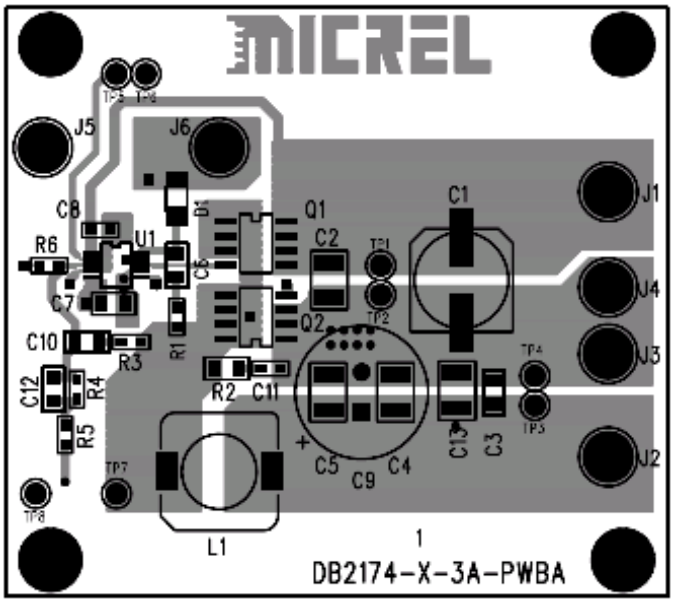



**Figure 11. MIC2174/MIC2174C Evaluation Board Top Layer**

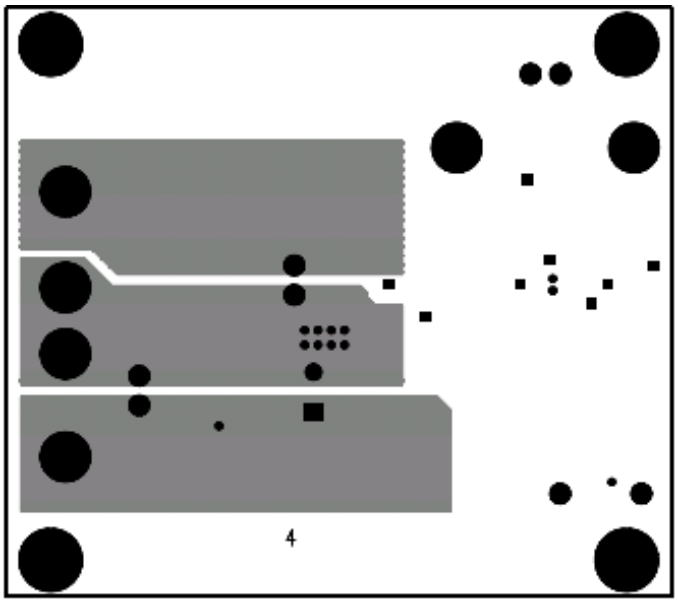


**Figure 12. MIC2174/MIC2174C Evaluation Board Bottom Layer**

## PCB Layout (Continued)

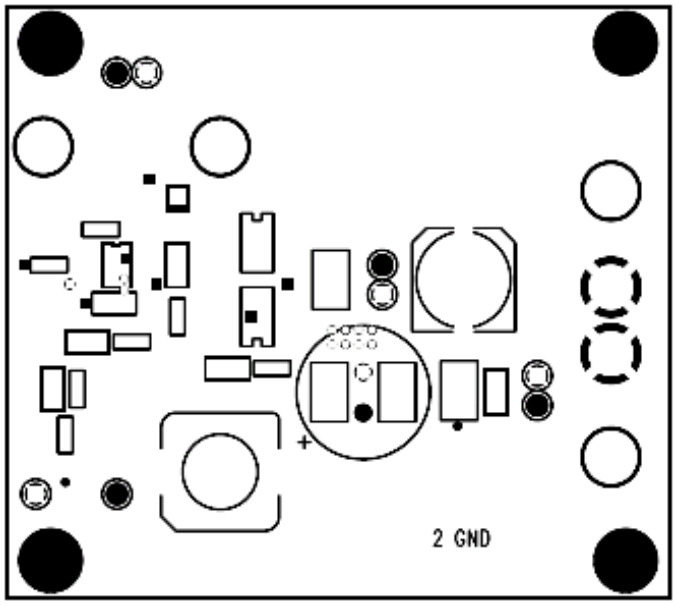



**Figure 13. MIC2174/MIC2174C Evaluation Board Mid-Layer 1**

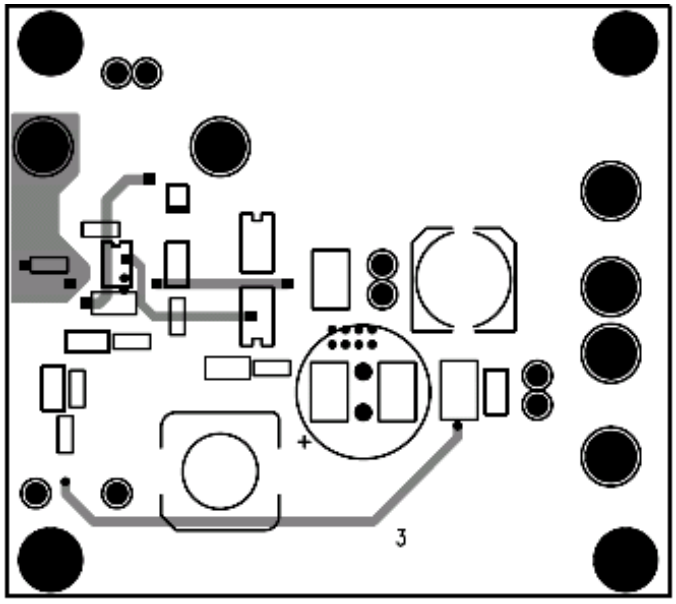
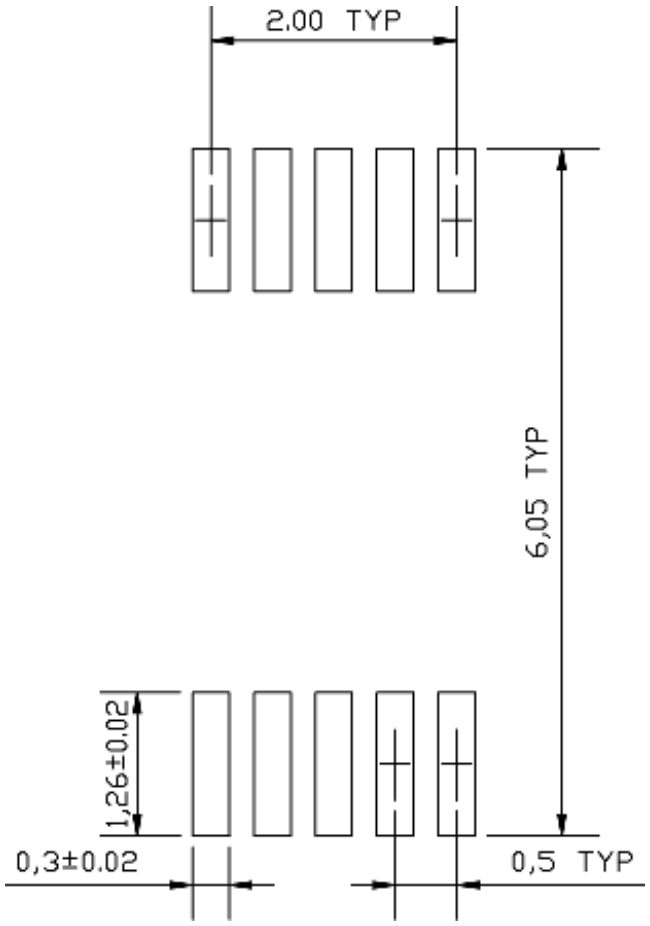


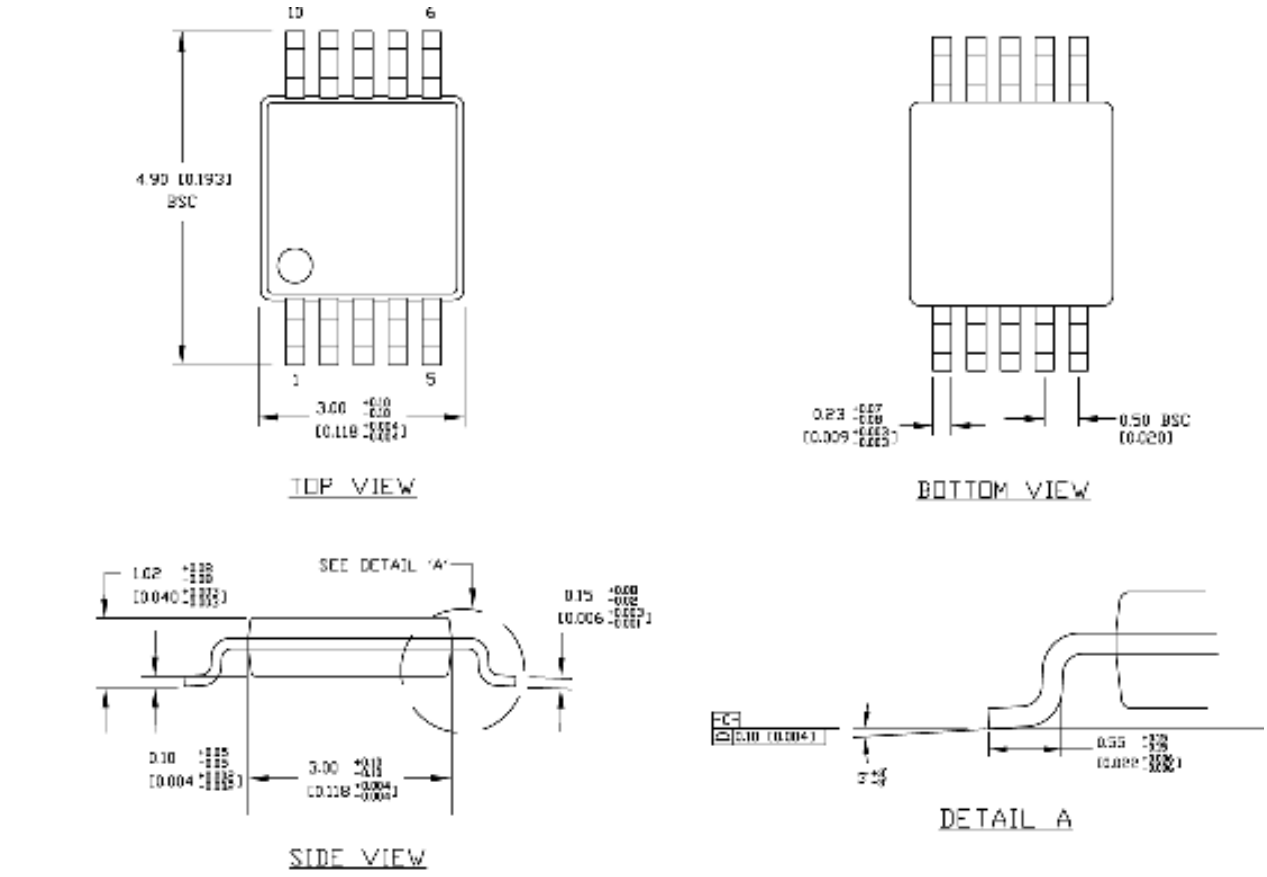

**Figure 14. MIC2174/MIC2174C Evaluation Board Mid-Layer 2**

## Recommended Land Pattern




**10-Pin MSOP (MM)**

## Package Information




NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

**10-Pin MSOP (MM)**

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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