MIC2584/MIC2585

Dual-Channel Hot Swap Controller/Sequencer

General Description

The MIC2584 and MIC2585 are dual-channel positive voltage hot swap controllers designed to facilitate the safe insertion of boards into live system backplanes. The MIC2584 and MIC2585 are available in 16-pin and 24-pin TSSOP packages, respectively. Using a few external discrete components and by controlling the gate drives of external N-Channel MOSFET devices, the MIC2584/85 provides inrush current limiting and output voltage slew rate control in harsh, critical power supply environments. Additionally, the MIC2585 provides output turn-on sequencing and output tracking during turn-on and turn-off. In combination, the devices' many features provide a simplified, robust solution for many network applications to meet the power sequencing and protection requirements of multiple-voltage logic systems.

Features

- 1.0V to 13.2V supply voltage operation
- Surge voltage protection up to 20V
- Current regulation limits inrush current regardless of load capacitance
- Programmable inrush current limiting
- Electronic circuit breaker
- Dual-level overcurrent fault sensing eliminates false tripping
- Fast response to short circuit conditions (< 1µs)
- Two sequenced output mode selections (MIC2585 only)
- Δ250mV supply tracking mode during turn-on/turn-off (MIC2585 only)
- Overvoltage and undervoltage output monitoring (Overvoltage for MIC2585 only)
- Undervoltage lockout protection
- /FAULT status output
- Power-On Reset and Power-Good status output (Power-Good for MIC2585 only)

Applications

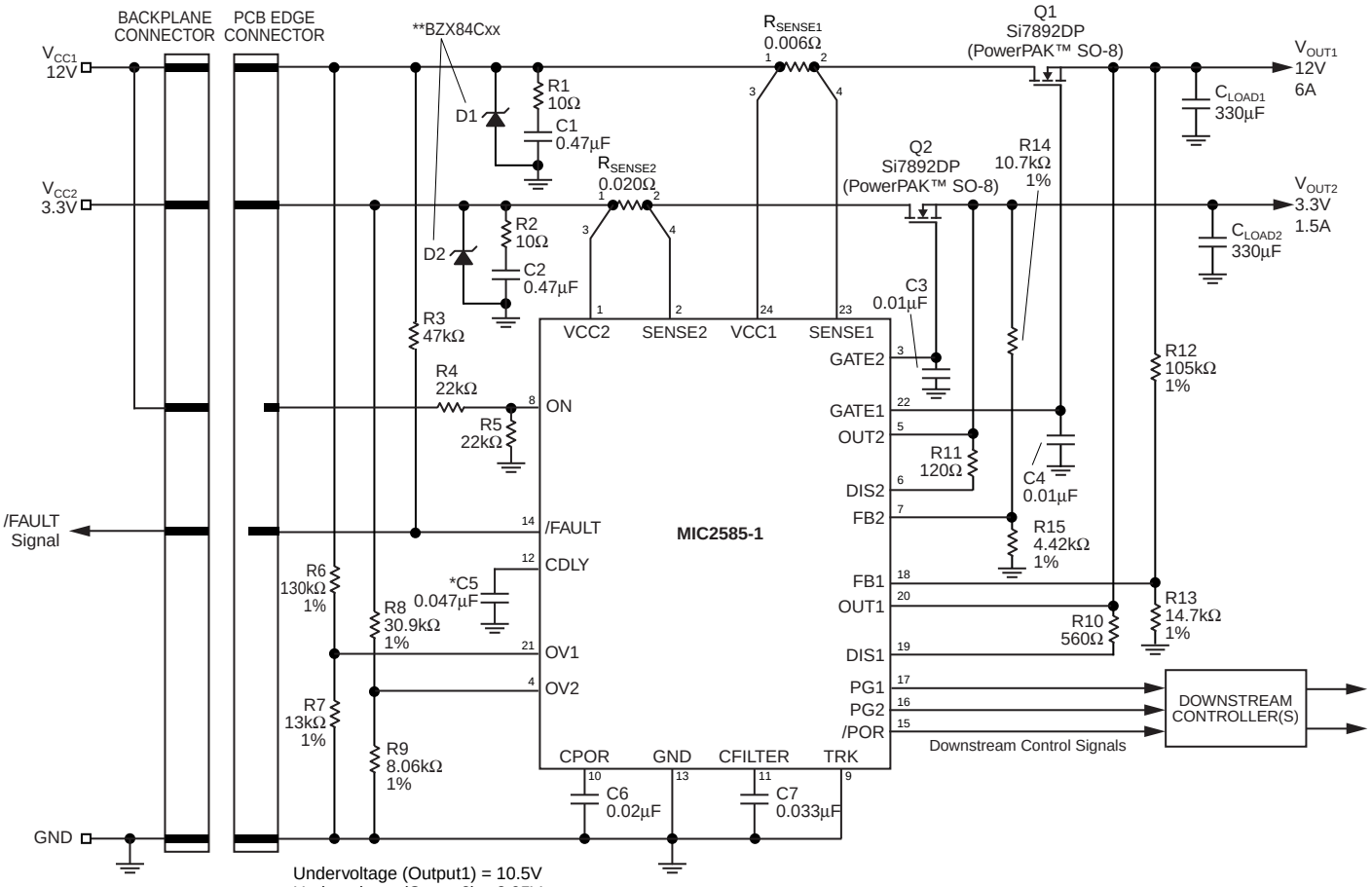
- RAID systems
- Network servers
- Base stations
- Network switches
- Hot-board insertion

Ordering Information

Part Number		Output Sequencing	Fast Circuit Breaker Threshold	Package
Standard	Pb-Free			
MIC2584-xBTS	MIC2584-xYTS	N/A	x = J, 100mV x = K, 150mV *	16-pin TSSOP
MIC2585-1xBTS MIC2585-2xBTS	MIC2585-1xYTS MIC2585-2xYTS	OUT2 follows OUT1 OUT1 follows OUT2	x = L, 200mV * x = M, Off *	24-pin TSSOP

* Contact Micrel for availability.

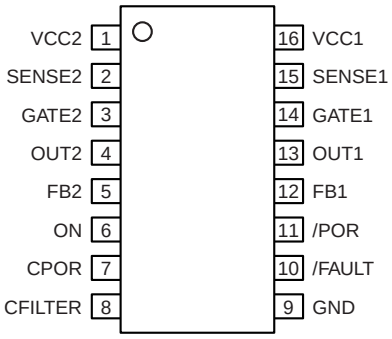
Typical Application



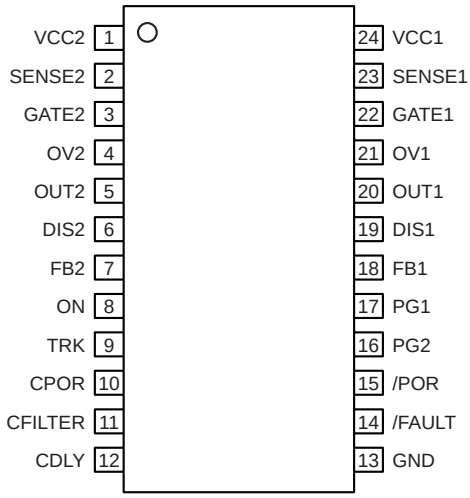
Undervoltage (Output1) = 10.5V
Undervoltage (Output2) = 2.95V
Overvoltage (Input1) = 13.2V
Overvoltage (Input2) = 3.65V
START-UP Delay = 2.5ms
POR Delay = 10ms
Circuit Breaker Response Time = 16ms
*C5 (optional) is used to set the delay for V_{OUT2} with respect to V_{OUT1}
V_{OUT2} Delay = 9.5ms
**D1 is BZX84C18 and D2 is BZX84C8V2
Resistor tolerances are 5% unless specified otherwise.

Figure 1. Typical Application Circuit

Pin Configuration



MIC2584
16-Pin TSSOP (TS)



MIC2585
24-Pin TSSOP (TS)

Pin Description

Pin Number MIC2584	Pin Number MIC2585	Pin Name	Pin Function
16	24	VCC1	Positive Supply (Input), Channel 1: This input is the main supply to the internal circuitry and must be in the range of 2.3V to 13.2V. The GATE1 pin is held low by an internal undervoltage lockout circuit until V_{CC1} and V_{CC2} exceed their respective undervoltage lockout threshold of 2.165V and 0.8V. This input is protected up to 20V.
1	1	VCC2	Positive Supply (Input), Channel 2: The GATE2 pin is held low by an internal undervoltage lockout circuit until V_{CC1} and V_{CC2} exceed their respective undervoltage lockout threshold of 2.165V and 0.8V. This input must be in the range of 1.0V to 13.2V and less than or equal to V_{CC1}. This input is protected up to 20V.
2, 15	2, 23	SENSE2, SENSE1	Circuit Breaker Sense (Inputs): A resistor between this pin and VCC1 and VCC2 sets the current limit threshold for each channel. Whenever the voltage across either sense resistor exceeds the slow trip current limit threshold ($V_{TRIPSLOW}$), the GATE voltage is adjusted to ensure a constant load current. If $V_{TRIPSLOW}$ (50mV) is exceeded for longer than time period t_{OCSLOW}, then the circuit breaker is tripped and both GATE outputs are immediately pulled low. If the voltage across either sense resistor exceeds the fast trip circuit breaker threshold, $V_{TRIPFAST}$, at any point due to fast, high amplitude power supply faults, then both GATE outputs are immediately brought low without delay. To disable the circuit breaker for either channel, the SENSE and VCC pins can be tied together. The default $V_{TRIPFAST}$ for either device is 100mV. Other fast trip thresholds are available: 150mV, 200mV, or OFF ($V_{TRIPFAST}$ disabled). Please contact factory for availability of other options.
6	8	ON	Enable (Input): Active High. The ON pin, an input to a Schmitt-triggered comparator used to enable/disable the controller, is compared to a 1.235V reference with 25mV of hysteresis. When a logic high is applied to the ON pin (V_{ON} > 1.235V), a start-up sequence begins when the GATE1 and GATE2 pins begin ramping up towards their final operating voltage. When the ON pin receives a logic low signal (V_{ON} < 1.21V), the GATE pins are grounded and /FAULT remains high if both inputs are above their respective UVLO thresholds. The ON pin must be low for at least 20µs in order to initiate a start-up sequence. Additionally, toggling the ON pin LOW to HIGH resets the circuit breaker.

Pin Number MIC2584	Pin Number MIC2585	Pin Name	Pin Function
3, 14	3, 22	GATE2, GATE1	Gate Drive (Outputs): Connect each output to the gates of external N-Channel MOSFETs. When ON is asserted, a 14µA current source is activated and begins to charge the gate of the N-Channel MOSFET connected to this pin. An internal clamp ensures that no more than 10V is applied between the GATE and Source when VCC1 or VCC2 is above 5V. When the circuit breaker trips or when an input undervoltage lockout condition is detected, the GATE1 and GATE2 pins are immediately brought low.
9	13	GND	Ground: Tie to analog ground.
7	10	CPOR	Power-On Reset Timer (Input): A capacitor connected between this pin and ground sets the start-up delay (t_{START}) and the power-on reset interval (t_{POR}). Once the lagging supply rises above its UVLO threshold and ON asserts, the capacitor connected to CPOR begins to charge. When the voltage at CPOR crosses 0.3V, the start-up threshold (V_{START}), a start cycle is initiated as the GATE outputs begin to ramp while capacitor C_{POR} is immediately discharged to ground. When the voltage at the lagging FB pin rises above its threshold (V_{FB}), capacitor CPOR begins to charge again. When the voltage at CPOR rises above the power-on reset delay threshold (V_{POR}) of 1.235V, the timer resets by pulling CPOR to ground and /POR is deasserted. If C_{POR} = 0, then t_{START} defaults to 20µs.
8	11	CFILTER	Current Limit Response Timer (Input): A capacitor connected to this pin defines the period of time, t_{OCSLOW}, in which an overcurrent event must last to signal a fault condition and trip the circuit breaker. When an overcurrent condition occurs, a 2.5µA current source begins to charge this capacitor. If the voltage at this pin reaches 1.235V, the circuit breaker is tripped, both GATE pins immediately shut off, and /FAULT is asserted. If C_{FILTER} = 0, then t_{OCSLOW} defaults to 20µs.
5, 12	7, 18	FB2, FB1	Power-Good Threshold Input (Undervoltage Detect): FB1 and FB2 are internally compared to 1.235V and 0.80V references with 25mV of hysteresis, respectively. External resistive divider networks may be used to set the voltage at these pins. If either FB input momentarily goes below its threshold, then /POR is activated for one timing cycle, t_{POR}, indicating an output undervoltage condition. The /POR signal deasserts one timing cycle after the FB pin exceeds its power-good threshold by 25mV. A 5µs filter on these pins prevents glitches from inadvertently activating the /POR signal.
10	14	/FAULT	Circuit Breaker Fault Status (Output): Active-Low, weak pull-up to VCC1 or open-drain. Asserted when the circuit breaker is tripped due to an overcurrent, undervoltage lockout, or overvoltage event. When deasserted, the MIC2585 will initiate a new start cycle by toggling the ON pin.
11	15	/POR	Power-On Reset (Output): Active Low, weak pull-up to VCC1 or open drain. This pin remains asserted during start-up until a time period (t_{POR}) after the lagging FB pin threshold (V_{FB1} or V_{FB2}) is exceeded. The timing capacitor C_{POR} determines t_{POR}. When the output voltage monitored at either FB pin falls below V_{FB}, /POR is asserted for a minimum of one timing cycle (t_{POR}).
4, 13	5, 20	OUT2, OUT1	Output Voltage Monitor (Inputs): For output tracking, connect these pins to their respective output to sense the output voltage.
N/A	12	CDLY	Output Sequence Delay Timer (Input): This pin is internally clamped to 6V. A capacitor connected to this pin sets a timer delay, t_{DLY}, between V_{OUT1} and V_{OUT2} as shown in Figure 5. With this pin pulled up to VCC1 through a resistor, and if $C_{GATE1} = C_{GATE2}$, both V_{OUT1} and V_{OUT2} ramp up and down with the same dv/dt as depicted in the Tracking Mode diagram while maintaining a maximum voltage differential between V_{OUT1} and V_{OUT2}.
N/A	9	TRK	Discharge Tracking Mode Pin (Input): Tie this pin to OUT1 or OUT2 to enable tracking during turn-off cycle. Ground this pin to disable tracking during turn-off. The TRK pin is not to be used as a digital input.

Pin Number MIC2584	Pin Number MIC2585	Pin Name	Pin Function
N/A	4, 21	OV2, OV1	Overvoltage Detect Inputs: Whenever the threshold voltage (V_{OV1}, V_{OV2}) on either input is exceeded, the circuit-breaker is tripped while /FAULT is asserted and the GATE1 and GATE2 outputs are immediately brought low.
N/A	6, 19	DIS2, DIS1	Discharge Outputs: When the ON pin receives a logic low signal (deasserts), these pins provide a low impedance path to ground in order to allow the discharging of any load capacitance. The DIS pins assert low if TRK is less than 0.3V once ON has been deasserted. The typical DIS pin resistance varies between 50Ω to 170Ω dependent upon input supply voltage (see Electrical Table). An external resistor is required. See "*Fast Output Discharge for Capacitive Load*" section in the Applications Information for more detail.
N/A	16, 17	PG2, PG1	Power-Good Outputs: Active-HIGH, weak pull-up to VCC1 or open-drain. These outputs are asserted whenever the FB1 and FB2 thresholds are exceeded and will not be asserted when FB1 and FB2 are below their thresholds.

Absolute Maximum Ratings (Note1)

All voltages are referred to GND)

Supply Voltage (V_{CC1}/V_{CC2}) ..... –0.3V to 20V
SENSE1/SENSE2 pins ..... –0.3V to $V_{CC1/2}$
TRK, ON, DIS1, DIS2, OUT1, OUT2, /POR, /FAULT, PG1, PG2 pins ..... –0.3V to 15V
GATE1/GATE2 pin ..... –0.3V to 25V
All other input pins ..... -0.3V to 15V
DIS1/DIS2 current ..... ±25mA
Junction Temperature ..... 125°C
ESD Rating
Human body model 1500V
Machine model 100V

Operating Ratings (Note 2)

Supply Voltage
V_{CC1} ..... 2.3V to 13.2V
V_{CC2} ..... 1.0V to 13.2V
Operating Temperature Range ..... –40°C to +85°C
Package Thermal Resistance
$R_{\theta(JA)}$, 16-pin TSSOP ..... 99.1°C/W
$R_{\theta(JA)}$, 24-pin TSSOP ..... 83.8°C/W

Electrical Characteristics (Note 4)

2.3V ≤ V_{CC1} ≤ 13.2V, 1.0V ≤ V_{CC2} ≤ 13.2V, T_A = 25°C unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ 85°C.

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			2.3		13.2	V
I_{CC1}	Supply Current				1.7	**3**	mA
V_{CC2}	Supply Voltage	$V_{CC2} \le V_{CC1}$		1.0		13.2	V
I_{CC2}	Supply Current				0.05	**0.15**	mA
V_{UV1}	V_{CC1} Undervoltage Lockout Threshold			**2.050**	2.165	**2.275**	V
V_{UV1HYS}	V_{CC1} Undervoltage Lockout Hysteresis				200		mV
V_{UV2}	V_{CC2} Undervoltage Lockout Threshold			**0.7**	0.8	**0.9**	V
V_{UV2HYS}	V_{CC2} Undervoltage Lockout Hysteresis				30		mV
$V_{TRIPSLOW}$	Slow Trip Overcurrent Threshold	$V_{CCx} - V_{SENSEx}$, $V_{CC1} = V_{CC2}$ = 5V		**42.5**	50	**57.5**	mV
$V_{TRIPHYS}$	Slow Trip Overcurrent Hysteresis				2.5		mV
$V_{TRIPFAST}$	Fast Trip Overcurrent Threshold	$V_{CC1} = V_{CC2}$ = 5V	x = J	**90**	100	**110**	mV
			x = K		150		mV
			x = L		200		mV
V_{GATE}	External Gate Drive (GATE1 and GATE2)	$V_{GATEx} - V_{CCx}$	V_{CC1} or V_{CC2} > 5V	**6**	8	**10**	V
			V_{CC1} or V_{CC2} < 5V	**3.5**	4.5	**8**	V
I_{GATE}	GATE Pin Pull-up Current	Start cycle		**–25**	–14	**–8**	µA
$I_{GATEOFF}$	GATE Pin Sink Current	/FAULT asserted			50		mA
		Turn off (ON deasserted)		**30**	45	**70**	µA
R_{DIS}	Discharge Pin Resistance	ON deasserted TRK < 0.3V	V_{CCx} = 2.3V		170		Ω
			V_{CCx} = 5.0V		70		Ω
			V_{CCx} = 13.2V		50		Ω
I_{TMR}	Overcurrent Timer Pin Charge Current	$V_{CCx} - V_{SENSEx}$ = 50mV		**–3.5**	–2.5	**–1.5**	µA
	Overcurrent Timer Pin Discharge Current	$V_{CCx} - V_{SENSEx}$ = 25mV		**1.5**	2.5	**3.5**	µA
V_{TMR}	Overcurrent Timer Pin Threshold			**1.190**	1.235	**1.290**	V

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CPOR}	Power-on Reset Current	V_{CC1} = 5V, C_{POR} = 0.5V	Charge current	**–3.5**	–2.5	**–1.5**	µA
			Sink current		2.5		
V_{POR}	Power-on Reset Delay Threshold	Start-up cycle		**1.190**	1.235	**1.290**	V
V_{PORHYS}	Power-on Reset Delay Threshold Hysteresis				25		mV
V_{START}	Start-up Threshold	Start-up cycle		**0.25**	0.30	**0.35**	V
V_{TRK}	TRK Pin Threshold (MIC2585 only)	ON deasserted, I_{GATE} > 10µA V_{CC1} = V_{CC2} = 5V		0.25	0.30	0.35	V
V_{TRKOFF}	TRK Pin Turn-off Voltage (MIC2585 only)	ON asserted, V_{SENSE2} – V_{OUT2} V_{CC1} = V_{CC2} = 5V		150	250	400	mV
V_{FB1}	FB1 Threshold			**1.190**	1.235	**1.290**	V
V_{FB1HYS}	FB1 Threshold Hysteresis				25		mV
V_{FB2}	FB2 Threshold			**0.75**	0.80	**0.85**	V
V_{FB2HYS}	FB2 Threshold Hysteresis				25		mV
V_{OV1}	OV1 Threshold (MIC2585 only)			**1.190**	1.235	**1.290**	V
V_{OV1HYS}	OV1 Threshold Hysteresis (MIC2585 only)				25		mV
V_{OV2}	OV2 Threshold (MIC2585 only)			**0.75**	0.80	**0.85**	V
V_{OV2HYS}	OV2 Threshold Hysteresis (MIC2585 only)				25		mV
I_{DELAY}	Delay Timer Pin Current	V_{CC1} = V_{CC2} = 5V	Timer charge current	**–9**	–6	**–3**	µA
	(MIC2585 only)		Timer discharge current		200		
V_{DELAY}	Delay Timer Pin Threshold (MIC2585 only)			**1.190**	1.235	**1.290**	V
V_{DLYHYS}	Delay Timer Pin Threshold Hysteresis (MIC2585 only)				25		mV
V_{ON}	ON Pin Input Threshold			**1.190**	1.235	**1.290**	V
V_{ONHYS}	ON Pin Hysteresis				25		mV
I_{ON}	ON Pin Input Current	V_{ON} = V_{CCX}			0.1	**0.5**	µA
V_{OL}	/FAULT , /POR , PG1, PG2 Output Low Voltage (PG1 and PG2 for MIC2585 only)	I_{OUT} = 1.6mA, V_{CC1} = 5V				**0.4**	V
I_{PULLUP}	/FAULT , /POR , PG1, PG2 Active Output Pull-up Current (PG1 and PG2 for MIC2585 only)	ON asserted, V_{FB1} > 1.25V, V_{FB2} > 0.8V /POR = V_{CC1} – 1V		**7**	12	**22**	µA
$V_{GATEWIN}$	GATE1 and GATE2 ON/OFF Voltage Window (Tracking enabled) **Note 3**	See Timing Diagram (Figure 2)			100	**250**	mV
AC Parameters							
t_{OCFAST}	Fast Overcurrent Sense to GATE Low Trip Time	V_{CCx} – V_{SENSEx} = 100mV, C_{GATE} = 10nF See Timing Diagram (Figure 3)			1		µs
t_{OCSLOW}	Slow Overcurrent Sense to GATE Low Trip Time	V_{CCx} – V_{SENSEx} = 50mV, C_{FILTER} = 0			20		µs

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. For the MIC2584, $V_{GATEWIN}$ is specified only when ON is asserted.

Note 4. Specification for packaged product only.

Timing Diagrams

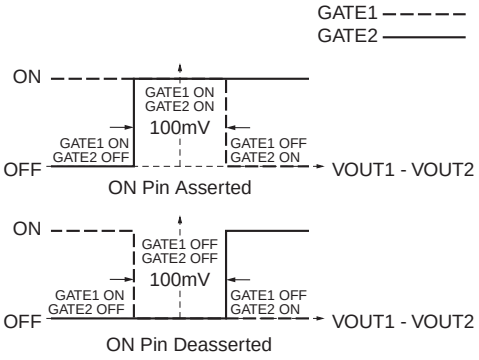


Figure 2. Gate Voltage Window — Tracking Mode

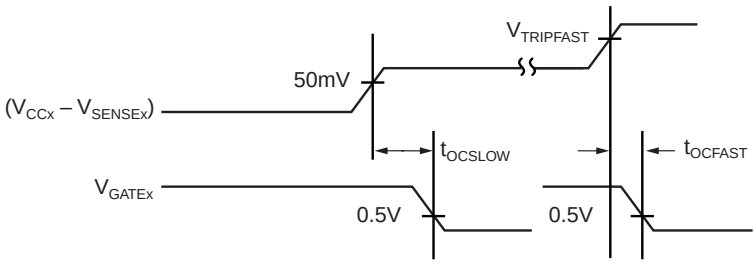


Figure 3. Current Limit Response

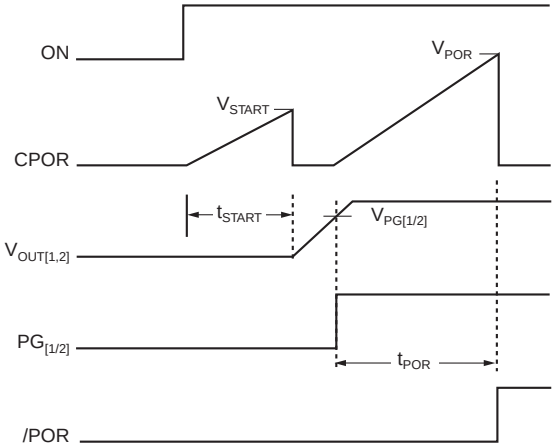


Figure 4. Start-Up Cycle Timing

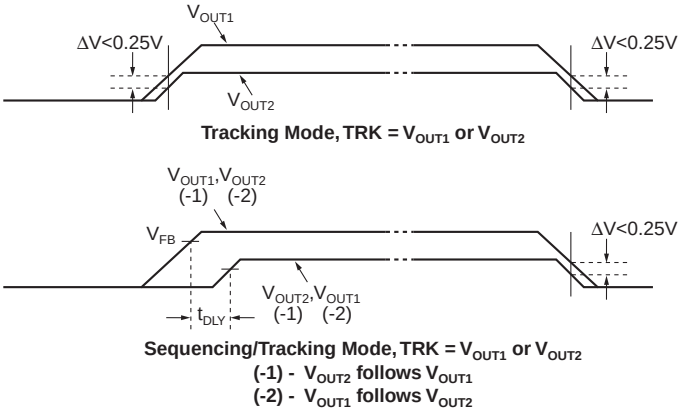
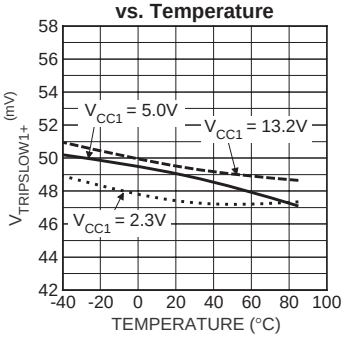


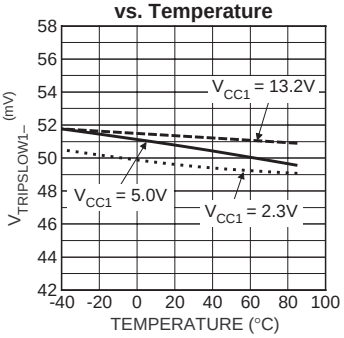
Figure 5. Sequencing Modes (MIC2585 only)

Typical Characteristics

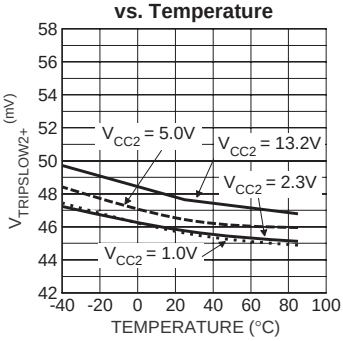
$V_{TRIPSLOW1+}$ vs. Temperature



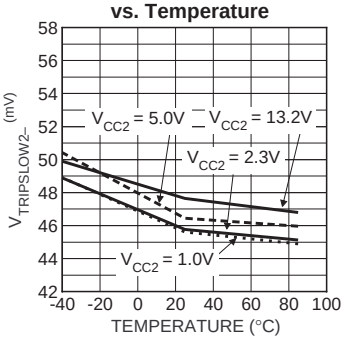
$V_{TRIPSLOW1-}$ vs. Temperature



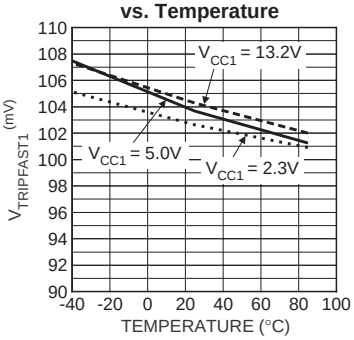
$V_{TRIPSLOW2+}$ vs. Temperature



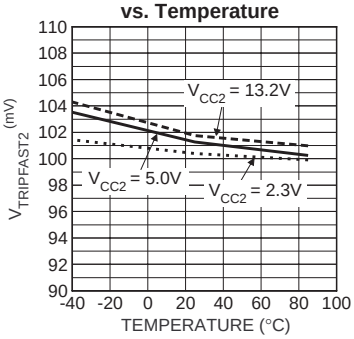
$V_{TRIPSLOW2-}$ vs. Temperature



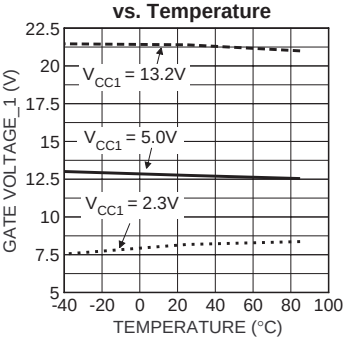
$V_{TRIPFAST1}$ vs. Temperature



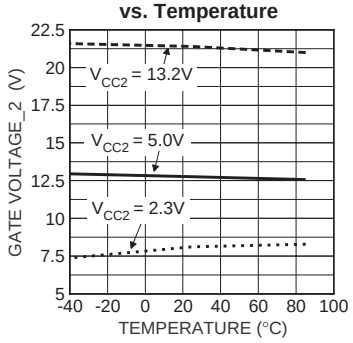
$V_{TRIPFAST2}$ vs. Temperature



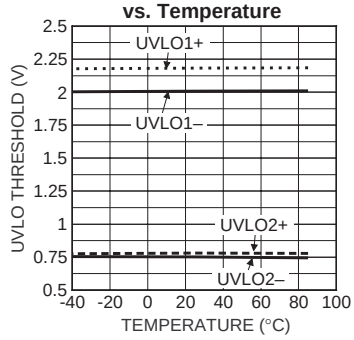
V_{GATE1} vs. Temperature



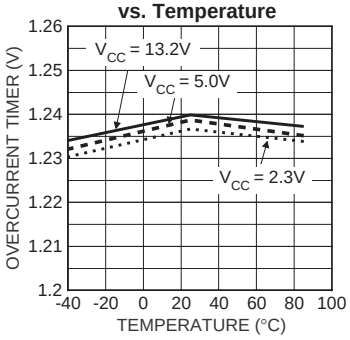
V_{GATE2} vs. Temperature



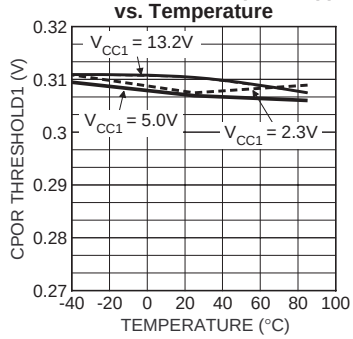
UVLO1 and UVLO2 vs. Temperature



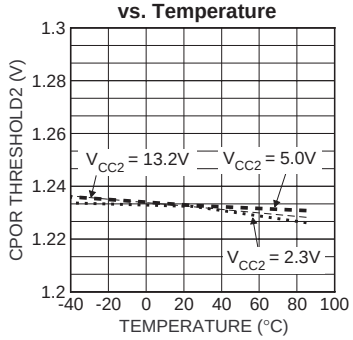
Overcurrent Timer Threshold vs. Temperature



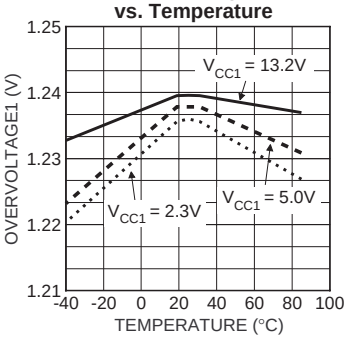
CPOR Threshold1 (Start-Up) vs. Temperature



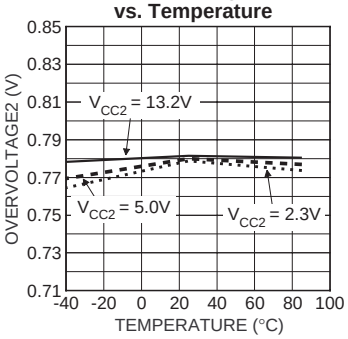
CPOR Threshold2 vs. Temperature



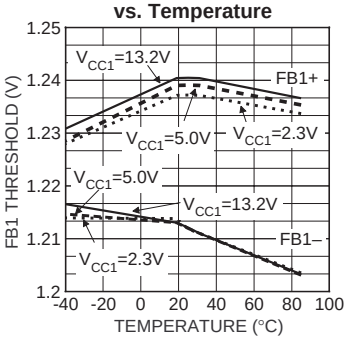
Overvoltage1 vs. Temperature



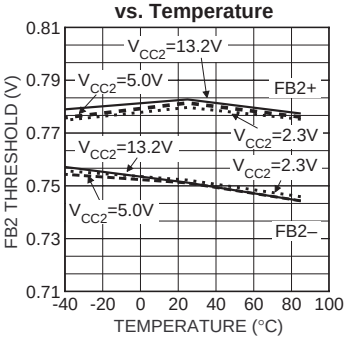
Overvoltage2 vs. Temperature



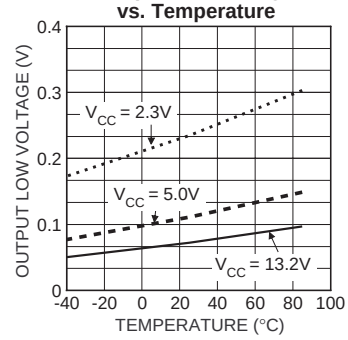
FB1 Threshold vs. Temperature



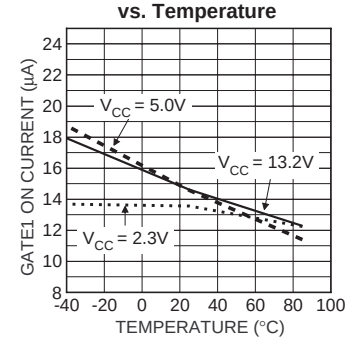
FB2 Threshold vs. Temperature



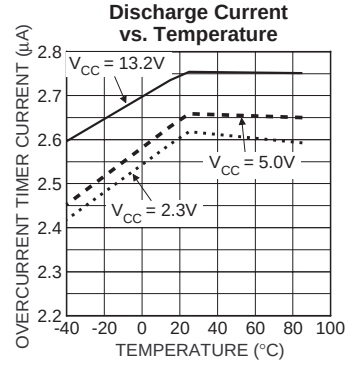
Output Low Voltage vs. Temperature



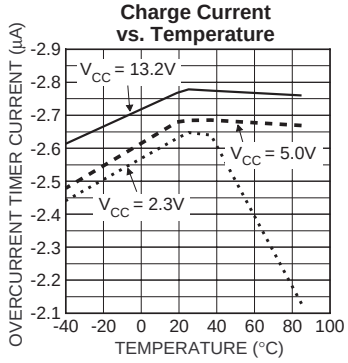
Gate1 On Current vs. Temperature



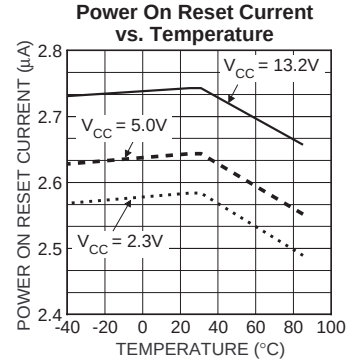
Overcurrent Timer Discharge Current vs. Temperature



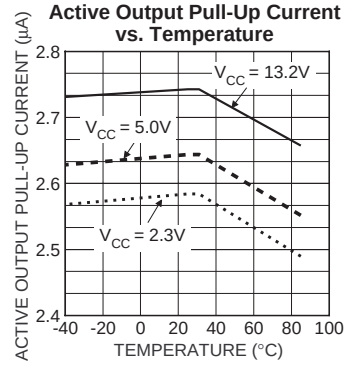
Overcurrent Timer Charge Current vs. Temperature



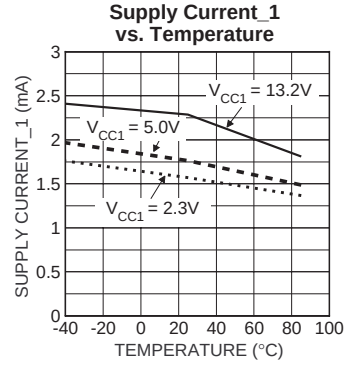
Power On Reset Current vs. Temperature



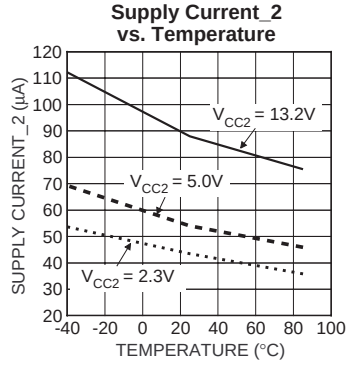
Active Output Pull-Up Current vs. Temperature



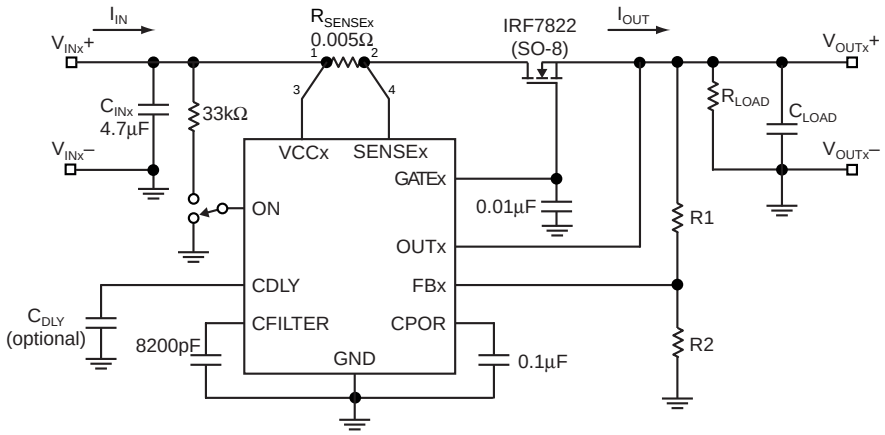
Supply Current_1 vs. Temperature



Supply Current_2 vs. Temperature



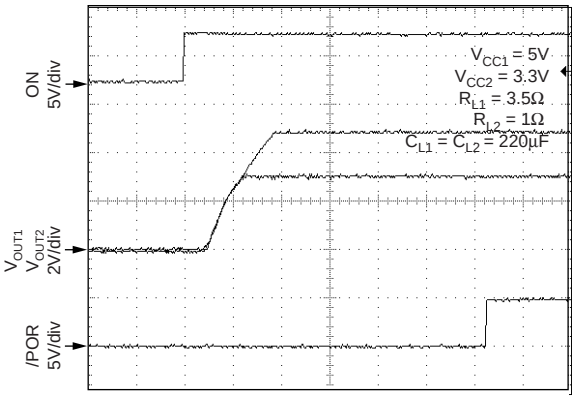
Test Circuit



(Not all pins shown for simplicity)

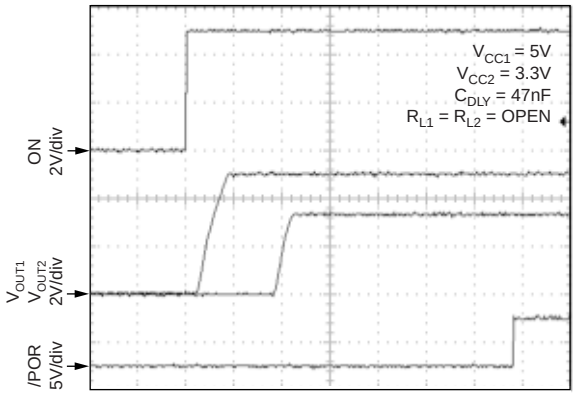
Functional Characteristics

Turn-On (No Delay)



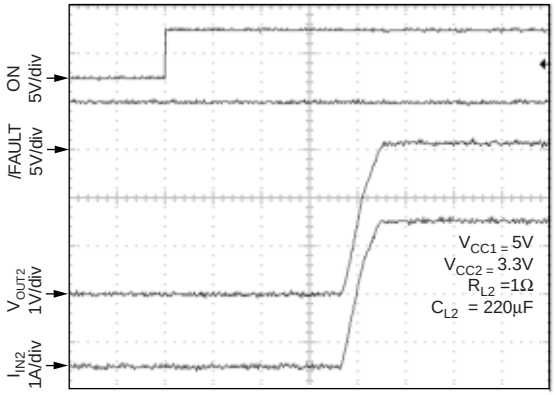
TIME (5ms/div.)

Turn-On, Staggered Mode (MIC2585-1BTS)



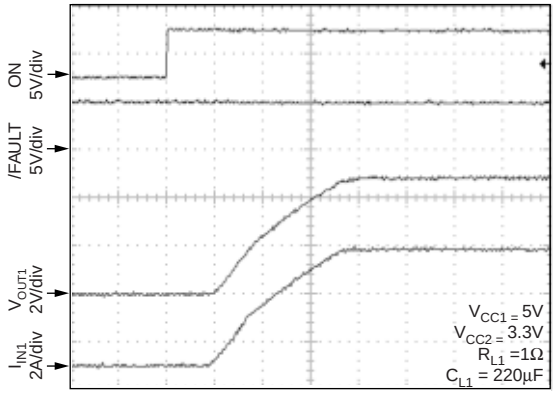
TIME (10ms/div.)

Turn-On (Channel 2)



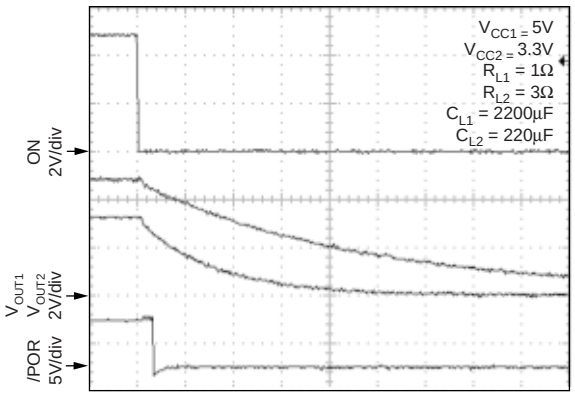
TIME (5ms/div.)

Turn-On (Channel 1)



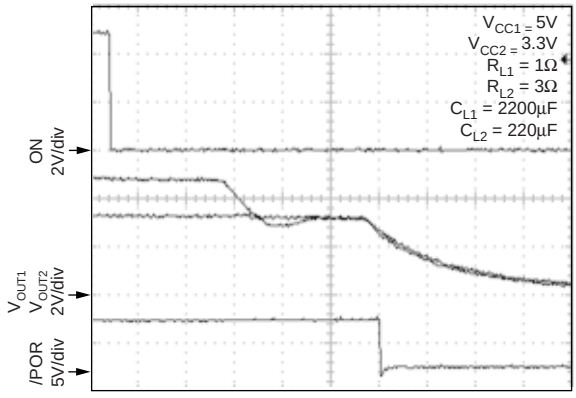
TIME (2.5ms/div.)

Turn-Off (Tracking Off)



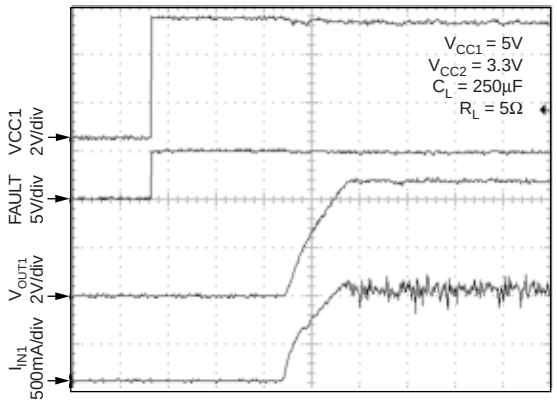
TIME (500µs/div.)

Turn-Off (Tracking On)

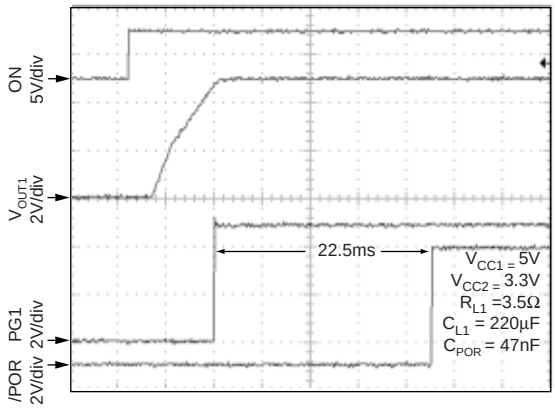


TIME (1ms/div.)

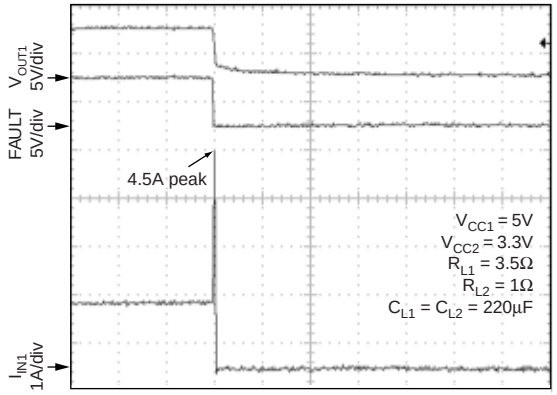
Turn-On Response (Hot Insert)



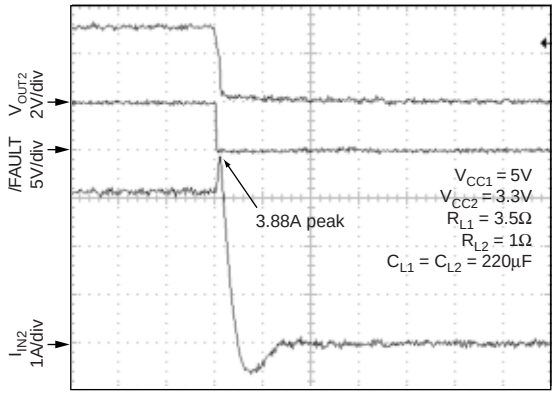
Power-On Reset Response



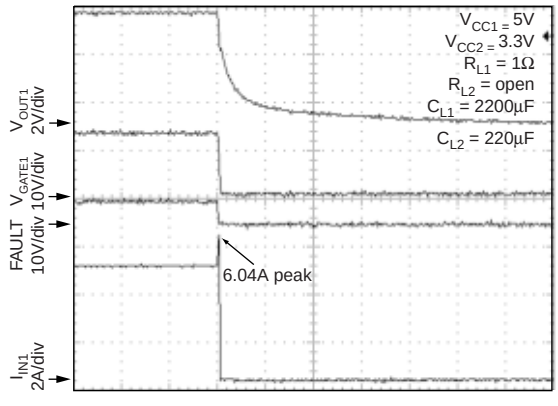
Short-Circuit Crowbar Channel 1
(SCR enabled through a PNP from DIS pin-MIC2585-1BTS)



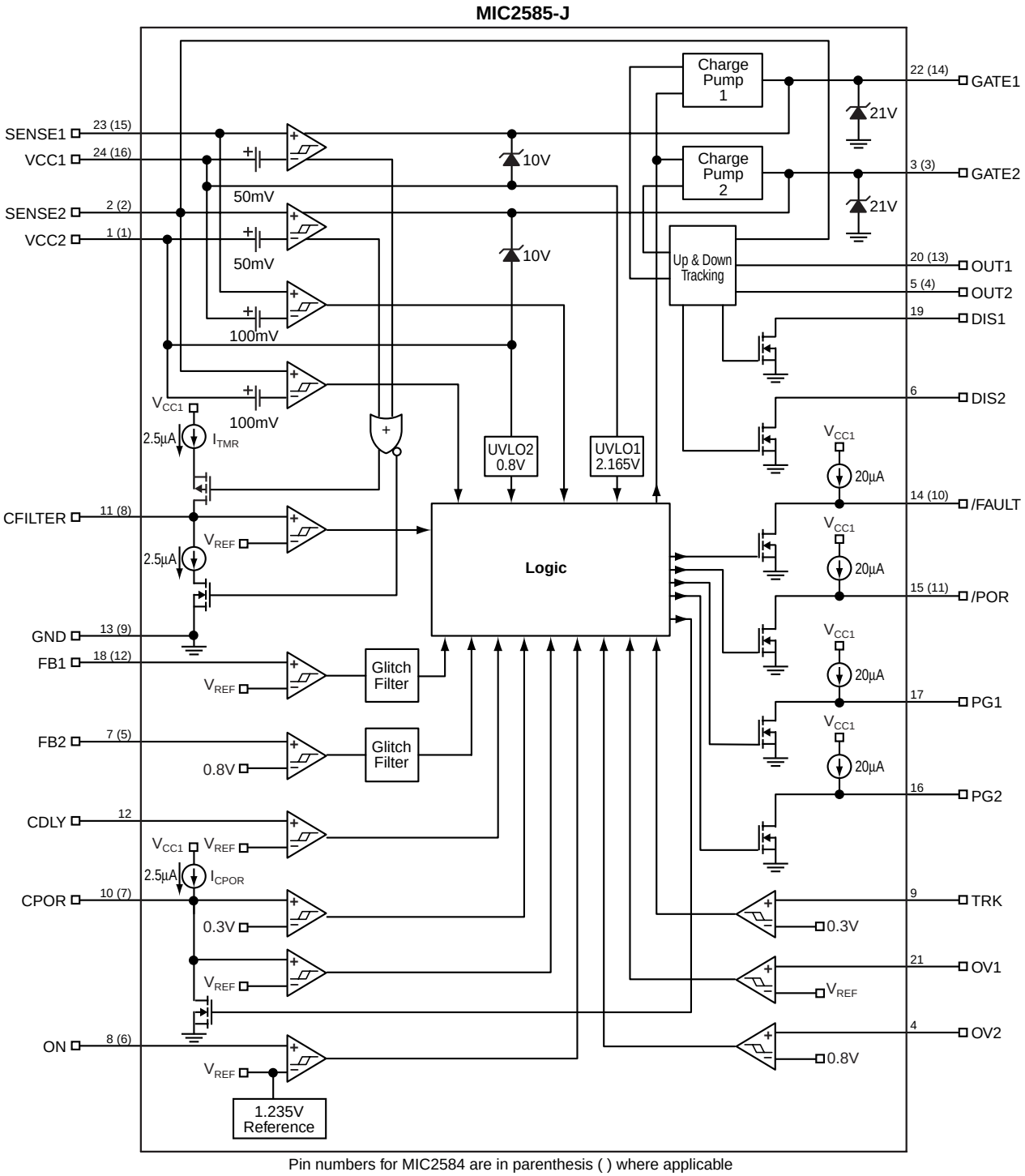
Short-Circuit Crowbar Channel 2
(SCR enabled through a PNP from DIS pin-MIC2585-1BTS)



Short-Circuit Response



Functional Diagram



Pin numbers for MIC2584 are in parenthesis ( ) where applicable

Functional Description

Hot Swap Insertion

When circuit boards are inserted into live system backplanes and supply voltages, high inrush currents can result due to the charging of bulk capacitance that resides across the supply pins of the circuit board. This inrush current, although transient in nature, may be high enough to cause permanent damage to on-board components or may cause the system's supply voltages to go out of regulation during the transient period which may result in system failures. The MIC2584 and MIC2585 act as a controller for external N-Channel MOSFET devices in which the gate drive is controlled to provide inrush current limiting and output voltage slew rate control during hot swap insertions.

Power Supply

VCC1 is the main supply input to the MIC2584/85 controller with a voltage range of 2.3V to 13.2V. The VCC2 supply input ranges from 1.0V to 13.2V and must be less than or equal to VCC1 for operation. Both inputs can withstand transient spikes up to 20V. In order to ensure stability of the supplies, a minimum 1µF capacitor from each VCC to ground is recommended. Alternatively, a low pass filter, shown in the typical application circuit, can be used to eliminate high frequency oscillations as well as help suppress transient spikes.

Also, due to the existence of undetermined parasitic inductance in the absence of bulk capacitance, placing a Zener diode at each VCC of the controller to ground in order to provide external supply transient protection is strongly recommended. See the typical application circuit in Figure 1.

Start-Up Cycle

Supply Contact Delay

During a hot insert of a PC board into a backplane or when the main supply (VCC1) is powered up from a cold start, as the voltage at the ON pin rises above its threshold (1.235V typical), the MIC2584/85 first checks that both supply voltages are above their respective UVLO thresholds. If so, then the device is enabled and an internal 2.5µA current source begins charging capacitor C_{POR} to 0.3V to initiate a start-up sequence. Once the start-up delay (t_{START}) elapses, the CPOR pin is pulled immediately to ground and a separate 14µA current source begins charging each GATE output to drive the external MOSFET that switches V_{IN} to V_{OUT}. The programmed contact start-up delay is calculated using the following equation:

$$t_{START} = C_{POR} \times \frac{V_{START}}{I_{CPOR}} \cong 0.12 \times C_{POR}\ (\mu F) \quad (1)$$

where the start-up delay timer threshold (V_{START}) is 0.3V, and the Power-On Reset timer current (I_{CPOR}) is 2.5µA. See Table 2 for some typical supply contact start-up delays using several standard value capacitors. As each GATE voltage continues ramping toward its final value (V_{CC} + V_{GS}) at a defined slew rate (See Load Capacitance/Gate Capacitance Dominated Start-Up sections), a second CPOR timing cycle begins if: 1)/FAULT is high and 2)CFILTER is low (i.e., not an overvoltage, undervoltage lockout, or overcurrent state). This second timing cycle (t_{POR}) begins when the lagging voltage exceeds its FB pin threshold (V_{FB}). See Figure 4 in the "*Timing Diagrams*". When the power supply is already present (i.e., not a "hot swapping" condition) and the MIC2584/85 device is enabled by applying a logic high signal at the ON pin, the GATE outputs begin ramping immediately as the first CPOR timing cycle is bypassed. Active current regulation is employed to limit the inrush current transient response during start-up by regulating the load current at the programmed current limit value (See "*Current Limiting and Dual-Level Circuit Breaker*" section). The following equation is used to determine the nominal current limit value:

$$I_{LIM} = \frac{V_{TRIPSLOW}}{R_{SENSE}} = \frac{50mV}{R_{SENSE}} \quad (2)$$

where $V_{TRIPSLOW}$ is the current limit slow trip threshold found in the electrical table and R_{SENSE} is the selected value that will set the desired current limit. There are two basic start-up modes for the MIC2584/85: 1)Start-up dominated by load capacitance and 2)start-up dominated by total gate capacitance. The magnitude of the inrush current delivered to the load will determine the dominant mode. If the inrush current is greater than the programmed current limit (I_{LIM}), then load capacitance is dominant. Otherwise, gate capacitance is dominant. The expected inrush current may be calculated using the following equation:

$$INRUSH \cong I_{GATE} \times \frac{C_{LOAD}}{C_{GATE}} \cong 14\mu A \times \frac{C_{LOAD}}{C_{GATE}} \quad (3)$$

where I_{GATE} is the GATE pin pull-up current, C_{LOAD} is the load capacitance, and C_{GATE} is the total GATE capacitance (C_{ISS} of the external MOSFET and any external capacitor connected from the MIC2584/85 GATE pin to ground).

Load Capacitance Dominated Start-Up

In this case, the load capacitance (C_{LOAD}) is large enough to cause the inrush current to exceed the programmed current limit but is less than the fast-trip threshold (or the fast-trip threshold is disabled, 'M' option). During start-up under this condition, the load current is regulated at the programmed current limit value (I_{LIM}) and held constant until the output voltage rises to its final value. The output slew rate and equivalent GATE voltage slew rate is computed by the following equation:

$$\text{Output Voltage Slew Rate, } dV_{OUT}/dt = \frac{I_{LIM}}{C_{LOAD}} \quad (4)$$

where I_{LIM} is the programmed current limit value. Consequently, the value of C_{FILTER} must be selected to ensure that the overcurrent response time, t_{OCSLOW}, exceeds the time needed for the output to reach its final value. For example, given a MOSFET with an input capacitance C_{ISS} = C_{GATE} = 2000pF, C_{LOAD} is 1000µF, and I_{LIM} is set to 5A with a 12V input, then the load capacitance dominates as determined by the calculated INRUSH > I_{LIM}. Therefore, the output voltage slew rate determined from Equation 4 is:

$$\text{Output Voltage Slew Rate, } (dV_{OUT}/dt) = \frac{5A}{100\mu F} = 5\frac{V}{ms}$$

and the resulting t_{OCSLOW} needed to achieve a 12V output is approximately 2.5ms. (See "*Power-On Reset, Overcurrent Timer, and Sequenced Output Delays*" section to calculate t_{OCSLOW}).

GATE Capacitance Dominated Start-Up

In this case, the value of the load capacitance relative to the GATE capacitance is small enough such that during start-up the output current never exceeds the current limit threshold as determined by Equation 3. The minimum value of C_{GATE} that will ensure that the current limit is never exceeded is given by the equation below:

$$C_{GATE}(Min) = \frac{I_{GATE}}{I_{LIMIT}} \times C_{LOAD}$$

Where C_{GATE} is the summation of the MOSFET input capacitance (C_{ISS}) specification and the value of the capacitor connected to the GATE pin of the MIC2584/85 (and MOSFET) to ground. Once C_{GATE} is determined, use the following equation to determine the output slew rate dV_{OUT}/dt for gate capacitance dominated start-up:

$$dV_{OUT}/dt = \frac{I_{GATE}}{C_{GATE}}$$

Table 1 depicts the output slew rate for various values of C_{GATE}.

I_{GATE} = 14µA	
C_{GATE}	**dV_{OUT}/dt**
0.001µF	14V/ms
0.01µF	1.4V/ms
0.1µF	0.14V/ms
1µF	0.014V/ms

Table 1. Output Slew Rate Selection for GATE Capacitance Dominated Start-Up

Current Limiting and Dual-Level Circuit Breaker

Many applications will require that the inrush and steady state supply current be limited at a specific value in order to protect critical components within the system. Connecting a sense resistor between the VCC and SENSE pins of each channel sets the nominal current limit value for each channel of the MIC2584/85 and the current limit is calculated using Equation 2.

The MIC2584/85 also features a dual-level circuit breaker triggered via 50mV and 100mV current limit thresholds sensed across the VCC and SENSE pins. The first level of the circuit breaker functions as follows. For the MIC2584/85, once the voltage sensed across these two pins exceeds 50mV on either channel, the overcurrent timer, its duration set by capacitor C_{FILTER}, starts to ramp the voltage at CFILTER using a 2.5µA constant current source. If the voltage at CFILTER reaches the overcurrent timer threshold (V_{TMR}) of 1.235V, then CFILTER immediately returns to ground as the circuit breaker trips and both GATE outputs are immediately shut down. For the second level, if the voltage sensed across VCC and SENSE of either channel exceeds 100mV (–J option) at any time, the circuit breaker trips and both GATE outputs shut down immediately, bypassing the overcurrent timer period. To disable current limit and circuit breaker operation, tie each channel's SENSE and VCC pins together and the CFILTER pin to ground.

Output Undervoltage Detection

The MIC2584/85 employ output undervoltage detection by monitoring the output voltage through a resistive divider connected at the FB pins. During turn on, while the voltage at either FB pin is below its threshold (V_{FB}), the /POR pin is asserted low. Once both FB pin voltages cross their respective threshold (V_{FB}), a 2.5µA current source charges capacitor C_{POR}. Once the CPOR pin voltage reaches 1.235V, the time period t_{POR} elapses as pin CPOR is pulled to ground and the /POR pin goes HIGH. If the voltage at either FB drops below V_{FB} for more than 10µs, the /POR pin resets for at least one timing cycle defined by t_{POR} (See "*Applications Information*" for an example).

Input/Output Overvoltage Protection

The MIC2585 monitors and detects overvoltage conditions in the event of excessive supply transients at the MIC2585 input(s)/output(s). Whenever the voltage threshold is exceeded at either OV1 or OV2 of the MIC2585, the circuit breaker is tripped and both GATE outputs are immediately brought low.

Power-On Reset, Overcurrent Timer, and Sequenced Output Delays

The Power-On Reset delay, t_{POR}, is the time period for the /POR pin to go HIGH once the lagging voltage exceeds the power-good threshold (V_{FB}) monitored at the FB pin. A capacitor connected to CPOR sets the interval and is determined by using Equation 1 with V_{POR} substituted for V_{START}. The resulting equation becomes:

$$t_{POR} = C_{POR} \times \frac{V_{POR}}{I_{CPOR}} \cong 0.5 \times C_{POR}(\mu F) \quad (7)$$

where the Power-On Reset threshold (V_{POR}) and timer current (I_{CPOR}) are typically 1.235V and 2.5µA, respectively.

For the MIC2584/85, a capacitor connected to CFILTER is used to set the timer which activates the circuit breaker during overcurrent conditions. When the voltage across either sense resistor exceeds the slow trip current limit threshold of 50mV, the overcurrent timer begins to charge for a period, t_{OCSLOW}, determined by C_{FILTER}. If t_{OCSLOW} elapses, then the circuit breaker is activated and both GATE outputs are immediately pulled to ground. The following equation is used to determine the overcurrent timer period, t_{OCSLOW}.

$$t_{OCSLOW} = C_{FILTER} \times \frac{V_{TMR}}{I_{TMR}} \cong 0.5 \times C_{FILTER}(\mu F) \quad (8)$$

where V_{TMR}, the overcurrent timer threshold, is 1.235V and I_{TMR}, the overcurrent timer current, is 2.5µA. If no capacitor for CFILTER is used, then t_{OCSLOW} defaults to 20µs.

The sequenced output feature is enabled for the MIC2585 by placing a capacitor from CDLY to ground. The –1 option allows for V_{OUT2} to follow V_{OUT1} and the –2 option allows for V_{OUT1} to follow V_{OUT2} during start-up (See "*Timing Diagrams, Figure 5*"). The sequenced output delay time is determined using the following equation:

$$t_{DLY} \cong C_{DLY} \times \frac{V_{DELAY}}{I_{DELAY}} \cong 0.2 \times C_{DLY}(\mu F) \qquad (9)$$

where V_{DELAY}, the CDLY pin threshold, is typically 1.235V, I_{DELAY}, the CDLY pin charge current, is typically 6µA, and C_{DLY} is the capacitor connected to CDLY. Tables 2, 3, and 4 provide a quick reference for several timer calculations using select standard value capacitors.

Undervoltage Lockout

Internal circuitry keeps both GATE output charge pumps off until VCC1 and VCC2 exceed 2.165V and 0.8V, respectively.

C_{POR}	t_{START}	t_{POR}
0.01µF	1.2ms	5ms
0.033µF	4ms	16.5ms
0.05µF	6ms	25ms
0.1µF	12ms	50ms
0.33µF	40ms	165ms
0.47µF	56ms	235ms
1µF	120ms	500ms

Table 2. Selected Power-On Reset and Start-Up Delays

C_{FILTER}	t_{OCSLOW}
220pF	110µs
680pF	340µs
1000pF	500µs
3300pF	1.6ms
0.01µF	5ms
0.047µF	23.5ms
0.1µF	50ms
0.33µF	165ms

Table 3. Selected Overcurrent Timer Delays

C_{DLY}	t_{DLY}
4700pF	950µs
0.01µF	2ms
0.047µF	9.5ms
0.1µF	20ms
0.33µF	66ms
0.82µF	165ms
1µF	200ms
2.2µF	440ms

Table 4. Selected Sequenced Output Delays

Applications Information

Output Tracking and Sequencing

The MIC2585 is equipped with optional supply settings: Tracking or Sequencing. There are many applications that require two supplies to track one another within a specified maximum potential difference (or time) during power-up and power-down, such as in switching a processor on and off. In many other systems and applications, supply sequencing during turn-on may be essential such as when a specific circuit block (e.g., a system clock) requires available power before another block of system circuitry. For either supply configuration, the MIC2585 requires only one additional component and can be used as an integrated solution to traditional, and most often complex, discrete circuit solutions. Additionally, the two optional supply settings may be combined to provide supply sequencing during start-up and supply tracking during turn-off (see Figure 6 below). The MIC2585 guarantees supply tracking within 250mV for power-up and power-down independent of the load capacitance of each supply. See "*Figure 2*" of the "*Timing Diagrams*".

Wiring the TRK pin to either OUT1 or OUT2 of the MIC2585 enables the tracking feature. The OUT1 and OUT2 pins provide output track sensing and are wired directly to the output (source) of the external MOSFET for Channel 1 and Channel 2, respectively.

The MIC2584/85 can also be used in systems that support more than two supplies. Figure 7 illustrates the generic use of two separate controllers configured to support four independent supply rails with an associated output timing response. The PG (or /POR) output of the first controller is used to enable the second controller. As configured, a fault condition on either V_{OUT1} or V_{OUT2} will result in all channels being shut down. For systems with multiple power sequencing requirements, the controllers' output tracking and sequencing features can be implemented in order to meet the system's timing demands.

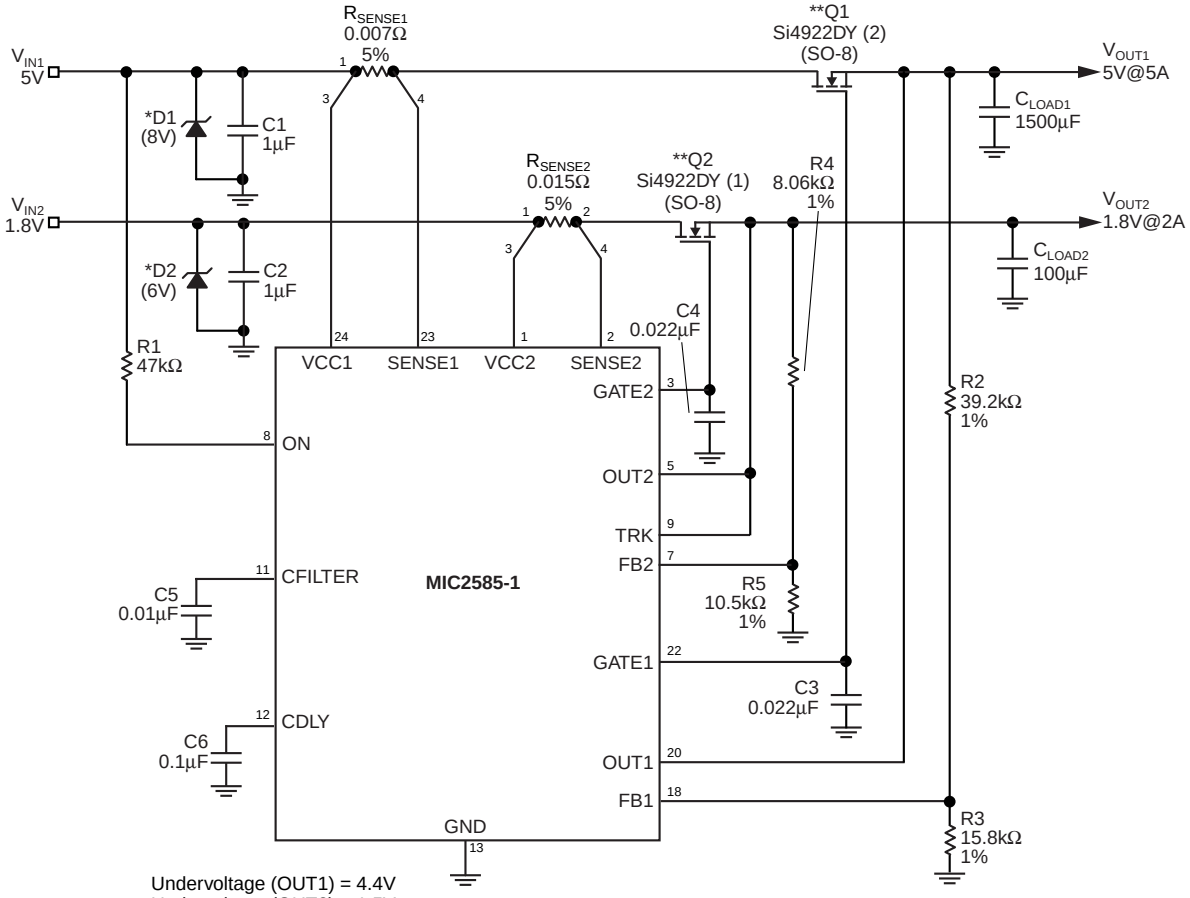


Figure 6. Output Sequencing/Tracking Combination

Fast Output Discharge for Capacitive Loads

In many applications where a switch controller is turned off by either removing the PCB from the backplane or the ON pin is reset, capacitive loading will cause the output to retain voltage unless a 'bleed' (low impedance) path is in place in order to discharge the capacitance. The MIC2585 is equipped with an internal MOSFET that allows the discharging of any load capacitance to ground through a 50Ω to 170Ω path. The discharge feature is configured by wiring the DIS pin to the output (source) of the external MOSFET and is enabled if the TRK pin is below 0.3V after the controller has been disabled by a logic low signal received at the ON pin of Figure 1. See the "*Typical Application*" circuit of Figure 1. A series resistor is required from DIS to V_{OUT} so that the maximum current of 25mA for the DIS pin is not exceeded.

Output Turn-Off Sequencing - No Tracking

There are many applications where it is necessary or desirable for the supply rails to sequence during turn-on and turn-off, as is the case with some microprocessor requirements. The MIC2585 can be configured to allow one output to shut off first, followed by the other output. Figure 8 illustrates an example circuit that sequences OUT1 and OUT2 in a first on–last off application. During start-up, capacitor C_{DLY} allows for V_{OUT1} to turn on followed by V_{OUT2} 20ms later. Once the ON pin receives a low signal by removing the PCB from the backplane, or by an external processor signal, DIS1 and DIS2 will assert low. The external crowbar circuit connected from the DIS2 pin will immediately bring V_{OUT2} to ground while V_{OUT1} will discharge to ground through the 750Ω (680Ω external, 70Ω internal) series path.

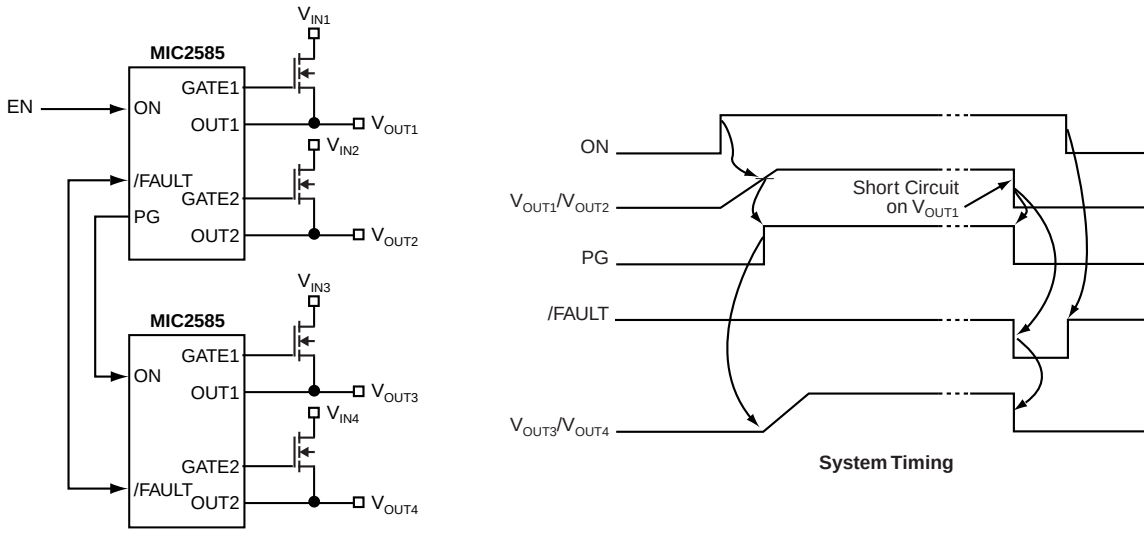


Figure 7. Supporting More Than Two Supplies

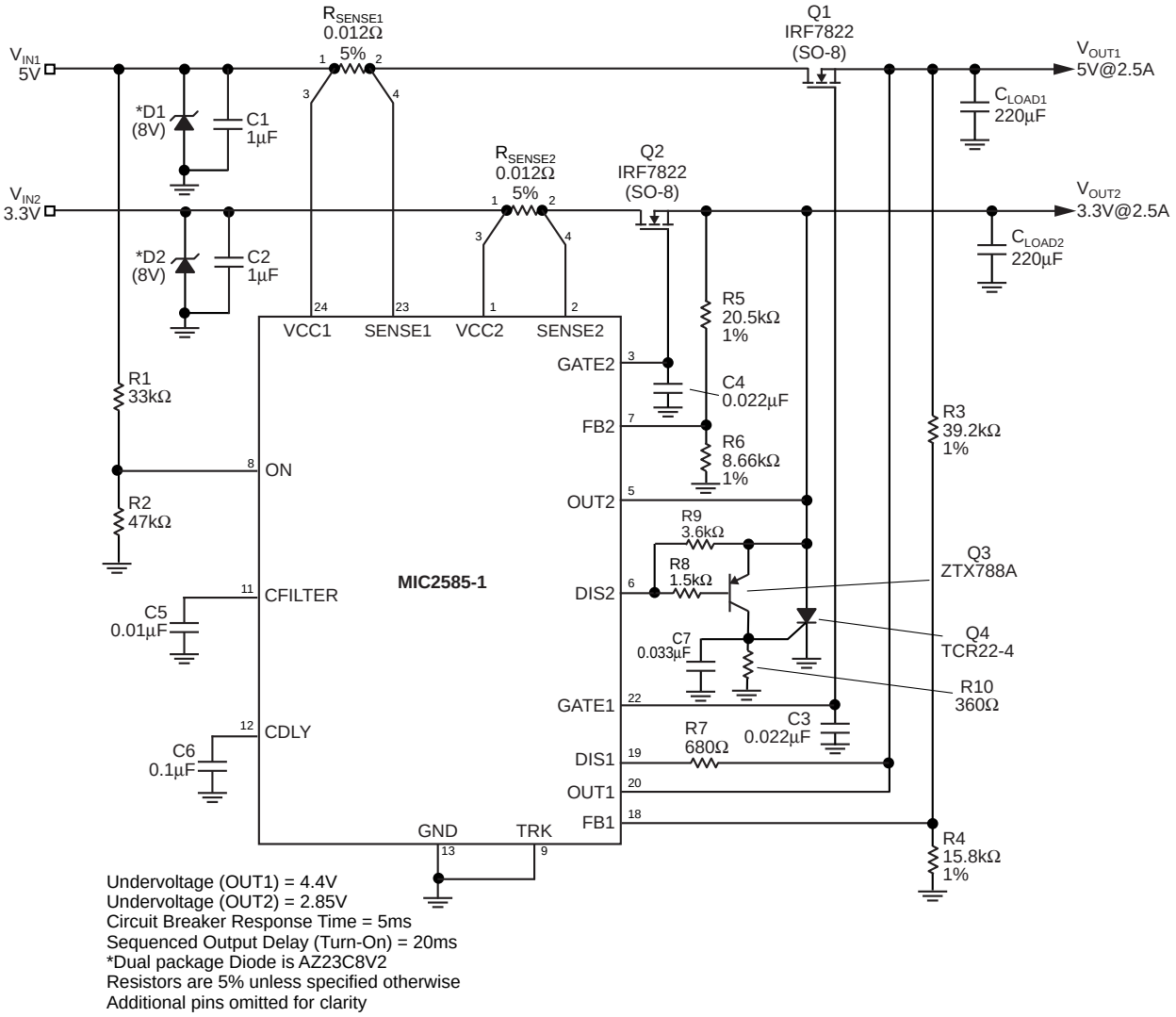


Figure 8. First On—Last Off Application Circuit

Output Undervoltage Detection

For output undervoltage detection, the first consideration is to establish the output voltage level that indicates "power is good." For this example, the output value for which a 12V supply will signal "good" is 10.5V. Next, consider the tolerances of the input supply and FB threshold (V_{FB}). For this example, given a 12V ±5% supply for Channel 1, the resulting output voltage may be as low as 11.4V and as high as 12.6V. Additionally, the FB1 threshold has ±50mV tolerance and may be as low as 1.19V and as high as 1.29V. Thus, to determine the values of the resistive divider network (R12 and R13) at the FB1 pin, shown in the typical application circuit on page 1, use the following iterative design procedure.

1) Choose R13 so as to limit the current through the divider to approximately 100µA or less.

$$R13 \cong \frac{V_{FB1(MAX)}}{100\mu A} \cong \frac{1.29V}{100\mu A} \cong 12.9k\Omega.$$

R13 is chosen as 14.7kΩ ± 1%.

2) Next, determine R12 using the output "good" voltage of 10.5V and the following equation:

$$V_{OUT1(Good)} = V_{FB1(MAX)}\left[\frac{(R12+R13)}{R13}\right] \qquad (10)$$

Using some basic algebra and simplifying Equation 10 to isolate R12, yields:

$$R12 = R13\left[\left(\frac{V_{OUT1(Good)}}{V_{FB1(MAX)}}\right)-1\right] \qquad (10.1)$$

where $V_{FB1(MAX)}$ = 1.29V, $V_{OUT1(Good)}$ = 10.5V, and R13 is 14.7kΩ. Substituting these values into Equation 10.1 now yields R12 = 104.95kΩ. A standard 105kΩ ± 1% is selected. Now, consider the 11.4V minimum output voltage, the lower tolerance for R13 and higher tolerance for R12, 14.55kΩ and 106.05kΩ, respectively. With only 11.4V available, the voltage sensed at the FB1 pin exceeds $V_{FB1(MAX)}$, thus the /POR and PG1 (MIC2585) signals will transition from LOW to HIGH, indicating "power is good" given the worse case tolerances of this example. A similar approach should be used for Channel 2.

Input Overvoltage Protection

A similar design approach as the previous Undervoltage Detection example is recommended for the overvoltage protection circuitry, resistors R6 and R7 for OV1, in Figure 1. For input overvoltage protection, the first consideration is to establish the input voltage level that indicates an overvoltage triggering a system (output voltage) shut down. For our example, the input value for which the Channel 1 12V supply will signal an "output shutdown" is 13.2V (+10%). Similarly, from the previous example:

1) Choose R7 to satisfy 100µA condition.

$$R7 \geq \frac{V_{OV1(MIN)}}{100\mu A} \geq \frac{1.19V}{100\mu A} \geq 11.9k\Omega$$

R7 is chosen as 13.0kΩ ±1%

2) Thus, following the previous example and substituting R6 and R7 for R12 and R13, respectively, $V_{OV1(MIN)}$ for $V_{FB1(MAX)}$, and 13.2V overvoltage for 10.5V output "good," the same formula yields R6 of 131.2kΩ. The nearest standard 1% value is 130kΩ.

Now, consider the 12.6V maximum input voltage (V_{CC1} +5%), the higher tolerance for R7 and lower tolerance for R6, 13.13kΩ and 128.7kΩ, respectively. With 12.6V input, the voltage sensed at the OV1 pin is below $V_{OV1(MIN)}$, and the MIC2584/85 will not indicate an overvoltage condition until V_{CC1} exceeds approximately 13.2V considering the given tolerances. A similar approach should be used for Channel 2.

PCB Connection Sense

There are several configuration options for the MIC2584/85's ON pin to detect if the PCB has been fully seated in the backplane before initiating a start-up cycle. In Figure 1, the MIC2584/85 is mounted on the PCB with a resistive divider network connected to the ON pin. R4 is connected to a short pin on the PCB edge connector. Until the connectors mate, the ON pin is held low which keeps the GATE output charge pump off. Once the connectors mate, the resistor network is pulled up to the input supply, 12V in this example, and the ON pin voltage exceeds its threshold (V_{ON}) of 1.235V and the MIC2584/85 initiates a start-up cycle. In Figure 9, the connection sense consisting of a discrete logic-level MOSFET and a few resistors allows for interrupt control from the processor or other signal controller to shut off the output of the MIC2584/85. R4 pulls the GATE of Q2 to V_{IN} and the ON pin is held low until the connectors are fully mated. Once the connectors fully mate, a logic LOW at the /ON_OFF signal turns Q2 off and allows the ON pin to pull up above its threshold and initiate a start-up cycle. Applying a logic HIGH at the /ON_OFF signal will turn Q2 on and short the ON pin of the MIC2584/85 to ground which turns off the GATE output charge pump.

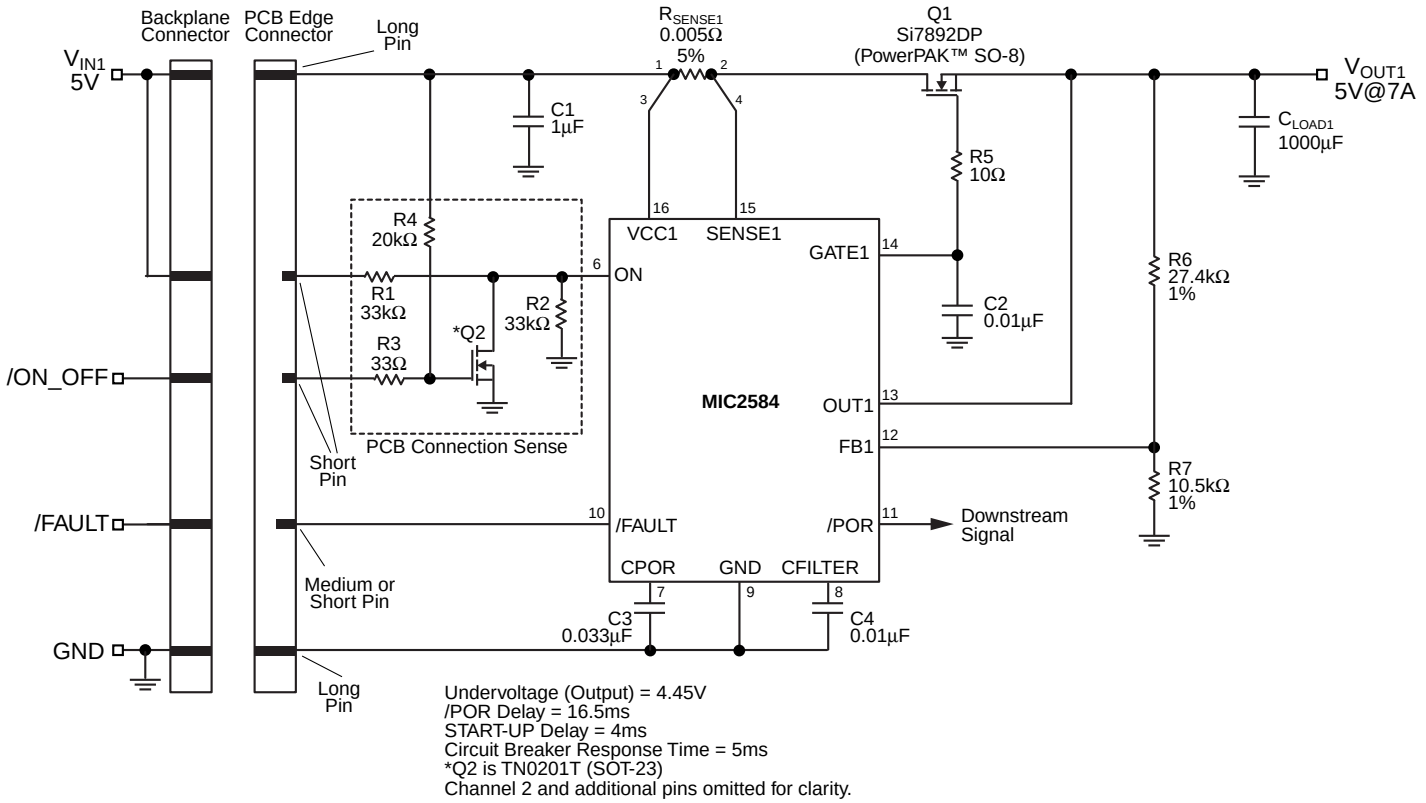


Figure 9. PCB Connection Sense with ON/OFF Control

Higher UVLO Setting

Once a PCB is inserted into a backplane (power supply), the internal UVLO circuit of the MIC2584/85 holds the GATE output charge pump off until VCC1 exceeds 2.165V and VCC2 exceeds 0.8V. If VCC1 falls below 1.935V or VCC2 falls below 0.77V, the UVLO circuit pulls the GATE output to ground and clears the overvoltage and/or current limit faults. For a higher UVLO threshold, the circuit in Figure 10 can be used to delay the output MOSFET from switching on until the desired input voltage is achieved. The circuit allows the charge pumps to remain off until V_{IN1} exceeds $\left(1+\frac{R1}{R2}\right)\times 1.235V$ provided that VCC2 has exceeded its threshold. Both GATE drive outputs will be shut down when V_{IN1} falls below $\left(1+\frac{R1}{R2}\right)\times 1.21V$. In the example circuit , the rising UVLO threshold is set at approximately 9.0V and the falling UVLO threshold is established as 8.9V. The circuit consists of an external resistor divider at the ON pin that keeps both GATE output charge pumps off until the voltage at the ON pin exceeds its threshold (V_{ON}) and after the start-up timer elapses.

Hot Swap Power Control for DSPs

In designing power supplies for dual supply logic devices, such as a DSP, consideration should be given to the system timing requirements of the core and I/O voltages for power-up and power-down operations. When power is provided to the core and I/O circuit blocks in an unpredictable manner, the effects can be detrimental to the life cycle of the DSP or logic device by allowing unexpected current to flow in the core and I/O isolation structures. Additionally, bus contention is one of the critical system-level issues supporting the need for power supply sequencing. Since the core supplies logic control for the bus, powering up the I/O before the core may result in both the DSP and an attached peripheral device being simultaneously configured as outputs. In this case, the output drivers of each device contend for control over sending data along the bus which may cause excessive current to flow in one of the paths (I_1 or I_2) shown in the bidirectional port of Figure 11. Upon powering down the system, the core voltage supply should turn off after the I/O as the bus control signal(s) may enter an indeterminate state if the core is powered down first. Thus, for power sequencing of a dual supply voltage DSP implementing the MIC2585 (if $V_{CORE} \geq V_{I/O}$), a circuit similar to Figure 8 is recommended with the core voltage supplied through Channel 1 and the I/O voltage supplied through Channel 2. For systems with $V_{CORE} < V_{I/O}$, the MIC2585-2 option with the I/O voltage through Channel 1 and core through Channel 2 is used to implement the first on-last off application.

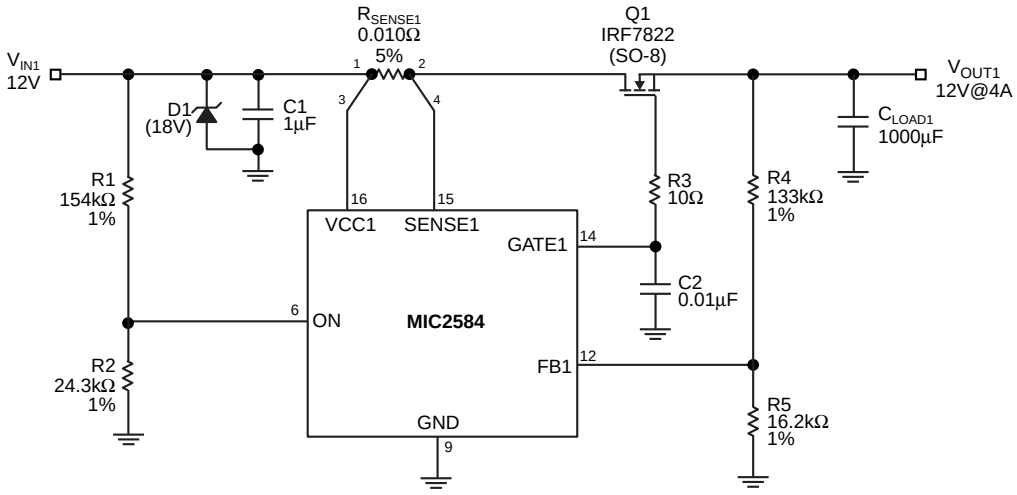
Sense Resistor Selection

The MIC2584 and MIC2585 use a low-value sense resistor to measure the current flowing through the MOSFET switch (and therefore the load). This sense resistor is nominally set at $50mV/I_{LOAD(CONT)}$. To accommodate worst-case tolerances for both the sense resistor (allow ±3% over time and temperature for a resistor with ±1% initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used.

The current limit threshold voltage (i.e., the “trip point”) for the MIC2584/85 may be as low as 42.5mV, which would equate to a sense resistor value of $42.5mV/I_{LOAD(CONT)}$. Carrying the numbers through for the case where the value of the sense resistor is 3% high yields:

$$R_{SENSE(MAX)} = \frac{42.5mV}{(1.03)\left(I_{LOAD(CONT)}\right)} = \frac{41.3mV}{I_{LOAD(CONT)}} \quad (11)$$

Once the value of R_{SENSE} has been chosen in this manner, it is good practice to check the maximum $I_{LOAD(CONT)}$ which the circuit may let through in the case of tolerance build-up in



Undervoltage Lockout Threshold (rising) = 9.0V
Undervoltage Lockout Threshold (falling) = 8.9V
Undervoltage (Output) = 11.4V
Channel 2 and additional pins omitted for clarity.

Figure 10. Higher UVLO Setting

the opposite direction. Here, the worst-case maximum current is found using a 57.5mV trip voltage and a sense resistor that is 3% low in value. The resulting equation is:

$$I_{LOAD(CONT,MAX)} = \frac{57.5mV}{(0.97)\left(R_{SENSE(NOM)}\right)} = \frac{59.3mV}{R_{SENSE(NOM)}} \quad (12)$$

As an example, if an output must carry a continuous 6A without nuisance trips occurring, Equation 11 yields: $R_{SENSE(MAX)} = \frac{41.3mV}{6A} = 6.88m\Omega$. The next lowest standard value is 6mΩ. At the other set of tolerance extremes for the output in question,

$I_{LOAD(CONT,MAX)} = \frac{59.3mV}{6.0m\Omega} = 9.88A$. Knowing this final datum, we can determine the necessary wattage of the sense resistor using $P = I^2R$, where I will be $I_{LOAD(CONT, MAX)}$, and R will be $(0.97)(R_{SENSE(NOM)})$. These numbers yield the following: $P_{MAX} = (9.88A)^2 (5.82m\Omega) = 0.568W$. In this example, a 1W sense resistor is sufficient.

MOSFET Selection

Selecting the proper external MOSFET for use with the MIC2584/85 involves three straightforward tasks:

- Choice of a MOSFET which meets minimum voltage requirements.
- Selection of a device to handle the maximum continuous current (steady-state thermal issues).
- Verify the selected part's ability to withstand any peak currents (transient thermal issues).

MOSFET Voltage Requirements

The first voltage requirement for the MOSFET is easily stated: the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$. For instance, a 12V input may reasonably be expected to see high-frequency transients as high as 18V. Therefore, the drain-source breakdown voltage of the MOSFET must be at least 19V. For ample safety margin and standard availability, the closest minimum value will be 20V.

The second breakdown voltage criterion that must be met is a bit subtler than simple drain-source breakdown voltage, but is not hard to meet. In MIC2584/85 applications, the gate of the external MOSFET is driven up to approximately 20V by the internal output MOSFET (again, assuming 12V operation). At the same time, if the output of the external MOSFET (its source) is suddenly subjected to a short, the gate-source voltage will go to (20V – 0V) = 20V. This means that the external MOSFET must be chosen to have a gate-source breakdown voltage of 20V or more, which is an available standard maximum value. However, if operation is above 12V, the 20V gate-source maximum will likely be exceeded. As a result, an external Zener diode clamp should be used to prevent breakdown of the external MOSFET when operating at voltages above 10V. A Zener diode with 10V rating is recommended as shown in Figure 12. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source breakdown rating or higher. As a general tip, choose surface-mount devices with a drain-source rating of 30V as a starting point.

Finally, the external gate drive of the MIC2584/85 requires a low-voltage logic level MOSFET when operating at voltages lower than 3V. There are 2.5V logic level MOSFETs available. See Table 5, "*MOSFET and Sense Resistor Vendors*" for suggested manufacturers.

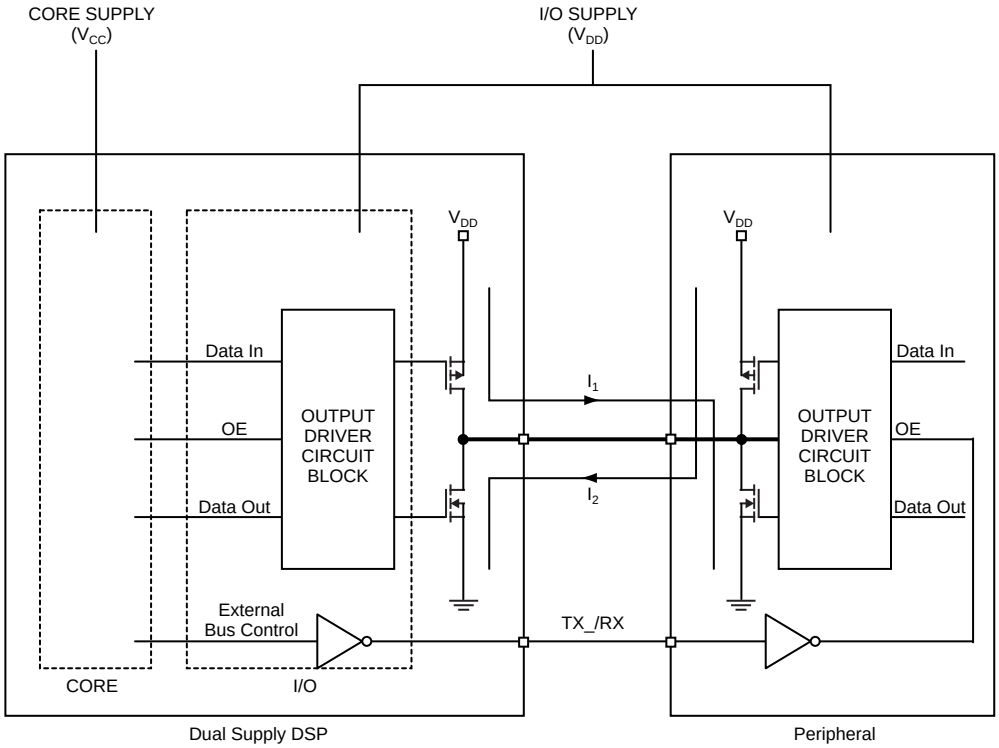


Figure 11. Bidirectional Port Bus Contention

MOSFET Steady-State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of $I_{LOAD(CONT, MAX.)}$ for the output in question (see "*Sense Resistor Selection*").
- The manufacturer's data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., can heat be dissipated into the ground plane or power plane, if using a surface-mount part? Is any airflow available?).

The data sheet will almost always give a value of on resistance given for the MOSFET at a gate-source voltage of 4.5V, and another value at a gate-source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on-resistance of the part with 8V of enhancement. Call this value R_{ON}. Since a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that's required to determine steady-state power dissipation is to calculate I^2R. The one addendum to this is that MOSFETs have a slight increase in R_{ON} with increasing die temperature. A good approximation for this value is 0.5% increase in R_{ON} per °C rise in junction temperature above the point at which R_{ON} was initially specified by the manufacturer. For instance, if the selected MOSFET has a calculated R_{ON} of 10mΩ at a T_J = 25°C, and the actual junction temperature ends up at 110°C, a good first cut at the operating value for R_{ON} would be:

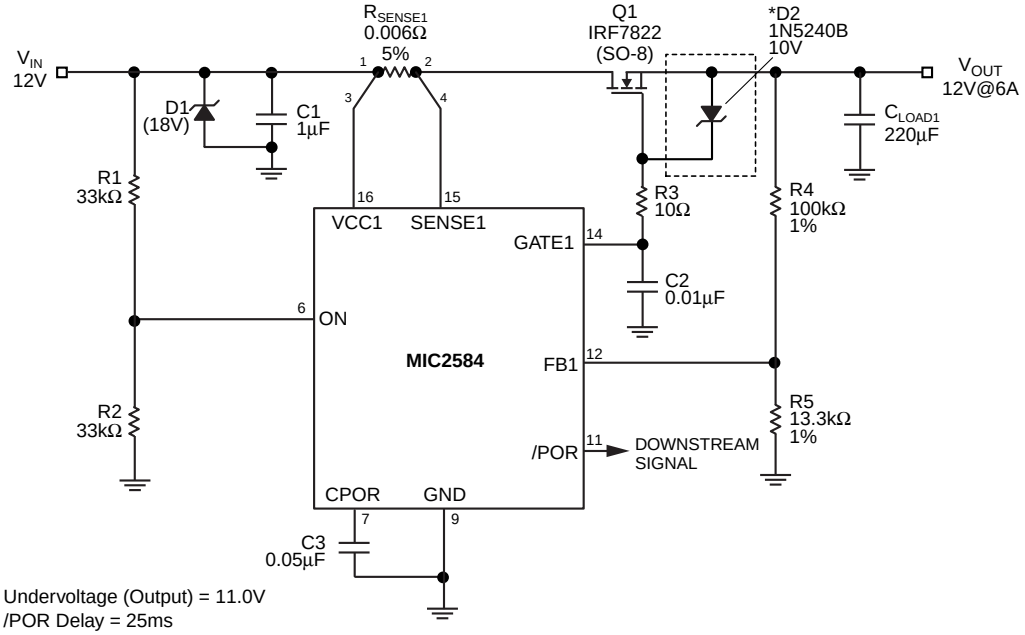
$$R_{ON} \cong 10m\Omega[1 + (110 - 25)(0.005)] \cong 14.3m\Omega$$

The final step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET's performance was specified by the manufacturer. Here are a few practical tips:

1. The heat from a surface-mount device such as an SO-8 MOSFET flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more, the copper will act as the heat sink for the part. This copper must be on the same layer of the board as the MOSFET drain.
2. Airflow works. Even a few LFM (linear feet per minute) of air will cool a MOSFET down substantially. If you can, position the MOSFET(s) near the inlet of a power supply's fan, or the outlet of a processor's cooling fan.
3. The best test of a surface-mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. Check the MOSFET's temperature in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

MOSFET Transient Thermal Issues

Having chosen a MOSFET that will withstand the imposed voltage stresses, and the worse case continuous I^2R power dissipation which it will see, it remains only to verify the MOSFET's ability to handle short-term overload power dissipation without overheating. A MOSFET can handle a much



Undervoltage (Output) = 11.0V
/POR Delay = 25ms
START-UP Delay = 6ms
*Recommended for MOSFETs with gate-source breakdown of 20V or less for catastrophic output short circuit protection. (IRF7822 V_{GS}(MAX) = 12V)
Channel 2 and additional pins omitted for clarity.

Figure 12. Zener Clamped MOSFET Gate

higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that, like everything else, thermal devices (silicon die, lead frames, etc.) have thermal inertia.

In terms related directly to the specification and use of power MOSFETs, this is known as “transient thermal impedance,” or $Z_{\theta(J-A)}$. Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve. For example, take the following case: V_{IN} = 12V, t_{OCSLOW} has been set to 100msec, $I_{LOAD(CONT.\ MAX)}$ is 1.2A, the slow-trip threshold is 50mV nominal, and the fast-trip threshold is 100mV. If the output is accidentally connected to a 6Ω load, the output current from the MOSFET will be regulated to 1.2A for 100ms (t_{OCSLOW}) before the part trips. During that time, the dissipation in the MOSFET is given by:

$$P = E \times I \quad E_{MOSFET} = [12V-(1.2A)(6\Omega)] = 4.8V$$
$$P_{MOSFET} = (4.8V \times 1.2A) = 5.76W \text{ for } 100msec.$$

At first glance, it would appear that a really hefty MOSFET is required to withstand this sort of fault condition. This is where the transient thermal impedance curves become very useful. Figure 13 shows the curve for the Vishay (Siliconix) Si4410DY, a commonly used SO-8 power MOSFET.

Taking the simplest case first, we’ll assume that once a fault event such as the one in question occurs, it will be a long time, 10 minutes or more, before the fault is isolated and the channel is reset. In such a case, we can approximate this as a “single pulse” event, that is to say, there’s no significant duty cycle. Then, reading up from the X-axis at the point where “Square Wave Pulse Duration” is equal to 0.1sec (=100msec), we see that the $Z_{\theta(J-A)}$ of this MOSFET to a highly infrequent event of this duration is only 8% of its continuous $R_{\theta(J-A)}$.

This particular part is specified as having an $R_{\theta(J-A)}$ of 50°C/W for intervals of 10 seconds or less. Thus:

Assume T_A = 55°C maximum, 1 square inch of copper at the drain leads, no airflow.

Recalling from our previous approximation hint, the part has an R_{ON} of (0.0335/2) = 17mΩ at 25°C.

Assume it has been carrying just about 1.2A for some time.

When performing this calculation, be sure to use the highest anticipated ambient temperature ($T_{A(MAX)}$) in which the MOSFET will be operating as the starting temperature, and find the operating junction temperature increase (ΔT_J) from that point. Then, as shown next, the final junction temperature is found by adding $T_{A(MAX)}$ and ΔT_J. Since this is not a closed-form equation, getting a close approximation may take one or two iterations, But it’s not a hard calculation to perform, and tends to converge quickly.

Then the starting (steady-state)T_J is:

$$T_J \cong T_{A(MAX)} + \Delta T_J$$
$$\cong T_{A(MAX)} + [R_{ON} + (T_{A(MAX)} - T_A)(0.005/°C)(R_{ON})] \times I^2 \times R_{\theta(J-A)}$$
$$T_J \cong 55°C + [17m\Omega + (55°C-25°C)(0.005)(17m\Omega)] \times (1.2A)^2 \times (50°C/W)$$
$$T_J \cong (55°C + (0.02815W)(50°C/W)$$
$$\cong 54.6°C$$

Iterate the calculation once to see if this value is within a few percent of the expected final value. For this iteration we will start with T_J equal to the already calculated value of 54.6°C:

$$T_J \cong T_A + [17m\Omega + (54.6°C-25°C)(0.005)(17m\Omega)] \times (1.2A)^2 \times (50°C/W)$$
$$T_J \cong (55°C + (0.02832W)(50°C/W) \cong 56.42°C$$

So our original approximation of 56.4°C was very close to the correct value. We will use T_J = 56°C.

Finally, add (5.76W)(50°C/W)(0.08) = 23°C to the steady-state T_J to get $T_{J(TRANSIENT\ MAX.)}$ = 79°C. This is an acceptable maximum junction temperature for this part.

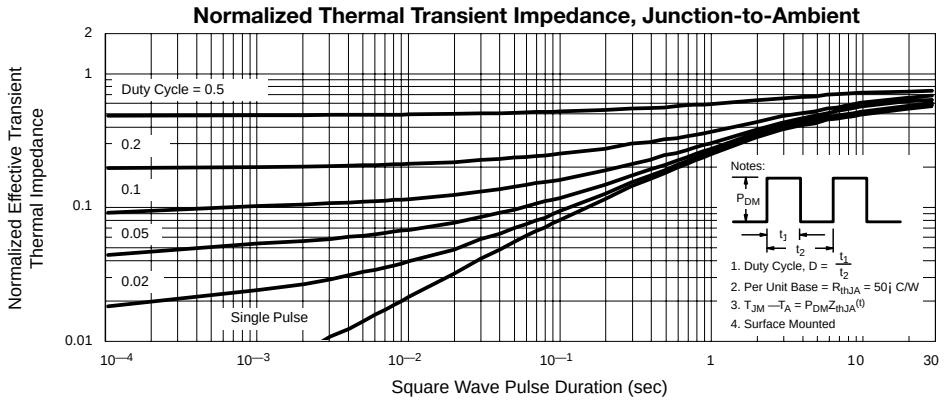


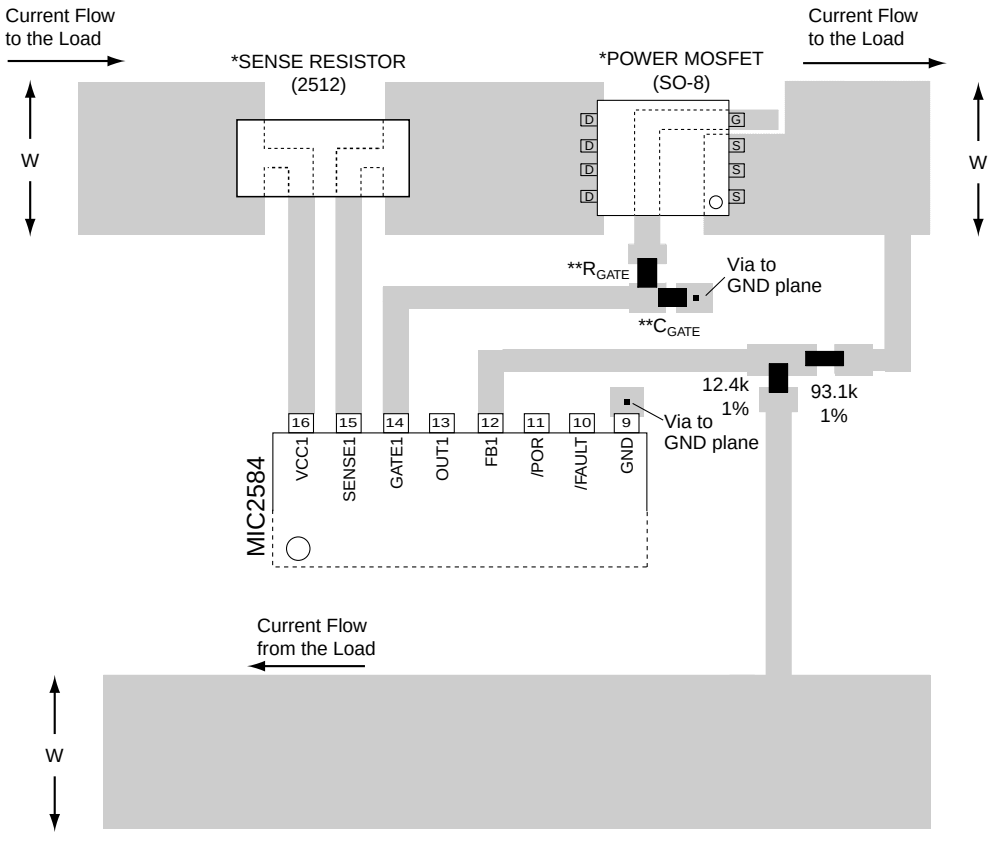
Figure 13. Transient Thermal Impedance

PCB Layout Considerations

Because of the low values of the sense resistors used with the MIC2584/85 controllers, special attention to the layout must be used in order for the device's circuit breaker function to operate properly. Specifically, the use of a 4-wire Kelvin connection to accurately measure the voltage across R_{SENSE} is highly recommended. Kelvin sensing is simply a means of making sure that any voltage drops in the power traces connecting to the resistors does not get picked up by the traces themselves. Additionally, these Kelvin connections should be isolated from all other signal traces to avoid introducing noise onto these sensitive nodes. Figure 14 illustrates a recommended, multi-layer layout for the R_{SENSE}, Power MOSFET, timer(s), and feedback network connections. The feedback network resistor values are selected for a 12V application. Many hot swap applications will require load currents of several amperes. Therefore, the power (V_{CC} and Return) trace widths (W) need to be wide enough to allow the current to flow while the rise in temperature for a given copper plate (e.g., 1oz. or 2oz.) is kept to a maximum of 10°C ~ 25°C. Also, these traces should be as short as possible in order to minimize the IR drops between the input and the load. For a starting point, there are many trace width calculation tools available on the web such as the following link:

http://www.aracnet.com/cgi-usr/gpatrick/trace.pl

Finally, the use of plated-through vias will be needed to make circuit connections to power and ground planes when utilizing multi-layer PC boards.



DRAWING IS NOT TO SCALE
Similar considerations should be used for Channel 2.
*See Table 5 for part numbers and vendors.
**Optional components.
Trace width (W) guidelines given in "PCB Layout Recommendations" section of the datasheet.

Figure 14. Recommended PCB Layout for Sense Resistor, Power MOSFET and Feedback Network

MOSFET and Sense Resistor Vendors

Device types and manufacturer contact information for power MOSFETs and sense resistors is provided in Table 5. Some of the recommended MOSFETs include a metal heat sink on the bottom side of the package that is connected to the drain leads. The recommended trace for the MOSFET gate of Figure 14 must be redirected when using MOSFETs packaged in this style. Contact the device manufacturer for package information.

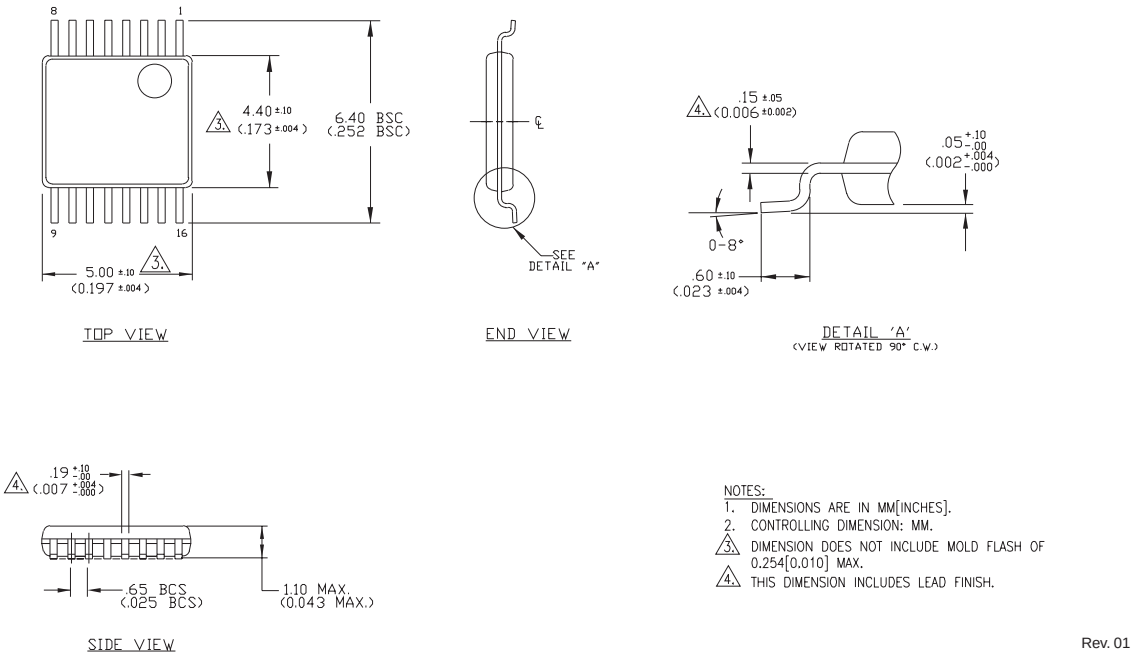
MOSFET Vendors	Key MOSFET Type(s)	*Applications	Contact Information
Vishay (Siliconix)	Si4420DY (SO-8 package) Si4442DY (SO-8 package) Si3442DV (SO-8 package) Si7860DP (PowerPAK™ SO-8) Si7892DP (PowerPAK™ SO-8) Si7884DP (PowerPAK™ SO-8) SUB60N06-18 (TO-263) SUB70N04-10 (TO-263)	$I_{OUT} \leq 10A$ I_{OUT} = 10A-15A, $V_{CC} \leq 5V$ $I_{OUT} \leq 3A$, $V_{CC} \leq 5V$ $I_{OUT} \leq 12A$ $I_{OUT} \leq 15A$ $I_{OUT} \leq 15A$ $I_{OUT} \geq 20A$, $V_{CC} \geq 5V$ $I_{OUT} \geq 20A$, $V_{CC} \geq 5V$	www.siliconix.com (203) 452-5664
International Rectifier	IRF7413 (SO-8 package) IRF7457 (SO-8 package) IRF7822 (SO-8 package) IRLBA1304 (Super220™)	$I_{OUT} \leq 10A$ $I_{OUT} \leq 10A$ I_{OUT} = 10A-15A, $V_{CC} \leq 5V$ $I_{OUT} \geq 20A$, $V_{CC} \geq 5V$	www.irf.com (310) 322-3331
Fairchild Semiconductor	FDS6680A (SO-8 package) FDS6690A (SO-8 package)	$I_{OUT} \leq 10A$ $I_{OUT} \leq 10A$, $V_{CC} \leq 5V$	www.fairchildsemi.com (207) 775-8100
Philips	PH3230 (SOT669-LFPAK)	$I_{OUT} \geq 20A$	www.philips.com
Hitachi	HAT2099H (LFPAK)	$I_{OUT} \geq 20A$	www.halsp.hitachi.com (408) 433-1990

* These devices are not limited to these conditions in many cases, but these conditions are provided as a helpful reference for customer applications.

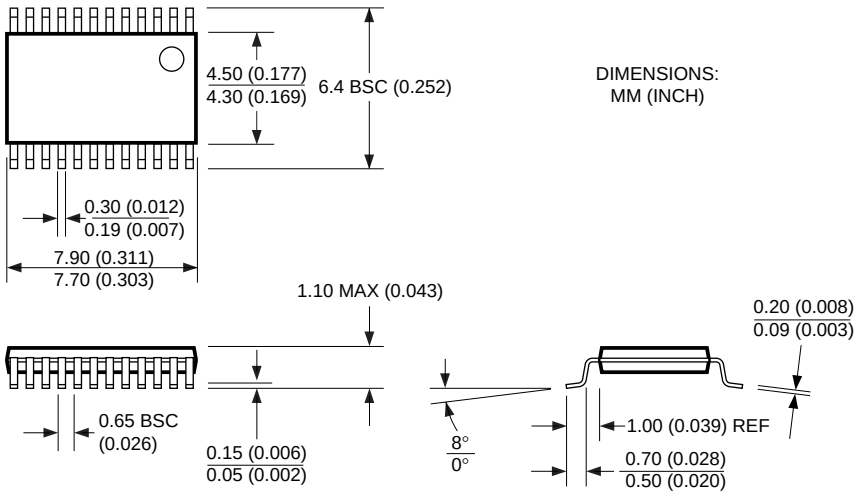
Resistor Vendors	Sense Resistors	Contact Information
Vishay (Dale)	“WSL” Series	www.vishay.com/docswsl_30100.pdf (203) 452-5664
IRC	“OARS” Series “LR” Series (second source to “WSL”)	www.irctt.com/pdf_files/OARS.pdf www.irctt.com/pdf_files/LRC.pdf (828) 264-8861

Table 5. MOSFET and Sense Resistor Vendors

Package Information



16-Pin TSSOP (TS)



24-Pin TSSOP (TS)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com

The information furnished by Micrel in this datasheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is at Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2005 Micrel, Incorporated.