MIC2590B

Dual-Slot PCI Hot Plug Controller

General Description

The MIC2590B is a power controller supporting power distribution requirements for Peripheral Component Interconnect (PCI) hot plug compliant systems incorporating the Intelligent Platform Management Interface (IPMI). The MIC2590B provides complete power control support for two PCI slots including the $3.3V_{AUX}$ defined by the PCI 2.2 specification.

Support for +5V, +3.3V, +12V and –12V supplies is provided including programmable constant-current inrush limiting, voltage supervision, programmable current limit, fault reporting and circuit breaker functions which provide fault isolation.

The MIC2590B also incorporates a SMBus interface in which complete status and control of power within each slot is provided. Data such as voltage and current from each supply of each slot can be obtained for IPMI sensor records in addition to power status of each slot.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Supports two independent PCI 2.2 slots
- SMBus interface for slot power control and status
- +5V, +3.3V, +12V, –12V, +3.3VAUX supplies supported per PCI specification 2.2
- Programmable inrush current-limiting
- Active current regulation controls inrush current
- Electronic circuit breaker
- Dual level fault detection for quick fault response without nuisance tripping
- Thermal isolation between circuitry for slot A and slot B

Applications

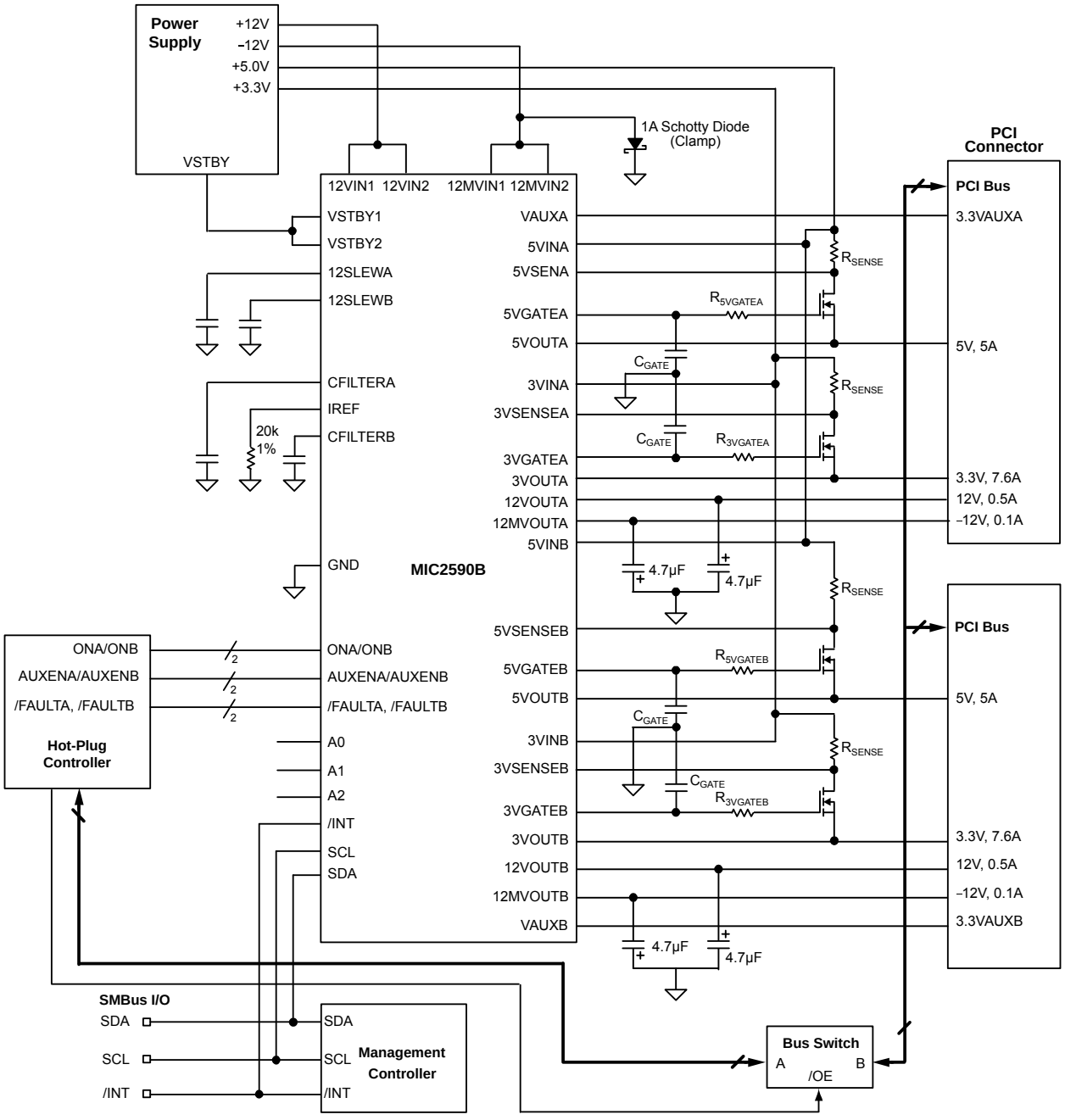
- PCI hot-plug power distribution

Ordering Information

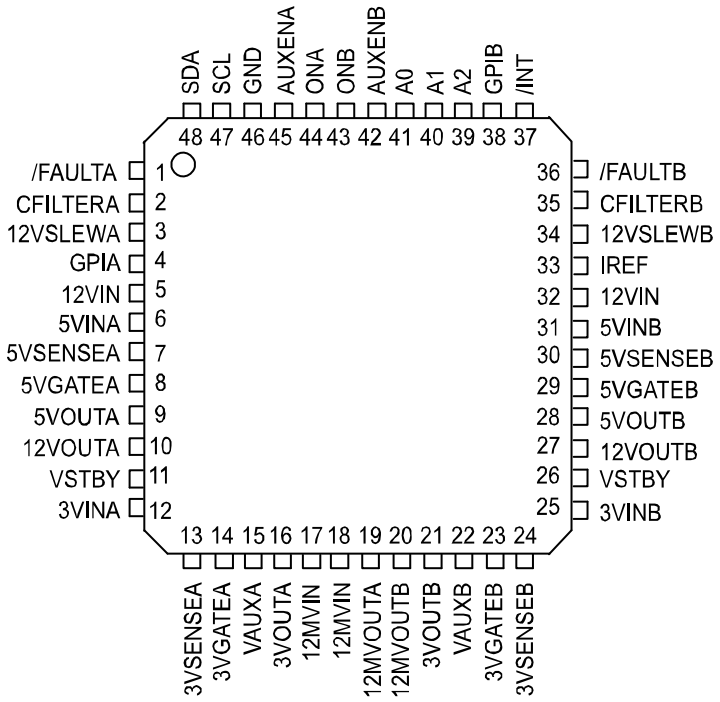
Part Number		5V & 3V Fast-trip Threshold	+12V & –12V Fast-trip Threshold	Operating Temp. Range	Package
Standard	Pb-Free				
MIC2590B-2BTQ	MIC2590B-2YTQ	100mV	1.5A/0.4A	0° to +70°C	48-Pin TQFP
MIC2590B-5BTQ*	MIC2590B-5YTQ*	Disabled	1.5A/0.4A	0° to +70°C	48-Pin TQFP

Note:
* Contact factory for availability.

Typical Application



Pin Configuration



48-Pin TQFP (TQ)

Pin Description

Pin Number	Pin Name	Pin Function
6, 31	5VINA, 5VINB	5V Supply Power and Sense Inputs [A/B]: Two pins are provided for Kelvin connection (one for each slot). Pin 6 is the Kelvin sense connection to the supply side of the sense resistor for 5V Slot A. Pin 31 is the Kelvin sense connection to the supply side of the sense resistor for 5V Slot B. These two pins must ultimately connect to each other within 10cm. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
12, 25	3VINA, 3VINB	3.3V Supply Power and Sense Inputs [A/B]: Two pins are provided for Kelvin connection (one for each slot). Pin 12 is the Kelvin sense connection to the supply side of the sense resistor for 3V Slot A. Pin 25 is the Kelvin sense connection to the supply side of the sense resistor for 3V Slot B. These two pins must ultimately connect to each other within 10cm. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
5, 32	12VIN – 2 pins	+12V Supply Input: An undervoltage lockout circuit prevents the switches from turning on while this input is less than its lockout threshold. Both pins must be tied together at the chip.
17, 18	12VMIN – 2 pins	–12V Supply Input: An undervoltage lockout circuit prevents the switches from turning on while this input is less than its lockout threshold. Both pins must be tied together at the chip.
10, 27	12VOUTA, 12VOUTB	12V output [A/B]
19, 20	12MVOUTA, 12MVOUTB	–12V output [A/B]
3, 34	12VSLEWA, 12VSLEWB	12V Slew Rate Control [A/B]: Connect capacitors between these pins and ground to set output slew rates of the +12V and -12V supplies.

Pin Number	Pin Name	Pin Function
45, 42	AUXENA, AUXENB	AUX Enable Inputs [A/B]: Rising-edge sensitive enable inputs for VAUXA and VAUXB outputs. Taking AUXENA/AUXENB low after a fault resets the respective slot's Aux Output Fault Latch. Tie these pins to ground if using SMBus-mode power control.
16, 21	3VOUTA, 3VOUTB	3.3V Power-Good Sense Inputs: Connect to 3.3V[A/B] outputs. Used to monitor the 3.3V output voltages for Power-Good status.
9, 28	5VOUTA, 5VOUTB	5V Power-Good Sense Inputs: Connect to 5V[A/B] outputs. Used to monitor the 5V output voltages for Power-Good status.
33	IREF	A resistor connected between this pin and ground sets the ADC current measurement gain. This resistor must be 20kΩ ±1%.
7, 30	5VSENSEA, 5VSENSEB	5V Circuit Breaker Sense Input [A/B]: The current-limit thresholds are set by connecting sense resistors between these pins and 5VIN[A/B]. When the current-limit threshold of IR = 50mV is reached, the 5VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT}, the circuit breaker is tripped and the GATE pin for the affected slot is immediately pulled low.
13, 24	3VSENSEA, 3VSENSEB	3V Circuit Breaker Sense Input [A/B]: The current limit thresholds are set by connecting sense resistors between these pins and 3VIN[A/B]. When the current limit threshold of IR = 50mV is reached, the 3VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT}, the circuit breaker is tripped and the GATE pin for the affected slot is immediately pulled low.
8, 29	5VGATEA, 5VGATEB	5V Gate Drive Outputs [A/B]: Each connects to the gate of an external N-Channel MOSFET. During power-up the C_{GATE} and the gate of the MOSFETs are charged by a 20µA current source. This controls the value ofdv/dt seen at the source of the MOSFETs, and hence the current flowing into the load capacitance. During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of t_{FLT}. Whenever an overcurrent, thermal shutdown or input undervoltage fault condition occur sthe GATE pin for the affected slot is immediately brought low. During power-down these pins are discharged by an internal current source.
14, 23	3VGATEA, 3VGATEB	3V Gate Drive Outputs [A/B]: Each connects to the gate of an external N-Channel MOSFET. During power-up the C_{GATE} and the gate of the MOSFETs are charged by a 20µA current source. This controls the value ofdv/dt seen at the source of the MOSFETs, and hence the current flowing into the load capacitance. During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of t_{FLT}. Whenever an overcurrent, thermal shutdown or input undervoltage fault condition occurs the GATE pin for the affected slot is immediately brought low. During power-down these pins are discharged by an internal current source.
11, 26	VSTBY – 2 pins	3.3V Standby input voltage required to support PCI 2.2 VAUX input: SMBus, internal registers and A/D converter run off of VSTBY to ensure chip access during standby modes. A UVLO circuit prevents turn-on of this supply until VSTBY rises above its UVLO threshold. Both pins must be tied together at the chip.
15, 22	VAUXA, VAUXB	V_{AUX}[A/B] output voltages to PCI card slots: These outputs connect the VAUX pin of the PCI 2. 2 Connectors VSTBY via internal 400mΩ MOSFETs which are current-limited and protected against short circuit faults.
44, 43	ONA, ONB	Enable input for MAIN outputs: Rising-edge sensitive. Used to enable or disable MAIN (5V, 3.3V, +12V, –12V) outputs. Taking ONA/ONB low after a fault resets the respective slot's Main Output Fault Latch. Tie these pins to ground if using SMBus-mode power control.

Pin Number	Pin Name	Pin Function
1, 36	/FAULTA, /FAULTB	Open Drain, Active-Low: Asserted whenever the circuit breaker trips due to a fault condition. /FAULT[A/B] is reset by bringing the faulted slot's ON pin low if /FAULT was asserted in response to a fault condition on one of the slot's MAIN outputs(+12V, +5V, +3.3V, or –12V). /FAULT[A/B] is reset by bringing the faulted slot's AUXEN pin low if /FAULT was asserted in response to a fault condition on the slot's VAUX output. If a fault condition occurred on both the MAIN and AUX outputs of the same slot, then both ON and AUXEN must be brought low to de-assert the /FAULT output.
2, 35	CFILTERA, CFILTERB	Filter Capacitor [A/B]: Capacitors connected between these pins and ground set the duration of t_{FLT}. t_{FLT} is the amount of time for which a slot remains incurrent-limit before its circuit breaker is tripped.
37	/INT	Interrupt Output: Open Drain, Active-low. Asserted whenever a power faulti s detected. Cleared by writing a logic 1 to the respective active bit into the Status Register.
48	SDA	SMBus Data: Bidirectional SMBus data line.
47	SCL	SMBus Clock: Input.
39, 40, 41	A2, A1, A0	SMBus Address Select pins: Connect to ground or leave open in order to program device SMBus base address. There is an internal pull-up to VSTBY on each of these inputs.
4, 38	GPIA, GPIB	General Purpose Inputs: The state of these inputs are available by reading the Common Status Register.
46	GND	Ground

Absolute Maximum Ratings[1]

Supply Voltage
($12V_{IN}$) ..... +14V
($12MV_{IN}$) ..... –14V
($5V_{IN}$) ..... +7V
($3V_{IN}$), (V_{STBY}) ..... +7V
Any Logic Output Voltage ..... –0.5 (min)/+5.5V (max)
Any Logic Input Voltage ..... –0.5 (min)/+5.5V (max
Output Current (FAILT[A/B]#, /INT, SDA). 10mA
Lead Temperature
IR Reflow, Peak Temperature ..... 235 +5/–0°C
Storage Temperature (T_s) ..... –65°C to +150°C
ESD Rating[3] 2kV

Operating Ratings[2]

Supply Voltage
($12V_{IN}$) ..... +11.65V to +12.6V
($12MV_{IN}$) ..... –11.0V to –13.2V
($5V_{IN}$) ..... +4.85V to 5.25V
($3V_{IN}$) ..... +3.1V to +3.6V
(V_{STBY}) ..... +3.15V to 3.6V
Ambient Temperature (T_A) ..... 0°C to +70°C
Junction Temperature (T_J) ..... 125°C
Thermal Resistance
TQFP (θ_{JA}) ..... 56.5°C/W

Electrical Characteristics[4]

$12V_{IN}$ = 12V; $12MV_{IN}$ = –12V; $5V_{IN}$ = 5V; $3V_{IN}$ = 3.3V; V_{STBY} = 3.3V; T_A = 0°C to 70°C; unless noted.

Power Control and Logic Sections

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC12}	Supply Current			0.6	2.0	mA
I_{CC5}				1.2	2.0	mA
I_{CC33}				0.5	0.7	mA
I_{CC12M}				–1.0	–2.0	mA
I_{CCVSBY}				2.5	5.0	mA
V_{UVLO}	Under Voltage Lockout	$12V_{IN}$ increasing	8	9	10	V
		$3V_{IN}$ increasing	2.2	2.5	2.75	V
		$5V_{IN}$ increasing	3.7	4.0	4.3	V
		$12MV_{IN}$ increasing	–10	–9	–8	V
		V_{STBY} increasing	2.8	2.9	3.0	V
V_{HYSUV}	Under Voltage Lockout Hysteresis - $12V_{IN}$, $12MV_{IN}$, $5V_{IN}$, $3V_{IN}$			180		mV
$V_{HYSSTBY}$	Under-voltage Lockout Hysteresis - V_{STBY}			50		mV
V_{UVTH}	Power Good Under-Voltage Thresholds					
$V_{UVTH(12V)}$	$12V_{OUT}$[A/B]	$12V_{OUT}$[A/B] decreasing	10.2	10.5	10.8	V
$V_{UVTH(12MV)}$	$12MV_{OUT}$ [A/B]	$12MV_{OUT}$[A/B] decreasing	–10.8	–10.6	–10.2	V
$V_{UVTH(3V)}$	$3V_{OUT}$ [A/B]	$3V_{OUT}$[A/B] decreasing	2.7	2.8	2.9	V
$V_{UVTH(5V)}$	$5V_{OUT}$ [A/B]	$5V_{OUT}$[A/B] decreasing	4.4	4.5	4.7	V
$V_{UVTH(VAUX)}$	V_{AUX}[A/B]	V_{AUX}[A/B] decreasing	2.7	2.8	2.9	V
V_{HYSPG}	Power-Good Detect Hysteresis			30		mV
V_{GATE}	$5V_{GATE}$/$3V_{GATE}$ Voltage		$12V_{IN}$–15		$12V_{IN}$	V
$I_{GATE(SOURCE)}$	$5V_{GATE}$/$3V_{GATE}$ Output Source	start cycle	15	25	35	µA
$I_{GATE(SINK)}$	$5V_{GATE}$/$3V_{GATE}$ Output Sink Fault Current	any fault condition, V_{GATE} = 5V		70		mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{FILTER}	C_{FILTER} Threshold Voltage		1.20	1.25	1.30	V
I_{FILTER}	C_{FILTER} [A/B] Charge Current	$V_{[5/3]}V_{IN} – V_{[5/3]}V_{SENSE} > V_{THILIMIT}$	1.80	2.5	5.0	µA
I_{SLEW}	$12V_{SLEW}$[A/B] Charge Current	During turn-on only	13	22	35	µA
$V_{THILIMIT}$	Current Limit Threshold Voltages					
	5V[A/B] Supplies	$V_{5VIN} – V_{5VSENSE}$	35	50	65	mV
	3.3V[A/B] Supplies	$V_{3VIN} – V_{3VSENSE}$	35	50	65	mV
V_{THFAST}	$5V_{OUT}$[A/B] and $3V_{OUT}$ [A/B]	MIC2590B-2	90	113	135	mV
	Fast-Trip Thresholds	MIC2590B-5		Disabled		
V_{IL}	LOW-Level Input Voltage				0.8	V
	(SCL,SDA,ON[A/B],A[0-2],GPI[A/B])					
V_{OL}	Output LOW Voltage	I_{OL} = 3mA			0.4	V
	/FAULT[A/B], /INT, SDA					
V_{IH}	HIGH-Level Input Voltage		2.1			V
	SCL,SDA,ON[A/B],A[0-2],					
	AUXEN[A/B],GPI[A/B])					
$R_{PULL-UP}$	Internal Pullups from A[0-2] to V_{STBY}			40		kΩ
I_{IL}	Input Leakage Current				±5	µA
	SCL, ON[A/B],AUXEN[A/B], GP[A/B])					
$I_{LKG(OFF)}$	Off-State Leakage Current				±5	µA
	SDA,/FAULT[A/B],/INT					
T_{OV}	Overtemperature Shutdown & Reset Thresholds, with overcurrent on slot	T_J Increasing, each slot, **Note 5**		140		°C
		T_J Decreasing, each slot, **Note 5**		130		°C
	Overtemperature Shutdown & Reset Thresholds, all other conditions (all outputs will latch OFF)	T_J Increasing, both slots, **Note 5**		160		°C
		T_J Decreasing, both slots, **Note 5**		150		°C
$R_{OUT(ON)}$	Output MOSFET Resistance					
$R_{OUT(12V)}$	12V MOSFET	I_{DS} = 500mA, T_J = 125°C			500	mΩ
$R_{OUT(12MV)}$	–12V MOSFET	I_{DS} = 100mA, T_J = 125°C			2	Ω
$R_{OUT(AUX)}$	V_{AUX} MOSFET	I_{DS} = 375mA, T_J = 125°C			400	mΩ
V_{OFF}	Off-State Output Offset Voltage					
$V_{OFF(+12V)}$	$12V_{OUT}$[A/B]	$12V_{OUT}$[A/B] = Off, T_J = 125°C			50	mV
$V_{OFF(–12V)}$	$12MV_{OUT}$[A/B]	$12MV_{OUT}$[A/B] = Off, T_J = 125°C	–50			mV
$V_{OFF(AUX)}$	V_{AUX}[A/B]	V_{AUX}[A/B] = Off, T_J = 125°C			50	mV
I_{THSLOW}	Current Limit Threshold					
$I_{LIM(12)}$	12V MOSFET	$12V_{OUT}$[A/B] = 0V	0.52	1.0	1.5	A
$I_{LIM(12M)}$	–12V MOSFET	$12MV_{OUT}$[A/B] = 0V	–0.11	–0.2	–0.3	A
I_{THFAST}	Fast-Trip Thresholds	$12V_{OUT}$[A/B] (MIC2590B-2)	1.0	2.15	3.0	A
		$12MV_{OUT}$[A/B] (MIC2590B-2)	–0.20	–0.45	–0.6	A
$I_{AUX(THRESH)}$	Auxiliary Output Current Limit Threshold **Figure 4**	Current which must be drawn from V_{AUX} to register as a fault		0.84		A
$I_{SC(TRAN)}$	Maximum Transient Short Circuit Current	V_{AUX} Enabled, then Grounded	$I_{MAX} = V_{STBY} / R_{DS(AUX)}$			A

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LIM(AUX)}$	Regulated Current after Transient	From end of $I_{SC(TRAN)}$ to C_{FILTER} Time Out	0.375	0.7	1.35	A
R_{DISCH}	Output Discharge Resistance					
$R_{(12V)}$	$12V_{OUT}$[A/B]	$12V_{OUT}$[A/B] = 6.0V		1600		Ω
$R_{(12MV)}$	$12MV_{OUT}$[A/B]	$12MV_{OUT}$[A/B] = –6.0V		600		Ω
$R_{(3V)}$	$3V_{OUT}$[A/B]	$3V_{OUT}$[A/B] = 1.65V		150		Ω
$R_{(5V)}$	$5V_{OUT}$[A/B]	$5MV_{OUT}$[A/B] = 2.5V		150		Ω
$R_{(3VAUX)}$	$3V_{AUX}$[A/B]	$5V_{OUT}$[A/B] = 1.65V		430		Ω
$t_{OFF(3)}$ $t_{OFF(5)}$	Current Limit Response Time for 3.3V and 5V Outputs, **Figure 2**	MIC2590B-2 with C_{GATE} = 10nF, $V_{IN} – V_{SENSE}$ = 200mV		1		µs
$T_{SC(TRAN)}$	V_{AUX} Current Limiter Response Time, **Figure 5**	V_{AUX}[A/B] = 0V, **Note 5**		33		µs
$t_{OFF(12)}$	12V Current Limit Response Time, **Figure 3**	$12V_{OUT}$[A/B] = 0V, **Note 5**		1		µs
$t_{OFF(12M)}$	–12V Current Limit Response Time, **Figure 3**	$12MV_{OUT}$[A/B] = 0V, **Note 5**		1		µs
$T_{PROP(3VFAULT)}$	Delay from 3V[A/B] overcurrent-limit to FAULT Output	MIC2590B-2, $V_{SENSE} – V_{THLIMIT}$ = 200mV, C_{FILTER} = open		1		µs
$T_{PROP(5VFAULT)}$	Delay from 5V[A/B] overcurrent-limit to FAULT Output	MIC2590B-2, $V_{SENSE} – V_{THLIMIT}$ = 200mV, C_{FILTER} = open		1		µs
t_W	ON[A/B], AUXEN[A/B] Pulse Width	**Note 5**		100		ns
t_{POR}	MIC2590B Power-On Reset Time after VSTBY becomes valid	**Note 5**			500	µs
8-Bit Analog to Digital Converter						
	Total Unadjusted Error Voltage,					
	All Outputs		–3		+3	%
	Current, $3V_{OUT}$[A/B]/$5V_{OUT}$ [A/B]	Measured as voltage across corresponding external R_{SENSE}	–3		+3	%
	Current, V_{AUX}[A/B], $12V_{OUT}$[A/B], $12MV_{OUT}$ [A/B]			±3		%
t_{CONV}	Conversion Time			60	100	ms
	Resolution Specifications:					
V_{AUXA}	Full Scale Voltage			3.85		V
V_{AUXB}	LSB of Voltage			15.1		mV
	Full Scale Current			375		mA
	LSB of Current			1.47		mA
$3V_{OUTA}$	Full Scale Voltage			3.85		V
$3V_{OUTB}$	LSB of Voltage			15.1		mV
	Full Scale Current	External R_{SENSE} = 6.00mΩ		11.6		A
	LSB of Current			45.5		mA
$5V_{OUTA}$	Full Scale Voltage			5.89		V
$5V_{OUTB}$	LSB of Voltage			23.1		mV
	Full Scale Current	External R_{SENSE} = 6.00mΩ		6.96		A
	LSB of Current			27.3		mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
$12V_{OUTA}$	Full Scale Voltage			13.8		V
$12V_{OUTB}$	LSB of Voltage			54.1		mV
	Full Scale Current			6.96		mA
	LSB of Current			27.3		mA
$12MV_{OUTA}$	Full Scale Voltage			–13.6		V
$12MV_{OUTB}$	LSB of Voltage			53.5		mV
	Full Scale Current			100		mA
	LSB of Current			0.392		mA
SMBus Timing, Note 5						
t_1	SCL (Clock) Period	**Figure 1**	2.5			µs
t_2	Data In Set-Up Time to SCL HIGH	**Figure 1**	100			ns
t_3	Data Out Stable after SCL LOW	**Figure 1**	300			ns
t_4	Data LOW Set-Up Time to SCL LOW	Start Condition, **Figure 1**	100			ns
t_5	Data HIGH Hold Time after SCL HIGH	Start Condition, **Figure 1**	100			ns

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. See Applications section.
5. Parameters guaranteed by design. Not 100% production tested.

Test Circuit

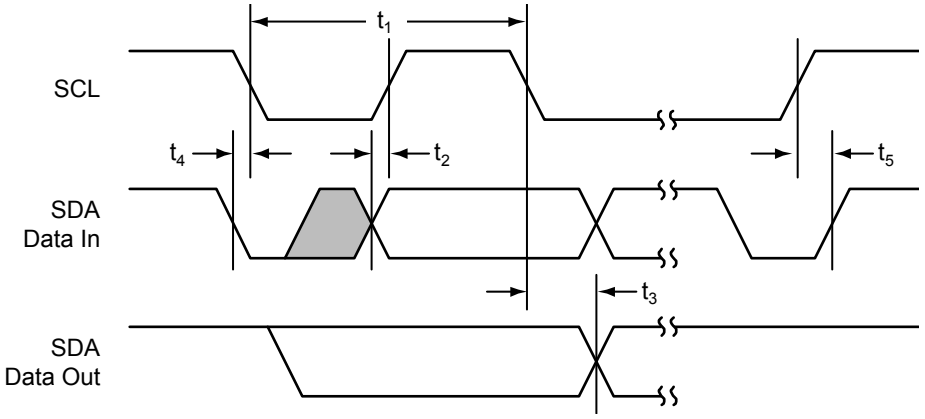


Figure 1. SMBus Timing

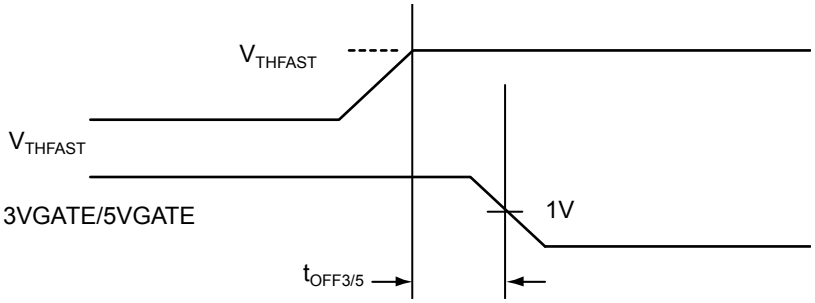


Figure 2. 3V/5V Current Limit Response Timing

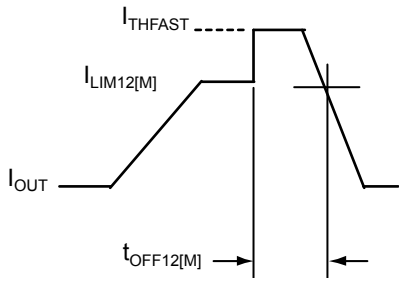


Figure 3. +12V/–12V Current Limit Response Timing

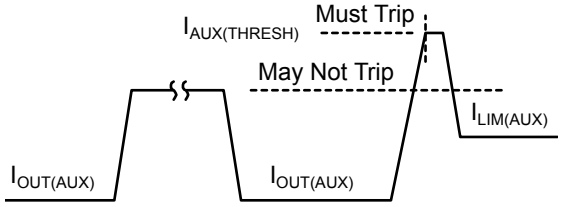


Figure 4. VAUX Current Limit Threshold

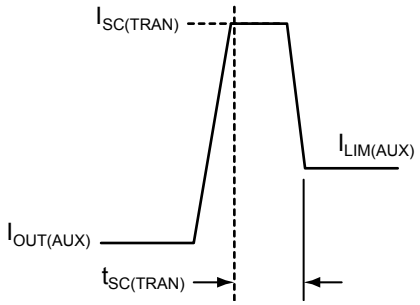


Figure 5. VAUX Current Limit Response Timing

Functional Description

Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages ("hot plugged"), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board's supply pins. This transient inrush current can cause the system's supply voltages to temporarily go out of regulation, causing data loss or system lock-up. In more extreme cases, the transients occurring during a hot plug event may cause permanent damage to connectors or on-board components.

The MIC2590B addresses these issues by limiting the inrush currents to the load (PCI Board), and thereby controlling the rate at which the load's circuits turn on. In addition, the MIC2590B offers input and output voltage supervisory functions and current-limiting to provide robust protection for both the host system and the PCI board.

System Interfaces

The MIC2590B employs two system interfaces. One is the hot plug Interface (HPI) which includes ON[A/B], AUXEN[A/B], and /FAULT[A/B]. The other is the System Management Interface (SMI) consisting of SDA, SCL and /INT, (whose signals conform to the specifications and format of Intel's SMBus standard). The MIC2590B can be operated exclusively from the SMI, or can employ the HPI for power control while continuing to use the SMI for access to all but the power control registers.

In addition to the basic power control features of the MIC2590B accessible by the HPI, the SMI also gives the host access to the following information from the part:

1. Output voltage from each supply.
2. Output current from each supply.
3. Fault conditions occurring on each supply.

When using the System Management Interface for power control, do not use the hot plug Interface. Conversely, when using the HPI for power control, do not execute power control commands over the SMI bus (all other register accesses via the SMI bus remain permissible while in the HPI control mode). Note that if power control is performed via the SMIbus, the AUXENA, AUXENB, ONA and ONB pins should be tied to ground.

Power-On Reset and Power Cycling

The MIC2590B utilizes V_{STBY} as the main supply input source. It is required for proper operation of the MIC2590B SMBus, registers and ADC and must be applied at all times. A Power-On Reset (POR) cycle is initiated after V_{STBY} rises above its UVLO threshold and remains valid at that voltage for 500µs. All internal registers except RESULT are cleared after POR. If V_{STBY} is recycled the MIC2590B enters a new power-on reset cycle. V_{STBY} must be the first supply input applied. Following the POR interval, the MAIN supply inputs of $12V_{IN}$, $12MV_{IN}$, $5V_{IN}$ and $3V_{IN}$ may be applied in any order. The SMBus is ready for access at the end of the POR interval. During t_{POR} all outputs are off.

Power-Up Cycle (See Typical Application Circuit)

When a slot is off, the $5V_{GATE}$ and $3V_{GATE}$ pins are held low with an internal pull-down current source. When a slot's main outputs are enabled, and all input voltages are above their respective undervoltage lockout thresholds, all four main supplies execute a controlled turn on. At this time, the GATE voltages of the 5V and 3.3V MOSFETs are ramped at a controlled rate from 0V to approximately 11.5V. This is sufficient to fully enhance the external MOSFETs for lowest possible DC losses. The ramp rate is controlled by 25µA (typ.) current sources from the GATE pins charging each C_{GATE}. The magnitude and slew rate of the output current is proportional to the value of C_{GATE} and the load capacitance. The minimum value of C_{GATE} is selected to ensure that during start-up the load current does not exceed the current-limit threshold. The following equation is used to determine the value of C_{GATE} (min):

$$C_{GATE}(min) = \frac{I_{GATE}}{I_{LIM}} \times C_{LOAD}$$

Where C_{LOAD} is the load capacitance connected to the 3.3V and 5V outputs and I_{LIM} and I_{GATE} are respectively the current-limit and gate charge current specifications as given in the Electrical Characteristics table. The output slew rate dv/dt is computed by:

$$dv/dt(load) = \frac{I_{GATE}}{C_{GATE} \times 10^6}$$

I_{SLEW} = 25µA	
C_{GATE}	**dv/dt (load)**
0.001µF	25000V/s
0.01µF	2500V/s
0.1µF	250V/s
1µF	25V/s

Table 1. 3.3V/5V Output Slew Rate Selection

For the +12V and –12V supplies, the output slew rate is controlled by capacitors connected to the $12V_{SLEWA}$ and $12V_{SLEWB}$ pins. To determine the minimum value of the slew rate capacitor, (C_{SLEW}), connected to $12V_{SLEW}$[A/B], the following equation is used:

$$C_{SLEW}(min) = \frac{I_{SLEW}}{I_{LIM}} \times C_{LOAD}$$

where C_{LOAD} is the load capacitance connected to the +12V and –12V outputs, and I_{LIM} and I_{SLEW} are respectively the current-limit and slew rate charge current values found in the Electrical Characteristics table. The

equation above computes the minimum value to guarantee the device does not enter into current limit. The slew rate dv/dt is computed by:

$$\text{dv/dt at load} = \frac{I_{SLEW}}{C_{SLEW} \times 10^6}$$

By appropriate selection of the value of C_{SLEW}, it can be ensured that the magnitude of the inrush current never exceeds the current limit for a given load capacitance. Since one capacitor fixes the slew rate for both +12V and –12V, the capacitor value should be chosen to provide the slower slew rate of the two. Table 2 depicts the output slew rate for various values of C_{SLEW}.

I_{SLEW} = 25µA	
C_{GATE}	dv/dt (load)
0.001µF	22000V/s
0.01µF	2200V/s
0.1µF	220V/s
1µF	22V/s

Table 2. ±12V Output Slew Rate Selection

Power Down Cycle

When a slot is turned off, internal switches are connected to each of the outputs to discharge the PCI board's bypass capacitors to ground.

Standby Mode

Standby mode is entered when any one (or more) enabled MAIN supply input(s) ($12V_{IN}$, $12MV_{IN}$, $5V_{IN}$ and $3V_{IN}$) drops below its respective UVLO threshold. The MIC2590B supplies two 3.3V auxiliary outputs, V_{AUX}[A/B], satisfying PCI 2.2 specifications. These outputs are fed via the V_{STBY} input, and controlled by the AUXEN[A/B] inputs or via their SMI bus Control Registers. These outputs are independent of the MAIN outputs: should one or more of the MAIN supply inputs move below its UVLO thresholds, V_{AUX}[A/B] still function as long as V_{STBY} is present. Prior to entering standby mode, ONA and ONB (or the MAINA and MAINB bits in the Control Registers) inputs should be de-asserted. If this is not done, the MIC2590B will assert /FAULT, and also /INT if interrupts are enabled, when the MIC2590B detects an undervoltage condition on a supply input.

Circuit Breaker Functions

The MIC2590B provides an electronic circuit breaker function that protects against excessive loads such as short circuits at each supply. When the current from one or more of a slot's MAIN outputs exceeds the current limit threshold (50mV/R_{SENSE} for 3.3V and 5V, 1.0A for +12V, and/or 0.2Afor –12V) for a duration greater than t_{FLT}, the circuit breaker is tripped and all MAIN supplies (all outputs except V_{AUX}[A/B]) are shut off. Should the load current exceed I_{THFAST} (+12V and –12V), or cause a MAIN output's V_{SENSE} to exceed V_{THFAST} (+3.3V and +5V), the outputs are shut off with no delay. Undervoltage conditions on the MAIN supply inputs also trip the circuit breaker, but only when the MAIN outputs are enabled (to signal a supply input brown-out condition).

The V_{AUX}[A/B] outputs have their own separate circuit breaker functions. V_{AUX} [A/B] do not incorporate a fast-trip threshold, but instead regulate the output current into a fault to avoid exceeding their operating current limit. The circuit breaker will trip due to overcurrents on V_{AUX} [A/B] when the fault timer expires. This use of the t_{FLT} timer prevents the circuit breaker from tripping prematurely due to brief current transients.

Following a fault condition, the outputs can be turned on again via the ON inputs (if the fault occurred on one of the MAIN outputs), via the AUXEN inputs (if the fault occurred on the AUX outputs), or by cycling both ON and AUXEN (if faults occurred on both the MAIN and AUX outputs). A fault condition can alternatively be cleared under SMI control of the ENABLE bits in the C_{NTRL}[A/B] registers. When the circuit breaker trips, /FAULT[A/B] will be asserted if the outputs were enabled through the hot plug Interface (non-SMI mode) inputs. At the same time, /INT will be asserted (unless interrupts are masked). Note that /INT is de-asserted by writing a logic 1 back into the respective fault bit position(s) in the STAT[A/B] register or the Common Status Register.

t_{FLT} is set by external capacitors, C_{FIL}[A/B], connected to the C_{FILTER}[A/B] pins. The equation below can be used to determine the capacitor value for a given duration of t_{FLT}:

$$C_{FIL} \cong 2.0\mu. \times \left(\frac{t_{FLT}}{1\text{second}} \right)$$

Thermal Shutdown

The internal +12V, –12V and VAUX MOSFETs are protected against damage not only by current limiting, but by dual-mode over-temperature protection as well. Each slot controller on the MIC2590B is thermally isolated from the other. Should an overcurrent condition raise the junction temperature of one slot's controller and internal pass elements to 140°C, all of the outputs for that slot (including V_{AUX}) will be shut off, and the slot's /FAULT output will be asserted. The other slot's operation will remain unaffected. However, should the MIC2590B's overall die temperature exceed 160°C, both slots (all outputs, including V_{AUXA} and V_{AUXB}) will be shut off, whether or not a current-limit condition exists. A 160°C overtemperature condition additionally sets the overtemperature bit (OT_INT) in the Common Status Register.

A/D Converter

The MIC2590B has a 20-channel, 8-bit A/D converter capable of monitoring the output voltage and current of each supply. This information is available via the System Management Interface. The information is particularly

intended for use by systems that support the IPMI standard, but may be used for any desired purpose.

Interrupt Generation

In the MIC2590B, the /INT pin can be asserted (driven low) whenever a fault condition trips the circuit breaker. The MIC2590B can thus operate in either polled mode or interrupt mode. In the polled mode, the Interrupt Mask bit in the Common Status Register should be set, to prevent the /INT pin from being asserted. Upon a circuit breaker fault event the appropriate status bit is also set in the corresponding status registers. In order to clear the status bit the system must write a logic 1 back to same bit in the status register. Upon occurrence of the write the /INT pin will be de-asserted (if interrupts were enabled), if no other interrupts are pending. This method of "echo reset" allows data to be retained in the status registers until such time as the system software is ready to deal with that data, and then to control the earliest time at which the next interrupt might occur.

System Management Interface (SMI)

The MIC2590B's System Management Interface uses the Read_Byte and Write_Byte subset of the SMBus protocols to communicate with its host via the System Management Interface bus. Additionally, the /INT output signals the controlling processor that one or more events need attention, if an interrupt-driven architecture is used. Note that theMIC2590B does not participate in the SMBus Alert Response Address (ARA) portion of the SMBus protocol.

The SMBus Read_Byte operation consists of sending the device's slave address, followed by the target register's internal address, and then clocking out the byte to be read from the target register. Similarly, the Write_Byte operation consists of sending the device's slave address, followed by the target register's internal address, and then clocking in the byte to be written to the target register. The target register addresses for the MIC2590B are given in Table 4.

MIC2590B SMBus Address Configuration

The MIC2590B responds to its own unique address which is assigned using A2, A1 and A0. These represent the 3 LSBs of its 7-bit address, as shown in Table 3. These address bits are assigned only during power up of the V_{STBY} supply input. These three bits allow up to eight MIC2590B devices in a single system. These pins are either grounded or left unconnected to specify a logical 0 or 1 respectively. A pin designated as a logical 1 may also be pulled up to V_{STBY}.

Inputs			MIC2590B Slave Addresses	
A2	A1	A0	Binary	Hex
0	0	0	$1000\ 000_b$	80_h
0	0	1	$1000\ 001_b$	82_h
0	1	0	$1000\ 010_b$	84_h
0	1	1	$1000\ 011_b$	86_h
1	0	0	$1000\ 100_b$	88_h
1	0	1	$1000\ 101_b$	$8A_h$
1	1	0	$1000\ 110_b$	$8C_h$
1	1	1	$1000\ 111_b$	$8E_h$

Table 3. MIC2590B SMBus Addressing

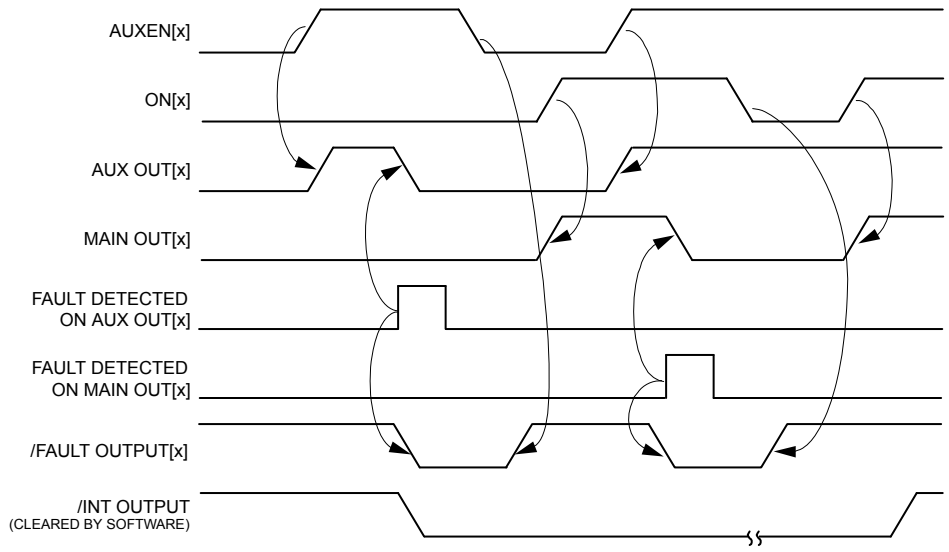


Figure 6. Hot Plug Interface Mode Operation

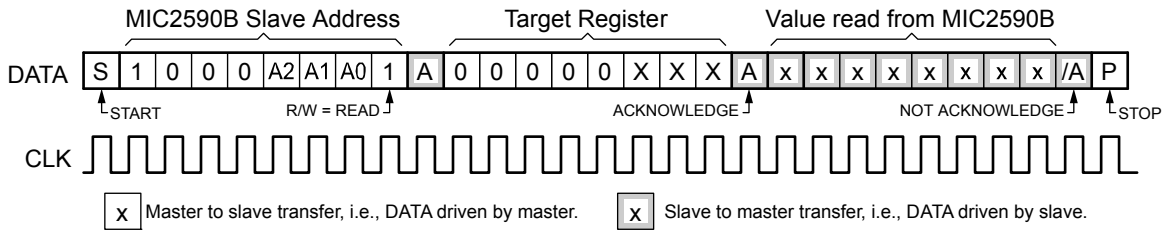


Figure 7. READ_BYTE Protocol

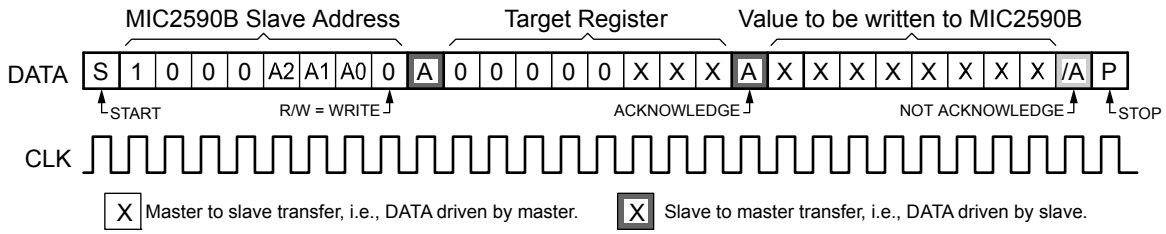


Figure 8. WRITE_BYTE Protocol

Register Set and Programmer's Model

Target Register		Common Byte Value		Power-On Default
Label	**Description**	**Read**	**Write**	
RESULT	ADC Conversion Result Register	00h	n/a	n/a
ADCNTRL	ADC Control Register	01_h	01_h	00_h
CNTRLA	Control Register Slot A	02_h	02_h	00_h
CNTRLB	Control Register Slot B	03_h	03_h	00_h
STATA	Slot A Status	04_h	04_h	00_h
STATB	Slot B Status	05_h	05_h	00_h
STAT	Common Status Register	06_h	06_h	00_h

Detailed Register Descriptions below:

Conversion Result Register (RESULT), 8-Bits Read Only							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-only	D[0] read-only
Voltage or Current Data from ADC							

Bit	Function	Operation
D[7:0]	Measure data from ADC	Read Only

Power-Up Default Value: Undefined following POR
Read Command Byte: $0000\ 0000_b = 00_h$

(ADC Control Register ADCNTRL), 8-Bits Read/Write							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-write	D[3] read-write	D[2] read-write	D[1] read-write	D[0] read-write
Busy	Reserved	Reserved	SEL	PAR	Supply Select SUP[2:0]		

Bit(s)	Function	Operation
BUSY	ADC Status	0 = ADC Quiescent 1 = ADC Busy
D[6]	Reserved	Always Read as Zero
D[5]	Reserved	Always Read as Zero
SEL	A/D Slot Select	Specifies Channel for A/D Conversion 0 = Slot A 1 = Slot B
PAR	Parameter Control Bit for ADC Conversion	0 = Current 1 = Voltage
SUP[2:0]	Supply Select for ADC Conversion	000 = No Conversion 001 = 3.3V Supply 010 = 5.0V Supply 011 = +12V Supply 100 = -12V Supply 101 = VAUX Supply

Power-Up Default Value: $0000\ 0000_b = 00_h$
Command Byte (R/W): $0000\ 0001_b = 01_h$

To operate the ADC the ADCNTRL register must first be initialized by selecting a slot, specifying whether voltage or current is to be measured and then specifying the specific supply that is to be monitored. The software must then wait 100ms, or poll the BUSY bit until it is zero. The RESULT register will then contain the valid result of the conversion.

Control Register, Slot A (CNTRLB), 8-Bits Read/Write							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-write	D[0] read-write
AUXAPG	MAINAPG	Reserved	Reserved	Reserved	Reserved	MAINA	AUXA

Bit(s)	Function	Operation
AUXAPG	AUX Output Power-Good Status, Slot A	1 = Power-Good (VAUXA output is above its V_{UVTH} threshold)
MAINAPG	MAIN Output Power-Good Status, Slot A	1 = Power-Good (MAINA output is above its V_{UVTH} threshold)
D[5]	Reserved	Always Read as Zero
D[4]	Reserved	Always Read as Zero
D[3]	Reserved	Always Read as Zero
D[2]	Reserved	Always Read as Zero
MAINA	MAIN Enable Control, Slot A	0 = OFF, 1 = ON
VAUXA	VAUX Enable Control, Slot A	0 = OFF, 1 = ON

Power-Up Default Value: $0000\ 0000_b = 00_h$
Command Byte (R/W): $0000\ 0010_b = 02_h$

The power-up default value is 00h. Slot A is disabled upon power-up, i.e., all supply outputs are off.

Control Register, Slot B (CNTRLB), 8-Bits Read/Write							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-only	D[2] read-only	D[1] read-write	D[0] read-write
AUXBPG	MAINBPG	Reserved	Reserved	Reserved	Reserved	MAINB	AUXB

Bit(s)	Function	Operation
AUXBPG	AUX Output Power-Good Status, Slot B	1 = Power-Good (VAUXB output is above its V_{UVTH} threshold)
MAINBPG	MAIN Output Power-Good Status, Slot B	1 = Power-Good (MAINB output is above its V_{UVTH} threshold)
D[5]	Reserved	Always Read as Zero
D[4]	Reserved	Always Read as Zero
D[3]	Reserved	Always Read as Zero
D[2]	Reserved	Always Read as Zero
MAINB	MAIN Enable Control, Slot B	0 = OFF, 1 = ON
VAUXB	VAUX Enable Control, Slot B	0 = OFF, 1 = ON

Power-Up Default Value: $0000\ 0000_b = 00_h$
Command Byte (R/W): $0000\ 0011_b = 03_h$

The power-up default value is 00h. Slot B is disabled upon power-up, i.e., all supply outputs are off.

Status Register, Slot A (STATA), 8-Bits Read Only							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-write	D[3] read-write	D[2] read-write	D[1] read-write	D[0] read-write
FAULTA	MAINA	VAUXA	VAUXAF	12MVAF	12VAF	5VAF	3VAF

Bit(s)	Function	Operation
FALUTA	FAULT Pin Status, Slot A	Notes 1 & 2
MAINA	MAIN Enable Status, Slot A	Represents actual state (on/off) of the four main power outputs for Slot A. (+12V, +5V, +3.3V and -12V) 1 = MAIN Power On 0 = MAIN Power Off
VAUXA	VAUX Enable Status, Slot A	Represents actual state (on/off) of the auxiliary power outputs for Slot A. 1 = MAIN Power On 0 = MAIN Power Off
VAUXFA	Overcurrent Fault VAUX Supply	1 = Fault 0 = No Fault
12MVFA	Overcurrent Fault -12V Supply	1 = Fault 0 = No Fault
12VFA	Overcurrent Fault 12V Supply	1 = Fault 0 = No Fault
5VFA	Overcurrent Fault 5V Supply	1 = Fault 0 = No Fault
3VFA	Overcurrent Fault 3V Supply	1 = Fault 0 = No Fault

Power-Up Default Value: $0000\ 0000_b = 00_h$

Read Command Byte (R/W): $0000\ 0100_b = 04_h$

The power-up default value is 00h. The slot is disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and de-assert /INT. The status of the /FAULTA pin is not affected by reading the Status Register.

Status Register, Slot B (STATB), 8-Bits Read Only							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-write	D[3] read-write	D[2] read-write	D[1] read-write	D[0] read-write
FAULTB	MAINB	VAUXB	VAUXBF	12MVBF	12VBF	5VBF	3VBF

Bit(s)	Function	Operation
FALUTB	FAULT Pin Status, Slot B	Notes 1 & 2
MAINB	MAIN Enable Status, Slot B	Represents actual state (on/off) of the four main power outputs for Slot B. (+12V, +5V, +3.3V and -12V) 1 = MAIN Power On 0 = MAIN Power Off
VAUXB	VAUX Enable Status, Slot B	Represents actual state (on/off) of the auxiliary power outputs for Slot B. 1 = MAIN Power On 0 = MAIN Power Off
VAUXFB	Overcurrent Fault VAUX Supply	1 = Fault 0 = No Fault
12MVFB	Overcurrent Fault -12V Supply	1 = Fault 0 = No Fault
12VFB	Overcurrent Fault 12V Supply	1 = Fault 0 = No Fault
5VFB	Overcurrent Fault 5V Supply	1 = Fault 0 = No Fault
3VFB	Overcurrent Fault 3V Supply	1 = Fault 0 = No Fault

Power-Up Default Value: $0000\ 0000_b = 00_h$

Read Command Byte (R/W): $0000\ 0101_b = 05_h$

The power-up default value is 00h. The slot is disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and de-assert /INT. The status of the /FAULTB pin is not affected by reading the Status Register.

Note 1. 1 = /FAULT[A/B] pin asserted, indicating a fault condition (/FAULT is LOW).

0 = /FAULT[A/B] pin is de-asserted (/FAULT is HIGH).

If FAULT[A/B] has been set by an overcurrent condition on one (or more) of the main outputs, the corresponding ON[A/B] must go LOW to reset FAULT. If FAULT[A/B] has been set by an overcurrent on a VAUX output, the corresponding AUXEN[A/B] must go LOW to reset FAULT. If an overcurrent has occurred on both a main output and VAUX output of a slot, both ON[A/B] and AUXEN[A/B] of the corresponding slot must go LOW to reset FAULT.

Note 2. The FAULT bits, and the /FAULT pins, are not active when the MIC2590B power paths are controlled by the System Management Interface (SMBus). When using SMI power path control for a slot, the AUXEN and ON pins for that slot must be tied to ground.

Common Status Register, (STAT), 8-Bits Read/Write							
D[7] read-only	D[6] read-only	D[5] read-only	D[4] read-only	D[3] read-write	D[2] read-write	D[1] read-write	D[0] read-only
Reserved	Reserved	GPIB	GPIA	INTMSK	UV_INT	OT_INT	Reserved

Bit(s)	Function	Operation
D[7]	Reserved	Always read as zero
D[6]	Reserved	Always read as zero
GPIB	General Purpose Input, Slot B	State of GPIB pin
GPIA	General Purpose Input, Slot A	State of GPIA pin
INTMSK	Interrupt Mask	0 = /INT generation is enabled 1 = /INT generation is disabled. The MIC2590B does not participate in the SMBus Alert Response Address (ARA) Protocol.
UV_INT	Undervoltage Interrupt	Set whenever a circuit Interrupt breaker fault condition occurs as a result of an undervoltage lockout condition on one of the main supply inputs. This bit is only set if a UVLO condition occurs while one or both of the ON[A/B] pins are asserted or the MAIN[A/B] enable control bits are set.
OT_INT	Overtemperature Interrupt	Set whenever a circuit breaker fault occurs as a result of an overtemperature condition exceeding 160°C shutting both channels off.
D[0]	Reserved	Read Undefined

Power-Up Default Value: $0000\ 0000_b = 00_h$

Command Byte (R/W): $0000\ 0110_b = 06_h$

To reset the OT_INT and UV_INT fault bits a logical 1must be written back to these bits.

Application Information

Current Sensing

For the three power supplies switched with internal MOSFETs (+12V, –12V, and V_{AUX}), the MIC2590B provides all necessary current sensing functions to protect the IC, the load, and the power supply. For the remaining four supplies which the part is designed to control, the high currents at which these supplies typically operate makes sensing the current inside the MIC2590B impractical. Therefore, each of these supplies (3VA, 5VA, 3VB, and 5VB) requires an external current sensing resistor. The V_{IN} connection to the IC from each supply (e.g., $5V_{INA}$) is connected to the positive terminal of the slot's current sense amplifier, and the corresponding SENSE input (in this case, $5V_{SENSEA}$) is connected to the negative terminal of the current sense amplifier.

Sense Resistor Selection

The MIC2590B uses low-value sense resistors to measure the current flowing through the MOSFET switches to the loads. These sense resistors are nominally valued at $50m\Omega/I_{LOAD(CONT)}$. To accommodate worst-case tolerances for both the sense resistor, (allow ±3% over time and temperature for a resistor with ±1% initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used.

The current limit threshold voltage (the "trip point") for the MIC2590B may be as low as 35mV, which would equate to a sense resistor value of $35m\Omega/I_{LOAD(CONT)}$. Carrying the numbers through for the case where the value of the sense resistor is 3% high, this yields:

$$R_{SENSE} = \frac{35m\Omega}{(1.03)(I_{LOAD(CONT)})} = \frac{34m\Omega}{I_{LOAD(CONT)}}$$

Once the value of R_{SENSE} has been chosen in this manner, it is good practice to check the maximum $I_{LOAD(CONT)}$ which the circuit may let through in the case of tolerance build-up in the opposite direction. Here, the worst-case maximum is found using a 65mV trip voltage and a sense resistor which is 3% low in value. The resulting current is:

$$I_{LOAD(CONT,MAX)} = \frac{65m\Omega}{(0.97)(R_{SENSE(NOM)})} = \frac{67m\Omega}{R_{SENSE(NOM)}}$$

As an example, if an output must carry a continuous 4.4A without nuisance trips occurring, R_{SENSE} for that output should be 34mΩ/4.4A = 7.73mΩ. The nearest standard value is 7.5mΩ, so a 7.5mΩ ±1% resistor would be a good choice. At the other set of tolerance extremes, $I_{LOAD(CONT,\ MAX)}$ for the output in question is then simply 67mV/7.5mΩ = 8.93A. Knowing this final datum, we can determine the necessary wattage of the sense resistor, using $P = I^2R$. Here I will be $I_{LOAD(CONT,\ MAX)}$, and R will be $(0.97)(R_{SENSE(NOM)})$. These numbers yield the following:

$$P_{MAX} = (8.93A)^2 (7.28m\Omega) = 0.581W$$

A 1.0W sense resistor would work well in this application.

Kelvin Sensing

Because of the low values of the sense resistors, special care must be used to accurately measure the voltage drop across them. Specifically, the voltage across each R_{SENSE} must employ Kelvin sensing. This is simply a means of making sure that any voltage drops in the power traces connecting to the resistors are not picked up in addition to the voltages across the sense resistors themselves. If accuracy must be paid for, it's worth keeping.

Figure 9 illustrates how Kelvin sensing is performed. As can be seen, all the high current in the circuit (let us say, from $+5V_{INA}$ through R_{SENSE} and then to the drain of the +5VA output MOSFET) flows directly through the power PCB traces and R_{SENSE}. The voltage drop resulting across R_{SENSE} is sampled in such a way that the high currents through the power traces will not introduce any extraneous IR drops.

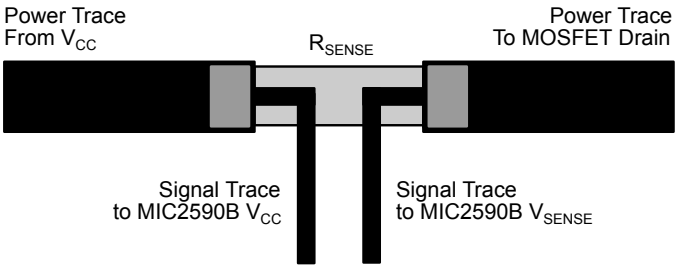


Figure 9. Kelvin Sensing Connections for R_{SENSE}

MOSFET Selection

Selecting the proper MOSFET for use as current pass and switching element for each of the 3V and 5V slots of the MIC2590B involves four straight forward tasks:

1. Choice of a MOSFET which meets the minimum voltage requirements.
2. Determination of maximum permissible on-state resistance [$R_{DS(ON)}$].
3. Selection of a device to handle the maximum continuous current (steady-state thermal issues).
4. Verification of the selected part's ability to withstand current peaks (transient thermal issues).

MOSFET Voltage Requirements

The first voltage requirement for each MOSFET is easily stated: the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$ for the slot in question. For instance, the 5V input may reasonably be expected to see high-frequency transients as high as 5.5V. Therefore, the drain-source breakdown voltage of the MOSFET must be at least 6V.

The second breakdown voltage criteria which must be met is a bit subtler than simple drain-source breakdown voltage, but is not hard to meet. Low-voltage MOSFETs generally have low breakdown voltage ratings from gate to source as well. In MIC2590B applications, the gates of the external MOSFETs are driven from the +12V input to the IC. That supply may well be at 12V + (5% x 12V) = 12.6V. At the same time, if the output of the MOSFET (its source) is suddenly shorted to ground, the gate-source voltage will go to (12.6V – 0V) = 12.6V. This means that the external MOSFETs must be chosen to have a gate-source breakdown voltage in excess of 13V; after 12V absolute maximum the next commonly available voltage class has a permissible gate-source voltage of 20V maximum. This is a very suitable class of device. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source breakdown rating or higher. As a general tip, look to surface mount devices with a drain-source rating of 30V as a starting point.

MOSFET Maximum On-State Resistance

The MOSFETs in the +3.3V and +5V MAIN power paths will have a finite voltage drop, which must be taken into account during component selection. A suitable MOSFET's datasheet will almost always give a value of on resistance for the MOSFET at a gate-source voltage of 4.5V, and another value at a gate-source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on resistance of the device with 7 Volts of enhancement (keep this in mind; we'll use it in the following Thermal Issues sections). The resulting value is conservative, but close enough. Call this value R_{ON}. Since a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that is required to calculate the voltage drop across the MOSFET is to multiply the maximum current times the MOSFET's R_{ON}. The one addendum to this is that MOSFETs have a slight increase in R_{ON} with increasing die temperature. A good approximation for this value is 0.5% increase in R_{ON} per °C rise in junction temperature above the point at which R_{ON} was initially specified by the manufacturer. For instance, the Vishay (Siliconix) Si4430DY, which is a commonly used part in this type of application, has a specified $R_{DS(ON)}$ of 8.0mΩ max. at V_{G-S} = 4.5V, and $R_{DS(ON)}$ of 4.7mΩ max. at V_{G-S} =10V. Then R_{ON} is calculated as:

$$R_{ON} = \frac{(4.7m\Omega + 8.0m\Omega)}{2} = 6.35m\Omega$$

at 25°C T_J. If the actual junction temperature is estimated to be 110°C, a reasonable approximation of R_{ON} for the Si4430DY at temperature is:

$$6.35m\Omega\left[1+(100^\circ - 25^\circ)\left(\frac{0.5\%}{^\circ C}\right)\right] = 6.35m\Omega\left[1+(85^\circ)\left(\frac{0.5\%}{^\circ C}\right)\right] \cong 9.05m\Omega$$

Note that this is not a closed-form equation; if more precision were required, several iterations of the calculation might be necessary. This is demonstrated in the section "MOSFET Transient Thermal Issues."

For the given case, if Si4430DY is operated at an I_{DRAIN} of 7.6A, the voltage drop across the part will be approximately (7.6A)(9.05mΩ) = 69mV.

MOSFET Steady-State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of $I_{LOAD(CONT,\ MAX)}$ for the output in question (see Sense Resistor Selection).
- The manufacturer's data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., Can heat be dissipated into the ground plane or power plane, if using a surface mount part? Is any airflow available?).

Now it gets easy: steady-state power dissipation is found by calculating I^2R. As noted in "MOSFET Maximum On-State Resistance," above, the one further concern is the MOSFET's increase in R_{ON} with increasing die temperature. Again, use the Si4430DY MOSFET as an example, and assume that the actual junction temperature ends up at 110°C. Then R_{ON} at temperature is again approximately 9.05mΩ. Again, allow a maximum I_{DRAIN} of 7.6A:

$$\text{Power Dissipation} \cong I_{DRAIN}^2 \times R_{ON} = (7.6A)^2 \times 9.05m\Omega \cong 0.523W$$

The next step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET's performance was specified by the manufacturer. Formally put, the steady-state electrical model of power dissipated at the MOSFET junction is analogous to a current source, and anything in the path of that power being dissipated as heat into the environment is analogous to a resistor. It's therefore necessary to verify that the thermal resistance from the junction to the ambient is equal to or lower than that value of thermal resistance (often referred to as $R_{\theta(JA)}$) for which the operation of the part is guaranteed. As an applications issue, surface mount MOSFETs are often less than ideally specified in this regard—it's become common practice simply to state that the thermal data for the part is specified under the conditions "Surface mounted on FR-4 board, t≤10seconds," or something equally mystifying. So here are a few practical tips:

1. The heat from a surface mount device such as an SO-8 MOSFET flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more of copper the copper will act as the heat sink for the part. This copper must be on the same layer of the board as

the MOSFET drain.

2. Since the rating for the part is given as "for 10seconds," derate the maximum junction temperature by 35°C. This is the standard good practice derating of 25°C, plus another 10°C to allow for the time element of the specification.
3. Airflow, if available, works wonders. This is not the place for a dissertation on how to perform airflow calculations, but even a few LFM (linear feet per minute) of air will cool a MOSFET down dramatically. If you can position the MOSFET(s) in question near the inlet of a power supply's fan, or the outlet of a processor's cooling fan, that's always a good free ride.
4. Although it seems a rather unsatisfactory statement, the best test of a surface-mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. The ideal evaluation is in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or in infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

MOSFET Transient Thermal Issues

Having chosen a MOSFET that will withstand the imposed voltage stresses, and be able to handle the worst-case continuous I^2R power dissipation which it will see, it remains only to verify the MOSFET's ability to handle short-term overload power dissipation without overheating. Here, nature and physics work in our favor: a MOSFET can handle a much higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that, like everything else, semiconductor devices (silicon die, lead frames, etc.) have thermal inertia. This is easily understood by all of us who have stood waiting for a pot of water to boil.

In terms related directly to the specification and use of power MOSFETs, this is known as "transient thermal impedance." Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve, which is a handy tool for making sure that you can safely get by with a less expensive MOSFET than you thought you might need. For example, take the case where t_{FLT} for the 5V supply has been set to 50ms, $I_{LOAD(CONT,MAX)}$ is 5.0A, the slow-trip threshold is 50mV nominal, and the fast-trip threshold is 100mV. If the output is connected to a 0.60Ω load, the output current from the MOSFET for the slot in question will be regulated to 5.0A for 50ms before the part's circuit breaker trips. During that time, the dissipation in the MOSFET is given by:

$$P = E \times I \; E_{MOSFET} = [5V - 5A(0.6\Omega A] = 2V$$

$$P_{MOSFET} = (2V \times 5A) = 10W \text{ for } 50ms$$

Wow! Looks like we need a really hefty MOSFET to withstand just this unlikely—but plausible enough to protect against—fault condition. Or do we? This is where the transient thermal impedance curves become very useful. Figure 10 shows those curves for the Vishay (Siliconix) Si4430DY, a commonly used SO-8 power MOSFET.

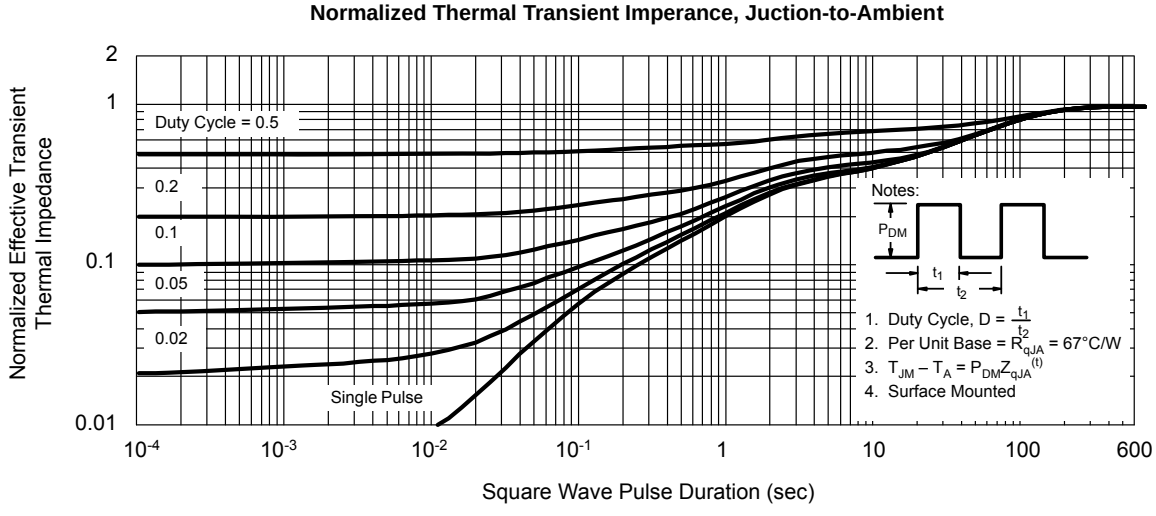


Figure 10. Si4430DY MOSFET Transient Thermal Impedance Curve

Using this graph is not nearly as daunting as it may at first appear. Taking the simplest case first, we'll assume that once a fault event such as the one in question occurs, it will be along time, 10 minutes or more, before the fault is isolated and the slot is reset. In such a case, we can approximate this as a "single pulse" event, that is to say, there's no significant duty cycle. Then, reading up from the X-axis at the point where "Square Wave Pulse Duration" is equal to 0.1sec (=100ms), we see that the effective thermal impedance of this MOSFET to a single pulse event of this duration is only 6% of its continuous $R_{\theta(JA)}$.

This particular part is specified as having an $R_{\theta(JA)}$ of 50°C/W for intervals of 10 seconds or less. So, some further math, just to get things ready for the finale:

Assume T_A = 55°C maximum, 1 square inch of copper at the drain leads, no airflow.

Assume the MOSFET has been carrying just about 5A for some time.

Then the starting (steady-state)T_J is:

$$T_J \cong 55°C + (7.3m\Omega)(5A)^2(30°C/W)$$

$$T_J \cong 60.5°C$$

Iterate the calculation once to see if this value is within a few percent of the expected final value. For this iteration we will start with T_J equal to the already calculated value of 67°C:

R_{ON} at T_J = 60.5°C =[1+(60.5°C–25°)(0.5%/°C)]×6.35mΩ

$$R_{ON} \text{ at } T_J = 60.5°C \cong 7.48m\Omega$$

$$T_J \cong 55°C + (7.3m\Omega)(5A)^2(30°C/W)$$

$$T_J \cong 60.6°C$$

At this point, the simplest thing to do is to approximate T_J as 61°C, which will be close enough for all practical purposes.

Finally, add (10W)(67°C/W)(0.03) = 21°C to the steady-state T_J to get $T_{J(TRANSIENT\ MAX)}$ = 82°C. The Si4430DY can easily handle this value of $T_{J(MAX)}$.

A second illustration of the use of the transient thermal impedance curves: assume that the system will attempt multiple retries on a slot showing a fault, with a one second interval between retry attempts. This frequency of restarts will significantly increase the dissipation in the Si4430DY MOSFET. Will the MOSFET be able to handle the increased dissipation? We get the following:

The same part is operating into a persistent fault, so it is cycling in a square-wave fashion (no steady-state load) with a duty cycle of (50msec/second = 0.05).

On the Transient Thermal Impedance Curves, read up from the X-axis to the line showing Duty Cycle equaling 0.05. The effective $R_{\theta(JA)}$ = (0.7 x 67°C/W) = 4.7°C/W.

Calculating the peak junction temperature:

$$T_{J(PEAK\ MAX)} = [(10W)(4.7°C/W) + 55°C] = 102°C$$

And finally, checking the RMS power dissipation just to be complete:

$$P_{RMS} = (5A)^2(7.47m\Omega)\sqrt{0.05} = 0.042W$$

which will result in a negligible temperature rise.

The Si4430DY is electrically and thermally suitable for this application.

MOSFET and Sense Resistor Selection Guide

Listed below, by Manufacturer and Type Number, are some of the more popular MOSFET and resistor types used in PCI hot plug applications. Although far from comprehensive, this information will constitute a good starting point for most designs.

MOSFET Vendors	Key MOSFET Type(s)	Web Address
Vishay (Siliconix)	Si4430DY ("LittleFoot" Series) Si4420DY ("LittleFoot" Series)	www.siliconix.com
International Rectifier	IRF7413A (SO-8 package part) Si4420DY (second source to Vishay)	www.irf.com
Fairchild Semiconductor	FDS6644 (SO-8 package part) FDS6670A (SO-8 package part) FDS6688 (SO-8 package part)	www.fairchildsemi.com

Resistor Vendors	Sense Resistors	Web Address
Vishay (Dale)	"WSL" Series	www.vishay.com/docs/wsl_30100.pdf
IRC	"OARS" Series "LR" Series (second source to "WSL")	irctt.com/pdf_files/OARS.pdf irctt.com/pdf_files/LRC.pdf

Power Supply Decoupling

In general, prudent system design requires that power supplies used for logic functions should have less than 100mV of noise at frequencies of 100kHz and above. This is especially true given the speeds of moden logic families, such as the 1.2micron CMOS used in the MIC2590B. In particular, the –12V supply should have less than 100mV of peak-to-peak noise at frequencies of 1MHz or higher. This is because the –12V supply is the most negative potential applied to the IC, and is therefore connected to the device's substrate. All of the subcircuits integrated onto the silicon chip are hence subjected by capacities coupling to any HF noise on the –12V supply. While individual capacitances are quite low, the amount of injected energy required to cause a "glitch" can also be quite low at the internal nodes of high speed logic circuits.

Less obviously, but equally important, is the fact that the internal charge pump for the $3.3V_{AUX}$ supplies is somewhat susceptible to noise on the +12V input when that input is at or near zero volts. The +12V supply should not carry HF noise in excess of 200mV peak-to-peak with respect to chip ground when it is in the "off" state.

If either the –12V input, the +12V input, of both supplies do carry significant HF noise (as can happen when they are locally derived by a switching converter), the solution is both small and inexpensive. An LC filter made of a ferrite bead between the noisy power supply input and the MIC2590B, followed by a "composite capacitor" from the affected MIC2590B input pin to ground will suffice for almost any situation. A good composite capacitor for this purpose is the parallel combination of a 47µF tantalum bulk decoupling capacitor, and one each 1µF and 0.01µF ceramic capacitors for high-frequency bypass. A suggested ferrite bead for such use is Fair-Rite Products Corporation part number 2743019447 (this is a surface-mountable part). Similar parts from other vendors will also work well, or a 0.27µH, air-core coil can be used.

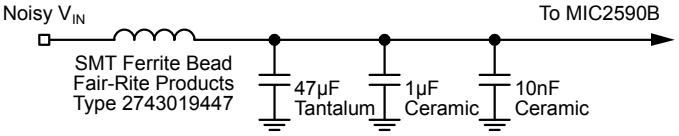


Figure 11. Filter Circuit for Noisy Supplies (+3.3V and/or –12V)

It is theoretically possible that high-amplitude, HF noise reflected back into one or both of the MIC2590B's –12V outputs could interfere with proper device operation, although such noisy loads are unlikely to occur in the real world. If this becomes an application-specific concern, a pair of filters similar to that in Figure 11 will provide the required HF bypassing. The capacitors would be connected to the MIC2590B's –12V output pins, and the ferrite beads would be placed between the –12V output pins and the loads.

–12V Input Clamp Diode

The –12V input to the MIC2590B is the most negative potential on the part, and is therefore connected to the chip's substrate (as described in "Power Supply Decoupling," above). Although no particular sequencing of the –12V supply relative to the other MIC2590B supplies is required for normal operation, this substrate connection does mean that the –12V input must never exceed the voltage on the GROUND pin of the IC by more than 0.3 volts. In some systems, even though the –12V supply will discharge towards ground potential when it is turned OFF, the possibility exists that power supply output ringing or L(di/dt) effects in the wiring and on the PCB itself will cause brief transient voltages in excess of +0.3V to appear at the –12V input. The simplest way to deal with such a transient is to clamp it with a Schottky diode. The diode's a node should be physically placed directly at the –12V input to the MIC2590B, and its cathode should have as short a path as possible back to the part's ground. A good SMT part for this application is ON Semiconductor's type MBRS140T3 (1A, 40V). Although the 40V rating of this part is a bit gratuitous, it is an inexpensive industry-standard part with many second sources. Unless it is absolutely known in advance that the voltage on the "–12V" inputs will never exceed 0.0V at the IC's –12V input pins, it's wise to at least leave a position for this diode in the board layout and then remove it later. This final determination should be made by observations of the voltage at the –12V input with a fast storage oscilloscope, under turn-on and turn-off conditions.

Gate Resistor Guidelines

The MIC2590B controls four external power MOSFETs, which handle the high currents for each of the two 3.3V and 5V outputs. A capacitor (C_{GATE}) is connected in the application circuit from each GATE pin of the MIC2590B to ground. Each C_{GATE} controls the ramp-up rate of its respective power output (e.g., $5V_{OUTB}$). These capacitors, which are typically in the 10nF range, cause the GATE outputs of the MIC2590B to have very low AC impedances to ground at any significant frequency. It is therefore necessary to place a modest value of gate damping resistance (R_{GATE}) between each C_{GATE} and the gate of its associated MOSFET. These resistances prevent high-frequency MOSFET source-follower oscillations from occurring. The exact value of the resistors used is not critical; 47Ω is usually a good choice. Each R_{GATE} should be physically located directly adjacent to the MOSFET gate lead to which it connects.

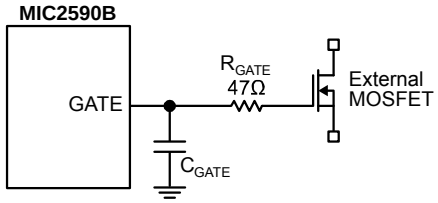
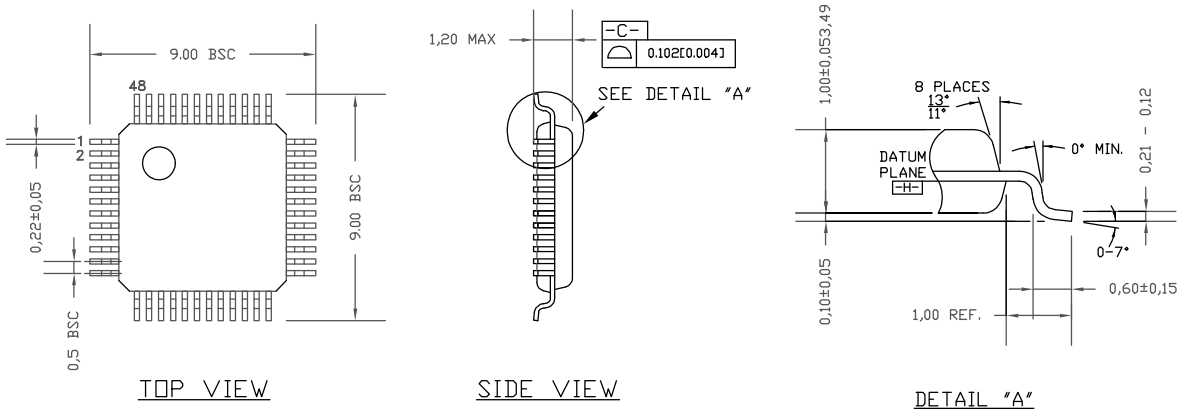
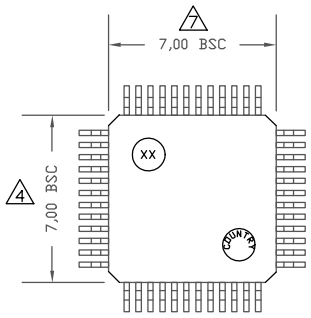


Figure 12. Proper Connection of C_{GATE} and R_{GATE}

Package Information





NOTES:

1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254MM.
2. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
3. PACKAGE TOP MOLD DIMENSIONS ARE SMALLER THAN BOTTOM
4. MOLD DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

48-Pin TQFP (TQ)

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