MIC59P60

8-Bit Serial-Input Protected Latched Driver

General Description

The MIC59P60 serial-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, CLOCK, SERIAL DATA INPUT, and OUTPUT ENABLE functions. Additional protection circuitry supplied on this device includes thermal shutdown, undervoltage lockout (UVLO), and overcurrent shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC59P60 has open-collector outputs capable of sinking 500mA, and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

Using a 5V logic supply, the MIC59P60 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds can be obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors. By using the serial data output, drivers may be cascaded for interface applications requiring additional drive lines.

Each of the eight outputs has an independent overcurrent shutdown of 500mA. Upon over-current shutdown, the affected channel will turn OFF, and the flag will go low until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2µs will not activate current shutdown.

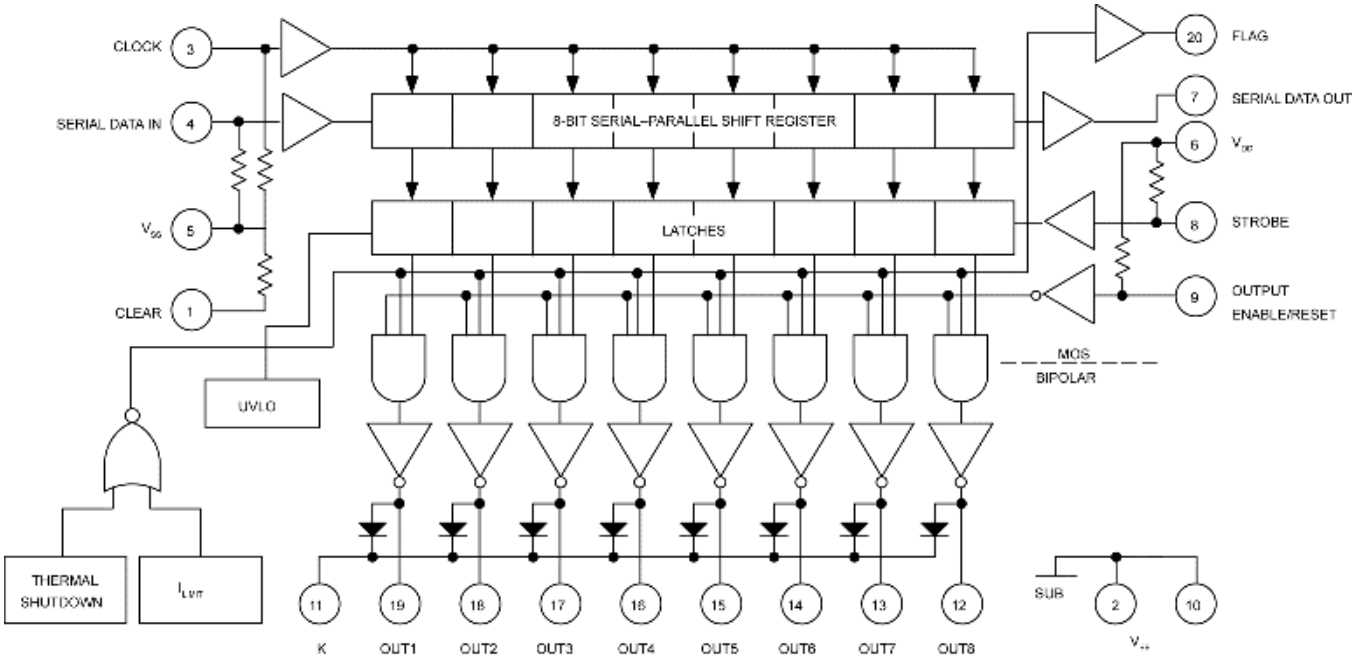
Temperatures above 165°C will shut down the device and activate the error flag. The UVLO circuit prevents operation at low V_{DD}; hysteresis of 0.5V is provided.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- 3.3MHz minimum data input rate
- Output current shutdown (500mA typical)
- Undervoltage lockout
- Thermal shutdown
- Output fault flag
- CMOS, PMOS, NMOS, and TTL compatible
- Internal pull-up/pull-down resistors
- Low-power CMOS logic and latches
- High-voltage current sink outputs
- Output transient-protection diodes
- Single or split supply operation

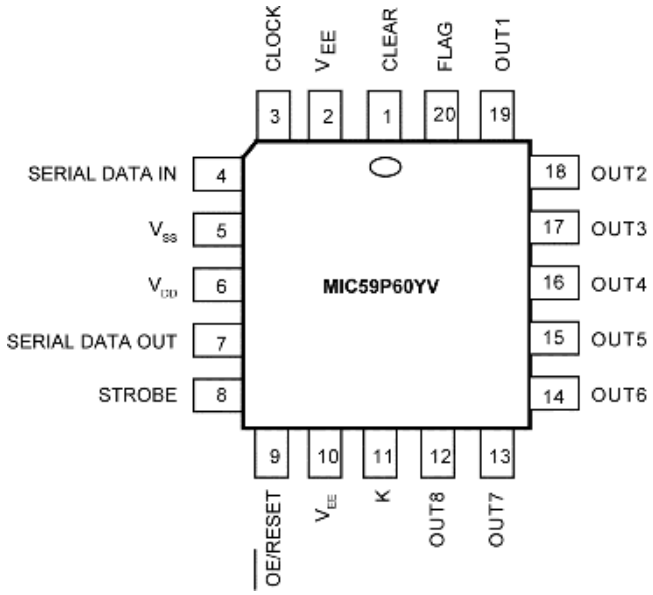
Functional Diagram



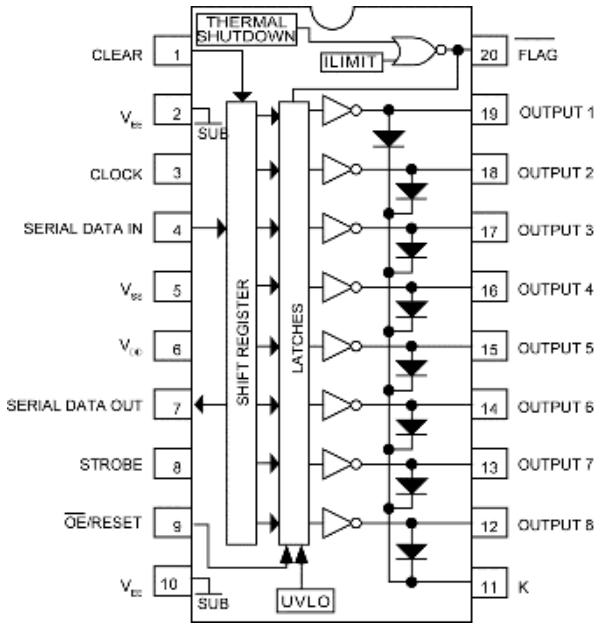
Ordering Information

Part Number	Junction Temperature Range	Package	Pb-Free
MIC59P60YN	–40°C to +85°C	20-Pin Plastic DIP	√
MIC59P60YV	–40°C to +85°C	20-Pin PLCC	√
MICP60YWM	–40°C to +85°C	20-Pin Wide SOIC	√

Pin Configuration



20-Pin PLCC (V)
(Top View)



20-Pin PDIP (N)
20-Pin Wide SOIC (WM)
(Top View)

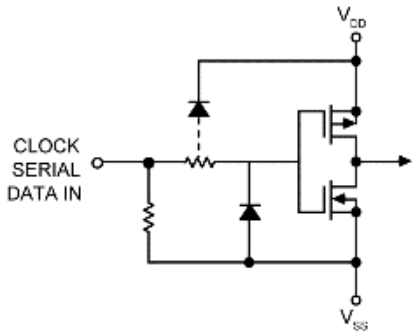
Pin Description

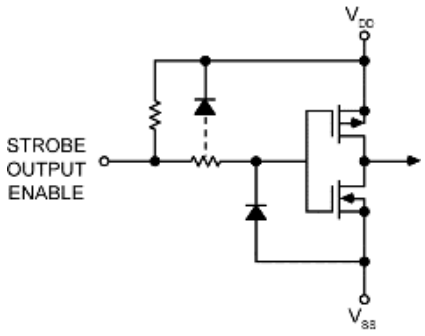
Pin Number	Pin Name	Pin Function
1	CLEAR	Sets All Latches OFF (open).
2, 10	VEE	Output Ground (Substrate). Most negative voltage in the system connects here.
3	CLOCK	Serial Data Clock. A CLEAR must also be clocked into the latches.
4	SERIAL DATA IN	Serial Data Input pin.
5	VSS	Logic reference (Ground) pin.
6	VDD	Logic Positive Supply voltage.
7	SERIAL DATA OUT	Serial Data Output pin. (Flow through).
8	STROBE	Output Strobe pin. Loads output latches when High. A STROBE is needed to CLEAR latches.
9	$\overline{OE}$ / RESET	When low, outputs are active. When high, device is inactive and reset from a fault condition. An under voltage condition emulates a high $\overline{OE}$/RESET input.

Pin Description (Continued)

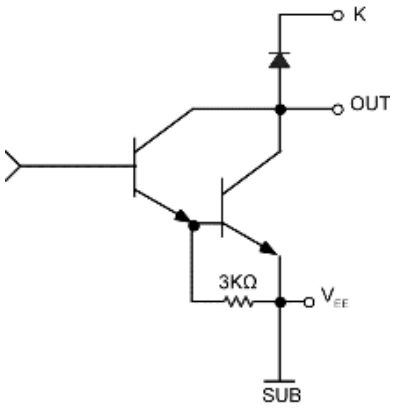
Pin Number	Pin Name	Pin Function
11	K	Transient suppression diode's cathode common pin.
12 – 19	OUT N	Open collector outputs 8 through 1.
20	$\overline{\text{FLAG}}$	Error flag. Open-collector output is low upon overcurrent or overtemperature fault. $\overline{\text{OE}}$/RESET must be pulled high to reset the flag and fault condition.

Typical Inputs





Typical Output Driver



Absolute Maximum Ratings[1]

Output Voltage (V_{CE}) ..... +80V
Output Voltage ($V_{CE(SUS)}$)[3] ..... +50V
Supply Voltage (V_{DD}) with reference to V_{SS} ..... +15V
Supply Voltage (V_{DD}) with reference to V_{EE} ..... +25V
Emitter Supply Voltage (V_{EE}) ..... –20V
Input Voltage Range (V_{IN}) ..... –0.3V to V_{DD} +0.3V
Protective Current[4] 1.5A
Storage Temperature Range (T_S) ..... –65°C to +150°C
ESD Rating[5][6] ..... ESD Sensitive

Operating Ratings[2]

Package Power Dissipation, P_D
Plastic DIP (N) 2.0W
Derate above T_A = +25°C ..... 20mW/°C
PLCC (V) 1.4W
Derate above T_A = +25°C ..... 16mW/°C
Wide SOIC (WM) 1.2W
Derate above TA = +25°C ..... 12mW/°C
Operating Temperature Range (T_A) ..... –40°C to +85°C

Electrical Characteristics[7]

V_{DD} = 5V, V_{SS} = V_{EE} = 0V; T_A = +25°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CEX}	Output Leakage Current	V_{OUT} = 80V			50	µA
		V_{OUT} = 80V, T_A = 70°C		100		
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	I_{OUT} = 100mA		0.9	1.1	V
		I_{OUT} = 200mA		1.1	1.3	
		I_{OUT} = 350mA		1.3	1.6	
$V_{CE(SUS)}$	Collector-Emitter Sustaining Voltage	I_{OUT} = 350mA, L = 2mH	50			V
$V_{IN(0)}$	Input Voltage				1.0	V
$V_{IN(1)}$		V_{DD} = 12V	10.5			V
		V_{DD} = 10V	8.5			
		V_{DD} = 5V[8]	3.5			
R_{IN}	Input Resistance	V_{DD} = 12V	50	200		kΩ
		V_{DD} = 10V	50	300		
		V_{DD} = 5V	50	600		
I_{OL}	$\overline{\text{Flag}}$ Output Current	V_{OL} = 0.4V		15		mA
I_{OH}	$\overline{\text{Flag}}$ Output Leakage			50		nA

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. For inductive load applications.
4. Each channel. VEE connection must be designed to minimize inductance and resistance.
5. Devices are input-static protected but can be damaged by extremely high static charges.
6. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
7. Specification for packaged product only
8. Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

Electrical Characteristics[7]

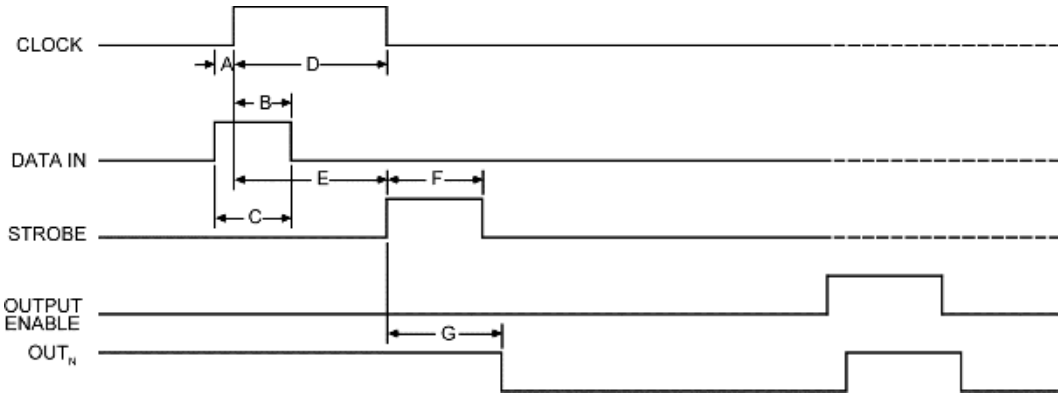
V_{DD} = 5V, V_{SS} = V_{EE} = 0V; T_A = +25°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DD(ON)}$	Supply Current	All Drivers ON, V_{DD} = 12V		6.4	10.0	mA
		All Drivers ON, V_{DD} = 10V		6.0	9.0	
		All Drivers ON, V_{DD} = 5V		4.6	7.5	
$I_{DD(1\ OUTPUT)}$		One Driver ON, All others OFF, V_{DD} = 12V		3.1	4.5	mA
		One Driver ON, All others OFF, V_{DD} = 10V		2.9	4.5	
		One Driver ON, All others OFF, V_{DD} = 5V		2.3	3.6	
$I_{DD(OFF)}$		All Drivers OFF, V_{DD} = 12V		2.6	4.2	mA
		All Drivers OFF, V_{DD} = 10V		2.4	3.6	
		All Drivers OFF, V_{DD} = 5V		1.9	3.0	
I_R	Clamp Diode Leakage Current	V_R = 80V			50	µA
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2.0	V
I_{LIM}	Overcurrent Shutdown Threshold			500		mA
V_{SU}	Start-Up Voltage	**Note 9**	3.5	4.0	4.5	V
$V_{DD\ MIN}$	Minimum Supply (V_{DD})		3.0	3.5	4.0	V
	Thermal Shutdown			165		°C
	Thermal Shutdown Hysteresis			10		°C

Note:

9. Undervoltage lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

Test Circuit



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}, V_{DD} = 5V)

A. Typical data active time before clock pulse (data set-up time) 75ns

B. Minimum data active time after clock pulse (data hold time) 75ns

C. Minimum data pulse width 150ns

D. Minimum clock pulse width 150ns

E. Minimum time between clock activation and strobe 300ns

F. Minimum strobe pulse width 100ns

G. Typical time between strobe activation and output transition 500ns

SERIAL DATA present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform. Holding CLEAR high results in a data logic "0" being clocked into the shift register, turning off respective channels.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high to prevent invalid output states.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches. A positive OE/RESET pulse resets the FLAG and the output after a current shutdown fault. Over-temperature faults are not latched and require no reset pulse.

MIC59P60 Truth Table

Serial Data Input	Clear Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Contents
			I_1 I_2 I_3 …… I_8			I_1 I_2 I_3 …… I_8		I_1 I_2 I_3 …… I_8
H		⎍	H R_1 R_2 …… R_7	R_7				
L		⎍	L R_1 R_2 …… R_7	R_7				
X		⎎	R_1 R_2 R_3 …… R_8	R_8				
	H	⎍	O O O…… O	L				
			X X X…… X	X	L	R_1 R_2 R_3 …… R_8		
			P_1 P_2 P_3 …… P_8	P_8	H	P_1 P_2 P_3 …… P_8	L	P_1 P_2 P_3 …… P_8
						X X X …… X	H	H H H …… H

Note:

L = Low Logic Level

H = High Logic Level

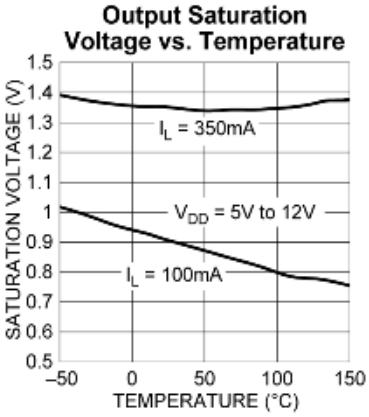
X = Irrelevant

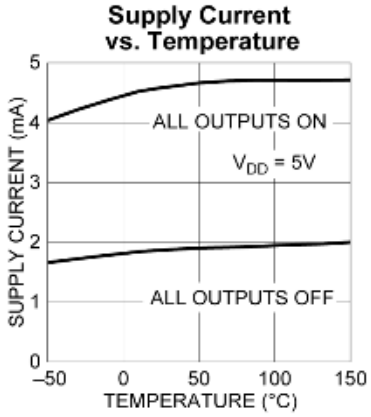
P = Present State

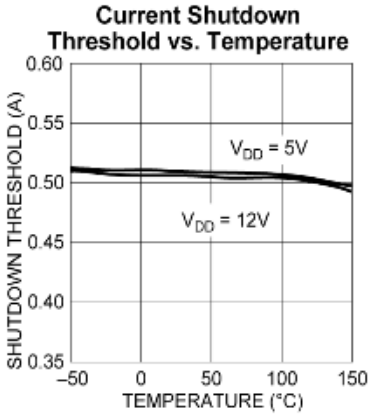
R = Previous State

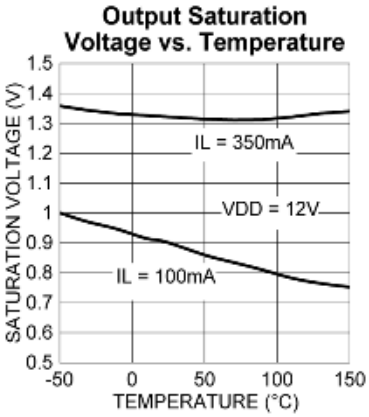
O = Output OFF

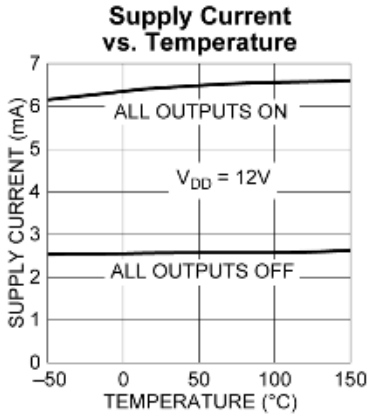
Typical Characteristics

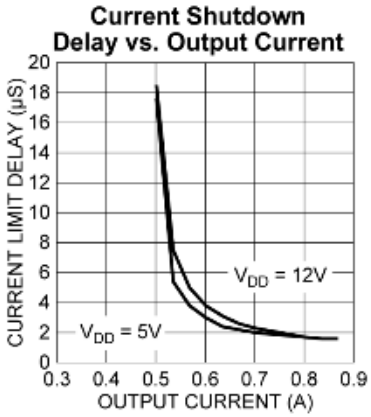












Maximum Allowable Duty Cycle (Plastic DIP)

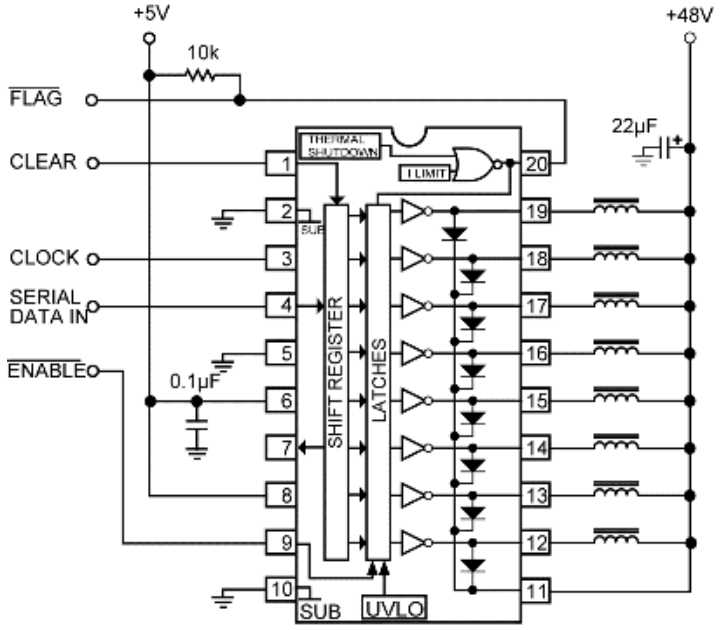
V_{DD} = 5.0V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

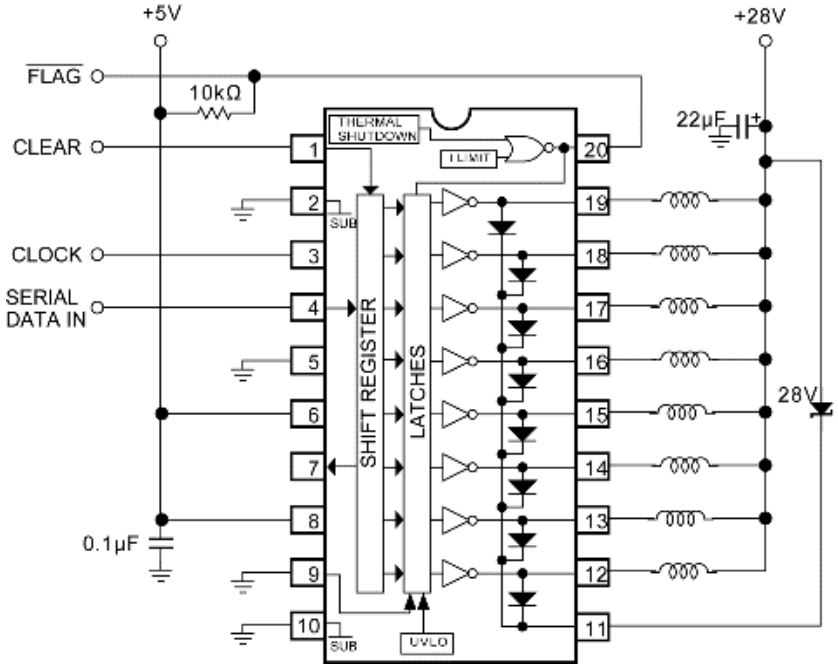
V_{DD} = 12V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

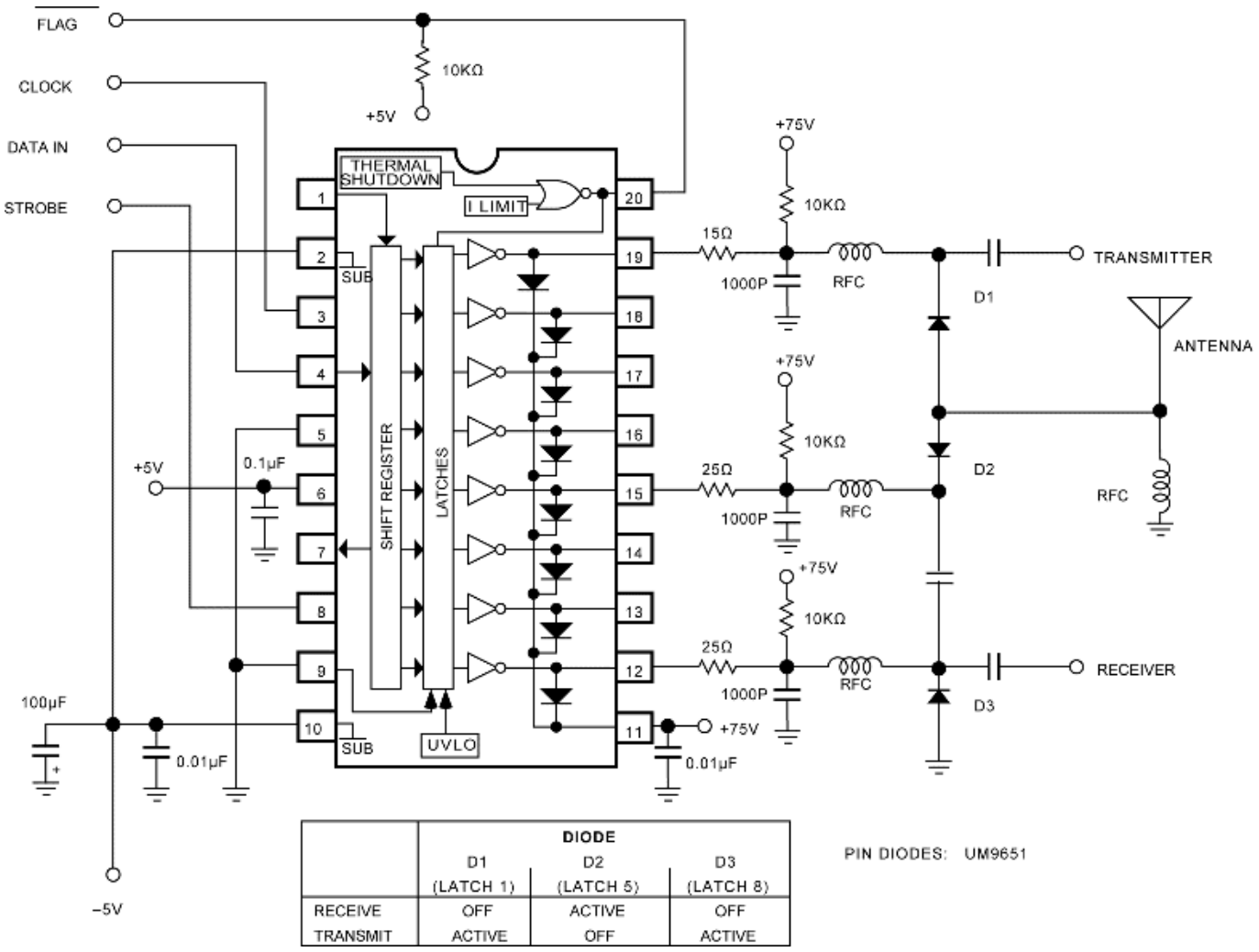
Typical Application



Protected Solenoid Driver with Output Enable



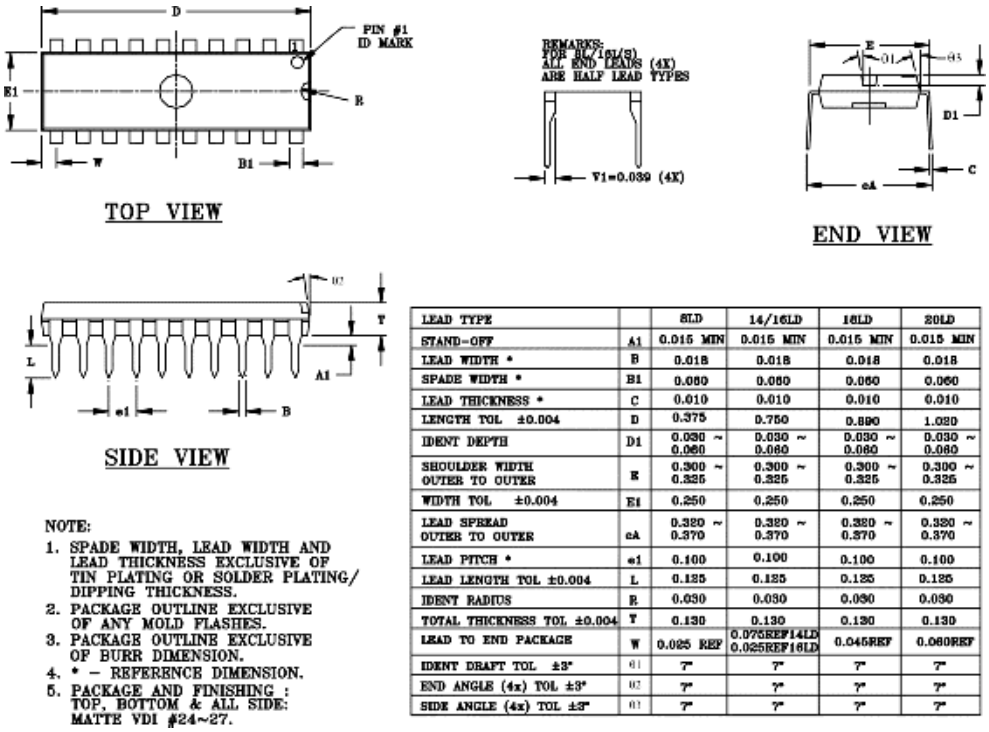
Hammer Driver



	DIODE		
	D1 (LATCH 1)	D2 (LATCH 5)	D3 (LATCH 8)
RECEIVE	OFF	ACTIVE	OFF
TRANSMIT	ACTIVE	OFF	ACTIVE

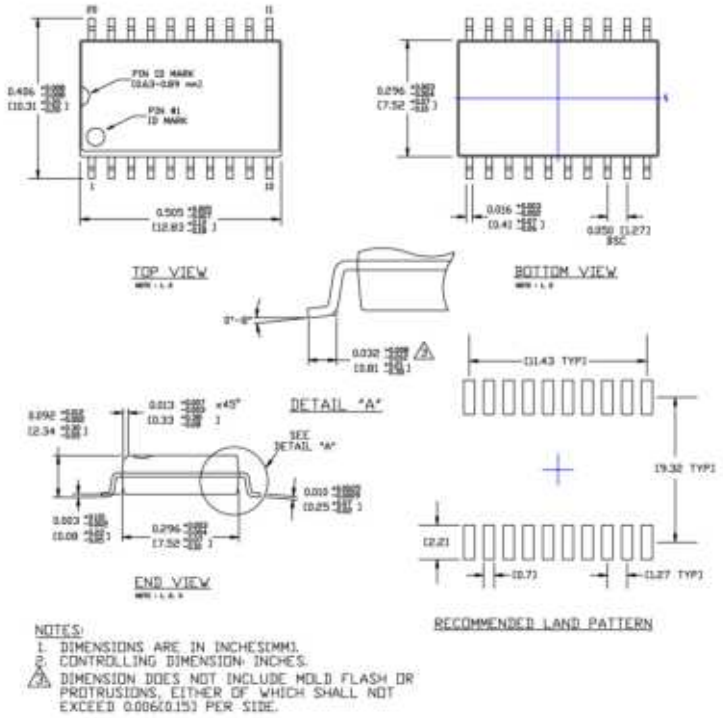
Protected Negative/Positive PIN Diode Driver Transmit/Receive Switch

Package Information and Recommended Landing Pattern[10]



LEAD TYPE		8LD	14/16LD	18LD	20LD
STAND-OFF	A1	0.015 MIN	0.015 MIN	0.015 MIN	0.015 MIN
LEAD WIDTH *	B	0.018	0.018	0.018	0.018
SPADE WIDTH *	B1	0.060	0.060	0.060	0.060
LEAD THICKNESS *	C	0.010	0.010	0.010	0.010
LENGTH TOL ±0.004	D	0.375	0.750	0.890	1.030
IDENT DEPTH	D1	0.030 ~ 0.060	0.030 ~ 0.060	0.030 ~ 0.060	0.030 ~ 0.060
SHOULDER WIDTH OUTER TO OUTER	E	0.300 ~ 0.325	0.300 ~ 0.325	0.300 ~ 0.325	0.300 ~ 0.325
WIDTH TOL ±0.004	E1	0.250	0.250	0.250	0.250
LEAD SPREAD OUTER TO OUTER	eA	0.320 ~ 0.370	0.320 ~ 0.370	0.320 ~ 0.370	0.320 ~ 0.370
LEAD PITCH *	e1	0.100	0.100	0.100	0.100
LEAD LENGTH TOL ±0.004	L	0.125	0.125	0.125	0.125
IDENT RADIUS	R	0.030	0.030	0.030	0.030
TOTAL THICKNESS TOL ±0.004	T	0.130	0.130	0.130	0.130
LEAD TO END PACKAGE	W	0.025 REF	0.075REF14LD 0.025REF16LD	0.045REF	0.080REF
IDENT DRAFT TOL ±3°	θ1	7°	7°	7°	7°
END ANGLE (4x) TOL ±3°	θ2	7°	7°	7°	7°
SIDE ANGLE (4x) TOL ±3°	θ3	7°	7°	7°	7°

20-Pin 300mil Plastic PDIP (N)

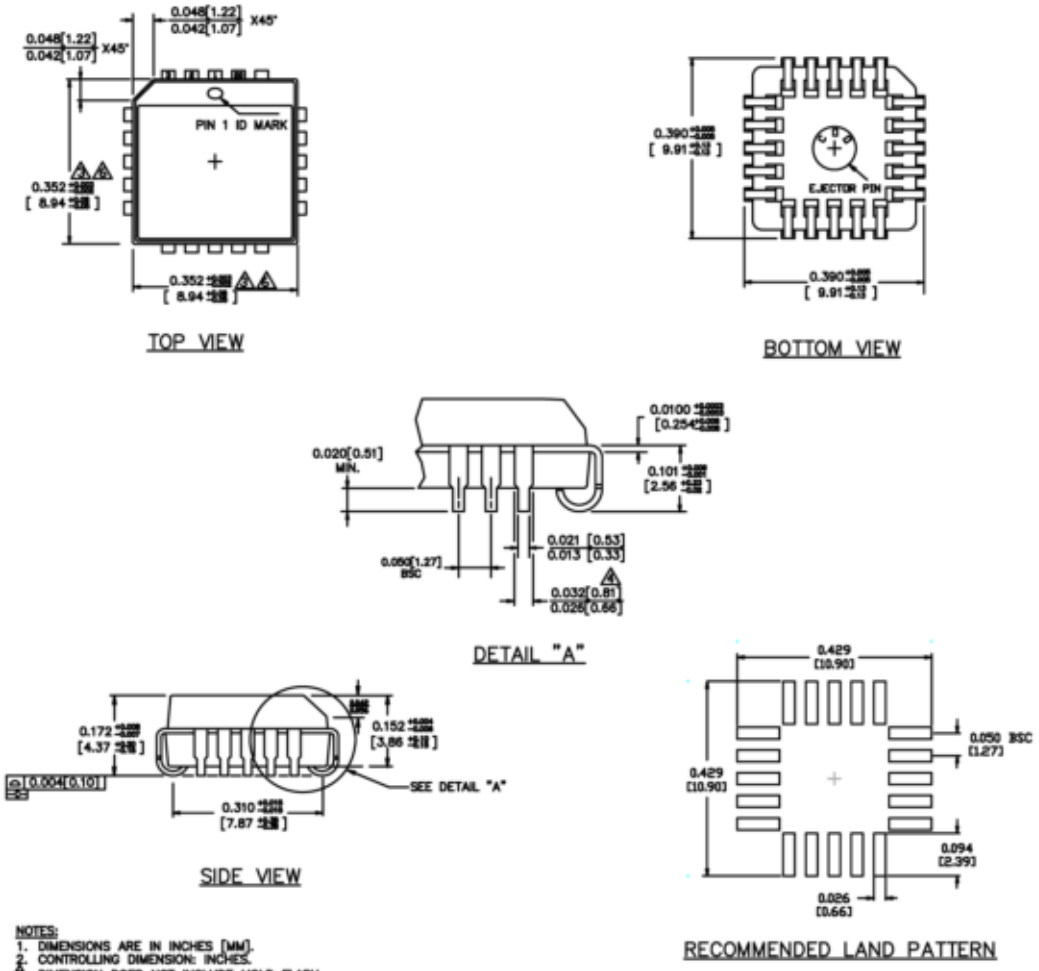


20-Pin Wide SOIC (WM)

Note:

10. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Landing Pattern[10] (Continued)



20-Pin PLCC (V)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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