# MICRF002/RF022

## 300-440MHz QwikRadio® ASK Receiver

## General Description

The MICRF002 is a single chip ASK/OOK (ON-OFF Keyed) RF receiver IC. This device is a true "antenna-in to data-out" monolithic device. All RF and IF tuning is accomplished automatically within the IC which eliminates manual tuning and reduces production costs. The result is a highly reliable yet low cost solution.

The MICRF002 is a fully featured part in 16-pin packaging, the MICRF022 is the same part packaged in 8-pin packaging with a reduced feature set (see "Ordering Information" for more information).

The MICRF002 is an enhanced version of the MICRF001 and MICRF011. The MICRF002 provides two additional functions over the MICRF001/011, (1) a Shutdown pin, which may be used to turn the device off for duty-cycled operation, and (2) a "Wake-up" output, which provides an output flag indicating when an RF signal is present. These features make the MICRF002 ideal for low and ultra-low power applications, such as RKE and remote controls.

All IF filtering and post-detection (demodulator) data filtering is provided within the MICRF002, so no external filters are necessary. One of four demodulator filter bandwidths may be selected externally by the user.

The MICRF002 offer two modes of operation; fixed-mode (FIX) and sweep-mode (SWP). In fixed-mode the MICRF002 functions as a conventional superhet receiver. In sweep-mode the MICRF002 employs a patented sweeping function to sweep a wider RF spectrum. Fixed-mode provides better selectivity and sensitivity performance and sweep-mode enables the MICRF002 to be used with low cost, imprecise transmitters.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.



QwikRadio®

## Features

- 300MHz to 440MHz frequency range
- Data-rate up to 10kbps (fixed-mode)
- Low Power Consumption
- 2.2mA fully operational (315MHz)
- 0.9µA in shutdown
- 220µA in polled operation (10:1 duty-cycle)
- Wake-up output flag to enable decoders and microprocessors
- Very low RF re-radiation at the antenna
- Highly integrated with extremely low external part count

## Applications

- Automotive remote keyless entry (RKE)
- Remote controls
- Remote fan and light control
- Garage door and gate openers

## Ordering Information

| Part Number | Demodulator Bandwidth | Operating Mode | Shutdown | WAKEB Output Flag | Package | Lead Finish |
|---|---|---|---|---|---|---|
| MICRF002YM | User Programmable | Fixed or Sweep | Yes | Yes | 16-Pin SOIC | Pb-Free |
| MICRF022YM-SW48 | 5000Hz | Sweep | No | Yes | 8-Pin SOIC | Pb-Free |
| MICRF022YM-FS12 | 1250Hz | Fixed | Yes | No | 8-Pin SOIC | Pb-Free |
| MICRF022YM-FS24 | 2500Hz | Fixed | Yes | No | 8-Pin SOIC | Pb-Free |
| MICRF022YM-FS48 | 5000Hz | Fixed | Yes | No | 8-Pin SOIC | Pb-Free |

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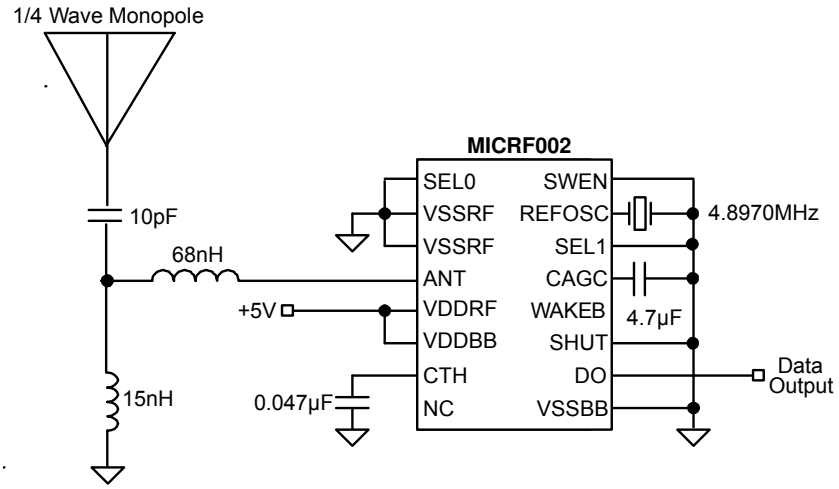
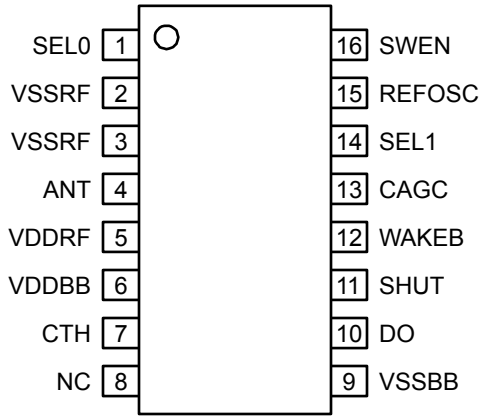
## Typical Application

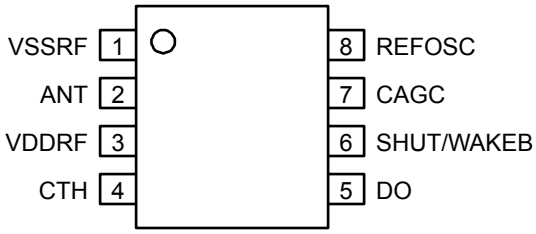



**315MHz 800bps On-Off Keyed Receiver**

## Pin Configuration




**16-Pin SOIC (M)**




**8-Pin SOIC (M)**

## 8-Pin Options

The standard 16-pin package allows complete control of all configurable features. Some reduced function 8-pin versions are also available, see “Ordering Information” on page 1.

For high-volume applications additional customized 8-pin devices can be produced. SWEN, SEL0 and SEL1 pins are internally bonded to reduce the pin count; pin 6 may be configured as either SHUT or WAKEB

| SEL0 | SEL1 | Demodulator Bandwidth | |
|---|---|---|---|
| | | Sweep-Mode | Fixed-Mode |
| 1 | 1 | 5000Hz | 10000Hz |
| 0 | 1 | 2500Hz | 5000Hz |
| 1 | 0 | 1250Hz | 2500Hz |
| 0 | 0 | 625Hz | 1250Hz |

**Table 1. Nominal Demodulator Filter Bandwidth vs. SEL0, SEL1 and Operating Mode**

## Pin Description

| Pin Number SOIC-16 | Pin Number SOIC-8 | Pin Name | Pin Name |
|---|---|---|---|
| 1 | – | SEL0 | Bandwidth Selection Bit 0 (Digital Input): Used in conjunction with SEL1 to set the desired demodulator filter bandwidth. See Table 1. Internally pulled-up to VDDRF. |
| 2, 3 | 1 | VSSRF | RF Power Supply: Ground return to the RF section power supply. |
| 4 | 2 | ANT | Antenna (Analog Input): For optimal performance the ANT pin should be impedance matched to the antenna. See “Applications Information” for information on input impedance and matching techniques. |
| 5 | 3 | VDDRF | RF Power Supply: Positive supply input for the RF section of the IC. |
| 6 | – | VDDBB | Base-Band Power Supply: Positive supply input for the baseband section (digital section) of the IC. |
| 7 | 4 | CTH | Data Slicing Threshold Capacitor (Analog I/O): Capacitor connected to this pin extracts the dc average value from the demodulated waveform which becomes the reference for the internal data slicing comparator. |
| 8 | – | NC | Not internally connected |
| 9 | – | VSSBB | Base-Band Power Supply: Ground return to the baseband section power supply. |
| 10 | 5 | DO | Data Output (Digital Output) |
| 11 | 6 | SHUT | Shutdown (Digital Input): Shutdown-mode logic-level control input. Pull low to enable the receiver. Internally pulled-up to VDDRF. |
| 12 | – | WAKEB | Wakeup (Digital Output): Active-low output that indicates detection of an incoming RF signal. |
| 13 | 7 | CAGC | Automatic Gain Control (Analog I/O): Connect an external capacitor to set the attack/decay rate of the on-chip automatic gain control. |
| 14 | – | SEL1 | Bandwidth Selection Bit 1 (Digital Input): Used in conjunction with SEL0 to set the desired demodulator filter bandwidth. See Table 1. Internally pulled-up to VDDRF. |
| 15 | 8 | REFOSC | Reference Oscillator: Timing reference, sets the RF receive frequency. |
| 16 | – | SWEN | Sweep-Mode Enable (Digital Input): Sweep- or Fixed-mode operation control input. SWEN high= sweep mode; SWEN low = conventional superheterodyne receiver. Internally pulled-up to VDDRF. |

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{DDRF}$, $V_{DDBB}$).....+7V
Input/Output Voltage ($V_{I/O}$). .....$V_{SS}$–0.3 to $V_{DD}$+0.3
Junction Temperature ($T_J$) .....+150°C
Storage Temperature ($T_s$) .....–65°C to 150°C
Lead Temperature (soldering, 10 sec.).....260°C
ESD Rating[3]

## Operating Ratings[2]

Supply Voltage ($V_{DDRF}$, $V_{DDBB}$)..... +4.75V to +5.5V
RF Frequency Range..... 300MHz to 440Hz
Data Duty-Cycle .....20% to 80%
Reference Oscillator Input Range..... $0.1V_{PP}$ to $1.5V_{PP}$
Ambient Temperature ($T_A$) .....–40°C to +85°C

## Electrical Characteristics[4]

$V_{DDRF}$ = $V_{DDBB}$ = $V_{DD}$ where +4.75V ≤ $V_{DD}$ ≤ 5.5V, $V_{SS}$ = 0V; $C_{AGC}$ = 4.7µF, $C_{TH}$ = 100nF; SEL0 = SEL1 = $V_{SS}$; fixed mode (SWEN = $V_{SS}$); $f_{REFOSC}$ = 4.8970MHz (equivalent to $f_{RF}$ = 315MHz); data-rate = 1kbps (Manchester encoded). $T_A$ = 25°C, **bold** values indicate –40°C ≤ $T_A$ ≤ +85°C; current flow into device pins is positive; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{OP}$ | Operating Current | continuous operation, $f_{RF}$ = 315MHz | | 2.2 | **3.2** | mA |
| | | polled with 10:1 duty cycle, $f_{RF}$ = 315MHz | | 220 | | µA |
| | | continuous operation, $f_{RF}$ = 433.92MHz | | 3.5 | | mA |
| | | polled with 10:1 duty cycle, $f_{RF}$ = 433.92MHz | | 350 | | µA |
| $I_{STBY}$ | Standby Current | $V_{SHUT}$ = $V_{DD}$ | | 0.9 | | µA |
| **RF Section, IF Section** | | | | | | |
| | Receiver Sensitivity (**Note 4**) | $f_{RF}$ = 315MHz | | –97 | | dBm |
| | | $f_{RF}$ = 433.92MHz | | –95 | | dBm |
| $f_{IF}$ | IF Center Frequency | **Note 6** | | 0.86 | | MHz |
| $f_{BW}$ | IF Bandwidth | **Note 6** | | 0.43 | | MHz |
| | Maximum Receiver Input | $R_{SC}$ = 50Ω | | –20 | | dBm |
| | Spurious Reverse Isolation | ANT pin, $R_{SC}$ = 50Ω, **Note 5** | | 30 | | $\mu V_{RMS}$ |
| | AGC Attack to Decay Ratio | $t_{ATTACK} \div t_{DECAY}$ | | 0.1 | | |
| | AGC Leakage Current | $T_A$ = +85°C | | ±100 | | nA |
| **Reference Oscillator** | | | | | | |
| $Z_{REFOSC}$ | Reference Oscillator Input Impedance | **Note 8** | | 290 | | kΩ |
| | Reference Oscillator Source Current | | | 5.2 | | µA |
| **Demodulator** | | | | | | |
| $Z_{CTH}$ | CTH Source Impedance | **Note 7** | | 145 | | kΩ |
| $I_{ZCTH(leak)}$ | CTH Leakage Current | $T_A$ = +85°C | | ±100 | | nA |
| | Demodulator Filter Bandwidth Sweep Mode (SWEN = VDD or OPEN) **Note 6** | $V_{SEL0}$ = $V_{DD}$. $V_{SEL1}$ = $V_{DD}$<br>$V_{SEL0}$ = $V_{SS}$. $V_{SEL1}$ = $V_{DD}$<br>$V_{SEL0}$ = $V_{DD}$. $V_{SEL1}$ = $V_{SS}$<br>$V_{SEL0}$ = $V_{SS}$. $V_{SEL1}$ = $V_{SS}$ | | 4000<br>2000<br>1000<br>500 | | Hz<br>Hz<br>Hz<br>Hz |
| | Demodulator Filter Bandwidth Fixed Mode (SWEN = VSS) **Note 6** | $V_{SEL0}$ = $V_{DD}$. $V_{SEL1}$ = $V_{DD}$<br>$V_{SEL0}$ = $V_{SS}$. $V_{SEL1}$ = $V_{DD}$<br>$V_{SEL0}$ = $V_{DD}$. $V_{SEL1}$ = $V_{SS}$<br>$V_{SEL0}$ = $V_{SS}$. $V_{SEL1}$ = $V_{SS}$ | | 8000<br>4000<br>2000<br>1000 | | Hz<br>Hz<br>Hz<br>Hz |

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital/Control Section** | | | | | | |
| $V_{IN(high)}$ | Input-High Voltage | SEL0, SEL1, SWEN | | | **0.8** | $V_{DD}$ |
| $V_{IN(low)}$ | Input-Low Voltage | SEL0, SEL1, SWEN | **0.2** | | | $V_{DD}$ |
| $I_{OUT}$ | Output Current | DO, WAKEB pins, push-pull | | 10 | | µA |
| $V_{OUT(high)}$ | Output High Voltage | DO, WAKEB pins, $I_{OUT}$ = –1µA | **0.9** | | | $V_{DD}$ |
| $V_{OUT(low)}$ | Output Low Voltage | DO, WAKEB pins, $I_{OUT}$ = +1µA | | | **0.1** | $V_{DD}$ |
| $t_R$, $t_F$ | Output Rise and Fall Times | DO, WAKEB pins, $C_{LOAD}$ = 15pF | | 10 | | µs |

**Notes:**

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive, use appropriate ESD precautions. Meets class 1 ESD test requirements, (human body model HBM), in accordance with MIL-STD-883C, method 3015. Do not operate or store near strong electrostatic fields.
4. Sensitivity is defined as the average signal level measured at the input necessary to achieve 10-2 BER (bit error rate). The RF input is assumed to be matched to 50Ω.
5. Spurious reverse isolation represents the spurious components which appear on the RF input pin (ANT) measured into 50Ω with an input RF matching network.
6. **Parameter scales linearly with reference oscillator frequency $f_T$.** For any reference oscillator frequency other than 4.8970MHz, compute new parameter value as the ratio:.

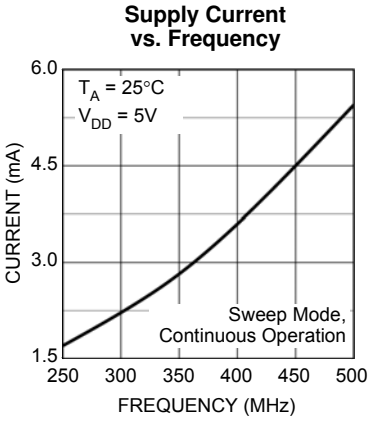
$$\frac{f_{REFOSC}\,MHz}{4.8970MHz} \times (\text{parameter value at } 4.8970MHz)$$

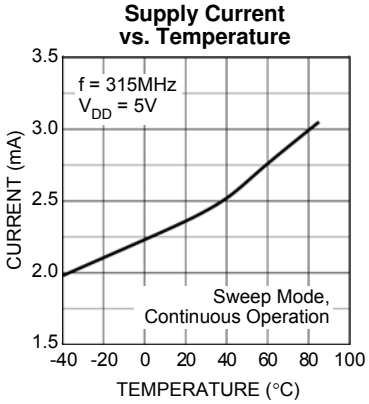
7. **Parameter scales inversely with reference oscillator frequency $f_T$.** For any reference oscillator frequency other than 4.8970MHz, compute new parameter value as the ratio:

$$\frac{4.8970MHz}{f_{REFOSC}\,MHz} \times (\text{parameter value at } 4.8970MHz)$$

8. Series resistance of the resonator (ceramic resonator or crystal) should be minimized to the extent possible. In cases where the resonator series resistance is too great, the oscillator may oscillate at a diminished peak-to-peak level, or may fail to oscillate entirely. Micrel recommends that series resistances for ceramic resonators and crystals not exceed 50Ohms and 100Ω respectively. Refer to Application Hint 35 for crystal recommendations.

## Typical Characteristics



## Functional Diagram

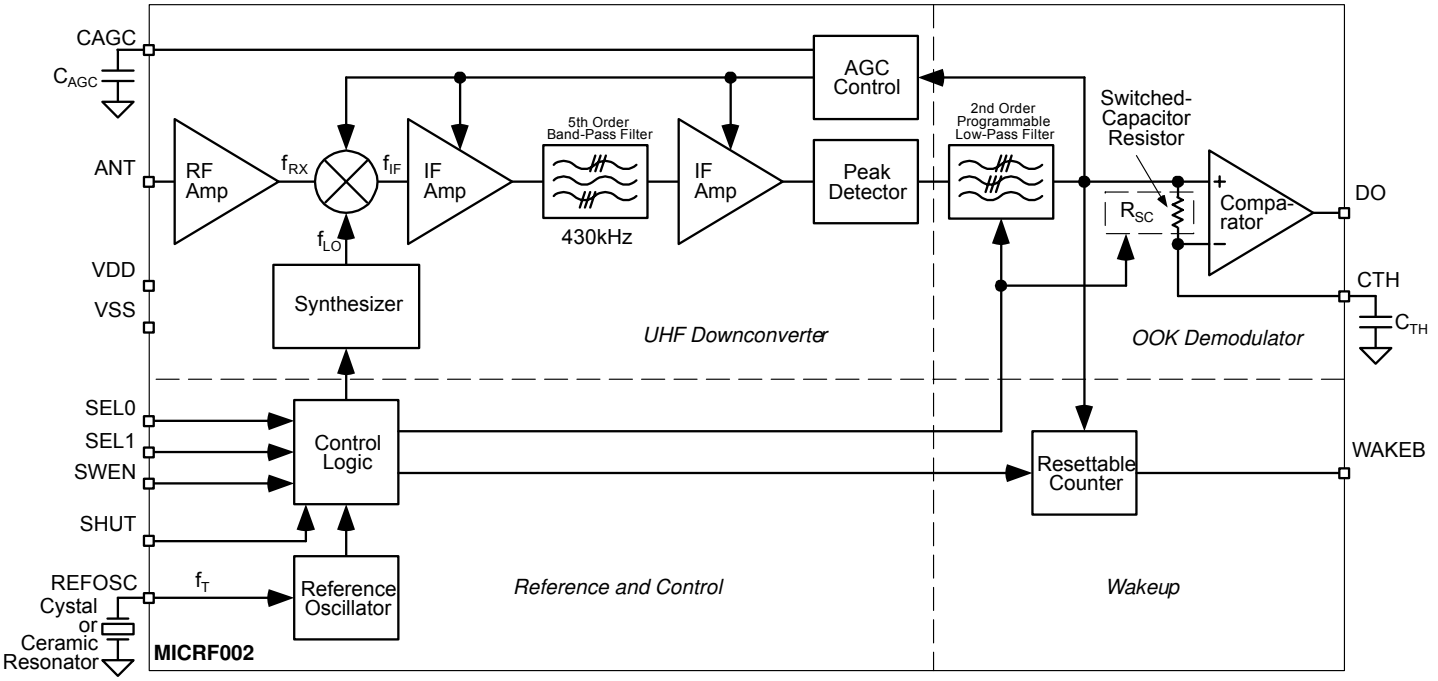



**Figure 1. MICRF002 Block Diagram**

## Application Information and Functional Description

Refer to Figure 1 "MICRF002 Block Diagram". Identified in the block diagram are the four sections of the IC: UHF Downconverter, OOK Demodulator, Reference and Control, and Wakeup. Also shown in the figure are two capacitors (CTH, CAGC) and one timing component, usually a crystal or ceramic resonator. With the exception of a supply decoupling capacitor, and antenna impedance matching network, these are the only external components needed by the MICRF002 to assemble a complete UHF receiver.

For optimal performance is highly recommended that the MICRF002 is impedance matched to the antenna, the matching network will add an additional two or three components.

Four control inputs are shown in the block diagram: SEL0, SEL1, SWEN, and SHUT. Using these logic inputs, the user can control the operating mode and selectable features of the IC. These inputs are CMOS compatible, and are internally pulled-up. IF Bandpass Filter Roll-off response of the IF Filter is 5th order, while the demodulator data filter exhibits a 2$^{nd}$ order response.

## Design Steps

The following steps are the basic design steps for using the MICRF002 receiver:

1. Select the operating mode (sweep or fixed)
2. Select the reference oscillator
3. Select the $C_{TH}$ capacitor
4. Select the $C_{AGC}$ capacitor
5. Select the demodulator filter bandwidth

### Step 1: Selecting the Operating Mode

#### *Fixed-Mode Operation*

For applications where the transmit frequency is accurately set (that is, applications where a SAW or crystal-based transmitter is used) the MICRF002 may be configured as a standard superheterodyne receiver (fixed mode). In fixed-mode operation the RF bandwidth is narrower making the receiver less susceptible to interfering signals. Fixed mode is selected by connecting SWEN to ground.

#### *Sweep-Mode Operation*

When used in conjunction with low-cost L-C transmitters the MICRF002 should be configured in sweep-mode. In sweep-mode, while the topology is still superheterodyne, the LO (local oscillator) is swept over a range of frequencies at rates greater than the data rate. This technique effectively increases the RF bandwidth of the

MICRF002, allowing the device to operate in applications where significant transmitter-receiver frequency misalignment may exist. The transmit frequency may vary up to ±0.5% over initial tolerance, aging, and temperature. In sweep-mode a band approximately 1.5% around the nominal transmit frequency is captured. The transmitter may drift up to ±0.5% without the need to retune the receiver and without impacting system performance.

The swept-LO technique does not affect the IF bandwidth, therefore noise performance is not degraded relative to fixed-mode. The IF bandwidth is 430kHz whether the device is operating in fixed- or sweep-mode. Due to limitations imposed by the LO sweeping process, the upper limit on data rate in sweep mode is approximately 5.0kbps.

Similar performance is not currently available with crystalbased superheterodyne receivers which can operate only with SAW- or crystal-based transmitters. In sweep-mode, a range reduction will occur in installations where there is a strong interferer in the swept RF band. This is because the process indiscriminately includes all signals within the sweep range. An MICRF002 may be used in place of a superregenerative receiver in most applications.

**Step 2: Selecting the Reference Oscillator**

All timing and tuning operations on the MICRF002 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of three ways:

1. Connect a ceramic resonator
2. Connect a crystal
3. Drive this pin with an external timing signal

The specific reference frequency required is related to the system transmit frequency and to the operating mode of the receiver as set by the SWEN pin.

***Crystal or Ceramic Resonator Selection***

Do not use resonators with integral capacitors since capacitors are included in the IC, also care should be taken to ensure low ESR capacitors are selected. Application Hint 34 and Application Hint 35 provide additional information and recommended sources for crystals and resonators.

If operating in fixed-mode, a crystal is recommended. In sweep-mode either a crystal or ceramic resonator may be used. When a crystal of ceramic resonator is used the minimum voltage is $300mV_{PP}$. If using an externally applied signal it should be AC-coupled and limited to the operating range of $0.1V_{PP}$ to $1.5V_{PP}$.

***Selecting Reference Oscillator Frequency $f_T$ (Fixed-Mode)***

As with any superheterodyne receiver, the mixing between the internal LO (local oscillator) frequency $f_{LO}$ and the incoming transmit frequency $f_{TX}$ ideally must equal the IF center frequency. Equation 1 may be used to compute the appropriate $f_{LO}$ for a given $f_{TX}$:

$$(1) \qquad f_{LO} = f_{TX} \pm \left(0.86 \frac{f_{TX}}{315}\right)$$

Frequencies $f_{TX}$ and $f_{LO}$ are in MHz. Note that two values of $f_{LO}$ exist for any given $f_{TX}$, distinguished as “high-side mixing” and “low-side mixing”. High-side mixing results in an image frequency above the frequency of interest and low-side mixing results in a frequency below.

After choosing one of the two acceptable values of $f_{LO}$, use Equation 2 to compute the reference oscillator frequency $f_T$:

$$(2) \qquad f_T = \frac{f_{LO}}{64.5}$$

Frequency $f_T$ is in MHz. Connect a crystal of frequency $f_T$ to REFOSC on the MICRF002. Four-decimal-place accuracy on the frequency is generally adequate. The following table identifies $f_T$ for some common transmit frequencies when the MICRF002 is operated in fixed mode.

| Transmit Frequency $f_{TX}$ | Reference Oscillator Frequency $f_T$ |
|---|---|
| 315MHz | 4.8970MHz |
| 390MHz | 6.0630MHz |
| 418MHz | 6.4983MHz |
| 433.92MHz | 6.7458MHz |

**Table 2. Fixed-Mode Recommended Reference Oscillator Values for Typical Transmit Frequencies (high-side mixing)**

***Selecting REFOSC Frequency $f_T$ (Sweep-Mode)***

Selection of the reference oscillator frequency $f_T$ in sweep-mode is much simpler than in fixed mode due to the LO sweeping process. Also, accuracy requirements of the frequency reference component are significantly relaxed.

In sweep-mode, $f_T$ is given by Equation 3:

$$(3) \qquad f_T = \frac{f_{LO}}{64.25}$$

In sweep-mode a reference oscillator with frequency accurate to two-decimal-places is generally adequate. A crystal may be used and may be necessary in some cases if the transmit frequency is particularly imprecise.

| Transmit Frequency $f_{TX}$ | Reference Oscillator Frequency $f_T$ |
|---|---|
| 315MHz | 4.88MHz |
| 390MHz | 6.05MHz |
| 418MHz | 6.48MHz |
| 433.92MHz | 6.73MHz |

**Table 3. Sweep-Mode Recommended Reference Oscillator Values for Typical Transmit Frequencies**

### Step 3: Selecting the $C_{TH}$ Capacitor

Extraction of the dc value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor $C_{TH}$ and the on-chip switched capacitor "resistor" $R_{SC}$, shown in the block diagram.

Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typically values range from 5ms to 50ms. Optimization of the value of $C_{TH}$ is required to maximize range.

#### *Selecting Capacitor $C_{TH}$*

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure (that is, existence of data preamble, etc.). This issue is covered in more detail in Application Note 22.

The effective resistance of $R_{SC}$ is listed in the electrical characteristics table as 145kΩ at 315MHz, this value scales linearly with frequency. Source impedance of the $C_{TH}$ pin at other frequencies is given by Equation 4, where $f_T$ is in MHz:

$$R_{SC} = 145k\Omega \frac{4.8970}{f_T} \quad (4)$$

τ of 5x the bit-rate is recommended. Assuming that a slicing level time constant τ has been established, capacitor $C_{TH}$ may be computed using Equation 5:

$$C_{TH} = \frac{\tau}{R_{SC}} \quad (5)$$

A standard ±20% X7R ceramic capacitor is generally sufficient. Refer to Application Hint 42 for $C_{TH}$ and CAGC selection examples.

### Step 4: Selecting the $C_{AGC}$ Capacitor

The signal path has AGC (automatic gain control) to increase input dynamic range. The attack time constant of the AGC is set externally by the value of the $C_{AGC}$ capacitor connected to the $C_{AGC}$ pin of the device. To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under $10mV_{PP}$ once the control voltage has attained its quiescent value. For this reason capacitor values of at least 0.47µF are recommended.

The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the MICRF002. When the device is placed into shutdown mode (SHUT pin pulled high), the AGC capacitor floats to retain the voltage. When operation is resumed, only the voltage droop due to capacitor leakage must be replenished. A relatively low-leakage capacitor is recommended when the devices are used in dutycycled operation.

To further enhance duty-cycled operation, the AGC push and pull currents are boosted for approximately 10ms immediately after the device is taken out of shutdown. This compensates for AGC capacitor voltage droop and reduces the time to restore the correct AGC voltage. The current is boosted by a factor of 45.

#### *Selecting $C_{AGC}$ Capacitor in Continuous Mode*

A $C_{AGC}$ capacitor in the range of 0.47µF to 4.7µF is typically recommended. The value of the $C_{AGC}$ should be selected to minimize the ripple on the AGC control voltage by using a sufficiently large capacitor. However if the capacitor is too large the AGC may react too slowly to incoming signals. AGC settling time from a completely discharged (zero-volt) state is given approximately by Equation 6:

$$\Delta t = 1.333 C_{AGC} - 0.44 \quad (6)$$

where:

$C_{AGC}$ sin in µF, and Δt is in seconds.

#### *Selecting $C_{AGC}$ Capacitor in Duty-Cycle Mode*

Voltage droop across the $C_{AGC}$ capacitor during shutdown should be replenished as quickly as possible after the IC is enabled. As mentioned above, the MICRF002 boosts the push-pull current by a factor of 45 immediately after start-up. This fixed time period is based on the reference oscillator frequency $f_T$. The time is 10.9ms for $f_T$ = 6.00MHz, and varies inversely with $f_T$. The value of $C_{AGC}$ capacitor and the duration of the shutdown time period should be selected such that the droop can be replenished within this 10ms period.

Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. Worst-case from a recovery standpoint is downward droop, since the AGC pull-up current is 1/10th magnitude of the pulldown current. The downward droop is replenished according to the Equation 7:

$$\frac{I}{C_{AGC}} = \frac{\Delta V}{\Delta t} \quad (7)$$

where:

I = AGC pullup current for the initial 10ms (67.5µA)

$C_{AGC}$ = AGC capacitor value

Δt = droop recovery time

ΔV = droop voltage

For example, if user desires Δt = 10ms and chooses a 4.7µF $C_{AGC}$, then the allowable droop is about 144mV. Using the same equation with 200nA worst case pin leakage and assuming 1µA of capacitor leakage in the same direction, the maximum allowable Δt (shutdown time) is about 0.56s for droop recovery in 10ms.

The ratio of decay-to-attack time-constant is fixed at 10:1 (that is, the attack time constant is 1/10th of the decay time constant). Generally the design value of 10:1 is adequate

for the vast majority of applications. If adjustment is required the constant may be varied by adding a resistor in parallel with the $C_{AGC}$ capacitor. The value of the resistor must be determined on a case by case basis.

**Step 5: Selecting The Demod Filter Bandwidth**

The inputs SEL0 and SEL1 control the demodulator filter bandwidth in four binary steps (625Hz to 5000Hz in sweep, 1250Hz to 10000Hz in fixed-mode), see Table 3. Bandwidth must be selected according to the application. The demodulator bandwidth should be set according to Equation 8:

$$\text{Demoulator bandwidth} = \frac{0.65}{\text{Shortest pulse} - \text{width}} \quad (8)$$

It should be noted that the values indicated in Table 1 are nominal values. The filter bandwidth scales linearly with frequency so the exact value will depend on the operating frequency. Refer to the “Electrical Characteristics” for the exact filter bandwidth at a chosen frequency.

| SEL0 | SEL1 | Demodulator Bandwidth | |
|---|---|---|---|
| | | Sweep-Mode | Fixed-Mode |
| 1 | 1 | 5000Hz | 10000Hz |
| 0 | 1 | 2500Hz | 5000Hz |
| 1 | 0 | 1250Hz | 2500Hz |
| 0 | 0 | 625Hz | 1250Hz |

**Table 1. Nominal Demodulator Filter Bandwidth vs. SEL0, SEL1 and Operating Mode**

## Additional Applications Information

In addition to the basic operation of the MICRF002 the following enhancements can be made. In particular it is strongly recommended that the antenna impedance is matched to the input of the IC.

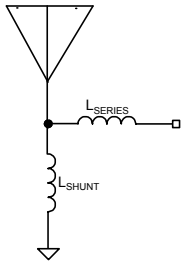
### Antenna Impedance Matching

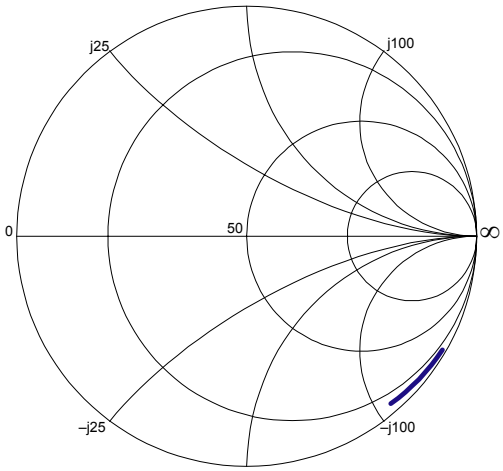
As shown in Table 4 the antenna pin input impedance is frequency dependant. The ANT pin can be matched to 50Ω with an L-type circuit. That is, a shunt inductor from the RF input to ground and another in series from the RF input to the antenna pin.

Inductor values may be different from table depending on PCB material, PCB thickness, ground configuration, and how long the traces are in the layout. Values shown were characterized for a 0.031 thickness, FR4 board, solid ground plane on bottom layer, and very short traces. MuRata and Coilcraft wire wound 0603 or 0805 surface mount inductors were tested, however any wire wound inductor with high SRF (self resonance frequency) should do the job.

### Shutdown Function

Duty-cycled operation of the MICRF002 (often referred to as polling) is achieved by turning the MICRF002 on and off via the SHUT pin. The shutdown function is controlled by a logic state applied to the SHUT pin. When VSHUT is high, the device goes into low-power standby mode. This pin is pulled high internally, it must be externally pulled low to enable the receiver.




| Frequency (MHz) | $Z_{IN}$ Z11 | S11 | $L_{SHUNT}$(nH) | $L_{SERIES}$(nH) |
|---|---|---|---|---|
| 300 | 12-j166 | 0.803-j0.529 | 15 | 72 |
| 305 | 12-j165 | 0.800-j0.530 | 15 | 72 |
| 310 | 12-j163 | 0.796-j0.536 | 15 | 72 |
| 315 | 13-j162 | 0.791-j0.536 | 15 | 72 |
| 320 | 12-j160 | 0.789-j0.543 | 15 | 68 |
| 325 | 12-j157 | 0.782-j0.550 | 12 | 68 |
| 330 | 12-j155 | 0.778-j0.556 | 12 | 68 |
| 335 | 12-j152 | 0.770-j0.564 | 12 | 68 |
| 340 | 11-j150 | 0.767-j0.572 | 15 | 56 |
| 345 | 11-j148 | 0.762-j0.578 | 15 | 56 |
| 350 | 11-j145 | 0.753-j0.586 | 12 | 56 |
| 355 | 11-j143 | 0.748-j0.592 | 12 | 56 |
| 360 | 11-j141 | 0.742-j0.597 | 10 | 56 |
| 365 | 11-j139 | 0.735-j0.603 | 10 | 56 |
| 370 | 10-j137 | 0.732-j0.612 | 12 | 47 |
| 375 | 10-j135 | 0.725-j0.619 | 12 | 47 |
| 380 | 10-j133 | 0.718-j0.625 | 10 | 47 |
| 385 | 10-j131 | 0.711-j0.631 | 10 | 47 |
| 390 | 10-j130 | 0.707-j0.634 | 10 | 43 |
| 395 | 10-j128 | 0.700-j0.641 | 10 | 43 |
| 400 | 10-j126 | 0.692-j0.647 | 10 | 43 |
| 405 | 10-j124 | 0.684-j0.653 | 10 | 39 |
| 410 | 10-j122 | 0.675-j0.660 | 10 | 39 |
| 415 | 10-j120 | 0.667-j0.667 | 10 | 39 |
| 420 | 10-j118 | 0.658-j0.673 | 10 | 36 |
| 425 | 10-j117 | 0.653-j0.677 | 10 | 36 |
| 430 | 10-j115 | 0.643-j0.684 | 10 | 33 |
| 435 | 10-j114 | 0.638-j0.687 | 10 | 33 |
| 440 | 8-j112 | 0.635-j0.704 | 8.2 | 33 |

**Table 4. Input Impedance vs. Frequency**

### Power Supply Bypass Capacitors

$V_{DDBB}$ and $V_{DDRF}$ should be connected together directly at the IC pins. Supply bypass capacitors are strongly recommended. They should be connected to $V_{DDBB}$ and $V_{DDRF}$ and should have the shortest possible lead lengths. For best performance, connect $V_{SSRF}$ to $V_{SSBB}$ at the power supply only (that is, keep $V_{SSBB}$ currents from flowing through the $V_{SSRF}$ return path).

### Increasing Selectivity with an Optional BandPass Filter

For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and $V_{SSRF}$ to provide additional receive selectivity and input overload protection. A minimum input configuration is included in Figure 7 it provides some filtering and necessary overload protection.

### Data Squelching

During quiet periods (no signal) the data output (DO pin) transitions randomly with noise. Most decoders can discriminate between this random noise and actual data but for some system it does present a problem. There are three possible approaches to reducing this output noise:

1. Analog squelch to raise the demodulator threshold
2. Digital squelch to disable the output when data is not present
3. Output filter to filter the (high frequency) noise glitches on the data output pin.

The simplest solution is add analog squelch by introducing a small offset, or squelch voltage, on the $C_{TH}$ pin so that noise does not trigger the internal comparator. Usually 20mV to 30mV is sufficient, and may be achieved by connecting a several-megohm resistor from the $C_{TH}$ pin to either $V_{SS}$ or $V_{DD}$, depending on the desired offset polarity. Since the MICRF002 has receiver AGC noise at the internal comparator input is always the same, set by the AGC. The squelch offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce sensitivity and also reduce range. Only introduce an amount of offset sufficient to quiet the output. Typical squelch resistor values range from 6.8MΩ to 10MΩ.

### Wake-Up Function

The WAKEB output signal can be used to reduce system power consumption by enabling the rest of a system when an RF signal is present. The WAKEB is an output logic signal which goes active low when the IC detects a constant RF carrier. The wake-up function is unavailable when the IC is in shutdown mode.

To activate the Wake-Up function, a received constant RF carrier must be present for 128 counts or the internal system clock. The internal system clock is derived from the reference oscillator and is 1/256 the reference oscillator frequency. For example:

$f_T$ = 6.4MHz

$f_S = f_T/256$ = 25kHz

$P_S = 1/f_S$ = 0.04ms

128 counts x 0.04ms = 5.12ms

where:

$f_T$ = reference oscillator frequency

$f_S$ = system clock frequency

$P_S$ = system clock period

The Wake-Up counter will reset immediately after a detected RF carrier drops. The duration of the Wake-Up signal output is then determined by the required wake up time plus an additional RF carrier on time interval to create a wake up pulse output.

WAKEB Output Pulse Time = $T_{WAKE}$ + Additional RF Carrier On Time

For designers who wish to use the wakeup function while squelching the output, a positive squelching offset voltage must be used. This simply requires that the squelch resistor be connected to a voltage more positive than the quiescent voltage on the $C_{TH}$ pin so that the data output is low in absence of a transmission.

### I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF002 are diagrammed in Figures 1 through 6. The ESD protection diodes at all input and output pins are not shown.

#### *$C_{TH}$ Pin*

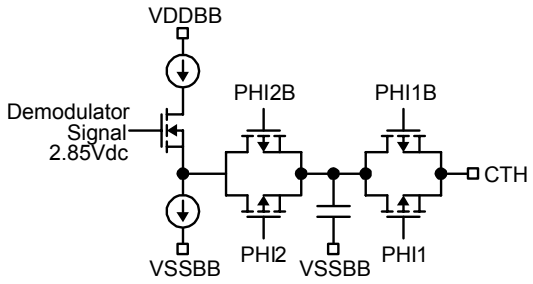



**Figure 2. CTH Pin**

Figure 2 illustrates the $C_{TH}$ pin interface circuit. The $C_{TH}$ pin is driven from a P-channel MOSFET source-follower with approximately 10µA of bias. Transmission gates TG1 and TG2 isolate the 6.9pF capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a "resistance" of approximately 100kΩ. The dc potential at the $C_{TH}$ pin is approximately 1.6V

### $C_{AGC}$ Pin

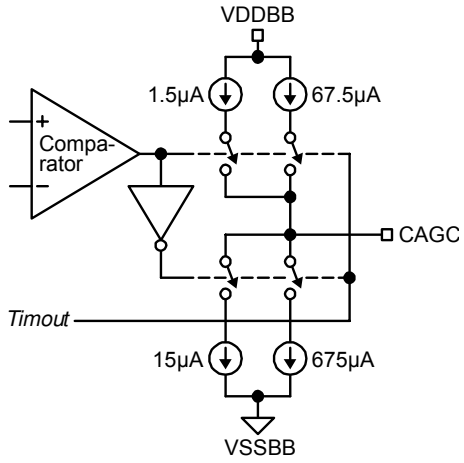



**Figure 3. CAGC Pin**

Figure 3 illustrates the $C_{AGC}$ pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor $C_{AGC}$. The attack current is nominally 15µA, while the decay current is a 1/10th scaling of this, nominally 1.5µA, making the attack/decay time constant ratio a fixed 10:1. Signal gain of the RF/IF strip inside the IC diminishes as the voltage at $C_{AGC}$ decreases. Modification of the attack/decay ratio is possible by adding resistance from the $C_{AGC}$ pin to either $V_{DDBB}$ or $V_{SSBB}$, as desired.

Both the push and pull current sources are disabled during shutdown, which maintains the voltage across $C_{AGC}$, and improves recovery time in duty-cycled applications. To further improve duty-cycle recovery, both push and pull currents are increased by 45 times for approximately 10ms after release of the SHUT pin. This allows rapid recovery of any voltage droop on $C_{AGC}$ while in shutdown.

### DO and WAKEB Pins

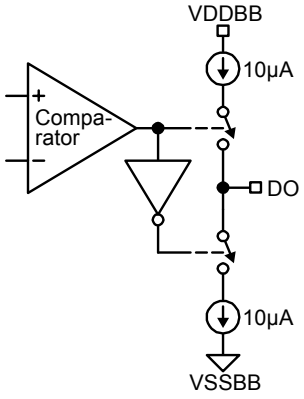



**Figure 4. DO and WAKEB Pins**

The output stage for DO (digital output) and WAKEB (wakeup output) is shown in Figure 4. The output is a 10µA push and 10µA pull switched-current stage. This output stage is capable of driving CMOS loads. An external buffer-driver is recommended for driving high-capacitance loads.

### REFOSC Pin

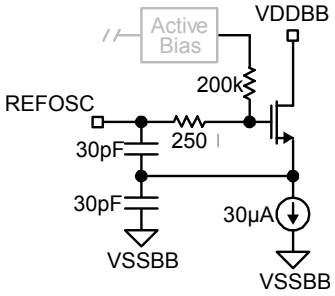



**Figure 5. REFOSC Pin**

The REFOSC input circuit is shown in Figure 5. Input impedance is high (200kΩ). This is a Colpitts oscillator with internal 30pF capacitors. This input is intended to work with standard ceramic resonators connected from this pin to the $V_{SSBB}$ pin, although a crystal may be used when greater frequency accuracy is required. The nominal dc bias voltage on this pin is 1.4V.

### SEL0, SEL1, SWEN, and SHUT Pins

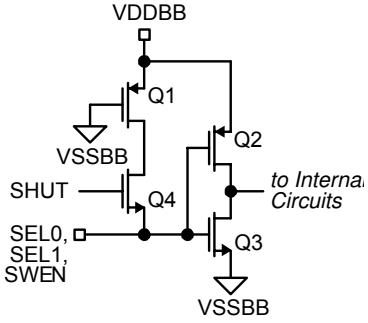



**Figure 6a. SEL0, SEL1, SWEN Pins**

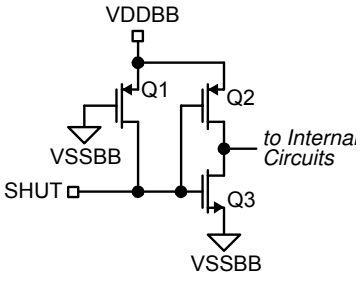



**Figure 6b. SHUT Pin**

Control input circuitry is shown in Figures 6a and 6b. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-channel MOSFET Q1 is a large channel length device which functions essentially as a "weak" pullup to $V_{DDBB}$. Typical pull-up current is 5µA, leading to an impedance to the $V_{DDBB}$ supply of typically 1MΩ.

## Applications Example

### 315MHz Receiver/Decoder Application

Figure 7 illustrates a typical application for the MICRF002 UHF Receiver IC. This receiver operates continuously (not duty cycled) in sweep mode, and features 6-bit address decoding and two output code bits.

Operation in this example is at 315MHz, and may be customized by selection of the appropriate frequency reference (Y1), and adjustment of the antenna length. The value of C4 would also change if the optional input filter is used. Changes from the 1kb/s data rate may require a change in the value of R1. A bill of materials accompanies the schematic.

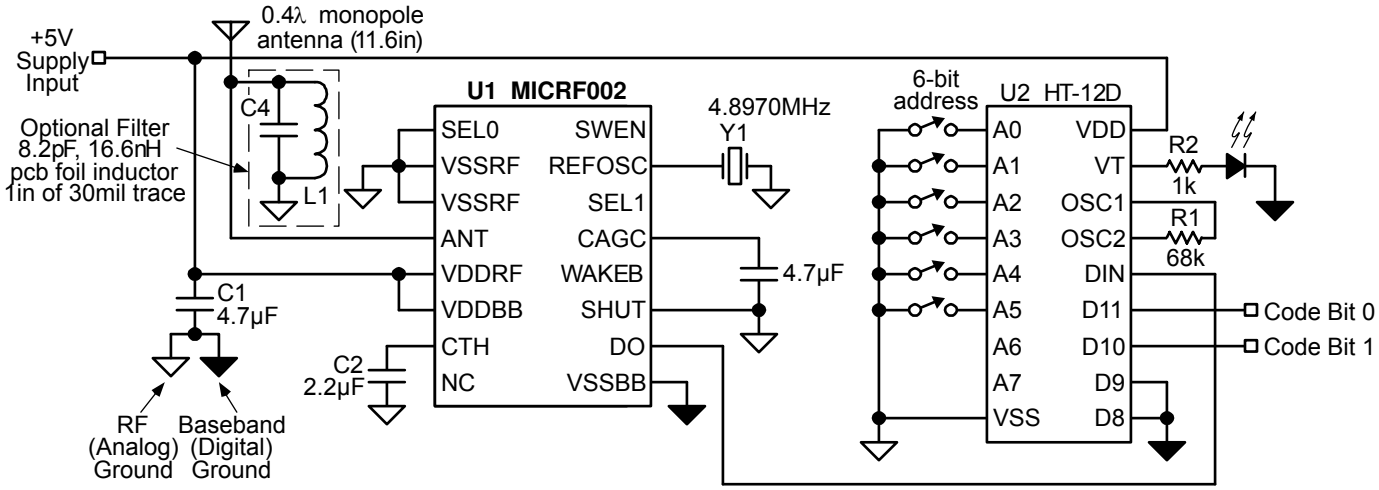



**Figure 7. 315MHz, 1kbps On-Off Keyed Recwiver/Decoder**

## Bill of Materials

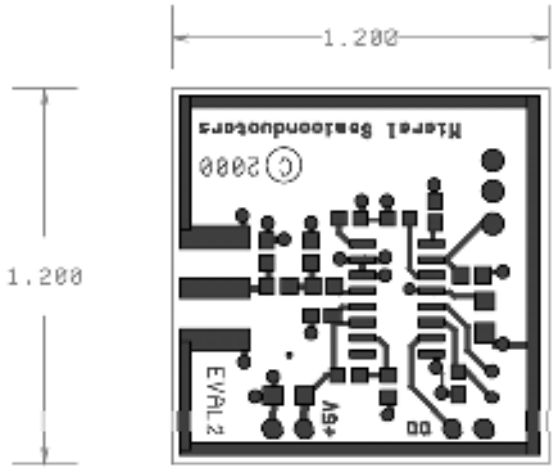
| Item | Part Number | Manufacturer | Description | Qty. |
|---|---|---|---|---|
| C1 | | Vishay[1] | 4.7µF, Dipped Tantalum Capacitor | 1 |
| C2 | | Vishay[1] | 2.2µF, Dipped Tantalum Capacitor | 1 |
| C3 | | Vishay[1] | 4.7µF, Dipped Tantalum Capacitor | 1 |
| C4 | | Vishay[1] | 8.2pF, COG Ceramic Capacitor | 1 |
| CR1 | CSA6.00MG | Murata[2] | 6.00MHz, Ceramic Resonator | 1 |
| D1 | SSF-LX100LID | Lumex[3] | RED LED | 1 |
| R1 | | | 68k, 1/4W, 5% | 1 |
| R2 | | Vishay[1] | 1k, 1/4W, 5% | 1 |
| **U1** | **MICRF002** | **Micrel, Inc.[4]** | **300-440MHz QwikRadio® ASK Receiver** | **1** |
| U2 | HT-12D | Holtek[5] | Logic Decoder | 1 |

**Notes:**

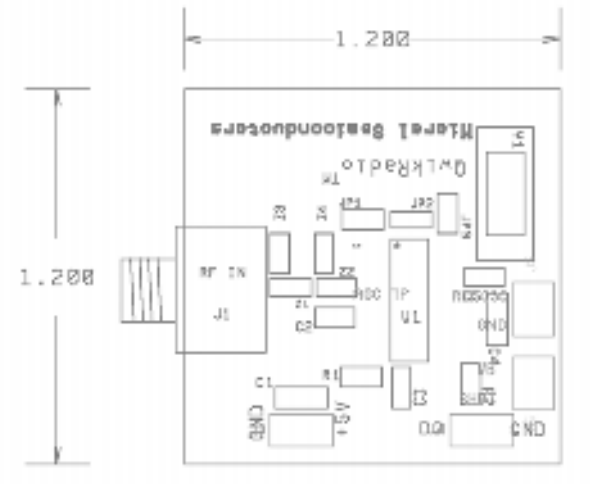
1. Vishay Tel: (203) 268-6261
2. Murata Tel: (800) 241-6574, Fx: (770) 436-3030
3. Lumex Tel: (800) 278-5666, Fx: (847) 359-8904
5. **Micrel, Inc.: (408) 944-0800**
5. Holtek Tel: (408) 894-9046, Fx: (408) 894-0838

## PCB Layout Information

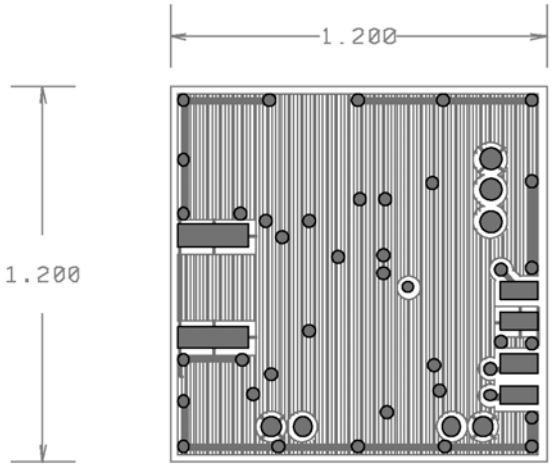
The MICRF002 evaluation board was designed and characterized using two sided 0.031 inch thick FR4 material with 1 ounce copper clad. If another type of printed circuit board material were to be substituted, impedance matching and characterization data stated in this document may not be valid. The gerber files for this board can be downloaded from the Micrel website at www.micrel.com.



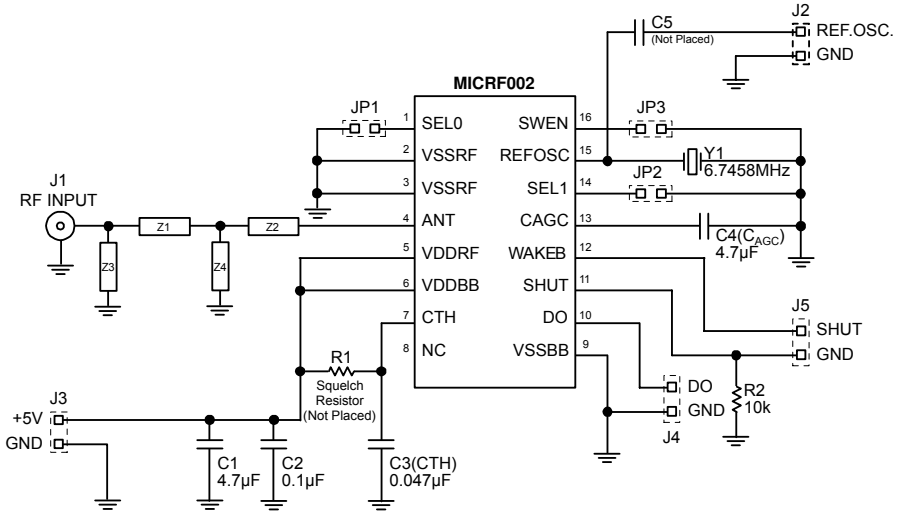

**PCB Silk Screen**



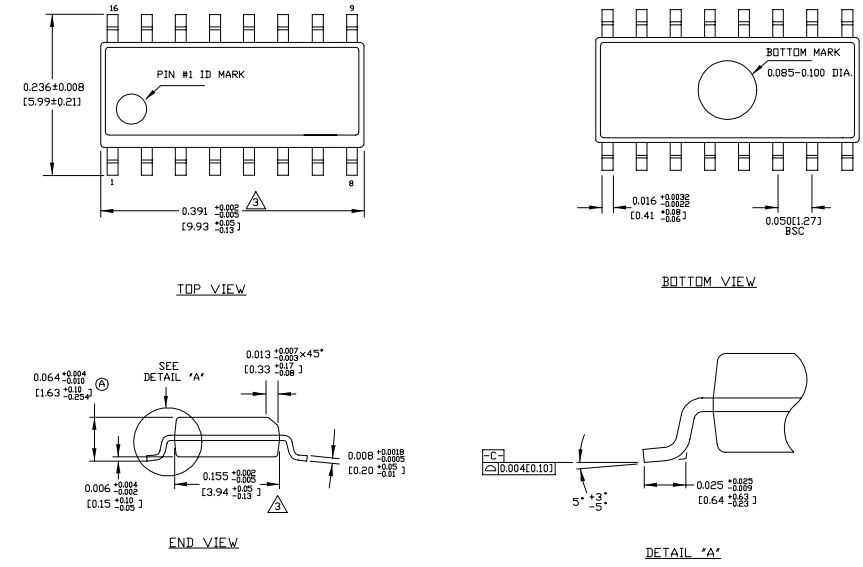

**PCB Component Side Layout**




**PCB Solder Side Layout**

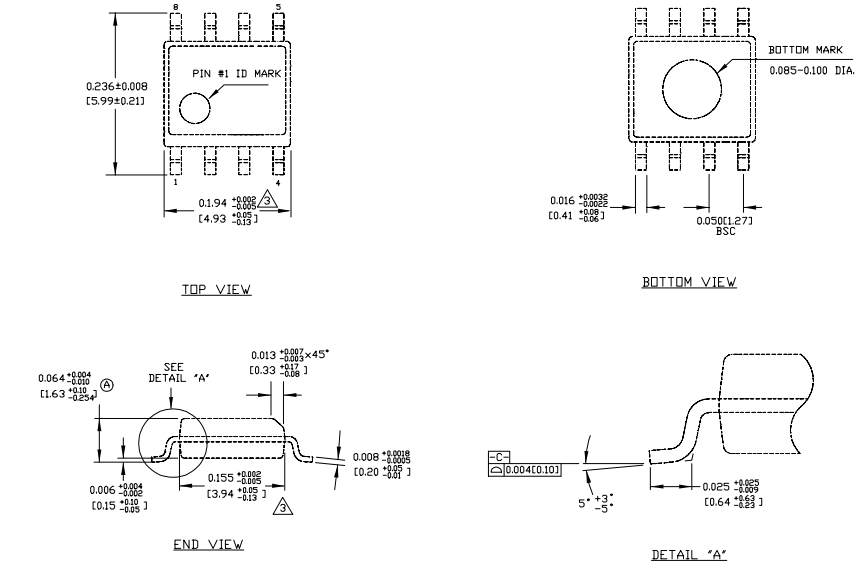


## Package Information




NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

**16-Pin SOIC (M)**




NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

**8-Pin SOIC (M)**

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