MLX90316 Rotary Position Sensor IC

Datasheet

Features and Benefits

- Absolute Rotary Position Sensor IC
- Simple & Robust Magnetic Design
- Tria⊗is® Hall Technology
- Programmable Angular Range up to 360 Degrees
- Programmable Linear Transfer Characteristic
- Selectable Analog (Ratiometric), PWM, Serial Protocol
- 12 bit Angular Resolution - 10 bit Angular Thermal Accuracy
- 40 bit ID Number
- Single Die – SOIC-8 Package RoHS Compliant
- Dual Die (Full Redundant) – TSSOP-16 Package RoHS Compliant



SOIC-8



TSSOP-16

Applications

- Absolute Rotary Position Sensor
- Steering Wheel Position Sensor
- Pedal Position Sensor
- Motor-shaft Position Sensor
- Throttle Position Sensor
- Float-Level Sensor
- Ride Height Position Sensor
- Non-Contacting Potentiometer



Description

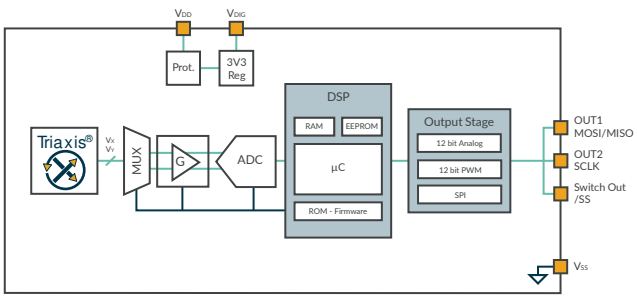
The MLX90316 is a Tria⊗is® Rotary Position Sensor providing the absolute angular position of a small dipole magnet rotating above the device surface (end-of-shaft magnet).

Thanks to an Integrated Magneto-Concentrator (IMC) on its surface, the monolithic device senses, in a contactless fashion, the horizontal component of the applied magnetic flux density.

This unique sensing principle applied to a rotary position sensor results into an impressive robustness of the angular position over the mechanical (airgap, off-axis) tolerances.

The rotation of this horizontal component is sensed over a wide range (up to 360 Deg. - complete revolution) and processed by the on-chip DSP (Digital Signal Processing) to ultimately report the absolute angular position of the magnet either as a ratiometric analog output or as PWM (Pulse-Width Modulation) signal or as a 14-bit data accessible through a 3-pin SPI (serial interface) channel.

The output transfer characteristic is fully programmable (e.g. offset, gain, clamping levels, linearity, thermal drift, filtering, range...) to match any specific requirement through end-of-line calibration. The Melexis programming unit PTC-04 communicates and calibrates the device exclusively through the connector terminals (VDD-VSS-OUT).



Melexis

INSPIRED ENGINEERING

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1. Ordering Information

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90316	S	DC	BCG-000	RE
MLX90316	E	DC	BCG-000	RE
MLX90316	K	DC	BCG-000	RE
MLX90316	L	DC	BCG-000	RE
MLX90316	E	GO	BCG-000	RE
MLX90316	K	GO	BCG-000	RE
MLX90316	L	GO	BCG-000	RE
MLX90316	K	DC	BCG-200	RE
MLX90316	K	GO	BCG-200	RE
MLX90316	K	DC	BCG-300	RE
MLX90316	K	GO	BCG-300	RE
MLX90316	E	DC	BDG-100	RE
MLX90316	K	DC	BDG-100	RE
MLX90316	L	DC	BDG-100	RE
MLX90316	E	GO	BDG-100	RE
MLX90316	K	GO	BDG-100	RE
MLX90316	L	GO	BDG-100	RE
MLX90316	L	GO	BDG-102	RE
MLX90316	L	DC	BDG-102	RE
MLX90316	L	DC	BCS-000	RE

Legend:

Temperature Code:	S: from -20 Deg.C to 85 Deg.C E: from -40 Deg.C to 85 Deg.C K: from -40 Deg.C to 125 Deg.C L: from -40 Deg.C to 150 Deg.C
Package Code:	"DC" for SOIC-8 package "GO" for TSSOP-16 package (dual die)
Option Code:	AAA-xxx: die version xxx-000: standard xxx-100: SPI xxx-102: SPI75AGC, see section 13.4.2 xxx-200: PPA (Pre-programmed Analog) xxx-300: PPD (Pre-programmed Digital)
Packing Form:	"RE" for Reel "TU" for Tube
Ordering Example:	MLX90316KDC-BCG-000-TU

Table 1 - Legend

2. Functional Diagram

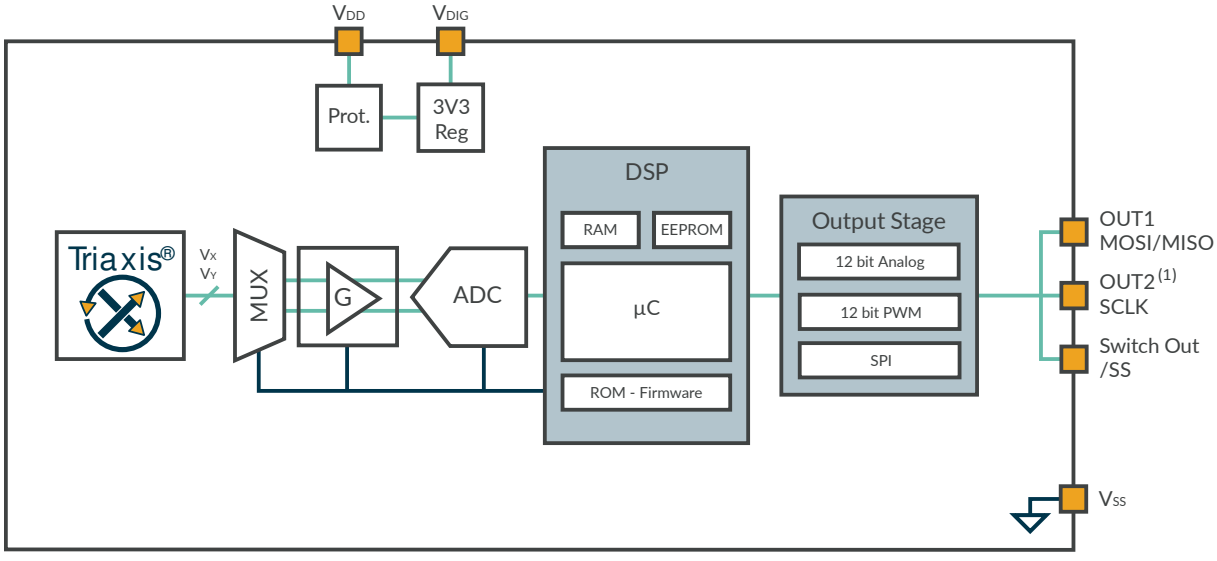


Figure 1 – Block Diagram

[1] *Output 2 only available on MLX90316xDC-BCS*

3. Glossary of Terms

Gauss (G), Tesla (T)	Units for the magnetic flux density - 1 mT = 10 G
TC	**T**emperature **C**oefficient (in ppm/Deg.C.)
NC	**N**ot **C**onnected
PWM	**P**ulse **W**idth **M**odulation
%DC	**D**uty **C**ycle of the output signal i.e. T_{ON} /(T_{ON} + T_{OFF})
ADC	**A**nalog-to-**D**igital **C**onverter
DAC	**D**igital-to-**A**nalog **C**onverter
LSB	**L**east **S**ignificant **B**it
MSB	**M**ost **S**ignificant **B**it
DNL	**D**ifferential **N**on-**L**inearity
INL	**I**ntegral **N**on-**L**inearity
RISC	**R**educed **I**nstruction **S**et **C**omputer
ASP	**A**nalog **S**ignal **P**rocessing
DSP	**D**igital **S**ignal **P**rocessing
ATAN	Trigonometric function: arctangent (or inverse tangent)
IMC	**I**ntegrated **M**agneto-**C**oncentrator (IMC®)
CoRDiC	**Co**ordinate **R**otation **Di**gital **C**omputer (i.e. iterative rectangular-to-polar transform)
EMC	**E**lectro-**M**agnetic **C**ompatibility

Table 2 – Glossary of Terms

4. Pinout

PIN	SOIC-8		TSSOP-16	
	Analog / PWM	Serial Protocol	Analog / PWM	Serial Protocol
1	VDD	VDD	$VDIG_1$	$VDIG_1$
2	Test 0	Test 0	VSS_1 ($Ground_1$)	VSS_1 ($Ground_1$)
3	Switch OUT	/SS	VDD_1	VDD_1
4	Not Used / OUT 2 [2]	SCLK	$Test\ 0_1$	$Test\ 0_1$
5	OUT	MOSI / MISO	$Switch\ OUT_2$	$/SS_2$
6	Test 1	Test 1	$Not\ Used_2$	$SCLK_2$
7	VDIG	VDIG	OUT2	$MOSI_2$ / $MISO_2$
8	VSS (Ground)	VSS (Ground)	$Test\ 1_2$	$Test\ 1_2$
9			$VDIG_2$	$VDIG_2$
10			VSS_2 ($Ground_2$)	VSS_2 ($Ground_2$)
11			VDD_2	VDD_2
12			$Test\ 0_2$	$Test\ 0_2$
13			$Switch\ OUT_1$	$/SS_1$
14			$Not\ Used_1$	$SCLK_1$
15			OUT1	$MOSI_1$ / $MISO_1$
16			$Test\ 1_1$	$Test\ 1_1$

For optimal EMC behavior, it is recommended to connect the unused pins (Not Used and Test) to the Ground (see section 16).

[2] *MLX90316xDC-BCS includes a programmable second output*

5. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, V_{DD} (overvoltage)	+ 20 V
Reverse Voltage Protection	- 10 V
Positive Output Voltage – Standard Version (Analog or PWM)	+ 10 V + 14 V (200 s max – T_A = + 25 Deg.C)
Positive Output Voltage – SPI Version	V_{DD} + 0.3V
Positive Output Voltage (Switch Out)	+ 10 V + 14 V (200 s max – T_A = + 25 Deg.C)
Output Current (I_{OUT})	± 30 mA
Reverse Output Voltage	- 0.3 V
Reverse Output Current	- 50 mA
Operating Ambient Temperature Range, T_A	- 40 Deg.C … + 150 Deg.C
Storage Temperature Range, T_S	- 40 Deg.C … + 150 Deg.C
Magnetic Flux Density	± 700 mT

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6. Electrical Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Nominal Supply Voltage	V_{DD}		4.5	5	5.5	V
Supply Current [3]	I_{DD}	Slow mode [4] Fast mode [4]		8.5 13.5	11 16	mA mA
POR Level	V_{DD} POR	Supply Under Voltage	2	2.7	3	V
Output Current	I_{OUT}	Analog Output mode PWM Output mode	-8 -20		8 20	mA mA
Output Short Circuit Current	I_{short}	VOUT = 0 V VOUT = 5 V VOUT = 14 V (T_A = 25 Deg.C)		12 12 24	15 15 45	mA mA mA
Output Load	R_L	Pull-down to Ground Pull-up to 5V [5]	1 1	10 10	∞ [6] ∞ [6]	kΩ kΩ
Analog Saturation Output Level	Vsat_lo	Pull-up load $R_L \geq$ 10 kΩ			3	%V_{DD}
	Vsat_hi	Pull-down load $R_L \geq$ 10 kΩ	96			%V_{DD}
Digital Saturation Output Level	VsatD_lo	Pull-up Low Side $R_L \geq$ 10 kΩ Push-Pull (IOUT = -20mA)			1.5	%V_{DD}
	VsatD_hi	Push-Pull (IOUT = 20mA)	97			%V_{DD}
Active Diagnostic Output Level	Diag_lo	Pull-down load $R_L \geq$ 10 kΩ Pull-up load $R_L \geq$ 10 kΩ			1 1.5	%V_{DD} %V_{DD}
	Diag_hi	Pull-down load $R_L \geq$ 10 kΩ Pull-up load $R_L \geq$ 10 kΩ	97 98			%V_{DD} %V_{DD}
Passive Diagnostic Output Level	BVssPD	Broken Vss [8] & Pull-down load RL ≤ 10 kΩ			4 [7]	%V_{DD}

[3] Supply current per silicon die. Dual die version will consume twice the current
[4] See section 13.4.1 for details concerning Slow and Fast mode
[5] Applicable for output in Analog and PWM (Open-Drain) mode
[6] $R_L < \infty$ for output in PWM mode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
(Broken Track Diagnostic) [7]	BVSSPU	Broken VSS [8] & Pull-up load $R_L \geq 1$ kΩ	99	100		%VDD
	BVDDPD	Broken VDD [8] & Pull-down load $R_L \geq 1$ kΩ		0	1	%VDD
	BVDDPU	Broken VDD & Pull-up load to 5 V	No Broken Track diagnostic			%VDD
Clamped Output Level [9]	Clamp_lo	Programmable	0		100	%VDD
	Clamp_hi	Programmable	0		100	%VDD
Switch Out [10]	Sw_lo	Pull-up Load 1.5 kΩ to 5 V	0.55		1.1	V
	Sw_hi	Pull-up Load 1.5 kΩ to 5 V	3.65		4.35	V

As an illustration of the previous table, the MLX90316 fits the typical classification of the output span described on the Figure 2.

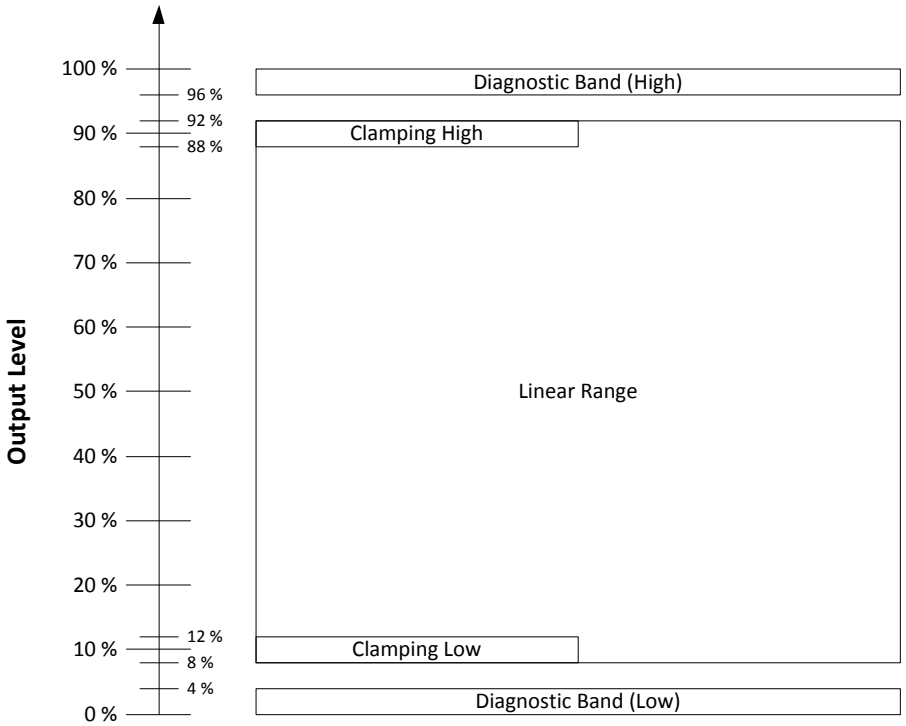


Figure 2 – Output Span Classification

[7] *For detailed information, see also section 14*
[8] *Not Valid for the SPI Version*
[9] *Clamping levels need to be considered vs the saturation of the output stage (see Vsat_lo and Vsat_hi)*
[10] *See section 13.1.4 for the application diagram*

7. Isolation Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L). Only valid for the package code GO i.e. dual die version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Isolation Resistance		Between dice	4			MΩ

8. Timing Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck	Slow mode [11] Fast mode [11]		7 20		MHz MHz
Sampling Rate		Slow mode [11] Fast mode [11]		600 200		µs µs
Step Response Time	Ts	Slow mode [11], Filter = 5 [12] Fast mode [11], Filter = 0 [12]		 400	4 600	ms µs
Watchdog	Wd	See section 14			5	ms
Start-up Cycle	Tsu	Slow and Fast mode [11]			15	ms
Analog Output Slew Rate		C_{OUT} = 42 nF C_{OUT} = 100 nF		200 100		V/ms V/ms
PWM Frequency	F_{PWM}	PWM Output Enabled	100		1000	Hz
Digital Output Rise Time		Mode 5 – 10 nF, R_L = 10 kΩ Mode 7 – 10 nF, R_L = 10 kΩ		120 2.2		µs µs
Digital Output Fall Time		Mode 5 – 10 nF, R_L = 10 kΩ Mode 7 – 10 nF, R_L = 10 kΩ		1.8 1.9		µs µs

[11] *See section 13.4.1 for details concerning Slow and Fast mode*
[12] *See section 13.5 for details concerning Filter parameter*

9. Accuracy Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ADC Resolution on the raw signals sine and cosine	R_{ADC}	Slow Mode [13] Fast Mode [13]		15 14		bits bits
Thermal Offset Drift #1 [14]		Thermal Offset Drift at the DSP input (excl. DAC and output stage) Temperature suffix S, E and K Temperature suffix L	 -60 -90		 60 90	 LSB_{15} LSB_{15}
Thermal Offset Drift #2 (to be considered only for the analog output mode)		Thermal Offset Drift of the DAC and Output Stage Temperature suffix S, E and K Temperature suffix L	 -0.3 -0.4		 0.3 0.4	 %V_{DD} %V_{DD}
Thermal Drift of Sensitivity Mismatch [15]		Temperature suffix S, E and K Temperature suffix L	-0.3 -0.5		0.3 0.5	% %
Intrinsic Linearity Error [16]	Le	T_A = 25 Deg.C	-1		1	Deg.
Analog Output Resolution	R_{DAC}	12 bits DAC (Theoretical – Noise free) INL DNL		0.025	 4 2	%V_{DD} /LSB LSB LSB
Output stage Noise		Clamped Output		0.05		%V_{DD}

[13] 15 bits corresponds to 14 bits + sign and 14 bits corresponds to 13 bits + sign. After angular calculation, this corresponds to 0.005Deg./LSB_{15} in Low Speed Mode and 0.01Deg./LSB_{14} in High Speed.

[14] For instance, Thermal Offset Drift #1 equal ± 60LSB_{15} yields to max. ± 0.3 Deg. angular error for the computed angular information (output of the DSP). See Front End Application Note for more details. This is only valid if automatic gain is set (See section 13.4.2)

[15] For instance, Thermal Drift of Sensitivity Mismatch equal ± 0.4% yields to max. ± 0.1 Deg. angular error for the computed angular information (output of the DSP). See Front End Application Note for more details.

[16] The Intrinsic Linearity Error refers to the IC itself (offset, sensitivity mismatch, orthogonality) taking into account an ideal rotating field. Once associated to a practical magnetic construction and the associated mechanical and magnetic tolerances, the output linearity error increases. However, it can be improved with the multi point end-user calibration that is available on the MLX90316.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Noise pk-pk [17]		RG = 9, Slow mode, Filter = 5 RG = 9, Fast mode, Filter = 0		0.03 0.1	0.06 0.2	Deg. Deg.
Ratiometry Error			-0.1	0	0.1	%V_{DD}
PWM Output Resolution	R_{PWM}	12 bits (Theoretical – Jitter free)		0.025		%DC/ LSB
PWM Jitter [18]	J_{PWM}	RG = 6, F_{PWM} = 250 Hz – 800 Hz			0.2	%DC
Serial Protocol Output Resolution	R_{SP}	14 bits – 360 Deg. Mapping (Theoretical – Jitter free)		0.022		Deg./ LSB

10. Magnetic Specification

DC Operating Parameters at V_{DD} = 5V (unless otherwise specified) and for T_A as specified by the Temperature suffix (S, E, K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Flux Density	B		20	50	70 [19]	mT
Magnet Temperature Coefficient	TCm		-2400		0	ppm/ Deg.C

11. CPU & Memory Specification

The DSP is based on a 16 bit RISC µController. This CPU provides 5 MIPS while running at 20 MHz.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ROM				10		KB
RAM				256		B
EEPROM				128		B

[17] The application diagram used is described in the recommended wiring. For detailed information, refer to section Filter in application mode (Section 13.5).
[18] Jitter is defined by ± 3 σ for 1000 successive acquisitions and the slope of the transfer curve is 100%DC/360 Deg.
[19] Above 70 mT, the IMC starts saturating yielding to an increase of the linearity error.

12. End-User Programmable Items

Parameter	Comments	Default Values				
		STANDARD	SPI / SPI75AGC	PPA	PPD	# bit
Output Mode	Output Stage Mode	4	N/A	4	7	3
	MLX90316BCS	2	N/A	2	N/A	3
PWMPOL1	PWM Polarity	0	N/A	N/A	1	1
PWMT	PWM Frequency	1000h	N/A	N/A	1kHz	16
CLOCKWISE		0	0	0	1	1
DP	Discontinuity Point	0h	0h	0h	0h	15
LNR_S0	Initial Slope	0h	N/A	N/A	N/A	16
LNR_A_X	AX Coordinate	8000h	0	0	0	16
LNR_A_Y	AY Coordinate	0h	0%	10%	10%	16
LNR_A_S	AS Slope	0h	100%/360d	80%/360d	80%/360d	16
LNR_B_X	BX Coordinate	FFFFh	FFFFh	FFFFh	FFFFh	16
LNR_B_Y	BY Coordinate	0h	FFFFh	FFFFh	FFFFh	16
LNR_B_S	BS Slope	0h	N/A	N/A	N/A	16
LNR_C_X	CX Coordinate	FFFFh	FFFFh	FFFFh	FFFFh	16
LNR_C_Y	CY Coordinate	FFFFh	FFFFh	FFFFh	FFFFh	16
LNR_C_S	CS Slope	0h	N/A	N/A	N/A	16
CLAMP_HIGH	Clamping High	8%	0%	10%	10%	16
CLAMP_LOW	Clamping Low	8%	100%	90%	90%	16
KD	Switch Out	FFFFh	FFFFh	FFFFh	FFFFh	16
	MLX90316BCS	0	N/A	FFFFh	N/A	16
KDHYST	Hysteresis on Switch Out	N/A	N/A	N/A	N/A	8
DEADZONE		0	0	0	0	8
FHYST		4	0	0	0	8
	MLX90316BCS	0	N/A	0	N/A	8

Parameter	Comments	Default Values				
		STANDARD	SPI / SPI75AGC	PPA	PPD	# bit
MLXID1 / MLXID2 / MLXID3 [20]		MLX	MLX	MLX	MLX	16
CUSTID1		1	1	1	1	8
CUSTID2 [21]		6 [22]	19 / 36	16	20	16
CUSTID3		MLX	MLX	MLX	MLX	16
FREE2		0	0	0	0	8
	MLX90316BCS	0	N/A	2Ah	N/A	16
FILTER		5	0	2	5	16
FILTER A1 [21]	Filter coefficient A1 for FILTER = 6	6600h	N/A	N/A	N/A	16
FILTER A2 [21]	Filter coefficient A2 for FILTER = 6	2A00h	N/A	N/A	N/A	16
ARGC	Auto Gain at Start Up	0	1	1	1	1
	MLX90316BCS	0	N/A	1	N/A	1
HIGHSPEED		0	1	0	1	1
FSWAP		1	1	0	1	1
FORCECRA75	Radius Adjustment to 75%	0	0 / 1	0	0	1
AUTO_RG	Automatic Rough Gain Selection	0	1	1	1	1
RoughGain		9	0	3	0	8
	MLX90316BCS	6	N/A	3	N/A	8
RGThresL		0	0	0	0	4
RGThresH		15	15	15	15	4
EEHAMHOLE		3131h	0	0	0	16
RESONFAULT		0	1	1	1	2

[20] *MLXIDs parameters contain unique ID programmed by Melexis to guarantee full part traceability*
[21] *Not available in MLX90316xDC-BCS*
[22] *For MLX90316SDC–BCG–000, the CUSTID2 parameter might differ from the given value (28d instead of 6d)*

Parameter	Comments	Default Values				
		STANDARD	SPI / SPI75AGC	PPA	PPD	# bit
MLXLOCK		0	1	1	1	1
LOCK		0	1	1	1	1
	MLX90316BCS	0	N/A	0	N/A	1
Parameters for MLX90316xDC-BCS only						
OUT2EN		1	N/A	1	N/A	1
OUT2 SLOPE RATIO	Was CUSTID2	N/A	N/A	-1	N/A	8
OUT2 OFFSET		MLX	N/A	100%	N/A	8
CLAMP_LOW OUT2		8%	N/A	10%	N/A	16
CLAMP_HIGH OUT2		8%	N/A	90%	N/A	16

13. Description of End-User Programmable Items

13.1. Output Mode

The MLX90316 output type is defined by the Output Mode parameter.

Parameter	Value	Description
Analog Output Mode	2, 4	Analog Rail-to-Rail
PWM Output Mode	5 7	Low Side (NMOS) Push-Pull
Serial Protocol Output Mode	N/A	Low Side (NMOS)

13.1.1. Analog Output Mode

The Analog Output Mode is a rail-to-rail and ratiometric output with a push-pull output stage configuration allows the use of a pull-up or pull-down resistor.

13.1.2. PWM Output Mode

If one of the PWM Output modes is selected, the output signal is a digital signal with Pulse Width Modulation (PWM).

In mode 5, the output stage is an open drain NMOS transistor (low side), to be used with a pull-up resistor to V_{DD}.

In mode 7, the output stage is a push-pull stage for which Melexis recommends the use of a pull-up resistor to V_{DD}.

The PWM polarity is selected by the PWMPOL1 parameter:

- PWMPOL1 = 0 for a low level at 100%
- PWMPOL1 = 1 for a high level at 100%

The PWM frequency is selected by the PWMT parameter.

Oscillator Mode	Pulse-Width Modulation Frequency (Hz)			
	100	200	500	1000
Low Speed	~35000	~17500	~7000	~3500
High Speed	-	~50000	~20000	~10000

Table 3 – PWM Frequency Code (based on typical main clock frequency)

For instance, in Low Speed Mode, set PWMT = 7000 (decimal) to set the PWM frequency around 500 Hz [23].

13.1.3. Serial Protocol Output Mode

The MLX90316 features a digital Serial Protocol mode. The MLX90316 is configured as a Slave node. See the dedicated Serial Protocol section for a full description (Section 15).

[23] *In order to compensate for the lot to lot variation of the main clock frequency (Ck), Melexis strongly recommends trimming the PWM frequency during EOL programming (see the PTC-04 documentation).*

13.1.4. Switch Out

Parameter	Value	Unit
KD	0 … 359.9999	Deg.
KDHYST	0 … 1.4	Deg.

The switch is activated (Sw_lo) when the digital angle is greater than the value stored in the KD parameter. This angle refers to the internal angular reference linked to the parameter DP and not to the absolute physical 0 Deg. angle.

The KDHYST defines the hysteresis amplitude around the Switch point. The switch is activated if the digital angle is greater than KD+KDHYST. It is deactivated if the digital angle is less than KD-KDHYST.

The mandatory application diagram to use this feature is depicted in the Figure 3. See section 6 for the electrical characteristic.

If the Switch feature is not used in the application, the output pin shall be connected to ground.

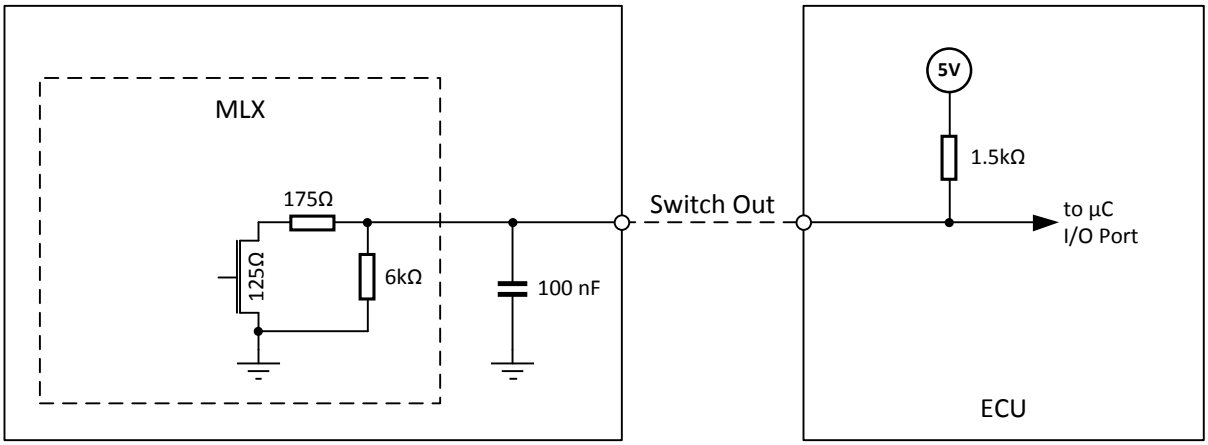


Figure 3 – Application Diagram for the Switch Out

13.2. Output Transfer Characteristic

Parameter	Value	Unit
CLOCKWISE	0 → CCW 1 → CW	
DP	0 … 359.9999	Deg.
LNR_A_X LNR_B_X LNR_C_X	0 … 359.9999	Deg.

Parameter	Value	Unit
LNR_A_Y LNR_B_Y LNR_C_Y	0 … 100	%
LNR_S0 LNR_A_S LNR_B_S	0 … 17	%/Deg.
LNR_C_S	-17 … 0 … 17	%/Deg.
CLAMP_LOW	0 … 100	%
CLAMP_HIGH	0 … 100	%
DEADZONE	0 … 359.9999	Deg.
MLX90316 xDC – BCS only		
OUT2 SLOPE RATIO	-8 … 0 … 8	-
OUT2 OFFSET	-400 … 400	%
CLAMP_LOW OUT2	0 … 100	%
CLAMP_HIGH OUT2	0 … 100	%

13.2.1. CLOCKWISE Parameter

The CLOCKWISE parameter defines the magnet rotation direction.

- CCW is the defined by the 1-4-5-8 pin order direction for the SOIC-8 package and 1-8-9-16 pin order direction for the TSSOP-16 package.
- CW is defined by the reverse direction: 8-5-4-1 pin order direction for the SOIC-8 and 16-9-8-1 pin order direction for the TSSOP-16 package.

Refer to the drawing in the IMC positioning sections (Sections 19.3 and 19.6).

13.2.2. Discontinuity Point (or Zero Degree Point)

The Discontinuity Point redefines the 0 Deg. point. The discontinuity point places the origin at any location of the trigonometric circle. The DP is used as reference for all the angular measurements.

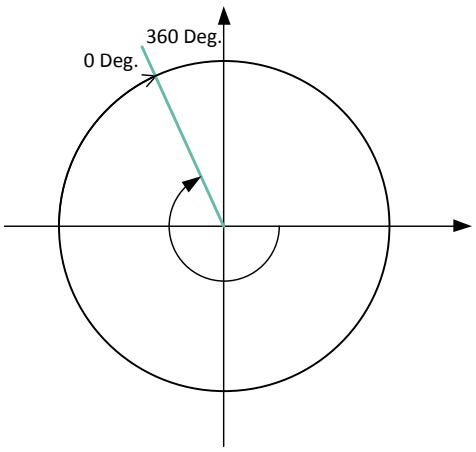


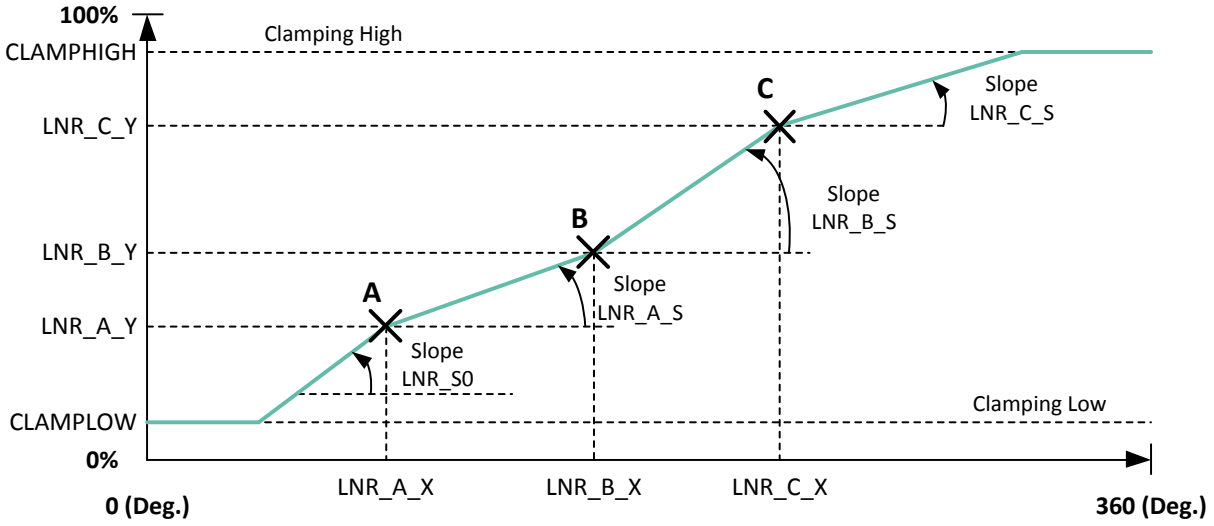
Figure 4 - The placement of the Discontinuity Point (Zero Degree Point) is programmable

13.2.3. LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90316 transfer function from the digital angle value to the output voltage is described by the drawing below. Six segments can be programmed but the clamping levels are necessarily flat.

Two to five calibration points are then available, reducing the overall non-linearity of the IC by almost an order of magnitude each time. Three to five point calibration will be preferred by customers looking for excellent non-linearity figures. Two-point calibrations will be preferred by customers looking for a lower cost calibration set-up and shorter calibration time.



13.2.4. CLAMPING Parameters

The clamping levels are two independent values to limit the output voltage range in normal operation. The CLAMP_LOW parameter sets the minimum output voltage level while the CLAMP_HIGH parameter sets the maximum output voltage level. Both parameters have 16 bits of adjustment. In analog mode the resolution

will be limited by the D/A converter (12 bits) to 0.024%VDD. In PWM mode the resolution will be 0.024%DC. In SPI mode the resolution is 14bits or 0.022 Deg. over 360 Deg.

13.2.5. DEADZONE Parameter

The dead zone is defined as the angle window between 0 and 359.9999 Deg.

When the digital angle lies in this zone, the IC is in fault mode (RESONFAULT must be set to "1" – See section 13.6.1).

13.2.6. Output 2 (MLX90316xDC-BCS ONLY)

The MLX90316BCS firmware offers the possibility to program a second output transfer characteristic of the single die version.

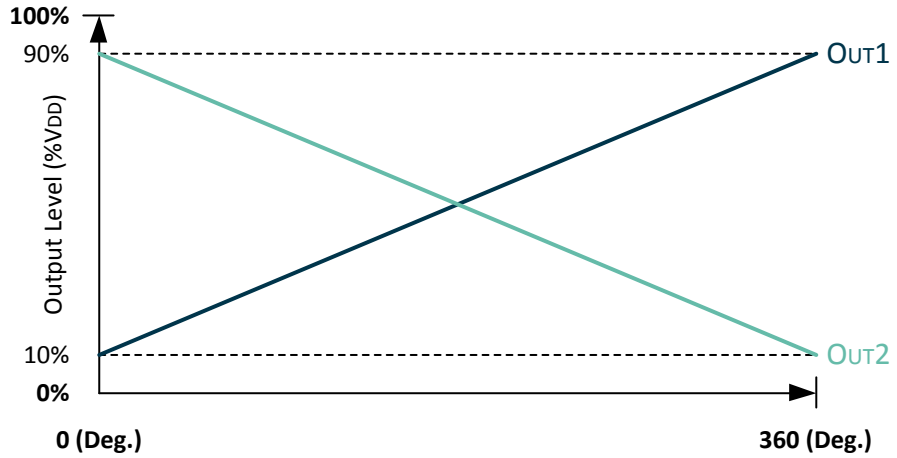
The following formula is used in the 90316BCS:

$$OUT2 = OUT2SlopeRatio * OUT1 + OUT2Offset$$

Range OUT2 = [Clamp_Low OUT2 … Clamp_High OUT2]

OUT2 SLOPE RATIO Controls the slope ratio OUT1 vs OUT2. The ratio can be positive or negative.

The example of MLX90316LDC-BCS-PPA is given in the figure below (slope = -1, OUT2 = -1 x slope OUT1 + 100%).



13.3. Identification

Parameter	Value	Unit
MLXID1	0 … 65535	
MLXID2	0 … 65535	
MLXID3	0 … 65535	
CUSTID1	0 … 255	
CUSTID2	0 … 65535	
CUSTID3	0 … 65535	

Identification number: 40 bits freely useable by Customer for traceability purpose.

13.4. Sensor Front-End

Parameter	Value	Unit
HIGHSPEED	0 = Slow mode 1 = Fast mode	
ARGC	0 = disable 1 = enable	
AUTO_RG	0 = disable 1 = enable	
RoughGain	0 … 15	
RGThresL	0 … 15	
RGThresH	0 … 15	

13.4.1. HIGHSPEED Parameter

The HIGHSPEED parameter defines the main frequency for the DSP:

- HIGHSPEED = 0 selects the Slow mode with a 7 MHz master clock.
- HIGHSPEED = 1 selects the Fast mode with a 20 MHz master clock.

For better noise performance, the Slow Mode must be enabled.

13.4.2. ARGC, AUTO_RG, RoughGain and FORCECRA75 Parameters

AUTO_RG and ARGC parameters enable the automatic gain control (AGC) of the analog chain. The AGC loop is based on

$$(V_X)^2 + (V_Y)^2 = (\text{Amplitude})^2 = (\text{Radius})^2$$

and it targets an amplitude of 90% of the ADC input span.

At Start-Up phase, the gain stored in the parameter RoughGain is always used. Depending of the AUTO_RG and ARGC settings, the AGC regulation acts as follow:

- If ARGC is set, the regulation proceeds by jump to reach the target gain. Note that this regulation is only valid if the starting gain does not saturate the ADC. Melexis recommendation is to use RoughGain ≤ 3 if ARGC = 1.
- If ARGC is "0" and AUTO_RG is set to "1", the regulation adapts every cycle by one gain code the current gain to reach the 90% ADC span target. Note that if the value of RoughGain is too far from the actual gain, the chip will enter the normal operating mode (after the Start-Up phase) with an incorrect gain which will cause the device to go in diagnostic low (field too low/field too high – See section 14).
- If ARGC and AUTO_RG are "0", the AGC regulation is off and the gain used is the value stored in the parameter RoughGain. Melexis does not advise the use of this mode.

The parameter AUTO_RG activates the automatic regulation during normal operation of the device as background task.

The parameter FORCECRA75 modifies the target of the AGC algorithm to 75% - instead of 90% - of the ADC span (at start-up and in normal operation).

Melexis strongly recommends to set ARGC = "1", AUTO_RG = "1" and RoughGain ≤ 3 for all types of application. If the magnetic specifications of the application are well known and under control, the appropriate RoughGain can also be programmed with ARGC set to "0" and AUTO_RG to "1".

Please note that the angular errors listed in the section 9 are only valid if the AUTO_RG is activated. AUTO_RG avoids also the saturation of the analog chain and the associated linearity error.

The current gain (RG) can be read out with the PTC-04 and gives a rough indication of the applied magnetic flux density (Amplitude).

13.4.3. RGThresL, RGThresH Parameters

RGThresL & RGThresH define the boundaries within the gain setting (Rough Gain) is allowed to vary. Outside this range, the output is set in diagnostic low.

13.5. FILTER

Parameter	Value	Unit
FHYST	0 … 11; step 0.04	Deg.
FILTER	0 … 6	
FSWAP	0 1	

The MLX90316 includes 3 types of filters:

- Hysteresis Filter: programmable by the FHYST parameter
- Low Pass FIR Filters controlled with the Filter parameter
- Low Pass IIR Filter controlled with the Filter parameter and the coefficients FILTER A1 and FILTER A2

Note: if the parameter FSWAP is set to “1”, the filtering is active on the digital angle. If set to “0”, the filtering is active on the output transfer function.

13.5.1. Hysteresis Filter

The FHYST parameter is a hysteresis filter. The output value of the IC is not updated when the digital step is smaller than the programmed FHYST parameter value. The output value is modified when the increment is bigger than the hysteresis. The hysteresis filter reduces therefore the resolution to a level compatible with the internal noise of the IC. The hysteresis must be programmed to a value close to the noise level.

Please note that for the programmable version, the FHYST parameter is set to 4 by default. If you do not wish this feature, please set it to “0”.

13.5.2. FIR Filters

The MLX90316 features 6 FIR filter modes controlled with Filter = 0 … 5. The transfer function is described below:

$$y_n = \frac{1}{\sum_{i=0}^{j} a_i} \sum_{i=0}^{j} a_i x_{n-i}$$

The characteristics of the filters no 0 to 5 is given in the Table 4.

Filter No (j)	0	1	2	3	4	5
Type	Disable	Finite Impulse Response				
Coefficients a_0... a_5	N/A	110000	121000	133100	111100	122210
Title	No Filter	Extra Light		Light		
90% Response Time	1	2	3	4	4	5
99% Response Time	1	2	3	4	4	5
Efficiency RMS (dB)	0	2.9	4.0	4.7	5.6	6.2
Efficiency P2P (dB)	0	2.9	3.6	5.0	6.1	7.0

Table 4 – FIR Filters Selection Table

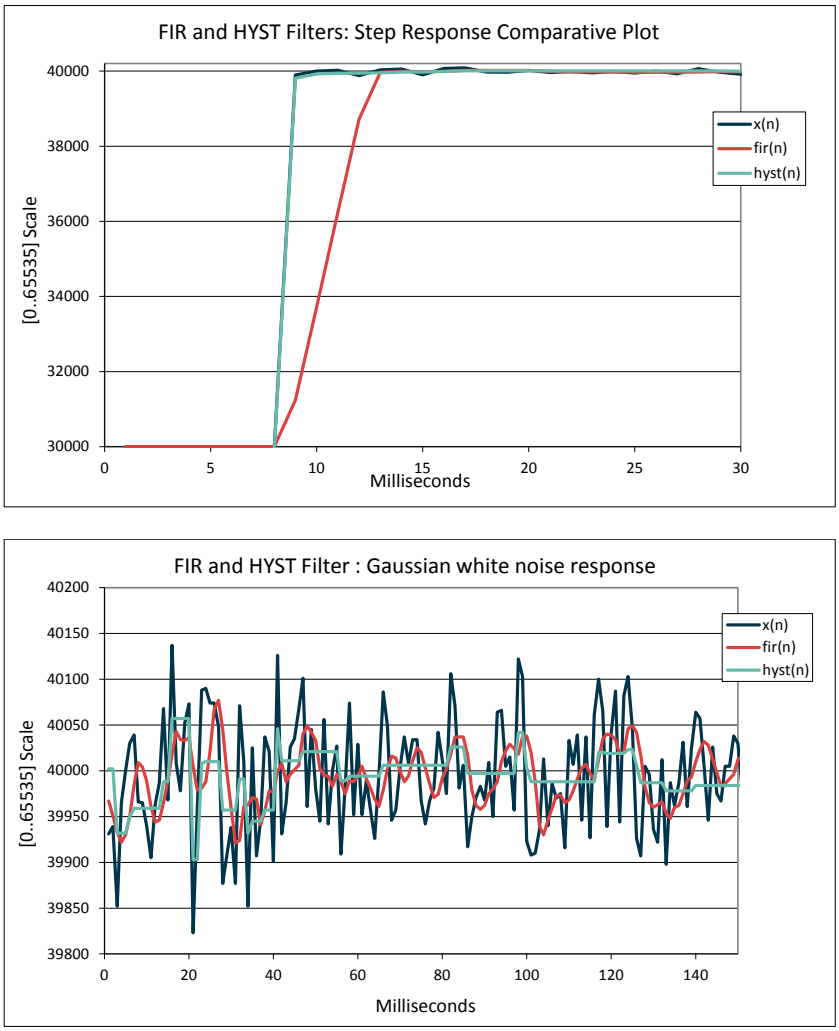


Figure 5 - Step Response and Noise Response for FIR (No 3) and FHYST = 10

13.5.3. IIR Filters

The IIR Filter is enabled with Filter = 6. The diagram of the IIR Filter implemented in the MLX90316 is given in Figure 6. Only the parameters A1 and A2 are configurable (See Table 5).

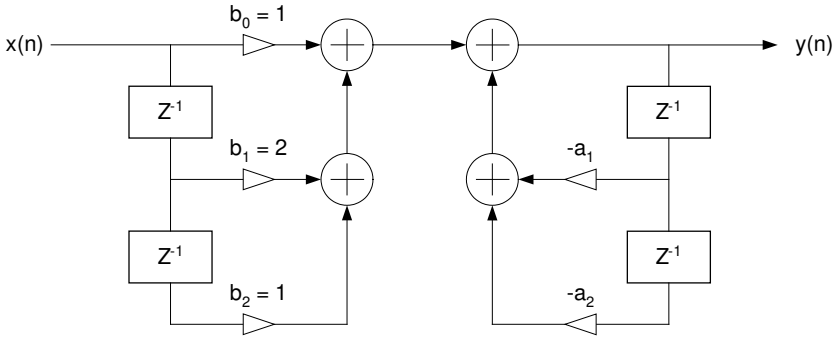


Figure 6 - IIR Diagram

Filter No	6					
Type	2nd Order Infinite Impulse Response (IIR)					
Title	Medium & Strong					
90% Response Time	11	16	26	40	52	100
Efficiency RMS (dB)	9.9	11.4	13.6	15.3	16.2	>20
Efficiency P2P (dB)	12.9	14.6	17.1	18.8	20.0	>20
Coefficient A1	26112	28160	29120	30208	31296	31784
Coefficient A2	10752	12288	12992	13952	14976	15412

Table 5 – IIR Filter Selection Table

The Figure 7 shows the response of the filter to a Gaussian noise with default coefficient A1 and A2.

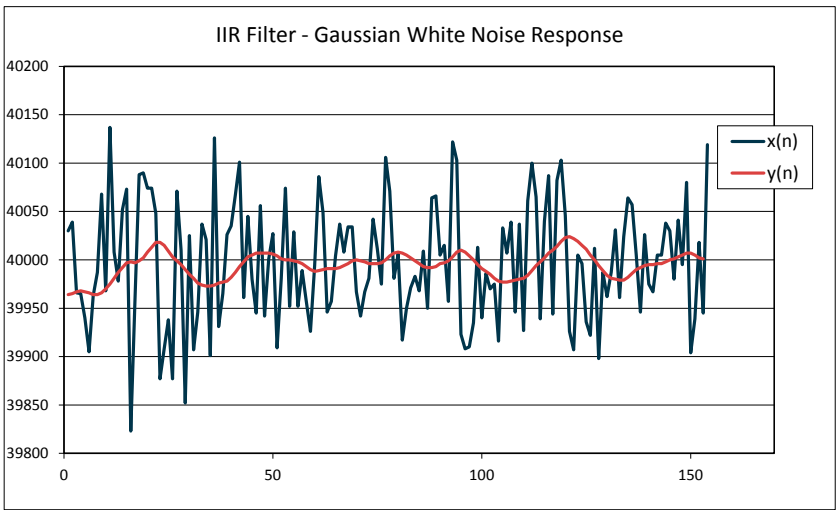


Figure 7 – Noise Response for the IIR Filter

13.6. Programmable Diagnostic Settings

Parameter	Value	Unit
RESONFAULT	0, 1	
EEHAMHOLE	0, 3131h	

13.6.1. RESONFAULT Parameter

This RESONFAULT parameter enables the soft reset when a fault is detected by the CPU when the parameter is set to 1. By default, the parameter is set to “0” but it is recommended to set it to “1” to activate the self diagnostic modes (See section 14).

Note that in the User Interface (MLX90316UI), the RESONFAULT is split in two bits:

- DRESONFAULT: disable the reset in case of a fault.
- DOUTINFAULT: disable output in diagnostic low in case of fault.

13.6.2. EEHAMHOLE Parameter

The EEHAMHOLE parameter disables the CRC check and the memory recovery (Hamming code) when it is equal to 3131h. Melexis strongly recommends to set the parameter to 0 (enable memory recovery). This is done automatically when using the MEMLOCK function.

13.7. Lock

Parameter	Value	Unit
MLXLOCK	0, 1	
LOCK	0, 1	

13.7.1. MLXLOCK Parameter

MLXLOCK locks all the parameters set by Melexis.

13.7.2. LOCK Parameter

LOCK locks all the parameters set by the user. Once the lock is enabled, it is not possible to change the EEPROM values. However it is still possible to read back the memory contents with the PTC-04 programmer.

Note that the lock bit should be set by the solver function “MemLock”.

14. Self Diagnostic

The MLX90316 provides numerous self-diagnostic features. Those features increase the robustness of the IC functionality as it will prevent the IC to provide erroneous output signal in case of internal or external failure modes ("fail-safe").

Fault Mode	Action	Effect on Outputs	Remark
ROM CRC Error at start up (64 words including Intelligent Watch Dog - IWD)	CPU Reset [24]	Diagnostic low [25]	All the outputs are already in Diagnostic low - (start-up)
ROM CRC Error (Operation - Background task)	Enter Endless Loop: - Progress (watchdog Acknowledge) - Set Outputs in Diagnostic low	Immediate Diagnostic low	
RAM Test Fail (Start-up)	CPU Reset	Diagnostic low	All the outputs are already in Diagnostic low (start-up)
Calibration Data CRC Error (Start-Up)	Hamming Code Recovery		Start-Up Time is increased by 3 ms if successful recovery
Hamming Code Recovery Error (Start-Up)	CPU Reset	Immediate Diagnostic low	See section 13.6.2
Calibration Data CRC Error (Operation - Background)	CPU Reset	Immediate Diagnostic low	
Dead Zone	Set Outputs in Diagnostic low. Normal Operation until the "dead zone" is left.	Immediate Diagnostic low	Immediate recovery if the "dead zone" is left
ADC Clipping (ADC Output is 0000h or 7FFFh)	Set Outputs in Diagnostic low. Normal mode and CPU Reset If recovery	Immediate Diagnostic low	

[24] CPU reset means

1. *Core Reset (same as Power-On-Reset). It induces a typical start up time.*
2. *Periphery Reset (same as Power-On-Reset)*
3. *Fault Flag/Status Lost*
4. *The reset can be disabled by clearing the RESONFAULT bit (See 13.6.1)*

[25] Refer to section 6 for the Diagnostic Output Level specifications

Fault Mode	Action	Effect on Outputs	Remark
Radius Overflow (> 100%) or Radius Underflow (< 50 %)	Set Outputs in Diagnostic low. Normal mode and CPU Reset If recovery	Immediate Diagnostic low	(50 % - 100 %) No magnet / field too high See also section 13.4.2
Fine Gain Clipping (FG < 0d or > 63d)	Set Outputs in Diagnostic low. Normal mode, and CPU Reset If recovery	Immediate Diagnostic low	
Rough Offset Clipping (RO is < 0d or > 127d)	Set Outputs in Diagnostic low. Normal mode, and CPU Reset If recovery	Immediate Diagnostic low	
Rough Gain Clipping (RG < RGTHRESLOW or RG > RGTHRESHIGH)	Set Outputs in Diagnostic low. Normal mode, and CPU Reset If recovery	Immediate Diagnostic low	See also section 13.4.2
DAC Monitor (Digital to Analog converter)	Set Outputs in Diagnostic low. Normal Mode with immediate recovery without CPU Reset	Immediate Diagnostic low	
ADC Monitor (Analog to Digital Converter)	Set Outputs in Diagnostic low. Normal Mode with immediate recovery without CPU Reset	Immediate Diagnostic low	ADC Inputs are Shorted
Undervoltage Mode	At Start-Up, wait until V_{DD} > 3V. During operation, CPU Reset after 3 ms debouncing	- V_{DD} < POR level => Outputs high impedance - POR level < V_{DD} < 3 V => Outputs in Diagnostic low	
Firmware Flow Error	CPU Reset	Immediate Diagnostic low	Intelligent Watchdog (Observer)
Read/Write Access out of physical memory	CPU Reset	Immediate Diagnostic low	100% Hardware detection
Write Access to protected area (IO and RAM Words)	CPU Reset	Immediate Diagnostic low	100% Hardware detection
Unauthorized entry in “SYSTEM” Mode	CPU Reset	Immediate Diagnostic low	100% Hardware detection
V_{DD} > 7 V	Set Output High Impedance (Analog)	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High [25]	100% Hardware detection

Fault Mode	Action	Effect on Outputs	Remark
V_{DD} > 9.4 V	IC is switched off (internal supply) CPU Reset on recovery	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High	100% Hardware detection
Broken V_{SS} [26]	CPU Reset on recovery	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High	100% Hardware detection. Pull down load ≤ 10 kΩ to meet Diag Low spec: - < 2% V_{DD} (temperature suffix S and E) - < 4% V_{DD} (temperature suffix K) - contact Melexis for temperature suffix L
Broken V_{DD} [26]	CPU Reset on recovery	Pull down resistive load => Diag. Low Pull up resistive load => Diag. High	No valid diagnostic for V_{PULLUP} = V_{DD}. Pull up load (≤ 10kΩ) to V_{PULLUP} > 8 V to meet Diag Hi spec > 96% V_{DD}.

[26] *Not Valid for SPI Version*

15. Serial Protocol

15.1. Introduction

The MLX90316 features a digital Serial Protocol mode. The MLX90316 is configured as a Slave node. The serial protocol of the MLX90316 is a three wires protocol (/SS, SCLK, MOSI-MISO):

- /SS pin is a 5 V tolerant digital input
- SCLK pin is a 5 V tolerant digital input
- MOSI-MISO pin is a 5 V tolerant open drain digital input/output

The basic knowledge of the standard SPI specification is required for the good understanding of the present section.

15.2. SERIAL PROTOCOL Mode

- CPHA = 1 → even clock changes are used to sample the data
- CPOL = 0 → active-Hi clock

The positive going edge shifts a bit to the Slave's output stage and the negative going edge samples the bit at the Master's input stage.

15.3. MOSI (Master Out Slave In)

The Master sends a command to the Slave to get the angle information.

15.4. MISO (Master In Slave Out)

The MISO of the slave is an open-collector stage. Due to the capacitive load, a >1 kΩ pull-up is used for the recessive high level (in fast mode). Note that MOSI and MISO use the same physical pin of the MLX90316.

15.5. /SS (Slave Select)

The /SS pin enables a frame transfer (if CPHA = 1). It allows a re-synchronization between Slave and Master in case of communication error.

15.6. Master Start-Up

/SS, SCLK, MISO can be undefined during the Master start-up as long as the Slave is re-synchronized before the first frame transfer.

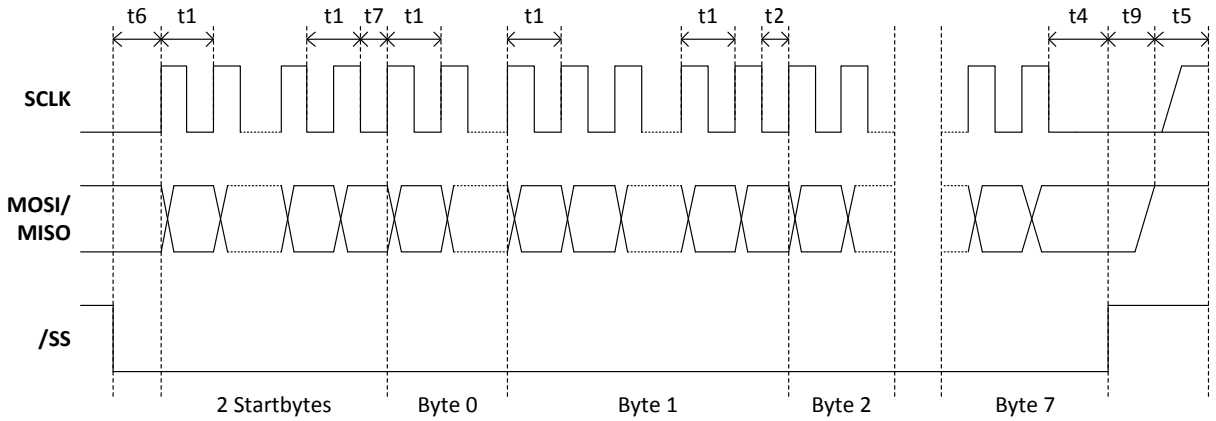
15.7. Slave Start-Up

The slave start-up (after power-up or an internal failure) takes 16 ms. Within this time /SS and SCLK is ignored by the Slave. The first frame can therefore be sent after 16 ms. MISO is Hi-Z (i.e. Hi-Impedance) until the Slave is selected by its /SS input. MLX90316 will cope with any signal from the Master while starting up.

15.8. Timing

To synchronize communication, the Master deactivates /SS high for at least t5 (1.5 ms). In this case, the Slave will be ready to receive a new frame. The Master can re-synchronize at any time, even in the middle of a byte transfer.

Note: Any time shorter than t5 leads to an undefined frame state, because the Slave may or may not have seen /SS inactive.



Timings	Min [27]	Max	Remarks
t1	2.3 µs / 6.9 µs	-	No capacitive load on MISO. t1 is the minimum clock period for any bits within a byte.
t2	12.5 µs / 37.5 µs	-	t2 the minimum time between any other byte
t4	2.3 µs / 6.9 µs	-	Time between last clock and /SS=high=chip de-selection
t5	300 µs / 1500 µs	-	Minimum /SS = Hi time where it's guaranteed that a frame re-synchronizations will be started.
t5	0 µs	-	Maximum /SS = Hi time where it's guaranteed that NO frame re-synchronizations will be started.
t6	2.3 µs / 6.9 µs	-	The time t6 defines the minimum time between /SS = Lo and the first clock edge

[27] *Timings shown for oscillator base frequency of 20MHz (Fast Mode) / 7 MHz (Slow Mode)*

Timings	Min [27]	Max	Remarks
t7	15 µs / 45 µs	-	t7 is the minimum time between the StartByte and the Byte0
t9	-	< 1 µs	Maximum time between /SS = Hi and MISO Bus High-Impedance
$T_{StartUp}$	-	< 10 ms / 16 ms	Minimum time between reset-inactive and any master signal change

15.9. Slave Reset

On internal soft failures the Slave resets after 1 second or after an (error) frame is sent. On internal hard failures the Slave resets itself. In that case, the Serial Protocol will not come up. The serial protocol link is enabled only after the completion of the first synchronization (the Master deactivates /SS for at least t5).

15.10. Frame Layer

15.10.1. Command Device Mechanism

Before each transmission of a data frame, the Master should send a byte AAh to enable a frame transfer. The latch point for the angle measurement is at the last clock before the first data frame byte.

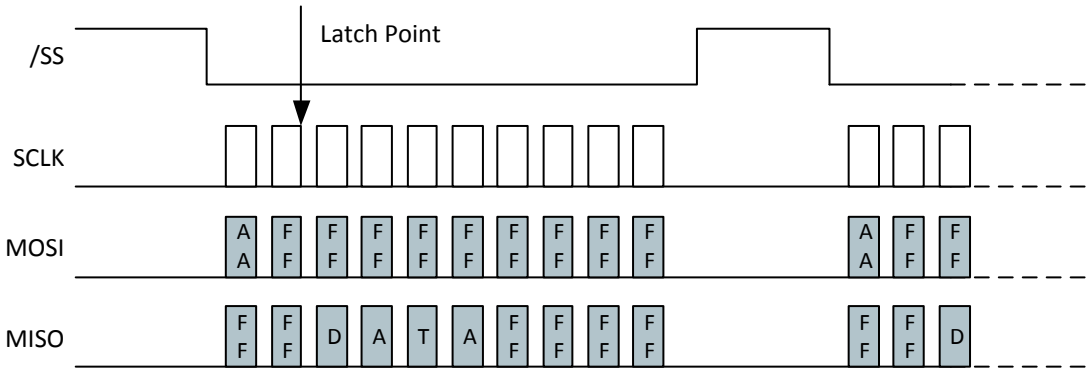


Figure 8 – Timing Diagram

15.10.2. Data Frame Structure

A data frame consists of 10 bytes:

- 2 start bytes (AAh followed by FFh)
- 2 data bytes (DATA16 – most significant byte first)
- 2 inverted data bytes (/DATA16 - most significant byte first)
- 4 all-Hi bytes

The Master should send AAh (55h in case of inverting transistor) followed by 9 bytes FFh. The Slave will answer with two bytes FFh followed by 4 data bytes and 4 bytes FFh.

15.10.3. Timing

There are no timing limits for frames: a frame transmission could be initiated at any time. There is no inter-frame time defined.

15.10.4. Data Structure

The DATA16 could be a valid angle or an error condition. The two meanings are distinguished by the LSB.

DATA16: Angle A[13:0] with (Angle Span)/2^{14}

Most Significant Byte								Least Significant Byte							
MSB							LSB	MSB							LSB
A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	0	1

DATA16: Error

Most Significant Byte								Least Significant Byte							
MSB							LSB	MSB							LSB
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

BIT	NAME	Description
E0	0	
E1	1	
E2	F_ADCMONITOR	ADC Failure
E3	F_ADCSATURA	ADC Saturation (Electrical failure or field too strong)
E4	F_RGTOOLOW	Analog Gain Below Trimmed Threshold (Likely reason: field too weak)
E5	F_MAGTOOLOW	Magnetic Field Too Weak
E6	F_MAGTOOHIGH	Magnetic Field Too Strong
E7	F_RGTOOHIGH	Analog Gain Above Trimmed Threshold (Likely reason: field too strong)
E8	F_FGCLAMP	Never occurring in serial protocol
E9	F_ROCLAMP	Analog Chain Rough Offset Compensation: Clipping
E10	F_MT7V	Device Supply VDD Greater than 7V

BIT	NAME	Description
E11	-	
E12	-	
E13	-	
E14	F_DACMONITOR	Never occurring in serial protocol
E15	-	

15.10.5. Angle Calculation

All communication timing is independent (asynchronous) of the angle data processing. The angle is calculated continuously by the Slave:

- Slow Mode: every 1.5 ms at most.
- Fast Mode: every 350 µs at most.

The last angle calculated is hold to be read by the Master at any time. Only valid angles are transferred by the Slave, because any internal failure of the Slave will lead to a soft reset.

15.10.6. Error Handling

In case of any errors listed in section 15.10.4, the Serial protocol will be initialized and the error condition can be read by the master. The slave will perform a soft reset once the error frame is sent.

In case of any other errors (ROM CRC error, EEPROM CRC error, RAM check error, intelligent watchdog error…) the Slave's serial protocol is not initialized. The MOSI/MISO pin will stay Hi-impedant (no error frames are sent).

16. Recommended Application Diagrams

16.1. Analog Output Wiring in SOIC-8 Package

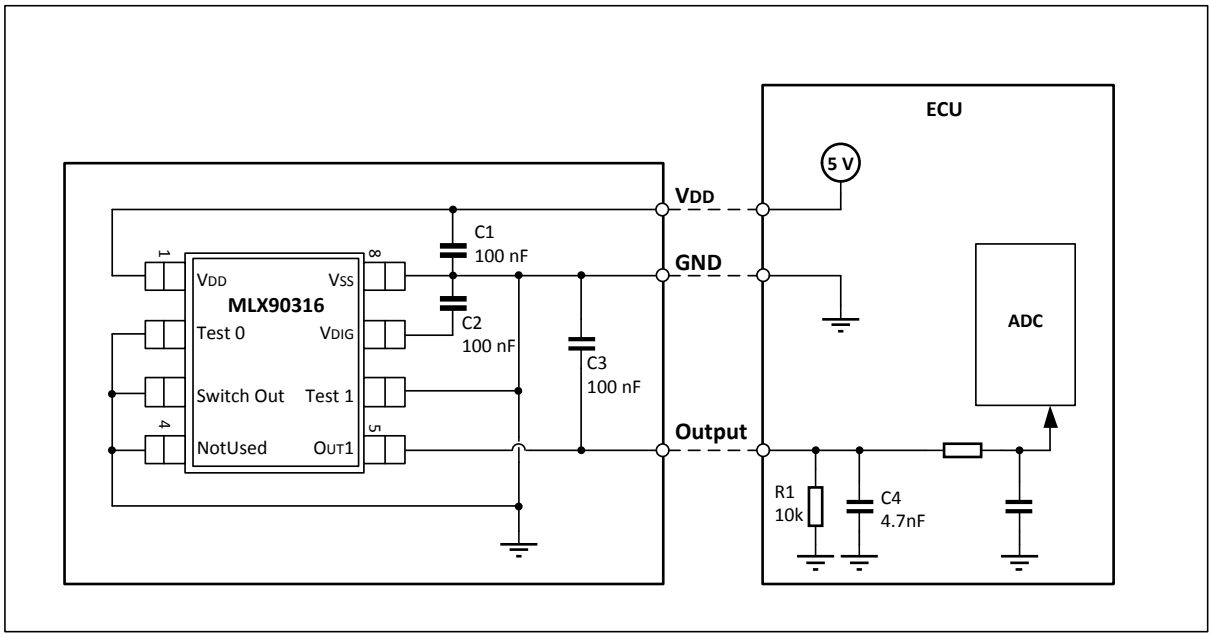


Figure 9 – Recommended wiring in SOIC-8 package [28]

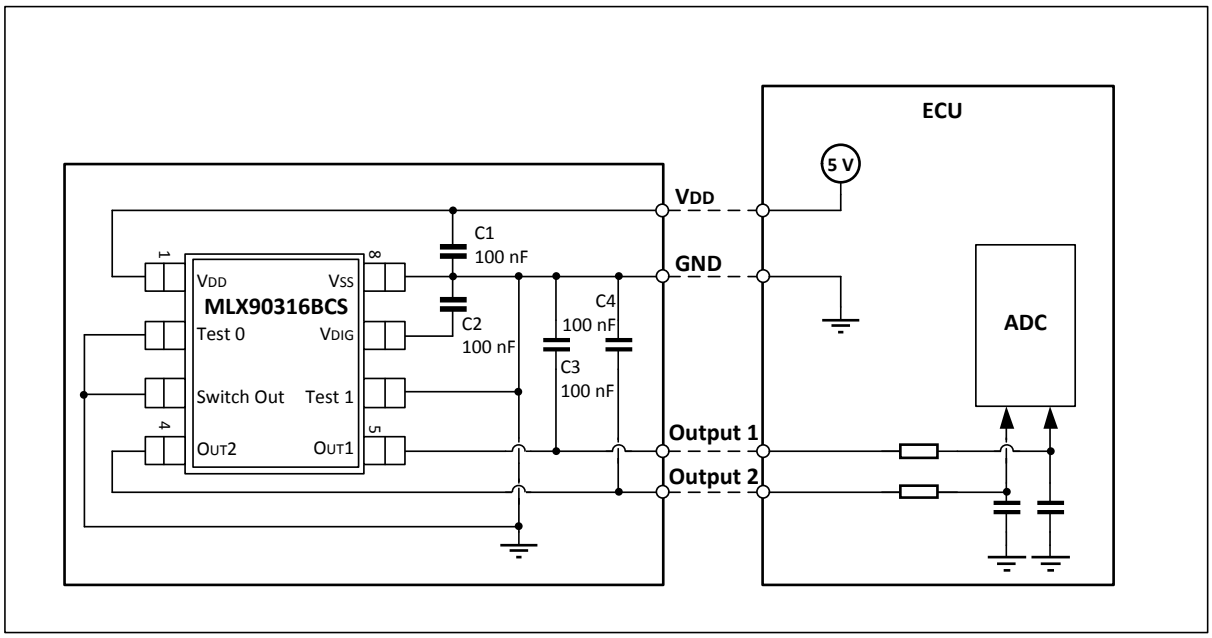


Figure 10 – Recommended wiring in SOIC-8 package – "BCS" Version

[28] *See section 13.1.4 if the Switch Output feature is used*

16.2. Analog Output Wiring in TSSOP-16 Package

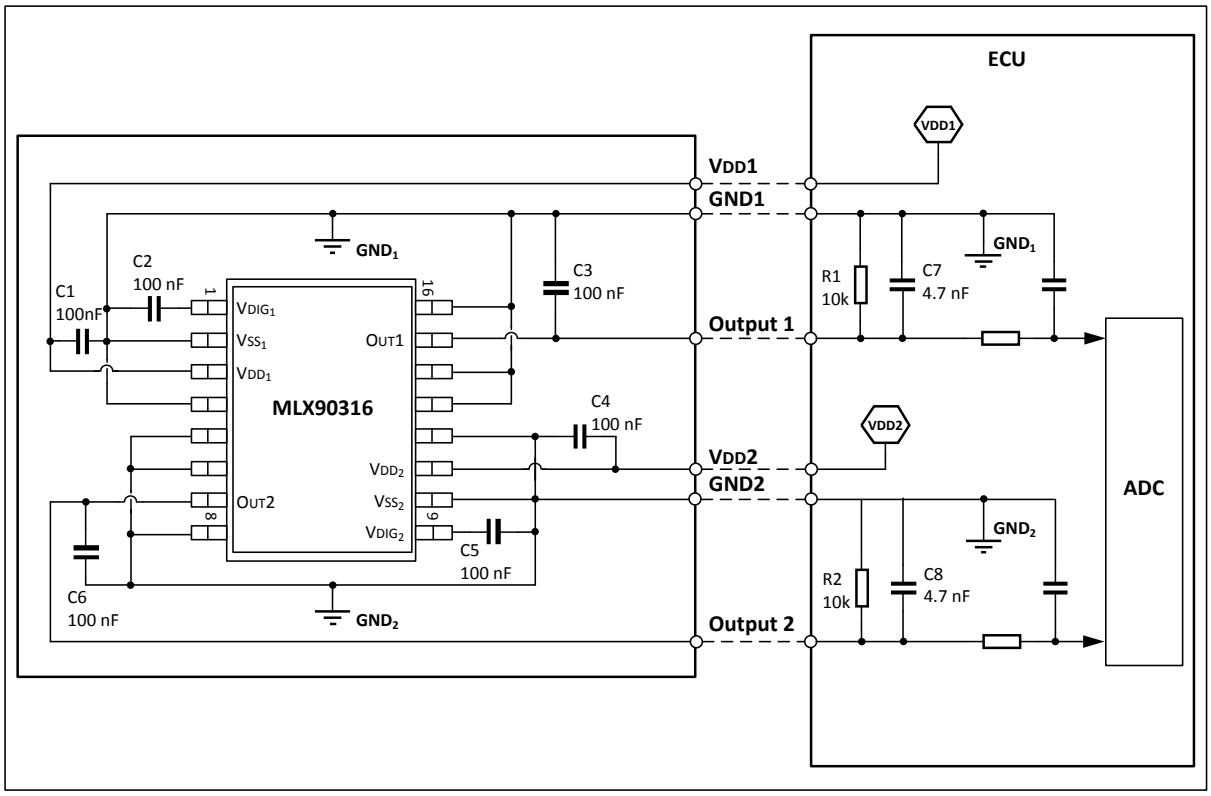


Figure 11 – Recommended wiring in TSSOP-16 package (dual die)

16.3. PWM Low Side Output Wiring

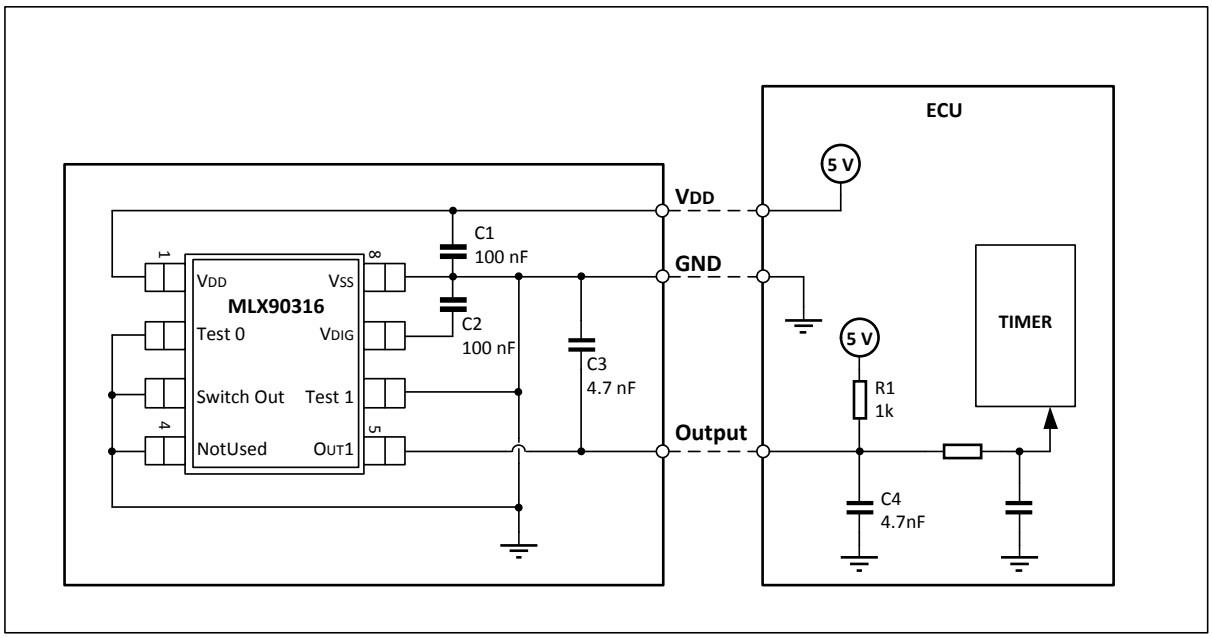


Figure 12 – Recommended wiring for a PWM Low Side Output configuration [28]

16.4. Serial Protocol

Generic schematics for single slave and dual slave applications are described.

16.4.1. SPI Version – Single Die

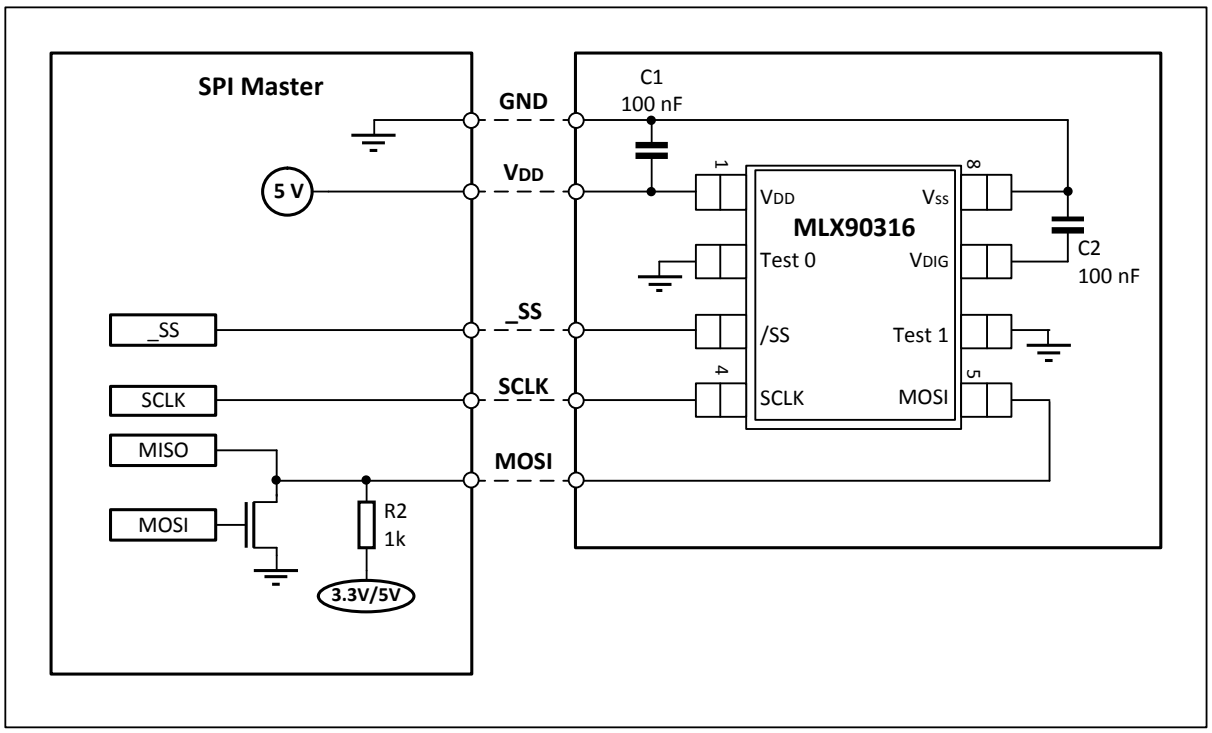


Figure 13 – SPI Version – Single Die – Application Diagram

16.4.2. SPI Version – Dual Die

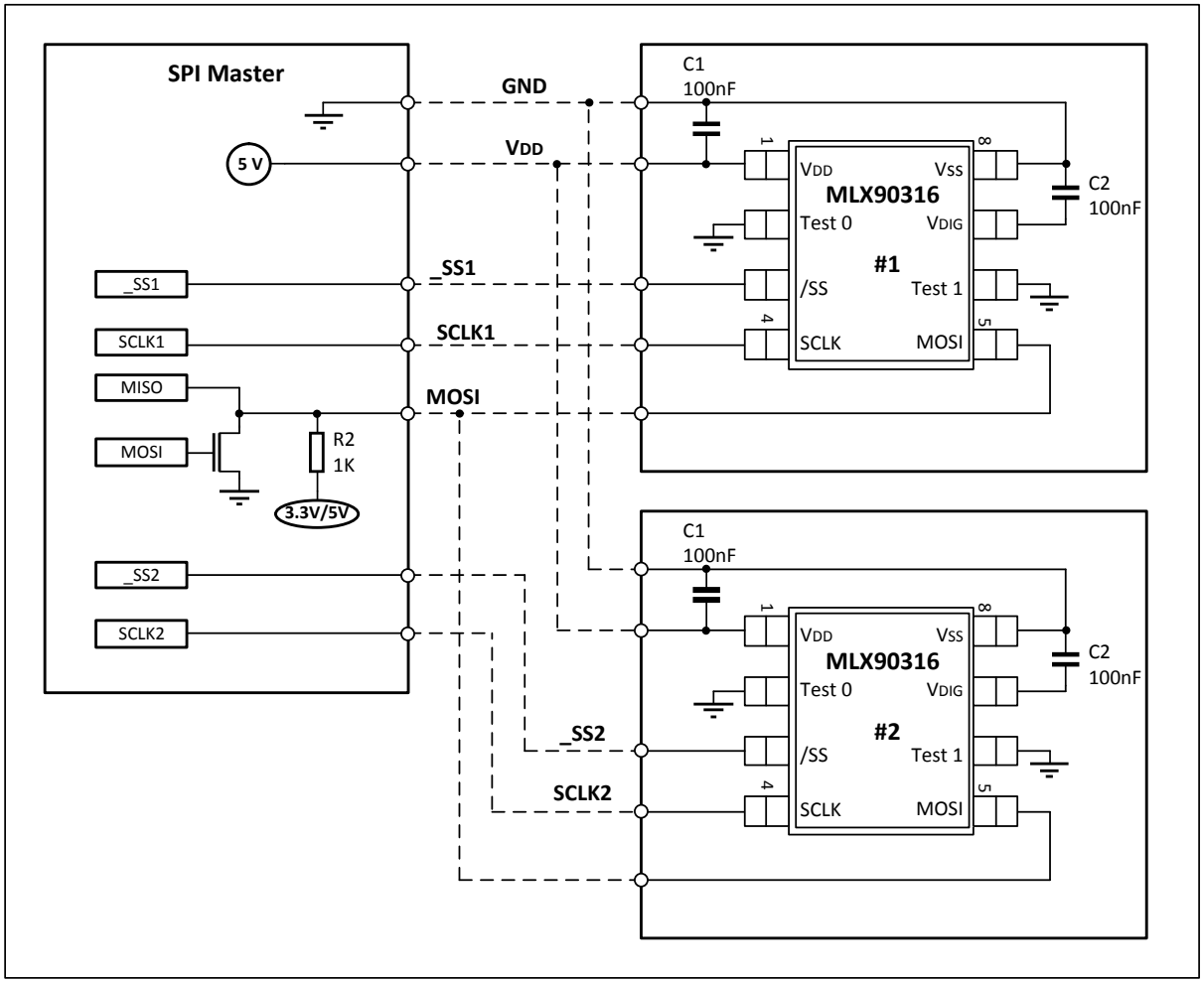


Figure 14 – SPI Version – Dual Die – Application Diagram

16.4.3. Non SPI Version (Standard Version)

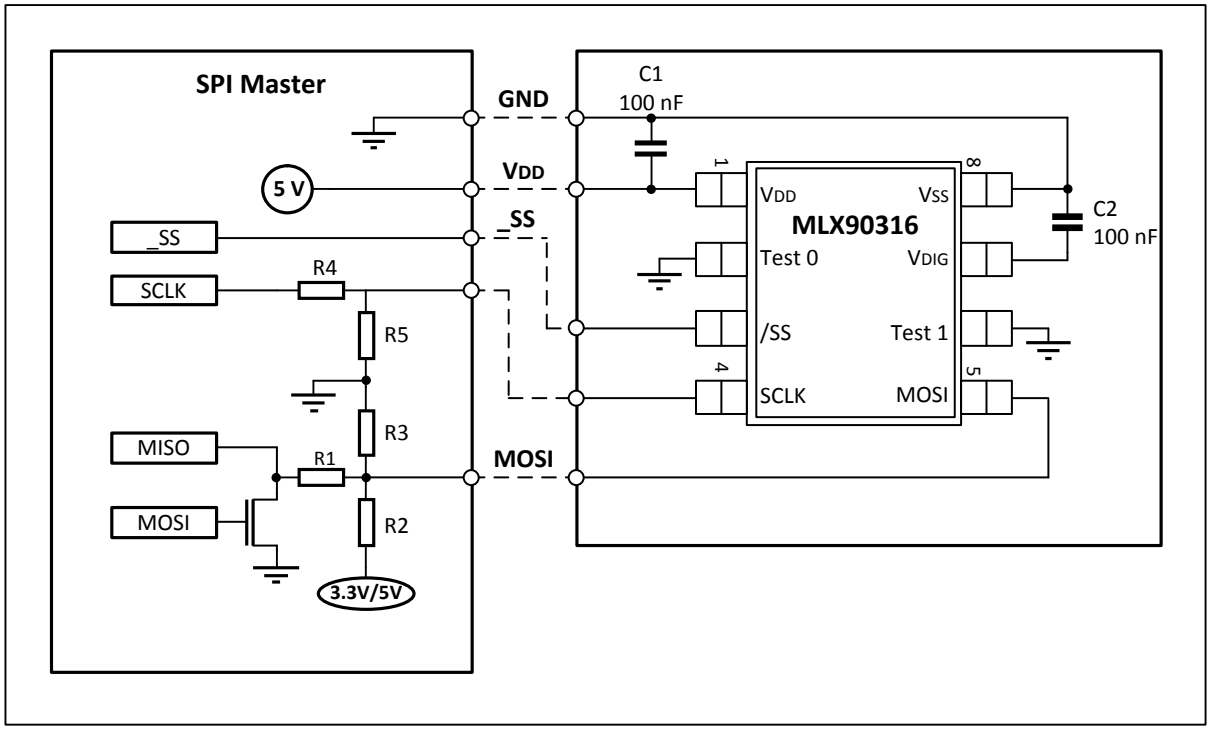


Figure 15 – Single Die - Serial Protocol Mode

Application Type	µCtrl Supply (V)	Pull-up Supply (V)	90316 Supply (V)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	MOS Type
5V µCtrl w/o O.D. w/o 3.3V	5V	5V	5V	100	1000	20,000	1000	20,000	BS170
5V µCtrl w/o O.D. w/ 3.3V	5V	3.3V	5V	150	1000	N/A	1000	20,000	BS170
3.3V µCtrl w/o O.D. [29]	3.3V	3.3V	5V	150	1000	N/A	N/A	N/A	BS170
5V µCtrl w/ O.D. w/o 3.3V [30]	5V	5V	5V	100	1000	20,000	1000	20,000	N/A
3.3V µCtrl w/ O.D.	3.3V	3.3V	5V	150	1000	N/A	N/A	N/A	N/A

Table 6 – Resistor Values for Common Specific Applications

[29] *µCtrl w/ O.D. : Micro-controller with open-drain capability (for instance NEC V850ES series)*
[30] *µCtrl w/o O.D. : Micro-controller without open-drain capability (like TI TMS320 series or ATMEL AVR)*

17. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/en/quality-environment/soldering).

For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends consulting the dedicated trim&forming recommendation application note: lead trimming and forming recommendations (http://www.melexis.com/en/documents/documentation/application-notes/lead-trimming-and-forming-recommendations).

Melexis is contributing to global environmental conservation by promoting lead free solutions. For more information on qualifications of RoHS compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment.

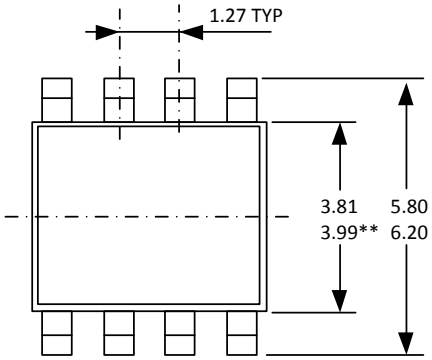
18. ESD Precautions

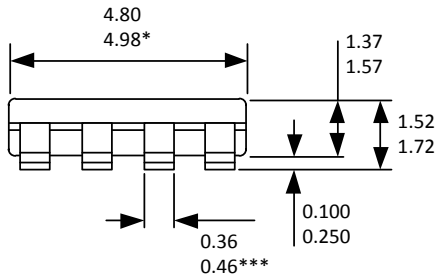
Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

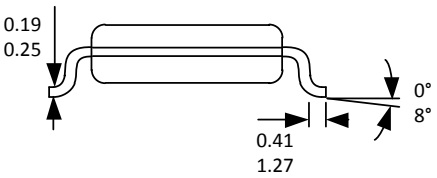
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

19. Package Information

19.1. SOIC-8 - Package Dimensions



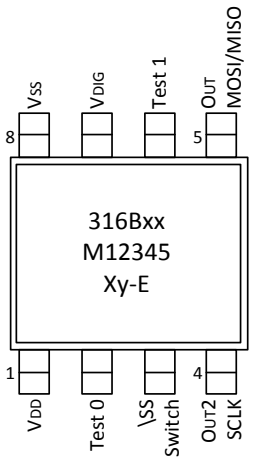




NOTES:

All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion.
Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition.
Dambar cannot be located on the lower radius of the foot.

19.2. SOIC-8 - Pinout and Marking



Marking :

Top

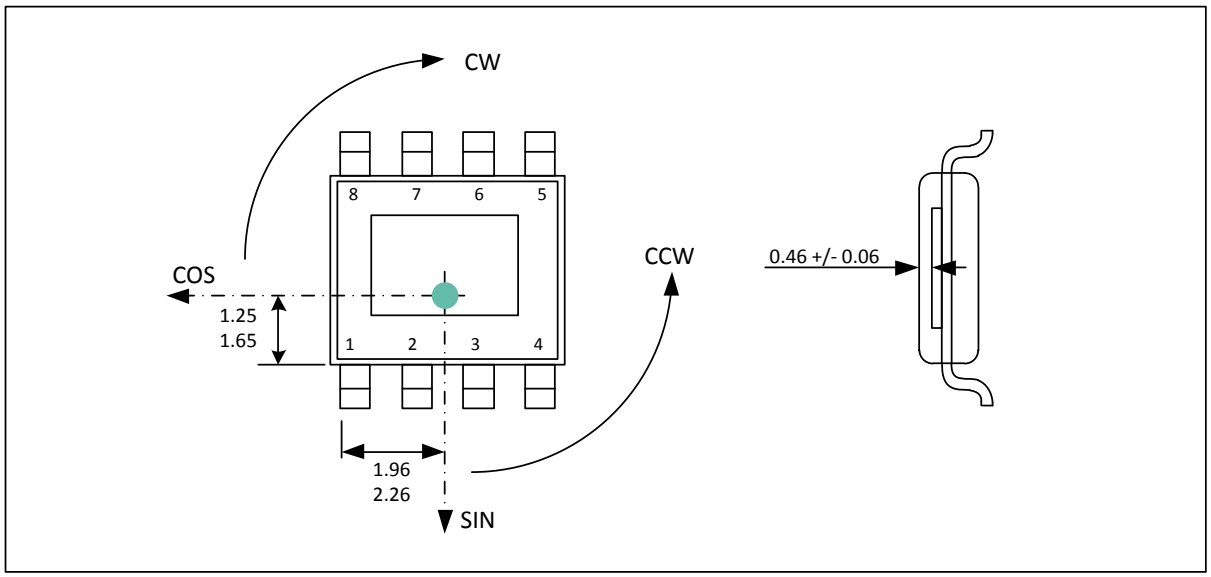
316 — Part Number MLX90316 (3 digits)
Die Version (3 digits)
BCG — Standard
BDG — SPI Version
BCS — BCS Version

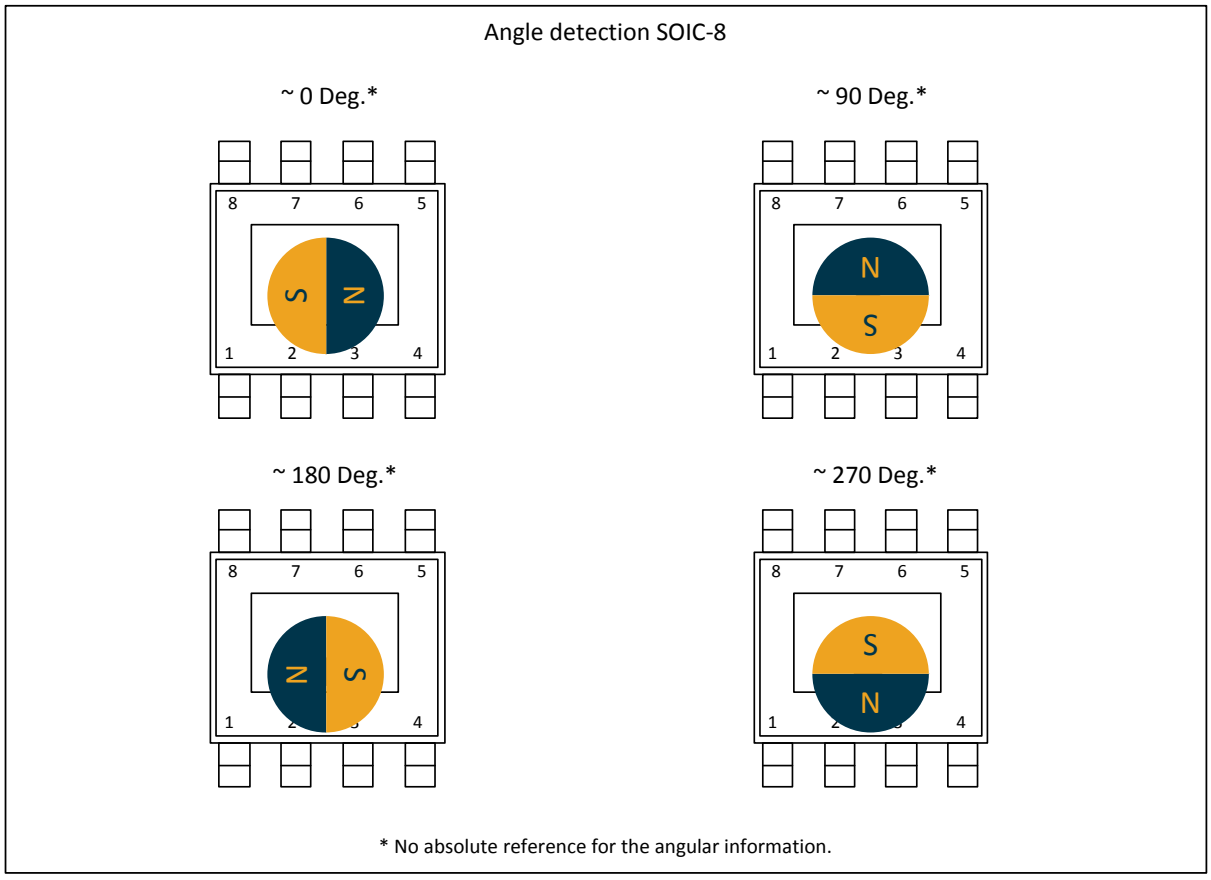
M12345 — Lot number: “M” + 5 digits
Xy-E — Split lot number + “-E” (Optional)

Bottom

YY WW
Week Date code (2 digits)
Year Date code (2 digits)

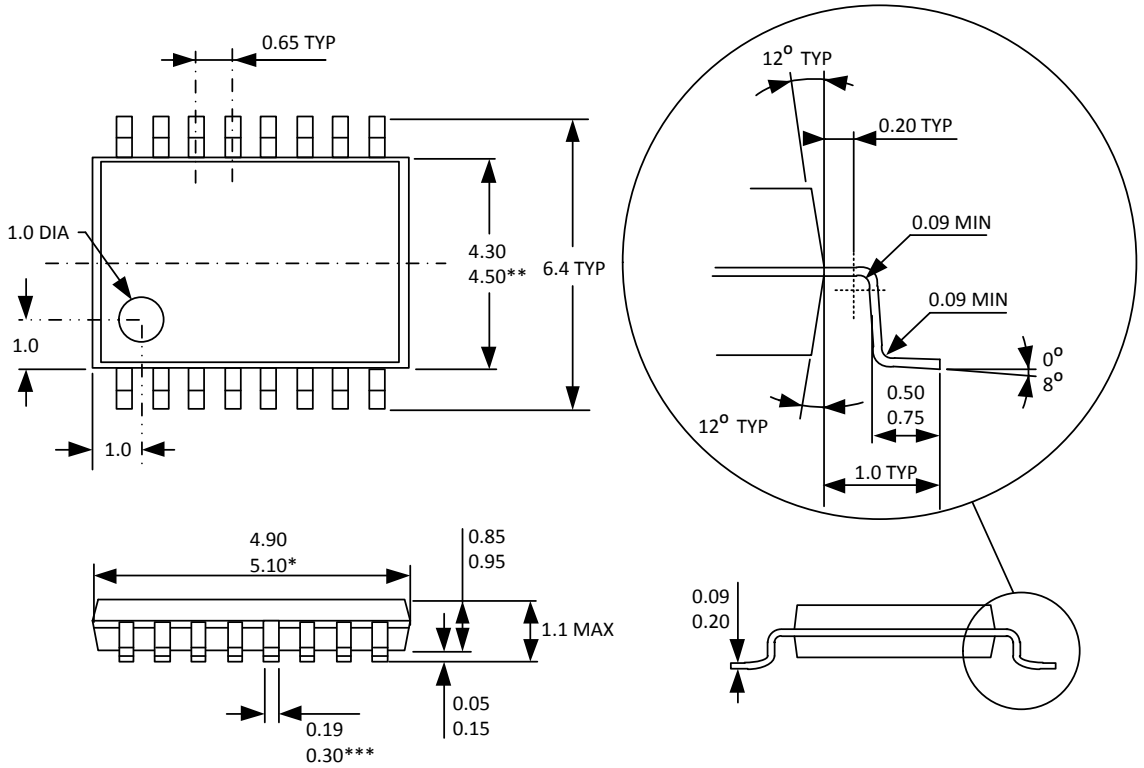
19.3. SOIC-8 - IMC Positionning





The MLX90316 is an absolute angular position sensor but the linearity error (Le – See section 9) does not include the error linked to the absolute reference 0 Deg. (which can be fixed in the application through the discontinuity point – See 13.2.2).

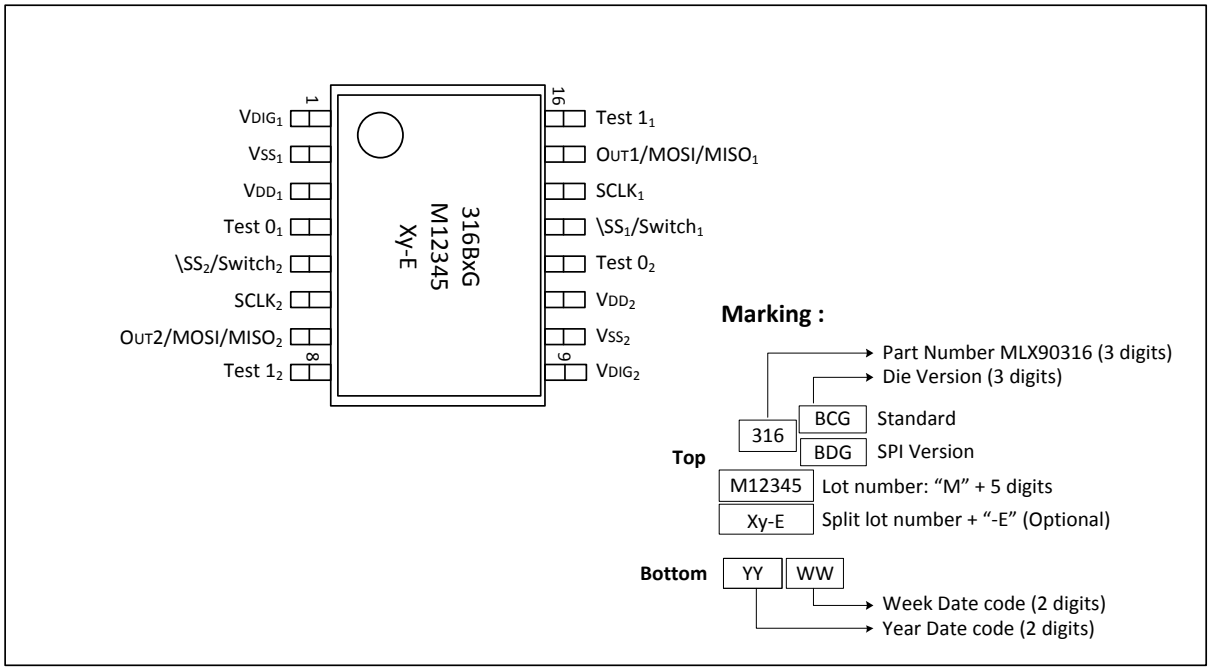
19.4. TSSOP-16 - Package Dimensions



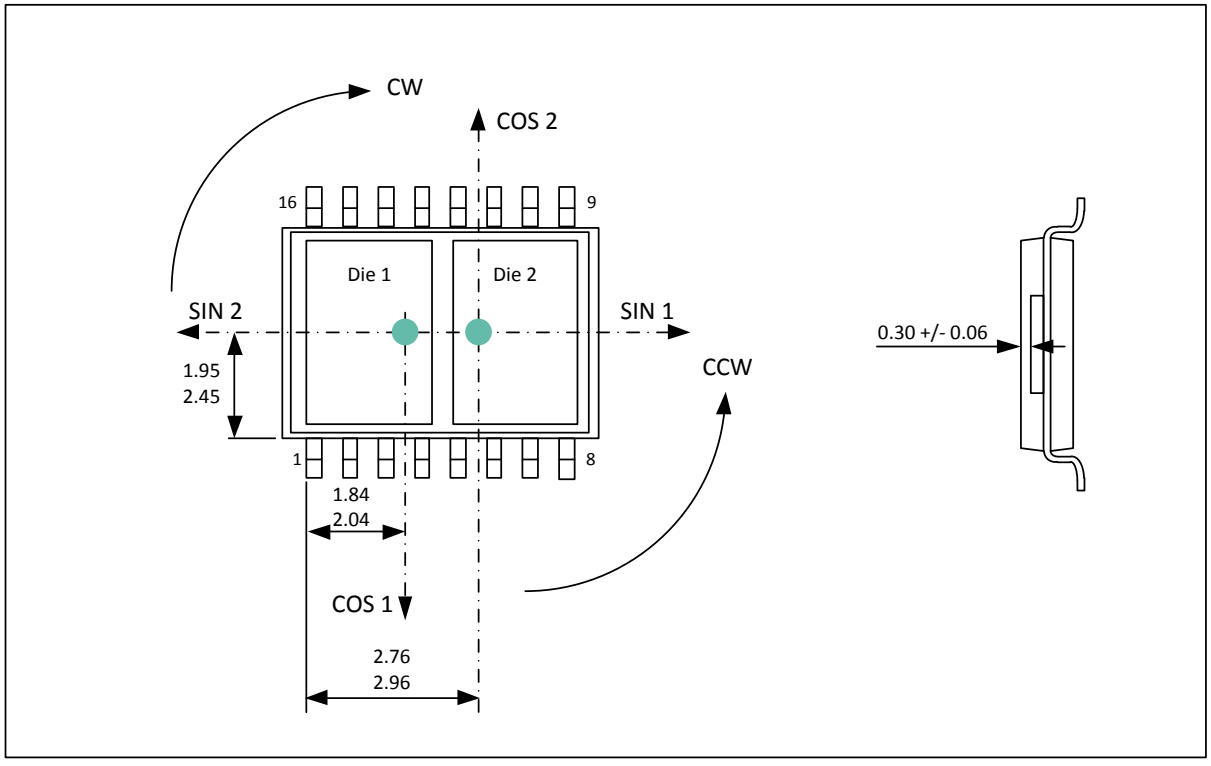
NOTES:

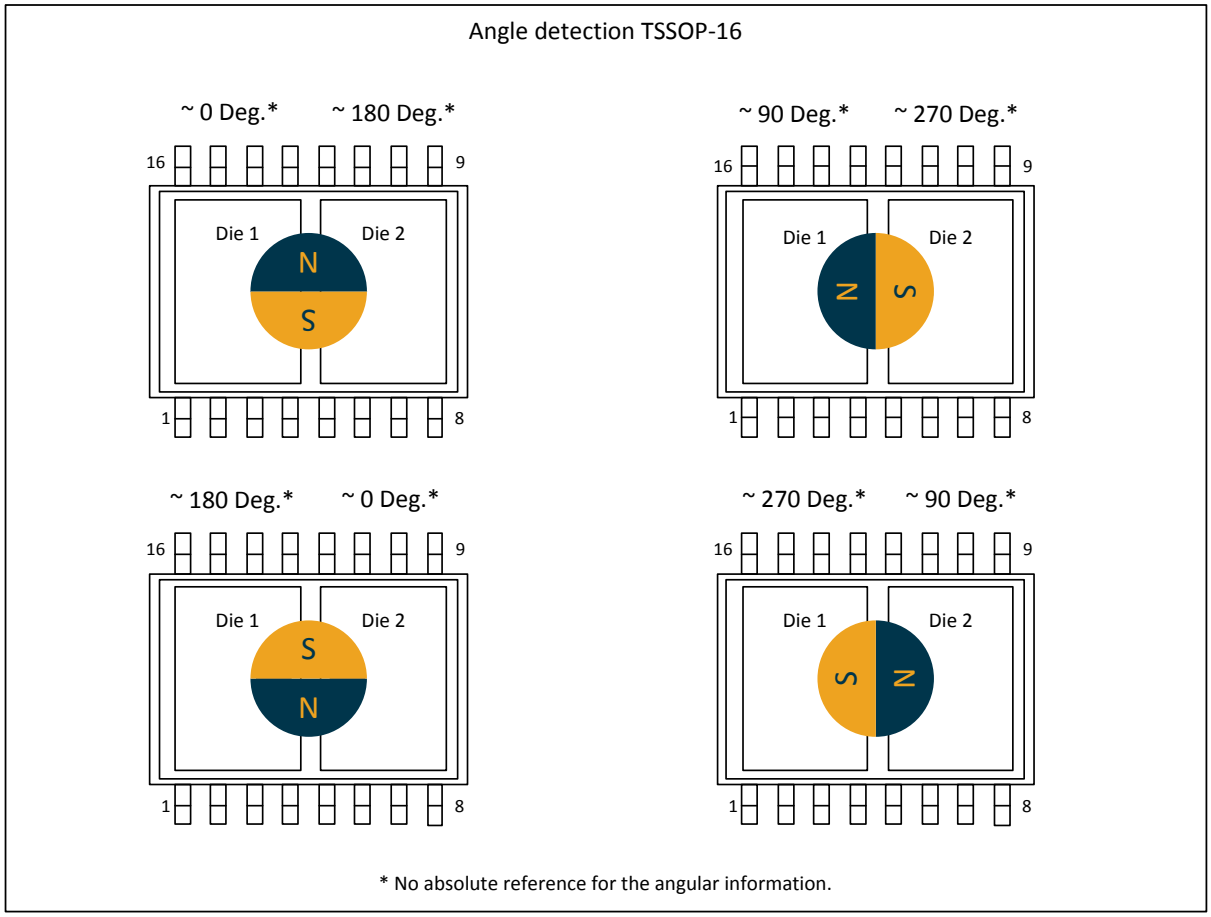
All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

19.5. TSSOP-16 - Pinout and Marking



19.6. TSSOP-16 - IMC Positionning





The MLX90316 is an absolute angular position sensor but the linearity error (Le – See section 9) does not include the error linked to the absolute reference 0 Deg. (which can be fixed in the application through the discontinuity point – See 13.2.2).

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