# NCV7708E

# Double Hex Driver

The NCV7708E is a fully protected Hex−Half Bridge−Driver designed specifically for automotive and industrial motion control applications. The six low and high side drivers are freely configurable and can be controlled separately. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states. The drivers are controlled via a standard SPI interface.

### Features

- Ultra Low Quiescent Current Sleep Mode
- Six Independent High−Side and Six independent Low−Side Drivers
- Integrated Freewheeling Protection (LS and HS)
- Internal Upper and Lower Clamp Diodes
- Configurable as H−Bridge Drivers
- 0.5 A Continuous (1 A peak) Current
- $R_{DS(on)}$ = 0.8 Ω (typ)
- 5 MHz SPI Control
- SPI Valid Frame Detection
- Compliance with 5 V and 3.3 V Systems
- Overvoltage Lockout
- Undervoltage Lockout
- Fault Reporting
- Current Limit
- Overtemperature Protection
- Internally Fused Lead in SOIC−28 Packaged for Better Thermal Performance
- These are Pb−Free Devices*

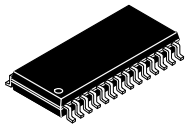
### Typical Applications

- Automotive
- Industrial
- DC Motor Management

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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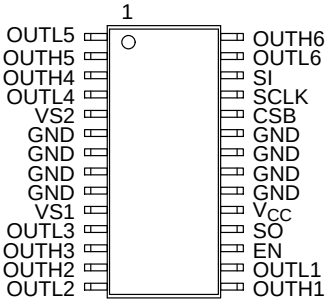
**SOIC−28**
**DW SUFFIX**
**CASE 751F**

### MARKING DIAGRAM




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

### PIN CONNECTIONS




### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCV7708EDWR2G | SOIC−28W (Pb−Free) | 1000/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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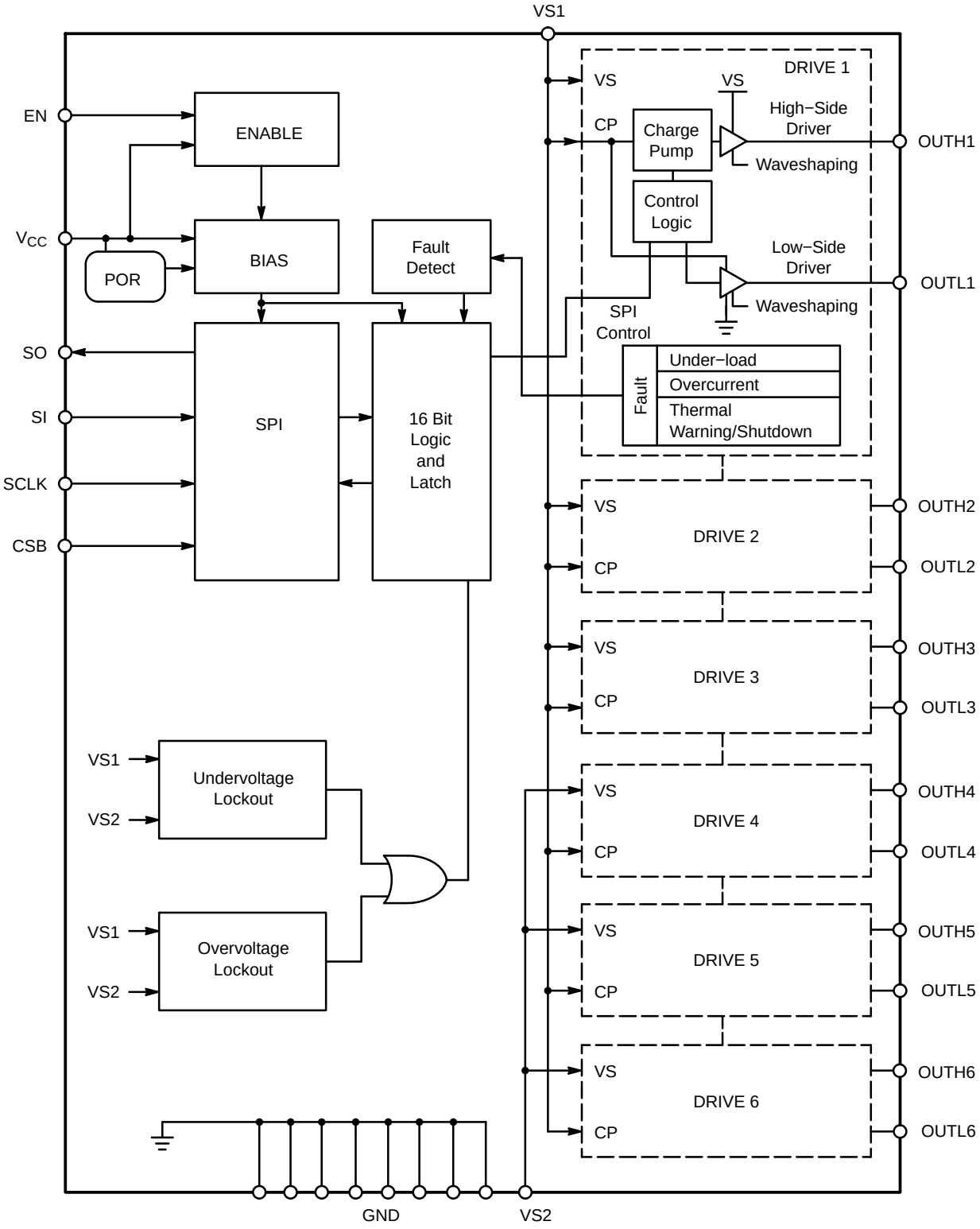



**Figure 1. Block Diagram**

**PIN DESCRIPTION**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | OUTL5 | Output Low Side 5. Open drain output driver with internal reverse diode. |
| 2 | OUTH5 | Output High Side 5. Open source output driver with internal reverse diode. Drain connected to VS2. |
| 3 | OUTH4 | Output High Side 4. Open source output driver with internal reverse diode. Drain connected to VS2. |
| 4 | OUTL4 | Output Low Side 4. Open drain output driver with internal reverse diode. |
| 5 | VS2 | Voltage Power Supply input for the High−Side Output Drivers 4, 5, and 6. |
| 6 | GND | Ground |
| 7 | GND | Ground |
| 8 | GND | Ground |
| 9 | GND | Ground |
| 10 | VS1 | Voltage Power Supply input for the High−Side Output Drivers 1, 2, and 3, All six low side pre−drivers, and all six charge pumps. |
| 11 | OUTL3 | Output Low Side 3. Open drain output driver with internal reverse diode. |
| 12 | OUTH3 | Output High Side 3. Open source output driver with internal reverse diode. Drain connected to VS1. |
| 13 | OUTH2 | Output High Side 2. Open source output driver with internal reverse diode. Drain connected to VS1. |
| 14 | OUTL2 | Output Low Side 2. Open drain output driver with internal reverse diode. |
| 15 | OUTH1 | Output High Side 1. Open source output driver with internal reverse diode. Drain connected to VS1. |
| 16 | OUTL1 | Output Low Side 1. Open drain output driver with internal reverse diode. |
| 17 | EN | Enable. Input high wakes the IC up from a sleep mode. |
| 18 | SO | Serial Output. 16 bit serial communications output. |
| 19 | $V_{CC}$ | Power supply input for Logic. |
| 20 | GND | Ground |
| 21 | GND | Ground |
| 22 | GND | Ground |
| 23 | GND | Ground |
| 24 | CSB | Chip Select Bar. Active low serial port operation. |
| 25 | SCLK | Serial Clock. Clock input for use with SPI communication. |
| 26 | SI | Serial Input. 16 bit serial communications input. |
| 27 | OUTL6 | Output Low Side 6. Open drain output driver with internal reverse diode. |
| 28 | OUTH6 | Output High Side 6. Open source output driver with internal reverse diode. Drain connected to VS2. |

## MAXIMUM RATINGS

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage (VS1, VS2)<br>(DC)<br>(AC), t < 500 ms, Ivsx > −2 A | <br>−0.3 to 40<br>−1.0 | V |
| Output Pin OUTHx<br>(DC)<br>(AC – inductive clamping) | <br>−0.3 to 40<br>−8.0 | V |
| Output Pin OUTLx<br>(DC)<br>(AC), t < 500 ms, IOUTLx > −2 A<br>(AC Inductive Clamping) | <br>−0.3 to 34<br>−1.0<br>48 | V |
| Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, $V_{CC}$) | −0.3 to 7.0 | V |
| Output Current (OUTL1, OUTL2, OUTL3, OUTL4, OUTL5, OUTL6, OUTH1, OUTH2, OUTH3, OUTH4, OUTH5, OUTH6)<br>(DC) Vds = 12 V<br>(DC) Vds = 20 V<br>(DC) Vds = 40 V<br>(AC) Vds = 12 V, (50 ms pulse, 1 s period)<br>(AC) Vds = 20 V, (50 ms pulse, 1 s period)<br>(AC) Vds = 40 V, (50 ms pulse, 1 s period) | <br><br>−1.5 to 1.5<br>−0.7 to 0.7<br>−0.25 to 0.25<br>−2.0 to 2.0<br>−0.9 to 0.9<br>−0.3 to 0.3 | A |
| Electrostatic Discharge, Human Body Model, VS1, VS2, OUTx | 4.0 | kV |
| Electrostatic Discharge, Human Body Model, all other pins | 2.0 | kV |
| Electrostatic Discharge, Machine Model | 200 | V |
| Electrostatic Discharge, Charged Device Model | 1.0 | kV |
| Operating Junction Temperature | −40 to 150 | °C |
| Storage Temperature Range | −55 to 150 | °C |
| Moisture Sensitivity Level | MSL 3 | − |
| Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 seconds at 217°C (Note 1) | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For additional information, please see or download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## RECOMMENDED OPERATING CONDITIONS

| Rating | Value | | Unit |
|---|---|---|---|
| | Min | Max | |
| Digital Supply Input Voltage ($V_{CC}$) | 3.0 | 5.5 | V |
| Battery Supply Input Voltage ($V_S$) | 5.1 | 28 | V |
| DC Output Current ($D_x$, $S_x$) | − | 0.5 | A |
| Junction Temperature ($T_J$) | −40 | 125 | °C |

## THERMAL CONDITIONS

| Thermal Parameters | Test Conditions, Typical Value | | Unit |
|---|---|---|---|
| | Board Details (Note 2) | Board Details (Note 3) | |
| Junction−to−Lead (psi−JL8, $\Psi_{JL8}$) or Pins 6−9, 20−23 | 10 | 11 | °C/W |
| Junction−to−Ambient ($R_{\theta JA}$, $\theta_{JA}$) | 73 | 56 | °C/W |

2. 1−oz copper, 240 $mm^2$ copper area, 0.062″ thick FR4. This is the minimum pad board size.
3. 1−oz copper, 986 $mm^2$ copper area, 0.062″ thick FR4.

## ELECTRICAL CHARACTERISTICS

(−40°C < $T_J$ < 150°C, 5.5 V < VSx < 40 V, 3 V < $V_{CC}$ < 5.25 V, EN = $V_{CC}$, unless otherwise specified)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| Supply Current (VS1 + VS2)<br>Sleep Mode (Note 4) | VS1 = VS2 = 13.2 V, $V_{CC}$ = CSB = 5 V,<br>EN = SI = SCLK = 0 V (−40°C to 85°C) | − | 1.0 | 5.0 | μA |
| Supply Current (VS1)<br>Active Mode | EN = $V_{CC}$, 5.5 V < VSx < 35 V<br>No Load | − | 2.0 | 4.0 | mA |
| Supply Current ($V_{CC}$) − Sleep Mode (Note 4) | CSB = $V_{CC}$, EN = SI = SCLK = 0 V<br>(−40°C to 85°C) | − | 1.0 | 2.5 | μA |
| Supply Current ($V_{CC}$) − Active Mode | EN = CSB = $V_{CC}$, SI = SCLK = 0 V | − | 1.5 | 3.0 | mA |
| Supply Current (VS2)<br>Active Mode | EN = $V_{CC}$, 5.5 V < VSx < 35 V<br>No Load | − | 0.5 | 1.0 | mA |
| $V_{CC}$ Power−On−Reset Threshold | | 2.60 | 2.80 | 3.00 | V |
| VSx Undervoltage Detection Threshold | VSx decreasing | 4.2 | 4.6 | 5.1 | V |
| VSx Undervoltage Detection Hysteresis | | 100 | − | 400 | mV |
| VSx Overvoltage Detection Threshold | VSx increasing | 35.0 | 37.5 | 40.0 | V |
| VSx Overvoltage Detection Hysteresis | | 1.5 | 3.5 | 5.5 | V |
| Thermal Warning (Note 5) | | 120 | 145 | 170 | °C |
| Thermal Warning Hysteresis (Note 5) | | − | 30 | − | °C |
| Thermal Shutdown (Note 5) | | 155 | 175 | 195 | °C |
| Ratio of Thermal Shutdown to Thermal Warning (Note 5) | | 1.05 | 1.20 | − | − |
| **OUTPUTS** | | | | | |
| Output High $R_{DSon}$ (source) | $I_{out}$ = −500 mA | | | | Ω |
| | 8 V < Vs < 40 V | − | − | 1.8 | |
| | 8 V < Vs < 40 V, T = 25°C | − | 0.8 | 1.0 | |
| | 5.5 V < Vs ≤ 8 V | − | − | 2.2 | |
| | 5.5 V < Vs ≤ 8 V, T = 25°C | − | 1.3 | − | |
| Output Low $R_{DSon}$ (sink) | $I_{out}$ = 500 mA | | | | Ω |
| | 8 V < Vs < 40 V | − | − | 1.8 | |
| | 8 V < Vs < 40 V, T = 25°C | − | 0.8 | 1.0 | |
| | 5.5 V < Vs ≤ 8 V | − | − | 2.2 | |
| | 5.5 V < Vs ≤ 8 V, T = 25°C | − | 1.3 | − | |
| Source Leakage Current | OUTH(1−6) = 0 V, VSx = 40 V, $V_{CC}$ = 5 V | −5.0 | − | − | μA |
| | OUTH(1−6) = 0 V, Vsx = 13.2 V, $V_{CC}$ = 5V | −1.0 | − | − | |
| Sink Leakage Current | OUTL(1−6) = 34 V, $V_{CC}$ = 5 V, T = 125°C | − | − | 5.0 | μA |
| | OUTL(1−6) = 34 V, $V_{CC}$ = 5 V, T = 25°C | − | − | 1.0 | |
| Overcurrent Shutdown Threshold (OUTHx) | $V_{CC}$ = 5 V, Vsx = 13.2 V | −1.9 | −1.45 | −1.0 | A |
| Current Limit (OUTHx) | $V_{CC}$ = 5 V, Vsx = 13.2 V | −5.0 | −3.0 | −2.0 | A |
| Overcurrent Shutdown Threshold (OUTLx) | $V_{CC}$ = 5 V, Vsx = 13.2 V | 1.0 | 1.45 | 1.9 | A |
| Overcurrent Shutdown Delay Time − Source | $V_{CC}$ = 5 V, Vsx = 13.2 V | 10 | 25 | 50 | μs |
| − Sink | | 10 | 25 | 50 | |

4. For temperatures above 85°C, refer to graphs for VSx and $V_{CC}$ Sleep Current vs. Temperature on page 13.
5. Thermal characteristics are not subject to production test.
6. Refer to “Typical High−Side Negative Clamp Voltage” graph on page 13.
7. Not production tested.

## ELECTRICAL CHARACTERISTICS

(−40°C < $T_J$ < 150°C, 5.5 V < VSx < 40 V, 3 V < $V_{CC}$ < 5.25 V, EN = $V_{CC}$, unless otherwise specified)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OUTPUTS** | | | | | |
| Current Limit (OUTLx) | $V_{CC}$ = 5 V, Vsx = 13.2 V | 2.0 | 3.0 | 5.0 | A |
| Under Load Detection Threshold (OUTLx) | $V_{CC}$ = 5 V, Vsx = 13.2 V | 3.0 | 8.0 | 15 | mA |
| Under Load Detection Threshold (OUTHx) | $V_{CC}$ = 5 V, Vsx = 13.2 V | −15 | −6.0 | −2.0 | mA |
| Under Load Detection Delay Time | $V_{CC}$ = 5 V, Vsx = 13.2 V | 200 | 350 | 600 | μs |
| Power Transistor Body Diode Forward Voltage | $I_F$ = 500 mA | − | 0.9 | 1.3 | V |
| High−Side Clamping Voltage (Note 6) | I(OUTHx) = −50 mA | − | − | −0.7 | V |
| Low−Side Clamping Voltage | I(OUTLx) = 50 mA | 34 | − | 48 | V |
| Low−Side Clamping Energy | I(OUTLx) = 0.6 A, $T_A$= 25°C, DC = 0.5% | − | − | 15 | mJ |
| **Logic Inputs (EN, SI, SCLK, CSB)** | | | | | |
| Input Threshold − High<br>− Low | | −<br>30 | −<br>− | 70<br>− | %$V_{CC}$ |
| Input Hysteresis | | 100 | 300 | 600 | mV |
| Input Pulldown Current (EN, SI, SCLK)<br>Sleep Mode (SI, SCLK) | EN = SI = SCLK = $V_{CC}$<br>EN = 0, SI = SCLK = $V_{CC}$ | 5.0<br>10 | 10<br>50 | 50<br>100 | μA |
| Input Pullup Current (CSB)<br>Sleep Mode | CSB = 0 V, EN = $V_{CC}$<br>EN = 0 V, $V_{CC}$ = 5 V | −50<br>−100 | −10<br>−50 | −5.0<br>−10 | μA |
| Input Capacitance (Note 7) | | − | 10 | 15 | pF |
| **Logic Output (SO)** | | | | | |
| Output High | $I_{out}$ = 1 mA | $V_{CC}$ – 1.0 | $V_{CC}$ – 0.7 | − | V |
| Output Low | $I_{out}$ = −1.6 mA | − | 0.2 | 0.4 | V |
| Tri−state Leakage | CSB = $V_{CC}$, 0 V < SO < $V_{CC}$ | −10 | − | 10 | μA |
| Tri−state Input Capacitance (Note 7) | CSB = $V_{CC}$, 0 V < $V_{CC}$ < 5.25 V | − | 10 | 15 | pF |
| **Timing Specifications** | | | | | |
| High Side Turn On Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 7.5 | 13 | μs |
| High Side Turn Off Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 3.0 | 6.0 | μs |
| Low Side Turn On Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 6.5 | 13 | μs |
| Low Side Turn Off Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 2.0 | 5.0 | μs |
| High Side Rise Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 4.0 | 8.0 | μs |
| High Side Fall Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 2.0 | 3.0 | μs |
| Low Side Rise Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 1.0 | 2.0 | μs |
| Low Side Fall Time | Vs = 13.2 V, $R_{load}$ = 25 Ω | − | 1.0 | 3.0 | μs |
| Non−Overlap Time | High Side Turn Off To Low Side Turn On | 1.5 | − | − | μs |
| Non−Overlap Time | Low Side Turn Off To High Side Turn On | 1.5 | − | − | μs |

4. For temperatures above 85°C, refer to graphs for VSx and $V_{CC}$ Sleep Current vs. Temperature on page 13.
5. Thermal characteristics are not subject to production test.
6. Refer to “Typical High−Side Negative Clamp Voltage” graph on page 13.
7. Not production tested.

## ELECTRICAL CHARACTERISTICS

(−40°C < $T_J$ < 150°C, 5.5 V < VSx < 40 V, EN = $V_{CC}$ = 5 V, unless otherwise specified)

| Characteristic | Conditions | Timing Chart # | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Serial Peripheral Interface** ($V_{CC}$ = 5 V) | | | | | | |
| SCLK Frequency | | | − | − | 5.0 | MHz |
| SCLK Clock Period | $V_{CC}$ = 5 V<br>$V_{CC}$ = 3.3 V | | 200<br>500 | −<br>− | −<br>− | ns |
| Maximum Input Capacitance (Note 8) | SI, SCLK | − | − | − | 12 | pF |
| SCLK High Time | | 1 | 85 | − | − | ns |
| SCLK Low Time | | 2 | 85 | − | − | ns |
| SCLK Setup Time | | 3<br>4 | 85<br>85 | −<br>− | −<br>− | ns |
| SI Setup Time | | 11 | 50 | − | − | ns |
| SI Hold Time | | 12 | 50 | − | − | ns |
| CSB Setup Time | | 5<br>6 | 100<br>100 | −<br>− | −<br>− | ns |
| CSB High Time (Note 9) | | 7 | 200 | − | − | ns |
| SO enable after CSB falling edge | | 8 | − | − | 50 | ns |
| SO disable after CSB rising edge | | 9 | − | − | 50 | ns |
| SO Rise Time | $C_{load}$ = 40 pF | − | − | 10 | 25 | ns |
| SO Fall Time | $C_{load}$ = 40 pF | − | − | 10 | 25 | ns |
| SO Valid Time | SCLK High to SO 50% | 10 | − | 20 | 50 | ns |

8. Not tested in production
9. This is the minimum time the user must wait between SPI commands.

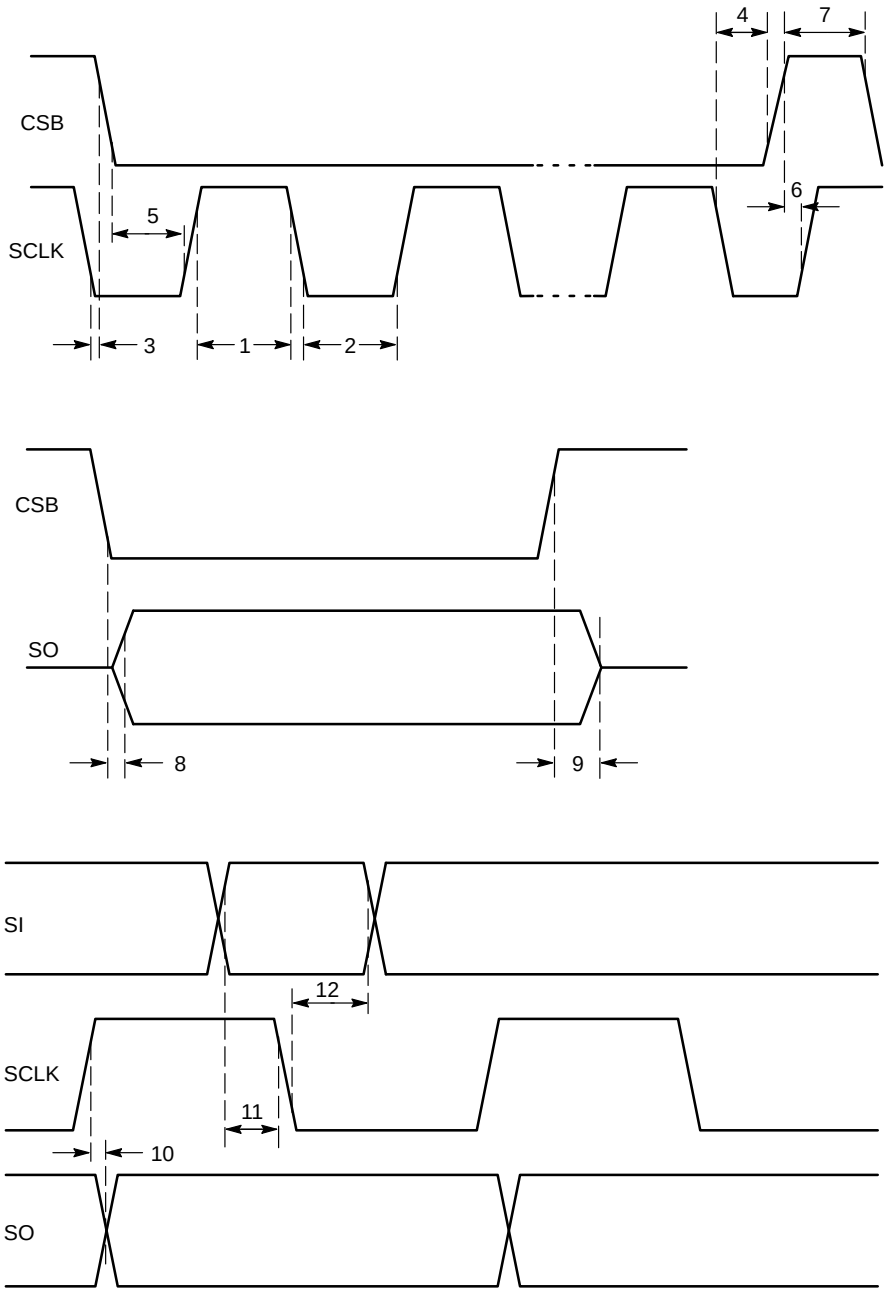



**Figure 2. SPI Timing Diagram**

**SPI Communication**

Standard 16−bit communication has been implemented for the communication of this IC to turn drivers on and off, and to report faults. (Reference the SPI Communication Frame Format Diagram). The LSB (Least Significant Bit) is clocked in first.

Communication is implemented as follows:

1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (serial input) pin. The SI input signal is latched on the falling edge of SCLK.
3. CSB goes high to transfer the clocked in information to the data registers. (Note: SO is tristate when CSB is high.)
4. The SI data will be accepted when a valid SPI frame is detected. A valid SPI frame consists of the above conditions and a complete set of multiples of 16 bit words.

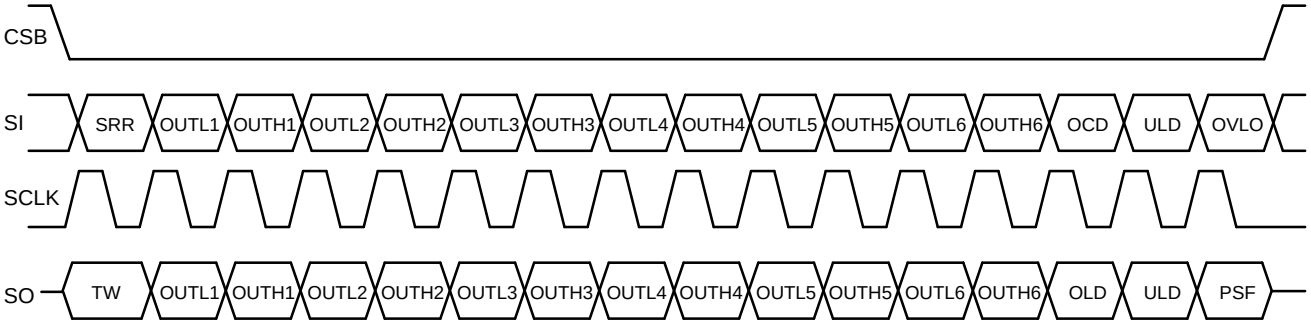



**Figure 3. SPI Communication Frame Format**

The table below defines the programming bits and diagnostic bits. Fault information is sequentially clocked out the SO pin of the NCV7708E as programming information is clocked into the SI pin of the device. Daisy chain communication between SPI compatible IC's is possible by connection of the serial output pin (SO) to the input of the sequential IC (SI).

| Input Data | | |
|---|---|---|
| **Bit Number** | **Bit Description** | **Bit Status** |
| 15 | Over Voltage Lock Out Control (OVLO) | 0 = Disable |
| | | 1 = Enable |
| 14 | Under Load Detection Shut Down Control (ULD) | 0 = Disable |
| | | 1 = Enable |
| 13 | Over Current Detection Shut Down Control (OCD) | 0 = Disable |
| | | 1 = Enable |
| 12 | OUTH6 | 0 = Off |
| | | 1 = On |
| 11 | OUTL6 | 0 = Off |
| | | 1 = On |
| 10 | OUTH5 | 0 = Off |
| | | 1 = On |
| 9 | OUTL5 | 0 = Off |
| | | 1 = On |
| 8 | OUTH4 | 0 = Off |
| | | 1 = On |
| 7 | OUTL4 | 0 = Off |
| | | 1 = On |
| 6 | OUTH3 | 0 = Off |
| | | 1 = On |
| 5 | OUTL3 | 0 = Off |
| | | 1 = On |
| 4 | OUTH2 | 0 = Off |
| | | 1 = On |
| 3 | OUTL2 | 0 = Off |
| | | 1 = On |
| 2 | OUTH1 | 0 = Off |
| | | 1 = On |
| 1 | OUTL1 | 0 = Off |
| | | 1 = On |
| 0 | Status Register Reset (SRR) | 0 = No Reset |
| | | 1 = Reset |

| Output Data | | |
|---|---|---|
| **Bit Number** | **Bit Description** | **Bit Status** |
| 15 | Power Supply Fail Signal (OVLO or UVLO = PSF) | 0 = No Fault |
| | | 1 = Fault |
| 14 | Under Load Detect Signal (ULD) | 0 = No Fault |
| | | 1 = Fault |
| 13 | Over Load Detect Signal (OLD) | 0 = No Fault |
| | | 1 = Fault |
| 12 | OUTH6* | 0 = Off |
| | | 1 = On |
| 11 | OUTL6* | 0 = Off |
| | | 1 = On |
| 10 | OUTH5* | 0 = Off |
| | | 1 = On |
| 9 | OUTL5* | 0 = Off |
| | | 1 = On |
| 8 | OUTH4* | 0 = Off |
| | | 1 = On |
| 7 | OUTL4* | 0 = Off |
| | | 1 = On |
| 6 | OUTH3* | 0 = Off |
| | | 1 = On |
| 5 | OUTL3* | 0 = Off |
| | | 1 = On |
| 4 | OUTH2* | 0 = Off |
| | | 1 = On |
| 3 | OUTL2* | 0 = Off |
| | | 1 = On |
| 2 | OUTH1* | 0 = Off |
| | | 1 = On |
| 1 | OUTL1* | 0 = Off |
| | | 1 = On |
| 0 | Thermal Warning (TW) | 0 = Not in TW |
| | | 1 = In TW |

*Output Bits [1:12] represent the state of the designated outputs.

## DETAILED OPERATING DESCRIPTION

### General

The NCV7708E Double Hex Driver provides drive capability for 3 independent H−Bridge configurations, or 6 High Side configurations with 6 Low Side configurations, or any combination of arrangements. Each output drive is characterized for a 500 mA load and has a typical 1.0 A surge capability (at 12 V). Strict adherence to integrated circuit die temperature is necessary. Maximum die temperature is 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting is handled via the SPI (Serial Peripheral Interface) port.

An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. No data is stored when the device is in sleep mode. A pull down current source is provided on the EN input to ensure the device is off if the input signal is lost. Pull down current sources are also provided on the SI and SCLK inputs. A pull up current source is provided for the CSB input for the same reason. A loss of signal pulls the CSB input high to stop any spurious signals into the SPI port.

### Power Up/Down Control

An under voltage lockout circuit prevents the output drivers from turning on unintentionally. This control is provided by monitoring the voltages on the VS1, VS2, and $V_{CC}$ pins. Each analog power pin (VS1 or VS2) powers their respective output drivers (VS1 powers OUTH1, OUTH2, OUTH3, all 6 charge pumps and all 6 low−side pre−drivers, VS2 powers OUTH4, OUTH5, and OUTH6). All drivers are initialized in the off (high impedance) condition, and will remain off regardless of the status of $V_{CC}$. This allows power up sequencing of $V_{CC}$, VS1, and VS2 up to the user. The voltage on VS1 and VS2 should be operated at the same potential.

A built−in hysteresis on the under voltage threshold is included to prevent an unknown region on the power pins. After a device has powered up and the output drivers are allowed to turn on, the output drivers will not turn off until the voltage on the supply pins is reduced from the initial under voltage threshold, or if shut down by either a SPI command or a fault condition.

Internal power−up circuitry on the logic supply pin supports a smooth turn on transition. $V_{CC}$ power up resets the internal logic such that all output drivers will be off as power is applied. Exceeding the under voltage lockout threshold on $V_{CC}$ allows information to be input through the SPI port for turn on control. Logic information remains intact over the entire VS1 and VS2 voltage range.

### Current Limitation

Input bit 13 (OCD) controls the action of driver shutoff during current limit. With a 0 for bit 13, there is no driver shutoff, and the drivers current limit at 3 A. With a 1 for input bit 13, the output drivers shut off when the shutdown threshold current is passed. Devices can be turned back on via the SPI port. Note: high currents could cause a high rise in die temperature. Devices will not turn on if the die temperature exceeds the thermal shutdown temperature.

**Over Current Detection Shut Down**

| OCD Input Bit 13 | OUTx OCD Condition | Output Data Bit 13 Over Load Detect (OLD) Status | OUTx Status | Current Limit of all Drivers |
|---|---|---|---|---|
| 0 | 0 | 0 | Unchanged | 3 A |
| 0 | 1 | 1 (Need SRR to reset) | Unchanged | 3 A |
| 1 | 0 | 0 | Unchanged | 3 A |
| 1 | 1 | 1 (Need SRR to reset) | OUTx Latches Off (Need SRR to reset) | 3 A |

### Under Load Detection

The under−load detection is accomplished by monitoring the current from each output driver. A minimum load current (this is the maximum open circuit detection threshold) is required when the drivers are turned on. If the under−load circuit detection threshold has been crossed for more than the under−load delay time, the bit indicator (output bit #14) for open circuit will be set to a 1. In addition, the offending driver will be turned off only if input bit 14 (ULD) is set to 1 (true).

**Under Load Detection Shut Down**

| ULD Input Bit 14 | OUTx ULD Condition | Output Data Bit 14 Under Load Detect (ULD) Status | OUTx Status |
|---|---|---|---|
| 0 | 0 | 0 | Unchanged |
| 0 | 1 | 1 (Need SRR to reset) | Unchanged |
| 1 | 0 | 0 | Unchanged |
| 1 | 1 | 1 (Need SRR to reset) | OUTx Latches Off (Need SRR to reset) |

### Over Voltage Shutdown

Over voltage shutdown circuitry monitors the voltage on the VS1 and VS2 pins. When the Over−voltage Threshold voltage level has been breached on both or either one of the VSx supply inputs, output bit 15 will be set and, if input bit 15 (OVLO) is set to 1, all outputs will turn off. Turn on/off status is maintained in the logic circuitry. When proper input voltage levels are re−established, the programmed outputs will turn back on. Over−voltage shutdown can be disabled by using the SPI input bit 15 (OVLO = 0).

**Over Voltage Lock Out (OVLO) Shut Down**

| OVLO Input Bit 15 | VSx OVLO Condition | Output Data Bit 15 Power Supply Fail (PSF) Status | OUTx Status |
|---|---|---|---|
| 0 | 0 | 0 | Unchanged |
| 0 | 1 | 1 (Need SRR to reset) | Unchanged |
| 1 | 0 | 0 | Unchanged |
| 1 | 1 | 1 (Need SRR to reset) | All Outputs Off (Remain off until VSx is out of OVLO) |

### Thermal Shutdown

Six independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two levels, one to give a Thermal Warning (TW) and a higher one, Over Temperature, which will shut the drivers off. When the part reaches the temperature point of Thermal Warning, the output data bit 0 (TW) will be set to a 1, and the outputs will remain on. With one or more sensors detecting the over temperature level, all channels will be turned off simultaneously. All outputs will return to normal operation when the part thermally recovers (Thermal toggling), because the over temperature shutdown does not change the actual channel selection. The output data bit 0, Thermal Warning, will latch and remain set, even after cooling, and is reset by using a software command to input bit 0 (SRR). Since thermal warning precedes a thermal shutdown, software polling of this bit will allow for load control and possible prevention of thermal shutdown conditions.

Thermal warning information can be retrieved immediately without performing a complete SPI access cycle. Figure 4 below displays how this is accomplished. Bringing the CSB pin from a 1 to a 0 condition immediately displays the information on the output data bit 0, thermal warning, even in the absence of a SCLK signal. As the temperature of the NCV7708E changes from a condition from below the thermal warning threshold to above the thermal warning threshold, the state of the SO pin changes and this level is available immediately when the CSB goes to 0. A 0 on SO indicates there is no thermal warning, while a 1 indicates the IC is above the thermal warning threshold. This warning bit is reset by using the input data bit 0, SRR.

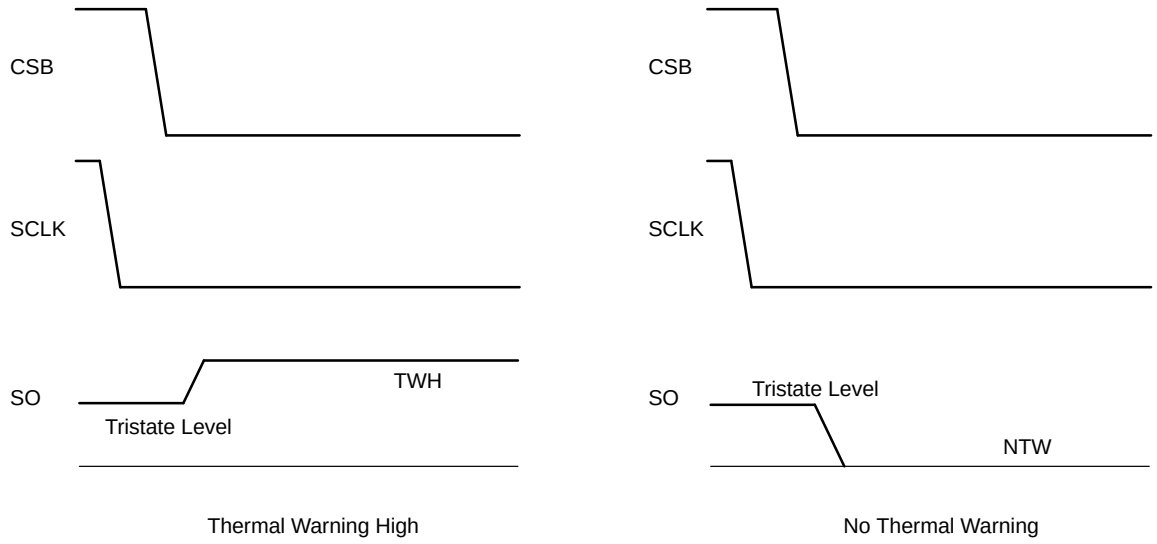



**Figure 4. Access to Temperature warning information shows the thermal information is available immediately with activation of the CSB signal without having to toggle the SCLK line.**

### Applications Drawing

The applications drawing below displays the range with which this part can drive a multitude of loads.

1. H−Bridge Driver configuration
2. Low Side Driver
3. High Side Driver

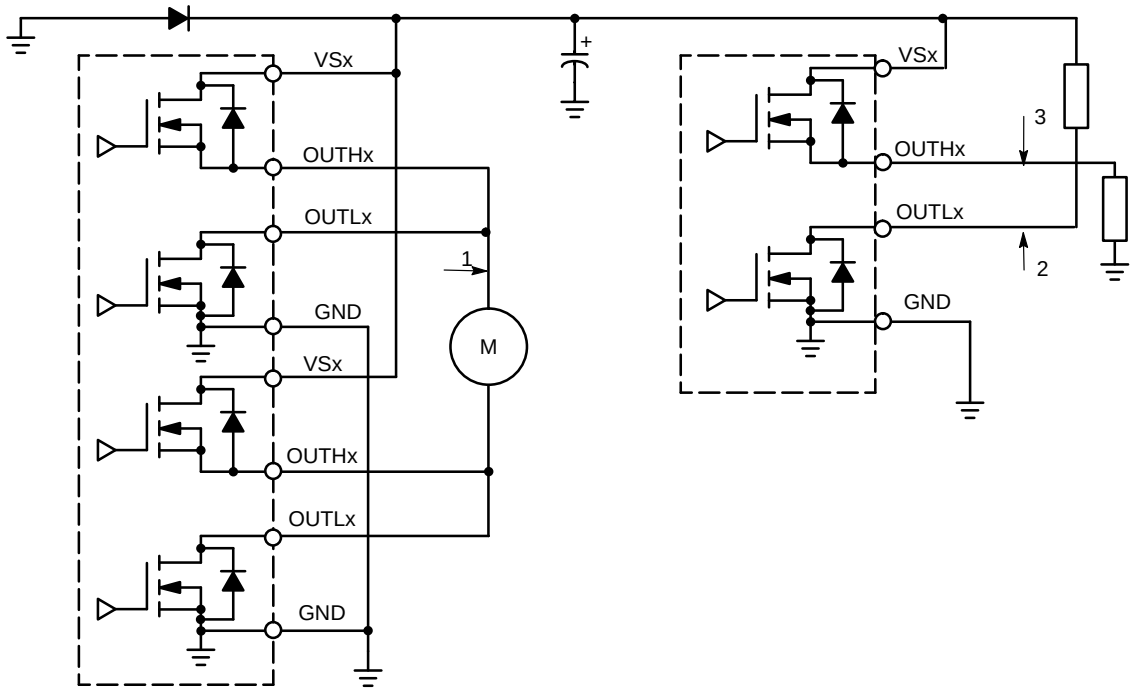



**Figure 5. Application Drawing**

Any combination of motors and high side drivers can be designed in. This allows for flexibility in many systems.

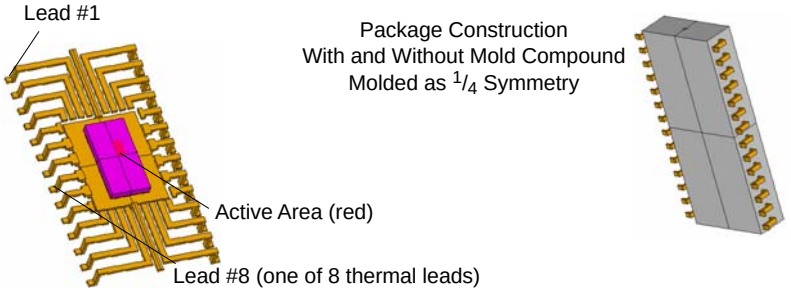
### H−Bridge Driver Configuration

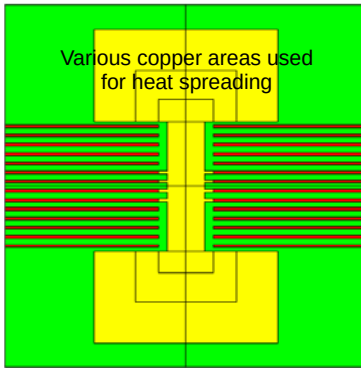
The NCV7708E has the flexibility of controlling each driver independently. When the device is set up in an H−Bridge configuration, the software design has to take care of avoiding simultaneous activation of connected HS and LS transistors. Resulting high shoot through currents could cause irreversible damage to the device.

### Overvoltage Clamping − Driving Inductive Loads

To avoid excessive voltages when driving inductive loads in a single−side−mode (LS or HS switch, no freewheeling path), the NCV7708E provides internal clamping diodes. Thus any load type can be driven without the requirement of external freewheeling diodes. Due to high power dissipation during clamping, the maximum energy capability of the driver transistor has to be considered.

### Thermal Model



## TYPICAL OPERATING CHARACTERISTICS

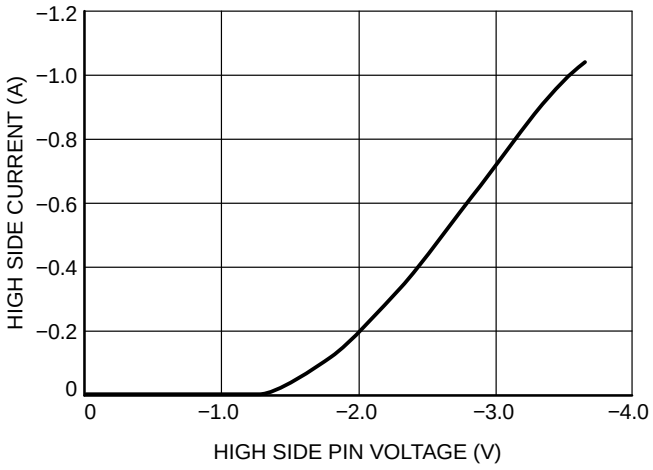



**Figure 6. Typical High−side Negative Clamp Voltage vs. Reverse Current, Room Temperature**

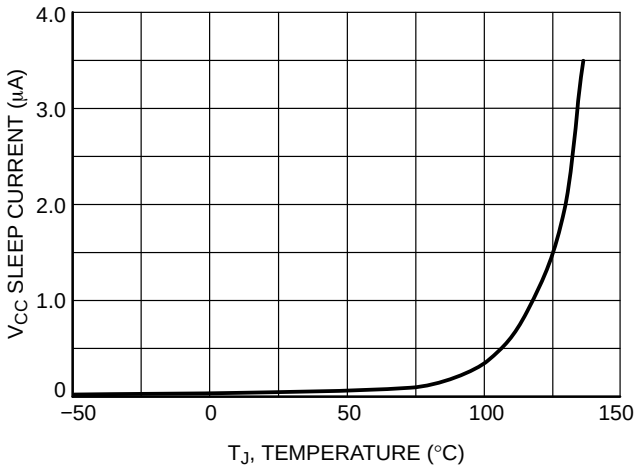



**Figure 7. $V_{CC}$ Sleep Supply Current vs. Temperature**

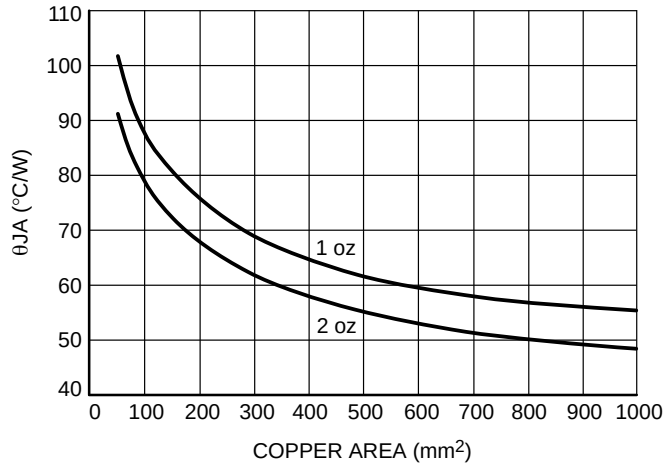



**Figure 8. θJA vs. Copper Spreader Area**

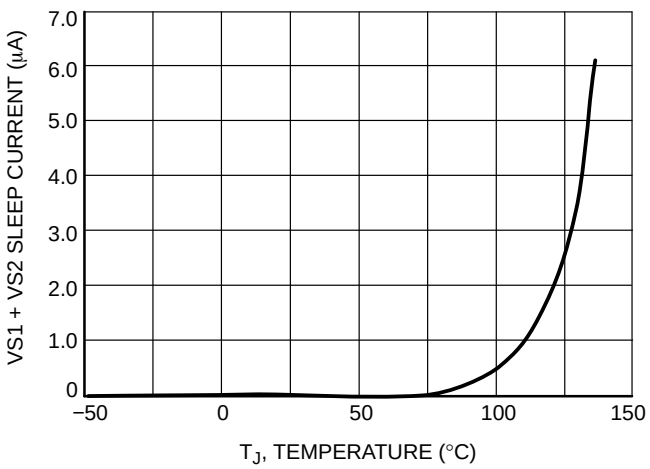



**Figure 9. VS1 + VS2 Sleep Current vs. Temperature**

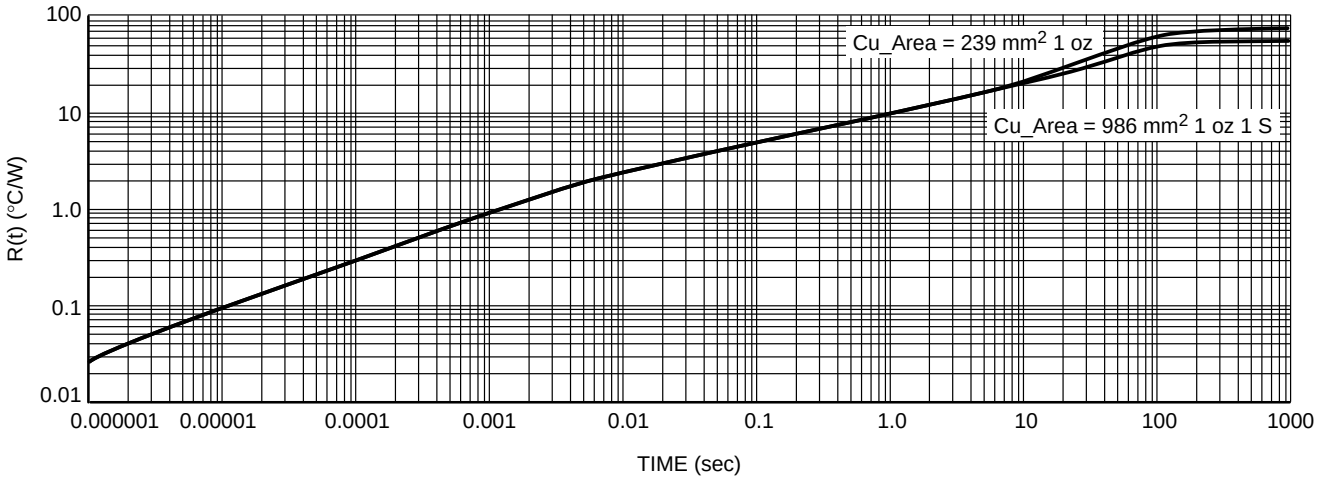



**Figure 10. SOIC 28−Lead Single Pulse Heating Curve**

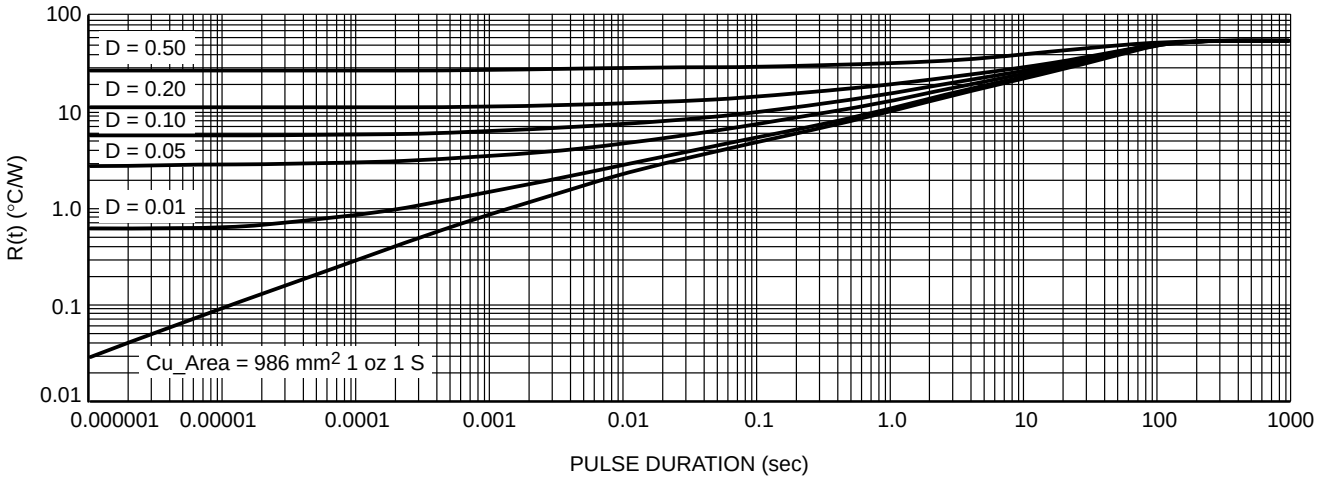



**Figure 11. SOIC 28−Lead Thermal Duty Cycle Curves on 1″ Spreader Test Board**

**SOIC 28−lead Thermal RC Network Models**

| **239 mm²** | **986 mm²** | | **239 mm²** | **986 mm²** | **Cu Area** |
|---|---|---|---|---|---|
| **Cauer Network** | | | **Foster Network** | | |
| **C's** | **C's** | **Units** | **Tau** | **Tau** | **Units** |
| **2.68E−05** | **2.68E−05** | W−s/C | **1.00E−06** | **1.00E−06** | sec |
| **1.02E−04** | **1.02E−04** | W−s/C | **1.00E−05** | **1.00E−05** | sec |
| **2.82E−04** | **2.84E−04** | W−s/C | **1.00E−04** | **1.00E−04** | sec |
| **9.58E−04** | **9.73E−04** | W−s/C | 5.00E−04 | 5.00E−04 | sec |
| **2.72E−03** | **2.63E−03** | W−s/C | 1.00E−03 | 1.00E−03 | sec |
| **2.02E−03** | **1.95E−03** | W−s/C | 1.00E−02 | 1.00E−02 | sec |
| **2.93E−02** | **3.12E−02** | W−s/C | 8.00E−02 | 8.00E−02 | sec |
| **0.116** | **0.091** | W−s/C | 4.00E−01 | 4.00E−01 | sec |
| 0.16 | 0.21 | W−s/C | 2.00E+00 | 2.00E+00 | sec |
| 1 | 1 | W−s/C | 6.00E+01 | 5.50E+01 | sec |
| R's | R's | | R's | R's | |
| **0.048** | **0.048** | °C/W | **2.84E−02** | **2.84E−02** | °C/W |
| **0.115** | **0.115** | °C/W | **6.14E−02** | **6.14E−02** | °C/W |
| **0.352** | **0.349** | °C/W | **1.94E−01** | **1.94E−01** | °C/W |
| **0.777** | **0.776** | °C/W | 0.100 | 0.100 | °C/W |
| **0.599** | **0.630** | °C/W | 0.500 | 0.480 | °C/W |
| **1.677** | **1.667** | °C/W | 1.839 | 1.933 | °C/W |
| **2.968** | **3.151** | °C/W | 2.207 | 1.836 | °C/W |
| **6.424** | **5.527** | °C/W | 1.249 | 2.291 | °C/W |
| 6.940 | 6.689 | °C/W | 8.225 | 8.000 | °C/W |
| 53.503 | 36.970 | °C/W | 59.000 | 41.000 | °C/W |

Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 28.4 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Both Foster and Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

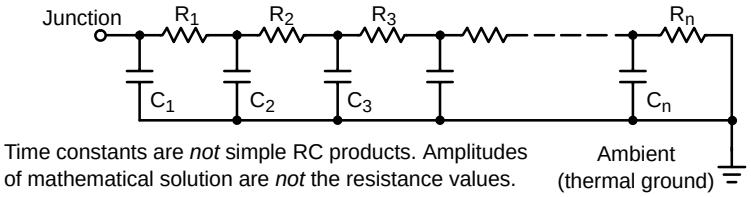



**Figure 12. Grounded Capacitor Thermal Network (“Cauer” Ladder)**

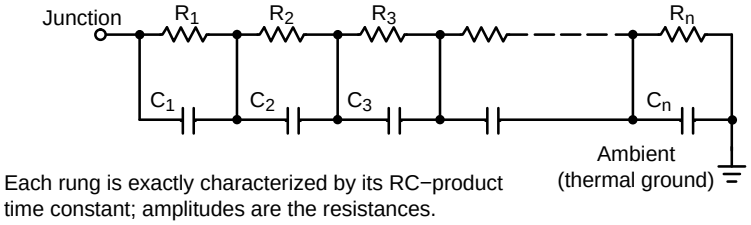
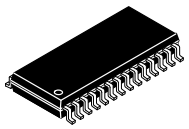


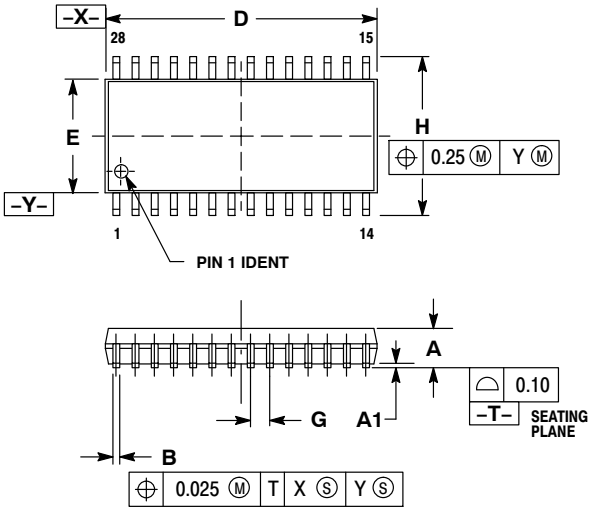

**Figure 13. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)**

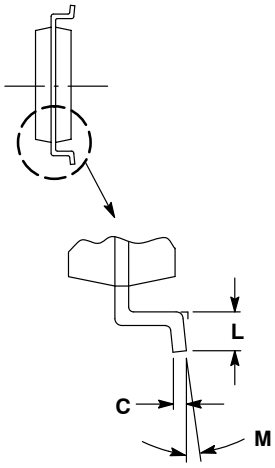


SCALE 1:1

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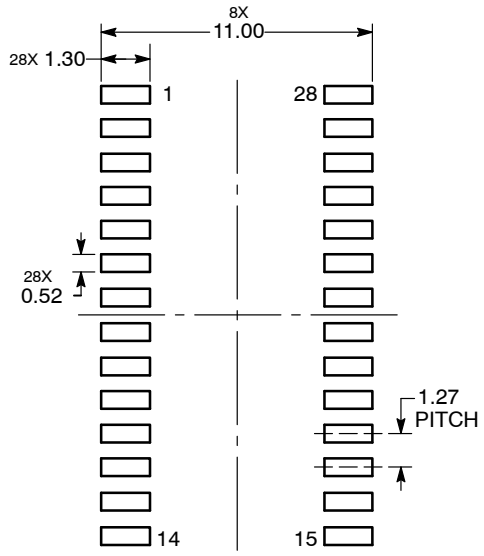



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.13 | 0.29 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 17.80 | 18.05 |
| E | 7.40 | 7.60 |
| G | 1.27 BSC | |
| H | 10.05 | 10.55 |
| L | 0.41 | 0.90 |
| M | 0 ° | 8 ° |

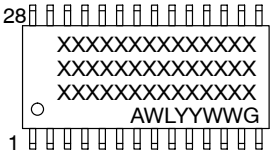
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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