Linear Voltage Regulator – LDO, Ultra Low Noise, High PSRR

200 mA

NCV8570B



DFN6
MN SUFFIX
CASE 506BA



TSOP-5
SN SUFFIX
CASE 483

The NCV8570B is a 200 mA Low Dropout, Linear Voltage Regulator with ultra low noise characteristics. It's low noise combined with high Power Supply Rejection Ratio (PSRR) make it especially suited for use in RF, audio or imaging applications. The device is manufactured in an advanced BiCMOS process to provide a powerful combination of low noise and excellent dynamic performance but with very low ground current consumption at full loads.

The NCV8570B is stable with small, low value capacitors allowing designers to minimise the total PCB space occupied by the solution. The device is packaged in a small 2x2.2 mm DFN6 package as well as in a TSOP-5 package.

Features

- Ultra Low Noise (typ. 10 μVrms @ V_{OUT} = 1.8 V)
- Very High PSRR (typ. 82 dB @ 1 kHz)
- Excellent Line and Load Regulation
- Stable with Ceramic Output Capacitors as low as 1 μF
- Very Low Ground Current (typ. 75 μA @ I_{OUT} = 200 mA)
- Low Sleep Mode Current (max. 1 μA)
- Active Discharge Circuit
- Current Limit and Thermal Shutdown Protection
- Output Voltage Options:
  - 1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V
  - Contact Factory for Other Voltage Options
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Applications

- Satellite and HD Radio
- Portable/Built-in DVD Entertainment Systems
- Noise Sensitive Applications (RF, Video, Audio)
- GPS Systems
- Camera for Lane Change Detection and Reverse View

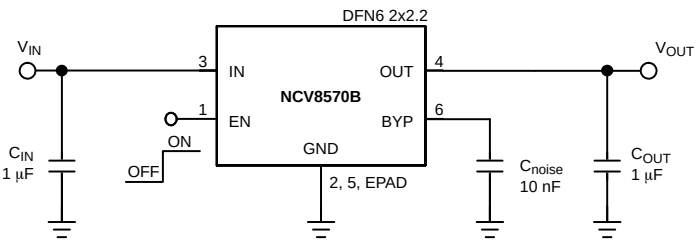
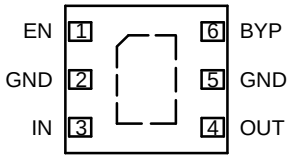
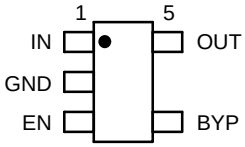


Figure 1. NCV8570B Typical Application Schematic

PIN CONNECTIONS

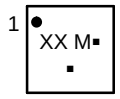


DFN6
(Top View)



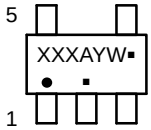
TSOP-5
(Top View)

MARKING DIAGRAMS



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package*

(*Note: Microdot may be in either location)



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package*

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 18 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 18.

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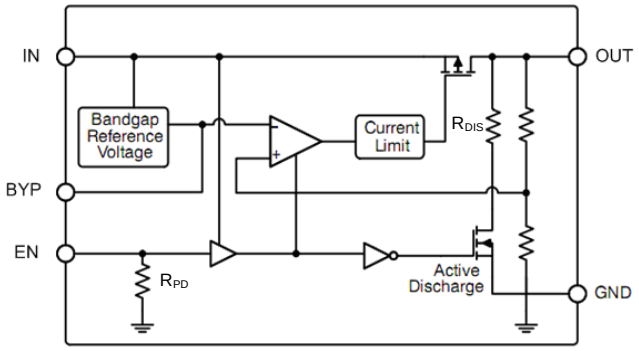


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. DFN6	Pin No. TSOP-5	Pin Name	Description
1	3	EN	Enable pin: This pin allows on/off control of the regulator. To disable the device, connect to GND. If this function is not in use, connect to Vin. Internal 5 MΩ Pull Down resistor is connected between EN and GND.
2, 5, EPAD	2	GND	Power Supply Ground (Pins are fused for the DFN6 package). Pins 2, 5 and EPAD are connected together through the lead frame in the DFN6 package.
3	1	IN	Power Supply Input Voltage
4	5	OUT	Regulated Output Voltage
6	4	BYP	Noise reduction pin. (Connect 10 nF or 100 nF capacitor to GND)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 2)	IN	−0.3 V to 6 V	V
Chip Enable Voltage	EN	−0.3 V to V_{IN} +0.3 V	
Noise Reduction Voltage	BYP	−0.3 V to V_{IN} +0.3 V	V
Output Voltage	OUT	−0.3 V to V_{IN} +0.3 V	V
Output Short-Circuit Duration	Infinity		
Maximum Junction Temperature	$T_{J(max)}$	125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V tested per MIL-STD-883, Method 3015
   Machine Model Method 200 V
   This device meets or exceeds AEC-Q100 standard

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Package Thermal Resistance, DFN6: (Notes 2, 3) Junction-to-Case (Pin 2) Junction-to-Ambient	 Ψ_{JL2} $R_{\theta JA}$	 38 110	°C/W
Package Thermal Resistance, TSOP-5: (Notes 2, 3) Junction-to-Case (Pin 2) Junction-to-Ambient	 Ψ_{JL2} $R_{\theta JA}$	 92 204	°C/W

2. Refer to APPLICATION INFORMATION for Safe Operating Area.
3. Single component mounted on 1 oz, FR4 PCB with 645 mm^2 Cu area.

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ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{OUT} + 0.5 V or 2.5 V (whichever is greater), V_{EN} = 1.2 V, C_{IN} = C_{OUT} = 1 μF, C_{noise} = 10 nF, I_{OUT} = 1 mA, T_J = −40 °C to 125 °C, unless otherwise specified) (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT							
Input Voltage Range			V_{IN}	2.5	–	5.5	V
Output Voltage 1.8 V 2.5 V 2.8 V 3.0 V 3.3 V	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V I_{OUT} = 1 mA to 200 mA		V_{OUT}	1.755 2.4375 2.730 2.925 3.2175 (−2.5%)	– – – – –	1.845 2.5625 2.870 3.075 3.3825 (+2.5%)	V
Power Supply Ripple Rejection	V_{IN} = V_{OUT} +1.0 V, I_{OUT} = 1 mA to 150 mA	f = 120 Hz f = 1 kHz f = 10 kHz	PSRR	– – –	80 82 63	– – –	dB
Line Regulation	V_{IN} = (V_{OUT} +0.5 V) to 5.5 V, I_{OUT} = 1 mA		ΔV_{OUT} / ΔV_{IN}	−0.1	–	0.1	%/V
Load Regulation	I_{OUT} = 1 mA to 200 mA		ΔV_{OUT} / ΔI_{OUT}	–	0.2	5.0	mV
Output Noise Voltage	V_{OUT} = 1.8 V, f = 10 Hz to 100 kHz, I_{OUT} = 1 mA to 150 mA	C_{noise} = 100 nF C_{noise} = 10 nF	V_N	– –	10 15	– –	μV_{RMS}
Output Current Limit	V_{OUT} = $V_{OUT(NOM)}$ – 0.1 V		I_{LIM}	200	310	470	mA
Output Short Circuit Current	V_{OUT} = 0V		I_{SC}	205	320	490	mA
Dropout Voltage (Note 5)	I_{OUT}= 150 mA	$V_{OUT(NOM)}$ = 2.5 V $V_{OUT(NOM)}$ = 2.8 V $V_{OUT(NOM)}$ = 3.0 V $V_{OUT(NOM)}$ = 3.3 V	V_{DO}	– – – –	100 90 85 80	180 165 150 145	mV
Dropout Voltage (Note 5)	I_{OUT}= 200 mA	$V_{OUT(NOM)}$ = 2.5 V $V_{OUT(NOM)}$ = 2.8 V $V_{OUT(NOM)}$ = 3.0 V $V_{OUT(NOM)}$ = 3.3 V	V_{DO}	– – – –	140 120 115 110	230 205 190 185	mV
GENERAL							
Ground Current	I_{OUT} = 1 mA I_{OUT} = 200 mA		I_{GND}	– –	70 75	110 130	μA
Disable Current	V_{EN} = 0 V		I_{DIS}	–	0.1	1.0	μA
Thermal Shutdown	Shutdown, Temperature Increasing		T_{SDU}	–	150	–	°C
	Reset, Temperature Decreasing		T_{SDD}	–	135	–	°C
OUTPUT ENABLE							
Enable Threshold Low High			$V_{th(EN)}$	– 1.2	– –	0.4 –	V
Internal Pull-Down Resistance (Note 6)			$R_{PD(EN)}$	2.5	5.0	10	MΩ
TIMING							
Turn-On Time	I_{OUT} = 10 mA, V_{OUT} = 0.975 $V_{OUT(NOM)}$	C_{noise} = 10 nF C_{noise} = 100 nF	t_{ON}	– –	0.4 4.0	– –	ms
Turn-Off Time	C_{noise} = 10 nF/100 nF, V_{OUT} = 0.1 $V_{OUT(NOM)}$	I_{OUT} = 1 mA I_{OUT} = 10 mA	t_{OFF}	– –	2.0 0.6	– –	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Measured when the output voltage falls 100 mV below the nominal output voltage (nominal output voltage is the voltage at the output measured under the condition V_{IN} = V_{OUT} + 0.5 V). In the case of devices having the nominal output voltage V_{OUT} = 1.8 V the minimum input to output voltage differential is given by the $V_{IN(MIN)}$ = 2.5 V.
6. Expected to disable the device when EN pin is floating.

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TYPICAL CHARACTERISTICS

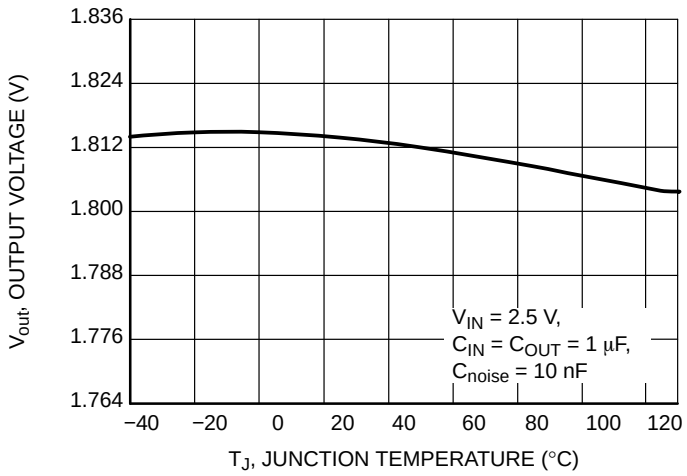


Figure 3. Output Voltage vs. Junction Temperature, V_{OUT} = 1.8 V

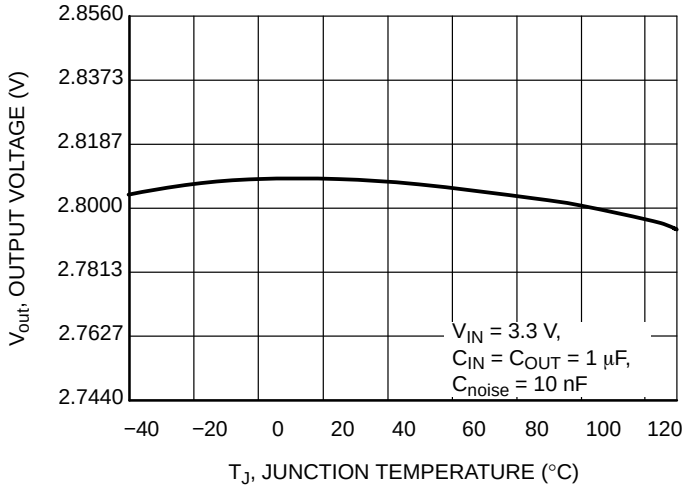


Figure 4. Output Voltage vs. Junction Temperature, V_{OUT} = 2.8 V

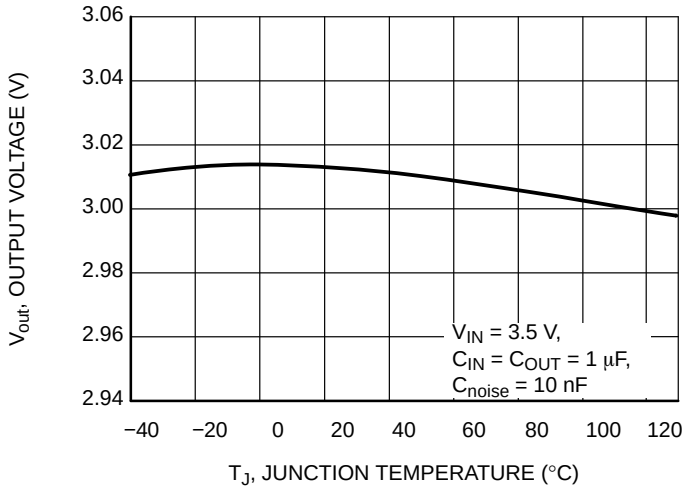


Figure 5. Output Voltage vs. Junction Temperature, V_{OUT} = 3.0 V

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TYPICAL CHARACTERISTICS

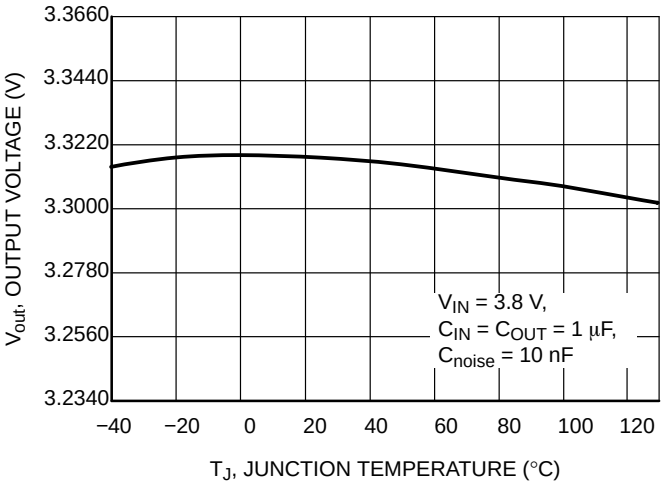


Figure 6. Output Voltage vs. Junction Temperature, V_{OUT} = 3.3 V

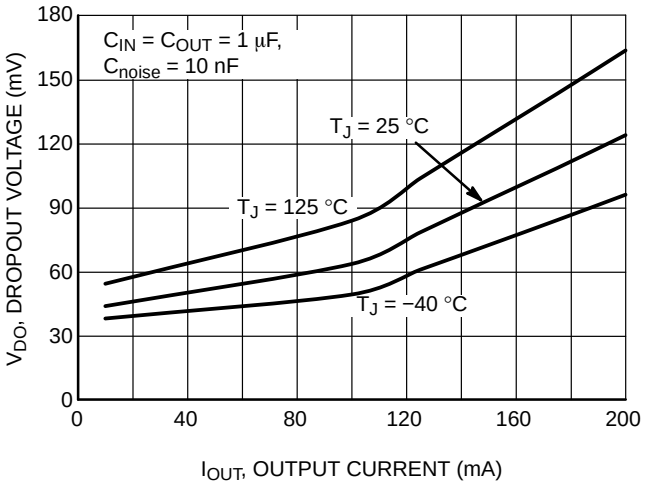


Figure 7. Dropout Voltage vs. Output Current, V_{OUT} = 2.8 V

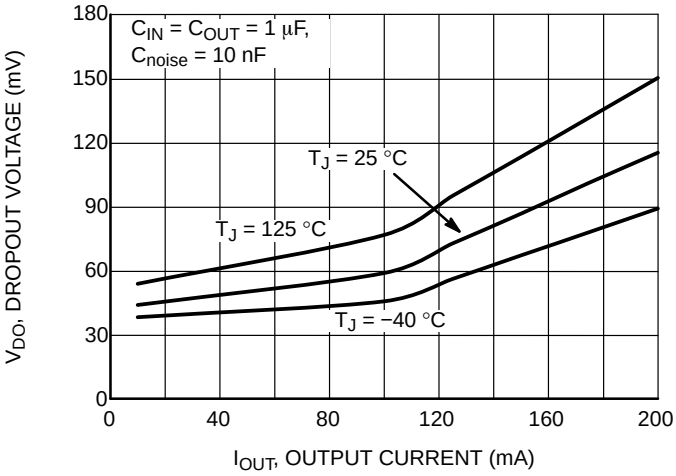


Figure 8. Dropout Voltage vs. Output Current, V_{OUT} = 3.0 V

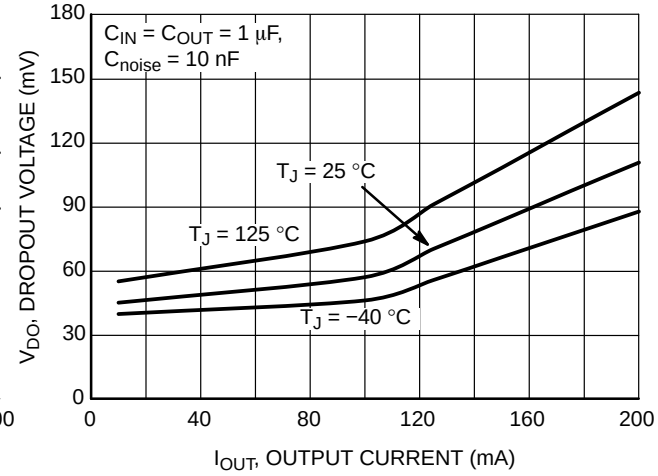


Figure 9. Dropout Voltage vs. Output Current, V_{OUT} = 3.3 V

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TYPICAL CHARACTERISTICS

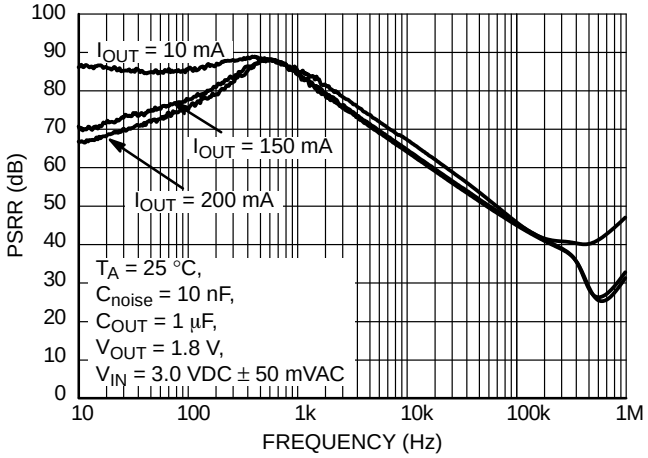


Figure 10. PSRR vs. Frequency, 1.8 V Output Voltage Option, C_{OUT} = 1 μF, C_{noise} = 10 nF

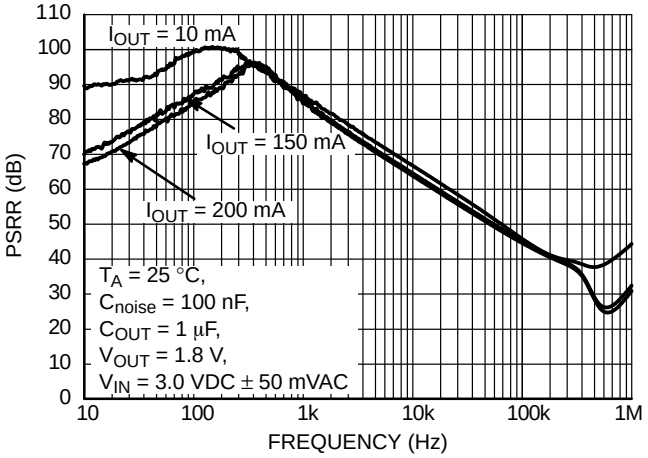


Figure 11. PSRR vs. Frequency, 1.8 V Output Voltage Option, C_{OUT} = 1μF, C_{noise} = 100nF

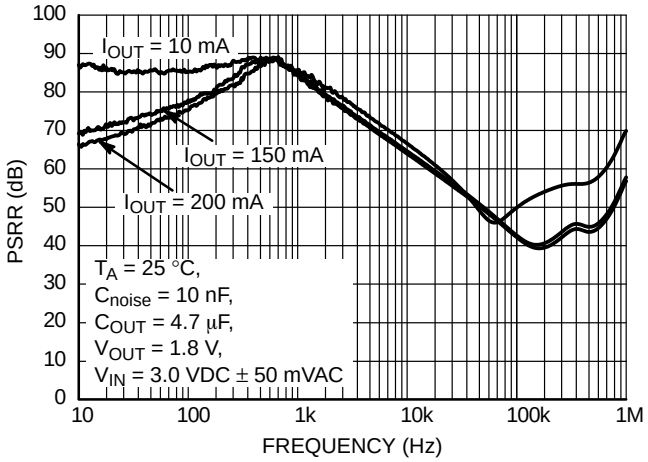


Figure 12. PSRR vs. Frequency, 1.8 V Output Voltage Option, C_{OUT} = 4.7 μF, C_{noise} = 10 nF

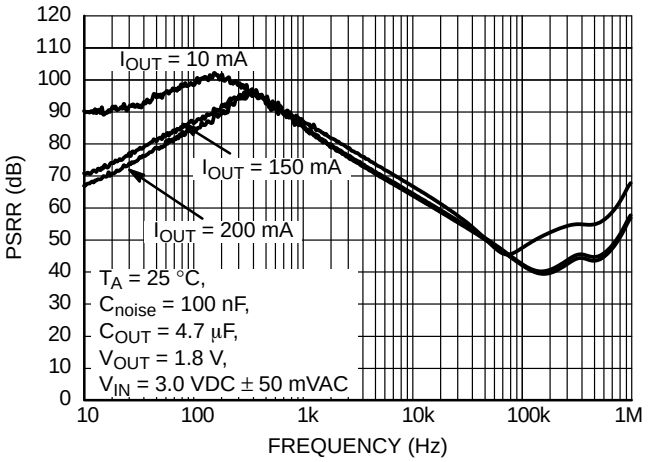


Figure 13. PSRR vs. Frequency, 1.8V Output Voltage Option, C_{OUT} = 4.7μF, C_{noise} = 100nF

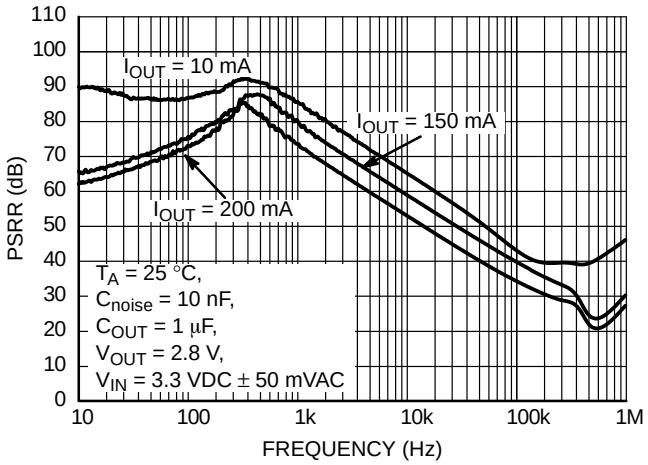


Figure 14. PSRR vs. Frequency, 2.8 V Output Voltage Option, C_{OUT} = 1 μF, C_{noise} = 10 nF

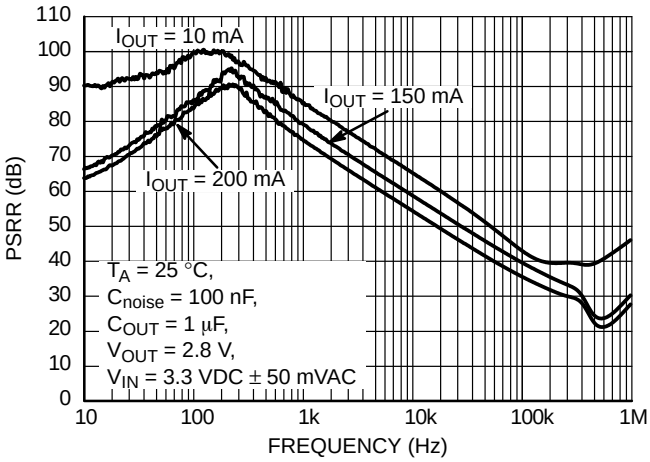


Figure 15. PSRR vs. Frequency, 2.8 V Output Voltage Option, C_{OUT} = 1 μF, C_{noise} = 100 nF

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TYPICAL CHARACTERISTICS

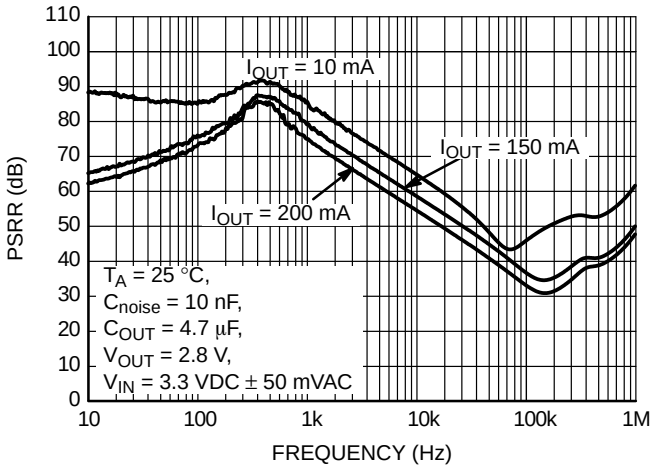


Figure 16. PSRR vs. Frequency, 2.8 V Output Voltage Option, C_{OUT} = 4.7 μF, C_{noise} = 10 nF

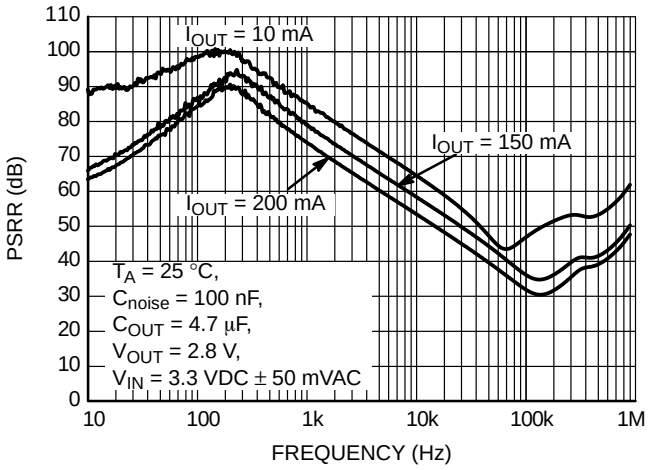


Figure 17. PSRR vs. Frequency, 2.8 V Output Voltage Option, C_{OUT} = 4.7 μF, C_{noise} = 100 nF

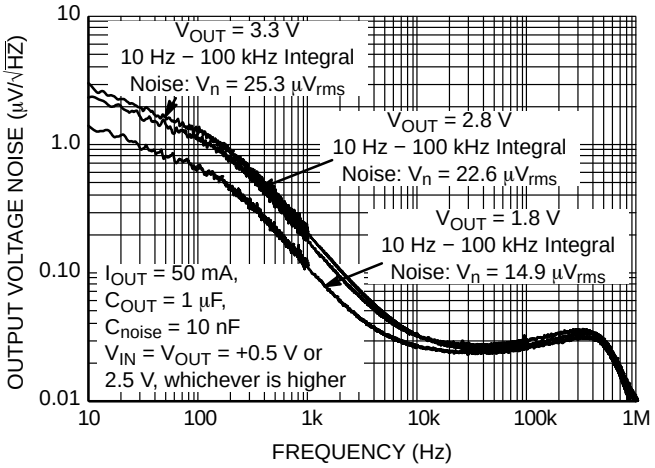


Figure 18. Output Noise vs. Frequency, C_{OUT} = 1 μF, C_{noise} = 10 nF, I_{OUT} = 50 mA

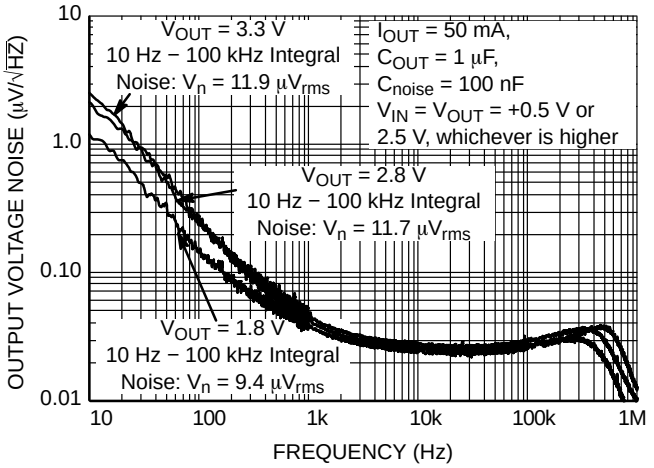


Figure 19. Output Noise vs. Frequency, C_{OUT} = 1 μF, C_{noise} = 100 nF, I_{OUT} = 50 mA

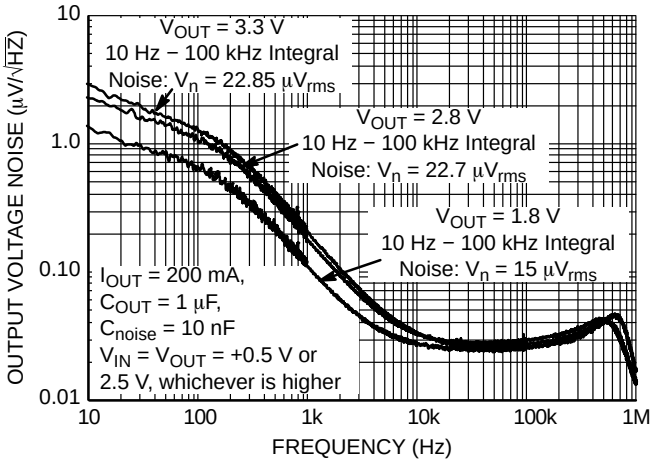


Figure 20. Output Noise vs. Frequency, C_{OUT} = 1 μF, C_{noise} = 10 nF, I_{OUT} = 200 mA

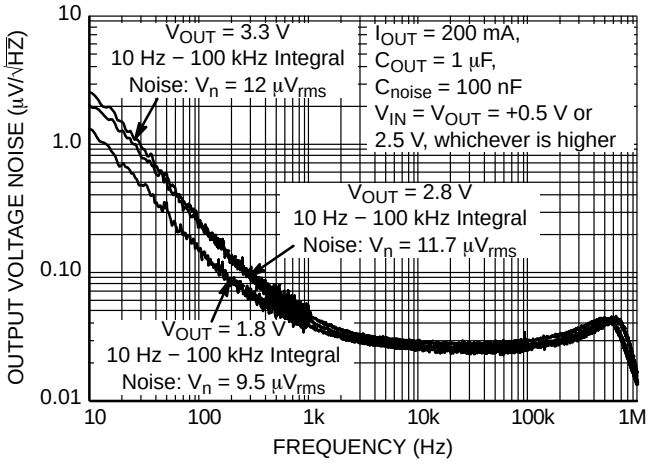


Figure 21. Output Noise vs. Frequency, C_{OUT} = 1 μF, C_{noise} = 100 nF, I_{OUT} = 200 mA

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TYPICAL CHARACTERISTICS

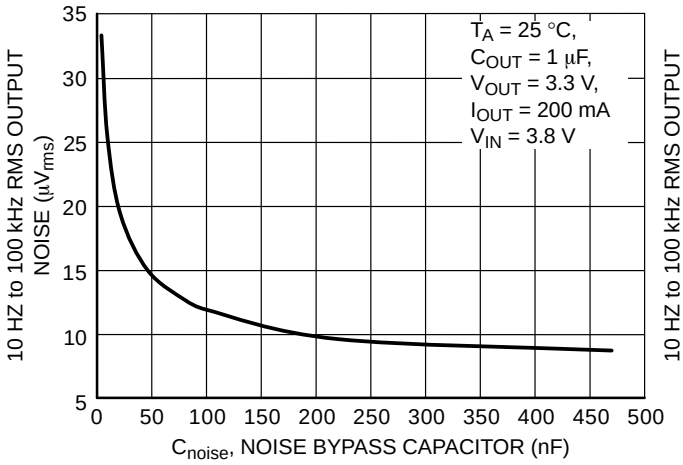


Figure 22. Output Noise vs. Noise Bypass Capacitance, C_{OUT} = 1 μF, V_{OUT} = 3.3 V, I_{OUT} = 200 mA

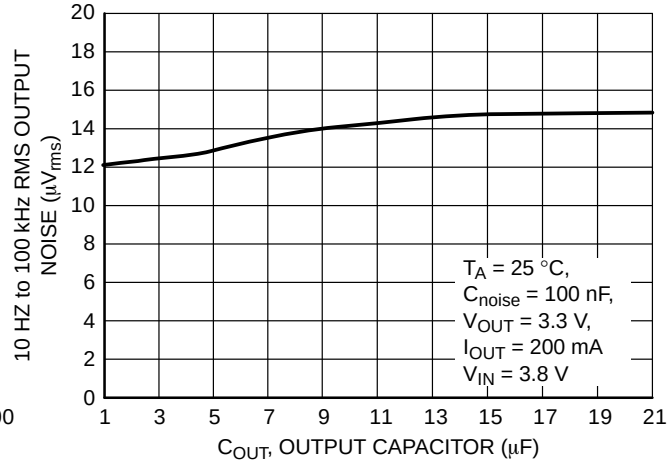


Figure 23. Output Noise vs. Output Capacitance, C_{noise} = 100 nF, V_{OUT} = 3.3 V, I_{OUT} = 200 mA

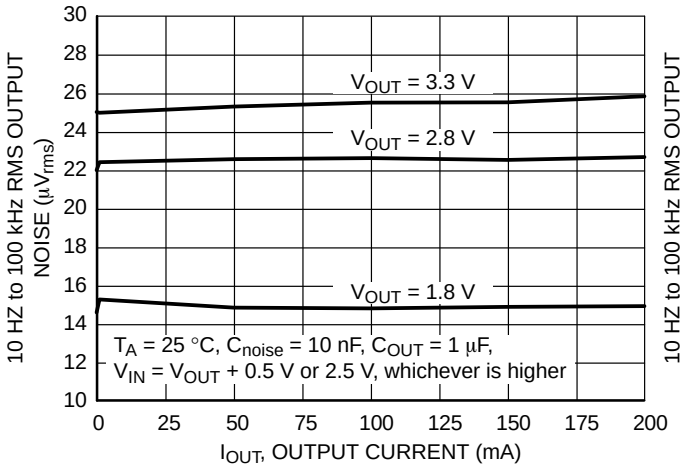


Figure 24. Output Noise vs. Load Current, C_{noise} = 10 nF, C_{OUT} = 1 μF

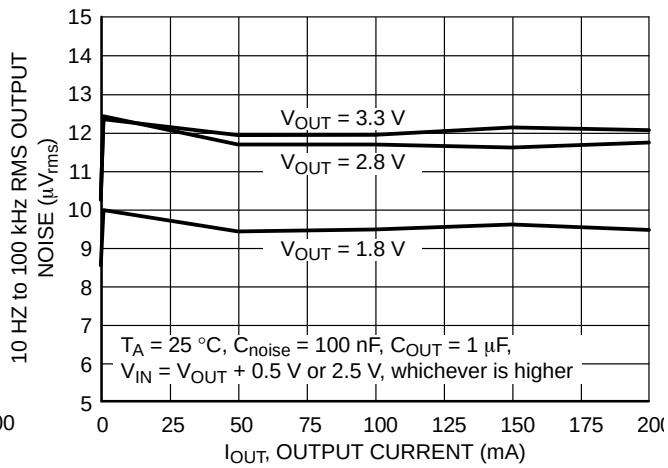


Figure 25. Output Noise vs. Load Current, C_{noise} = 100 nF, C_{OUT} = 1 μF

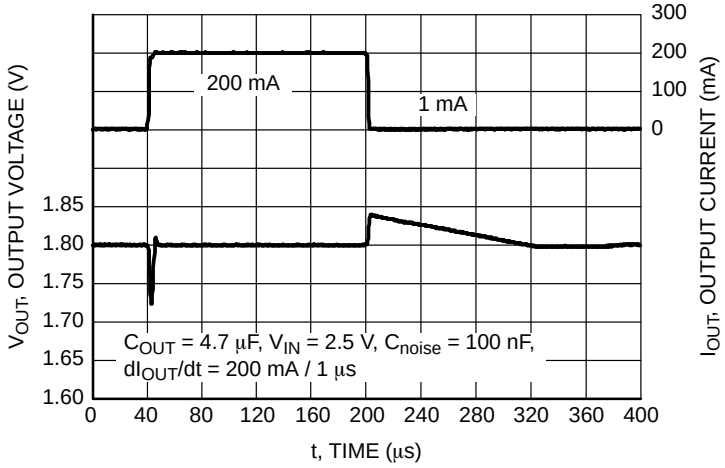


Figure 26. Load Transient Response, V_{OUT} = 1.8 V, C_{OUT} = 4.7 μF, C_{noise} = 100 nF

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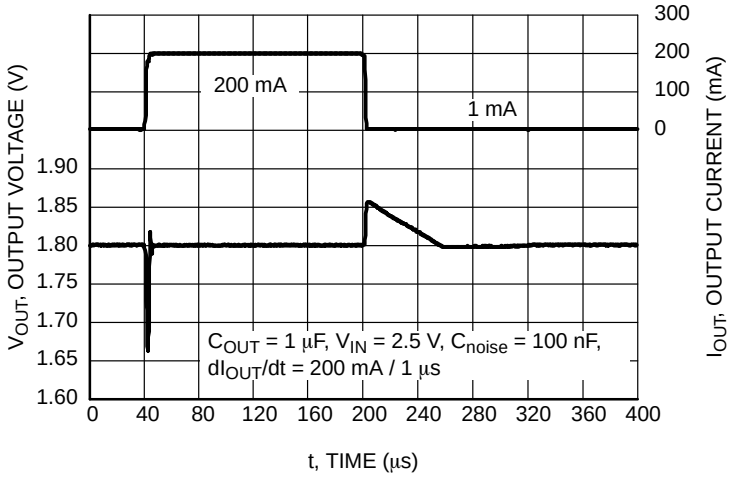


Figure 27. Load Transient Response, V_{OUT} = 1.8 V, C_{OUT} = 1 µF, C_{noise} = 100 nF

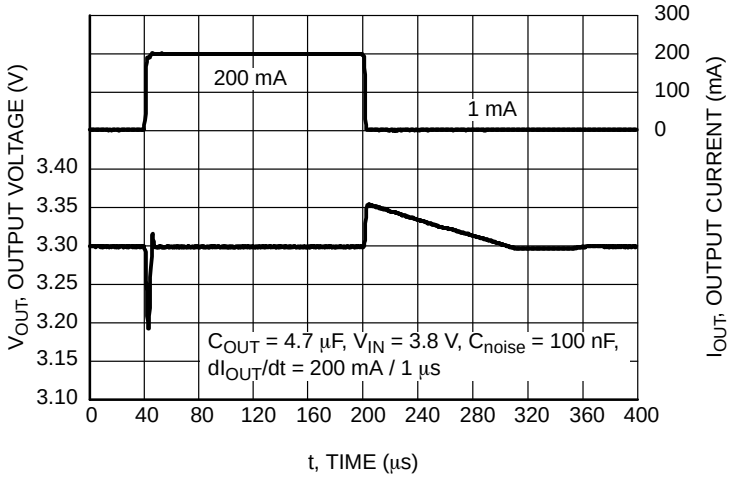


Figure 28. Load Transient Response, V_{OUT} = 3.3 V, C_{OUT} = 4.7 µF, C_{noise} = 100 nF

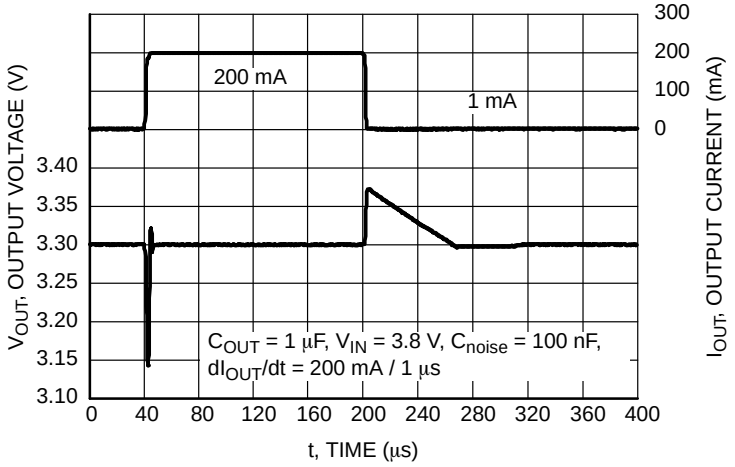


Figure 29. Load Transient Response, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, C_{noise} = 100 nF

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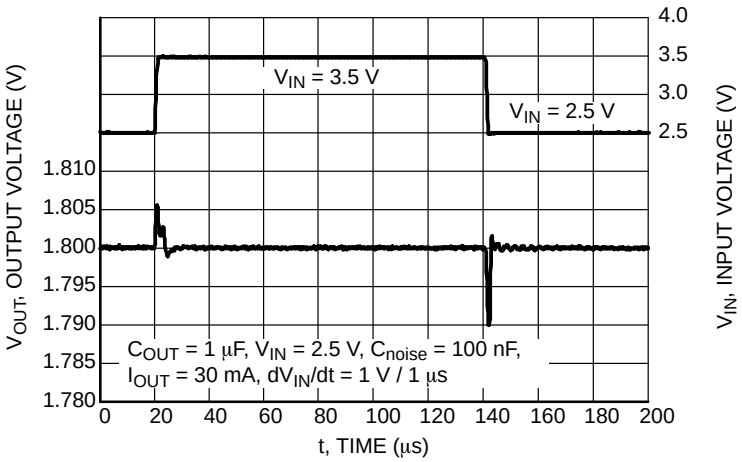


Figure 30. Line Transient Response, V_{OUT} = 1.8 V, C_{OUT} = 1 µF, I_{OUT} = 30 mA

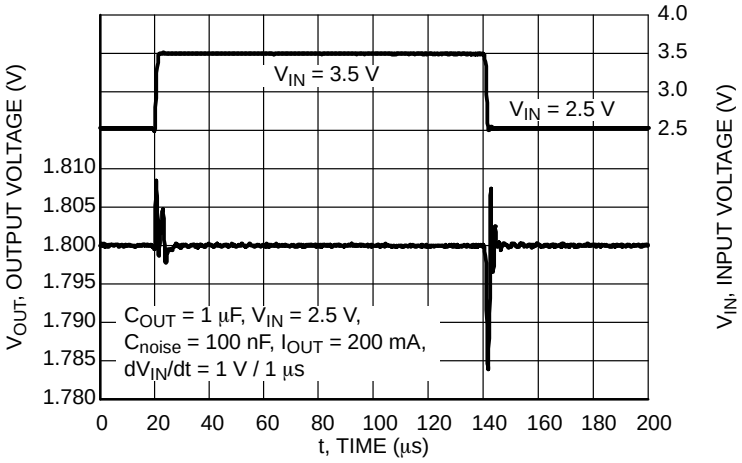


Figure 31. Line Transient Response, V_{OUT} = 1.8 V, C_{OUT} = 1 µF, I_{OUT} = 200 mA

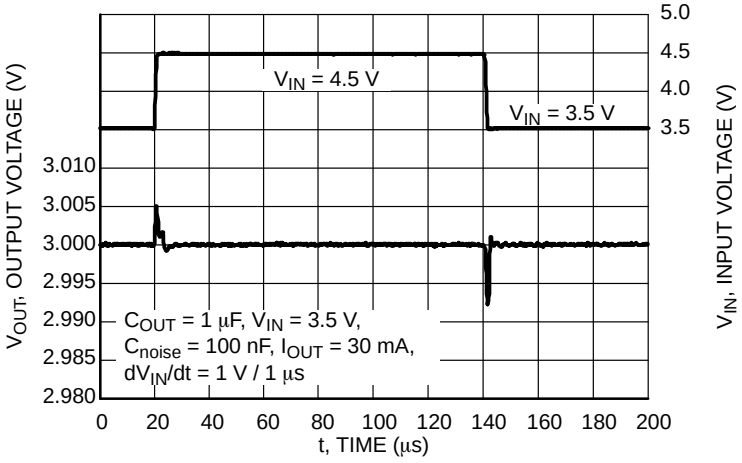


Figure 32. Line Transient Response, V_{OUT} = 3.0 V, C_{OUT} = 1 µF, I_{OUT} = 30 mA

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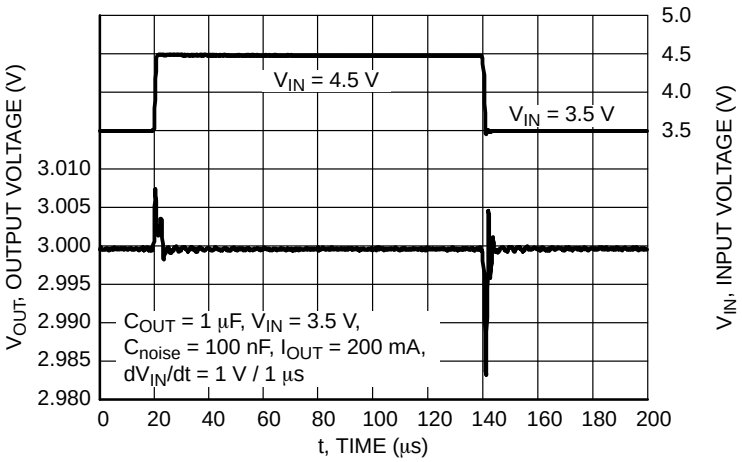


Figure 33. Line Transient Response, V_{OUT} = 3.0 V, C_{OUT} = 1 μF, I_{OUT} = 200 mA

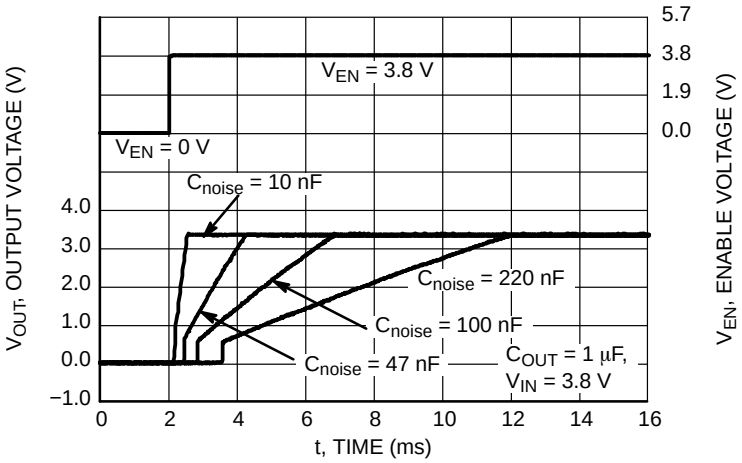


Figure 34. Turn-On Response V_{OUT} = 3.3 V, C_{OUT} = 1 μF, I_{OUT} = 30 mA

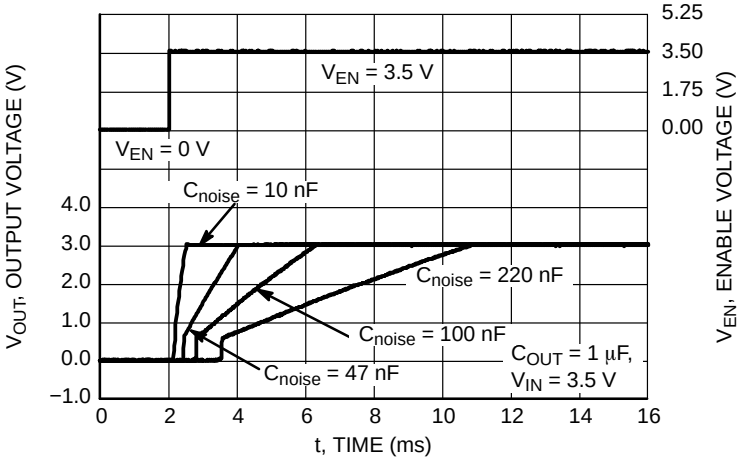


Figure 35. Turn-On Response V_{OUT} = 3 V, C_{OUT} = 1 μF, I_{OUT} = 30 mA

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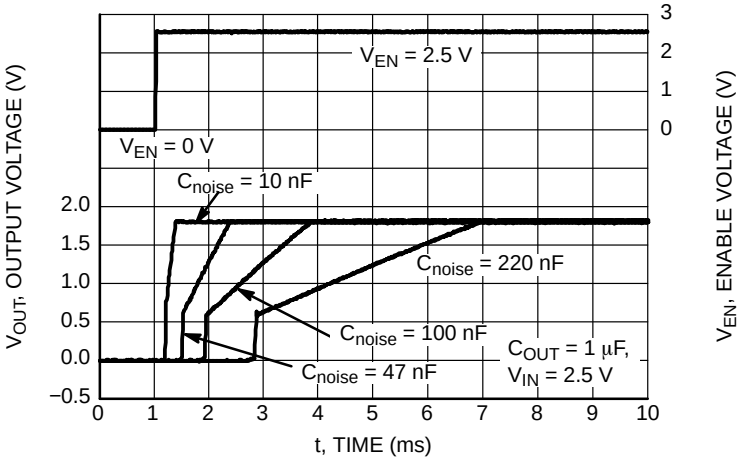


Figure 36. Turn-On Response
V_{OUT} = 1.8 V, C_{OUT} = 1 μF, I_{OUT} = 30 mA

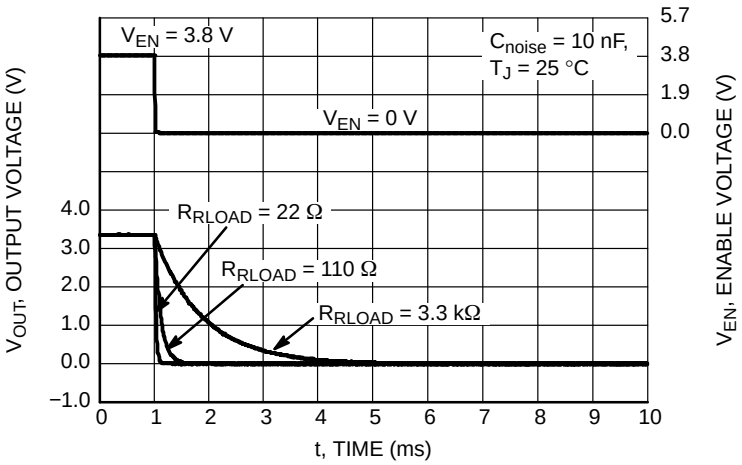


Figure 37. Turn-Off Response
V_{OUT} = 3.3 V, C_{OUT} = 1 μF

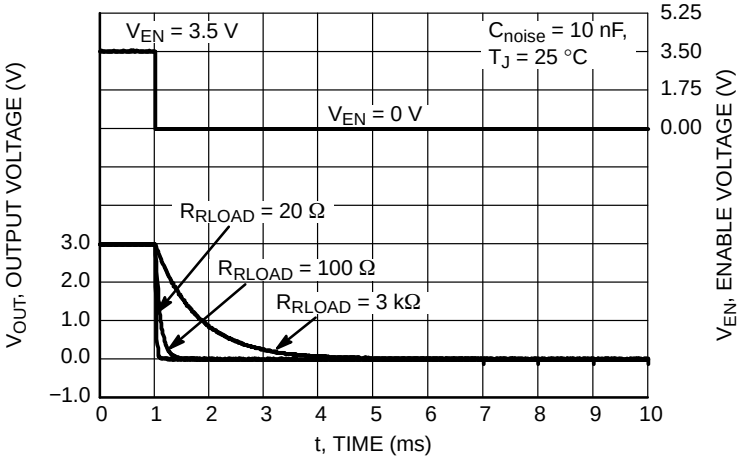


Figure 38. Turn-Off Response
V_{OUT} = 3 V, C_{OUT} = 1 μF

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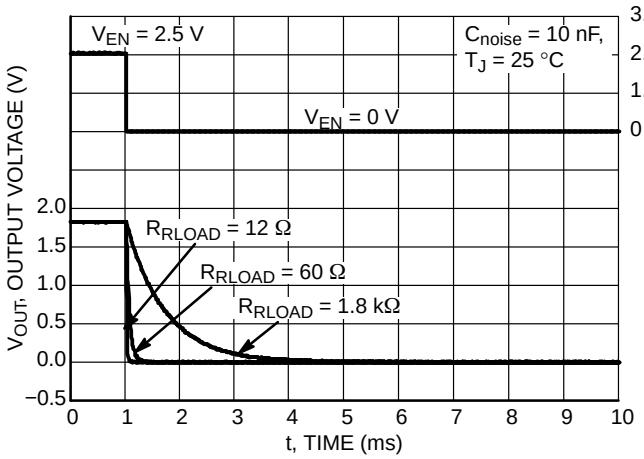


Figure 39. Turn-Off Response
V_{OUT} = 1.8 V, C_{OUT} = 1 μF

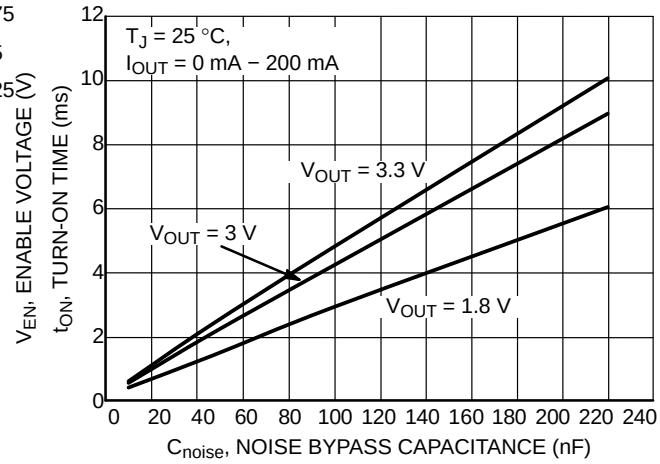


Figure 40. Turn-On Time vs. Noise Bypass Capacitance, C_{OUT} = 1 μF, I_{OUT} = 0 mA − 200 mA

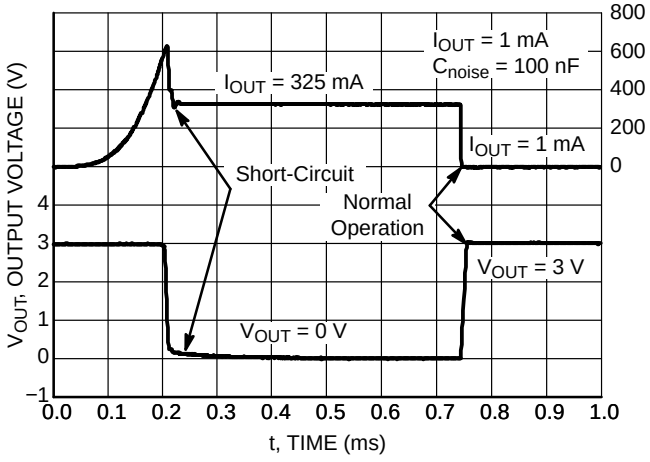


Figure 41. Short-Circuit Protection,
V_{OUT} = 3 V, C_{OUT} = 1 μF, C_{noise} = 100 nF

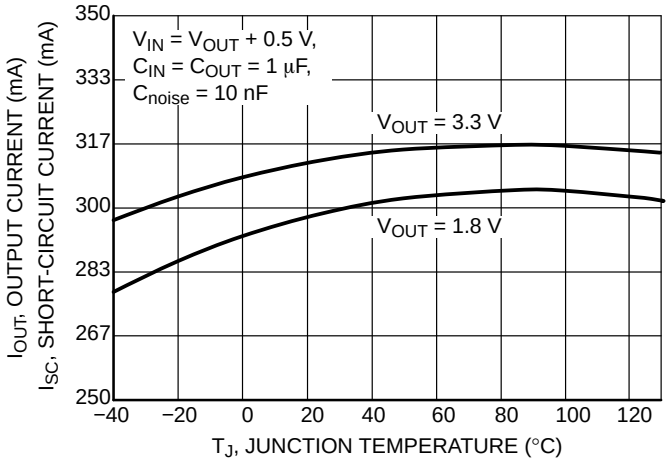


Figure 42. Short-Circuit Current vs. Junction Temperature, V_{OUT} = 1.8 V, 3.3 V

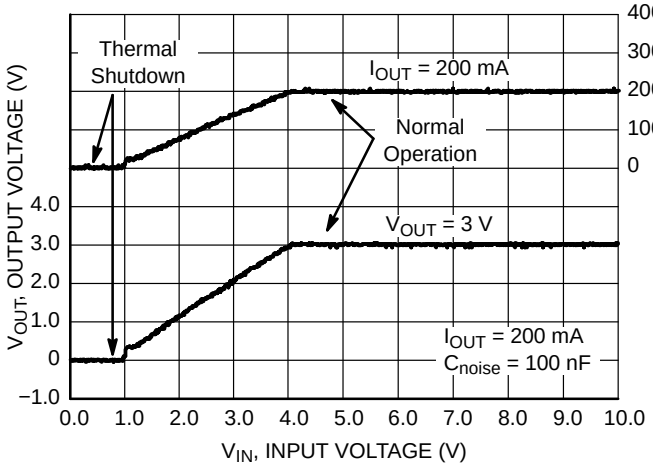


Figure 43. Thermal Shutdown Protection
V_{OUT} = 3 V, C_{noise} = 100 nF, C_{OUT} = 1 μF

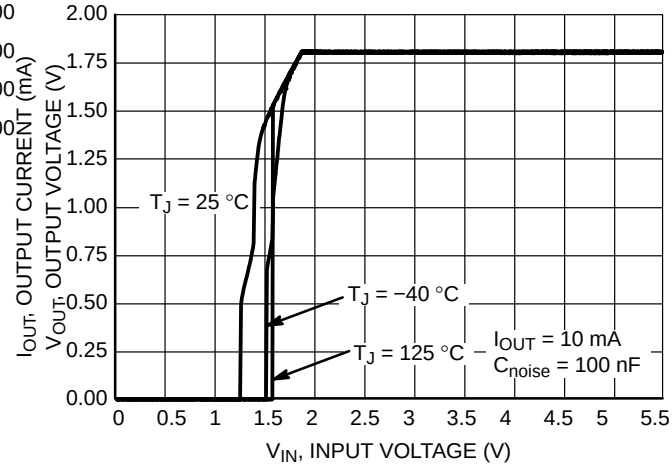


Figure 44. Output Voltage vs. Input Voltage,
V_{OUT} = 1.8 V, C_{OUT} = 1 μF

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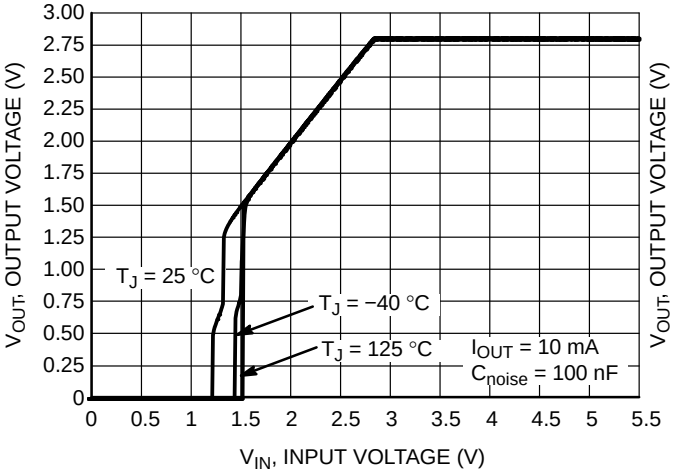


Figure 45. Output Voltage vs. Input Voltage, V_{OUT} = 2.8 V, C_{OUT} = 1 μF

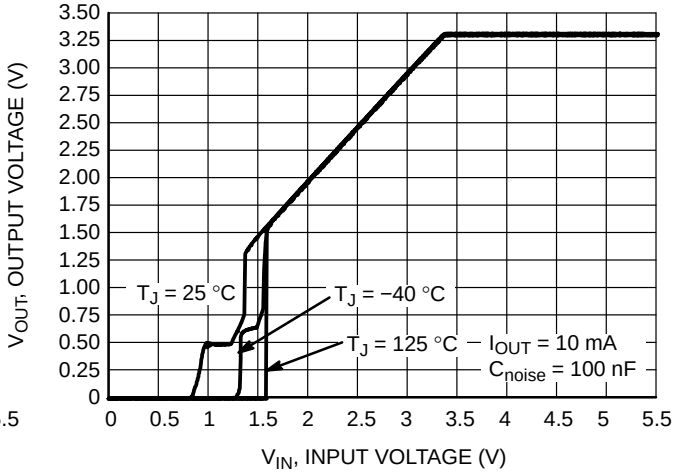


Figure 46. Output Voltage vs. Input Voltage, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

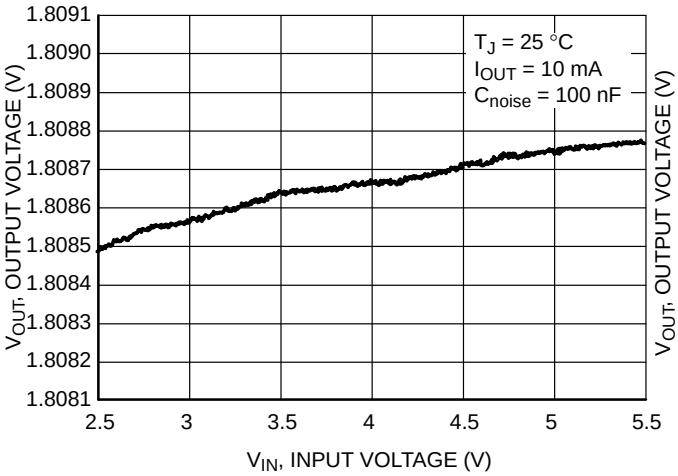


Figure 47. Output Voltage vs. Input Voltage, V_{OUT} = 1.8 V, C_{OUT} = 1 μF

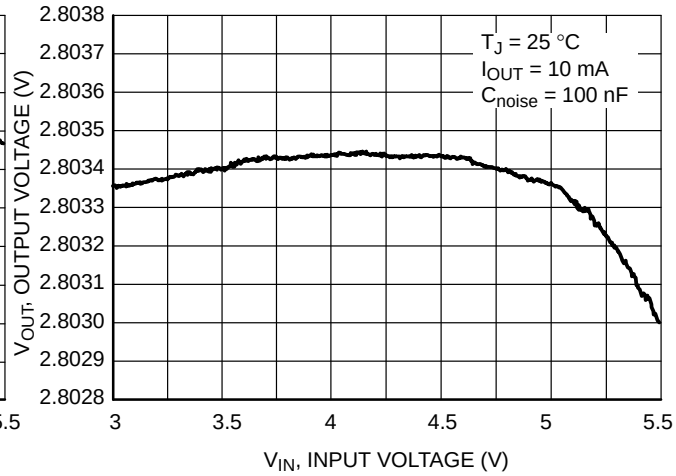


Figure 48. Output Voltage vs. Input Voltage, V_{OUT} = 2.8 V, C_{OUT} = 1 μF

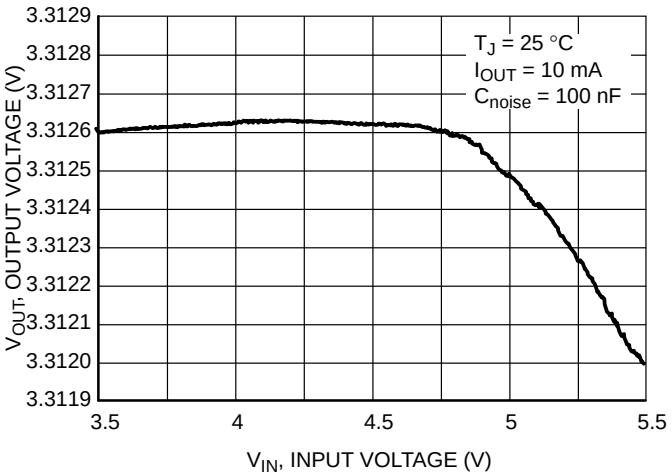


Figure 49. Output Voltage vs. Input Voltage, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

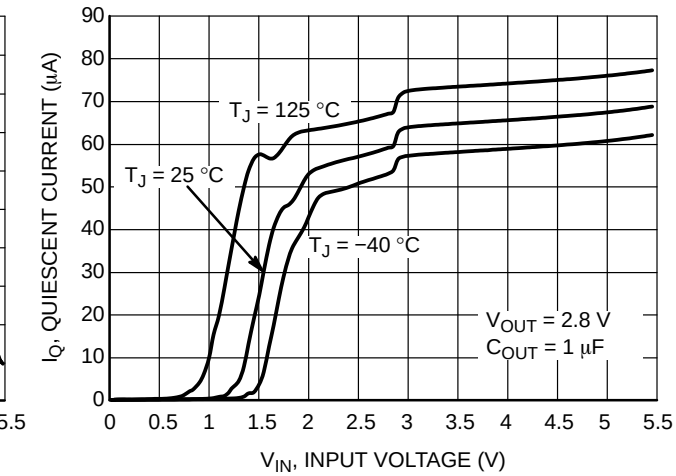


Figure 50. Quiescent Current vs. Input Voltage, V_{OUT} = 2.8 V, C_{OUT} = 1 μF

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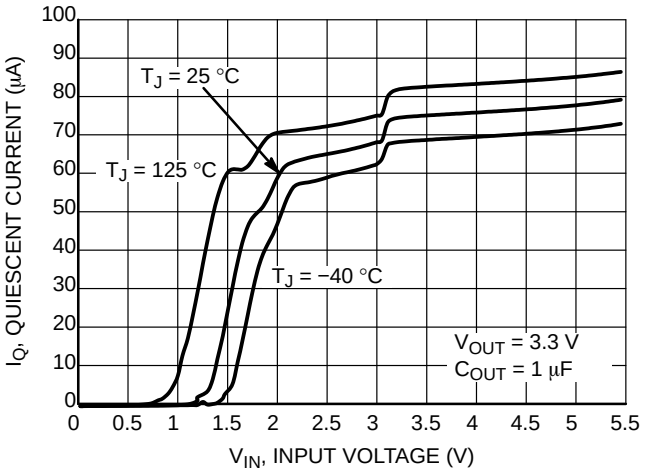


Figure 51. Quiescent Current vs. Input Voltage, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

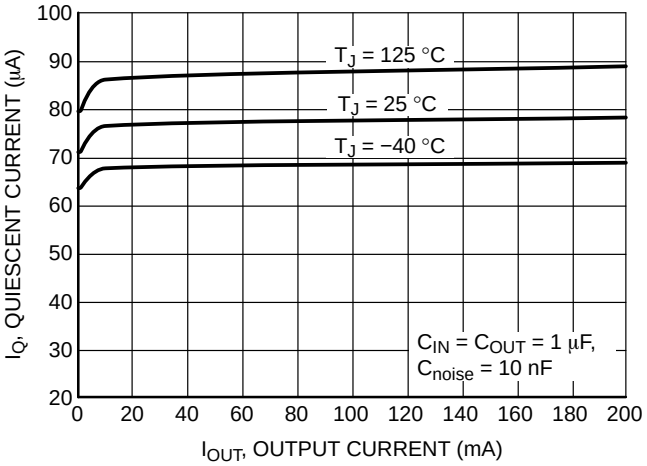


Figure 52. Quiescent Current vs. Output Current, V_{OUT} = 3.3 V

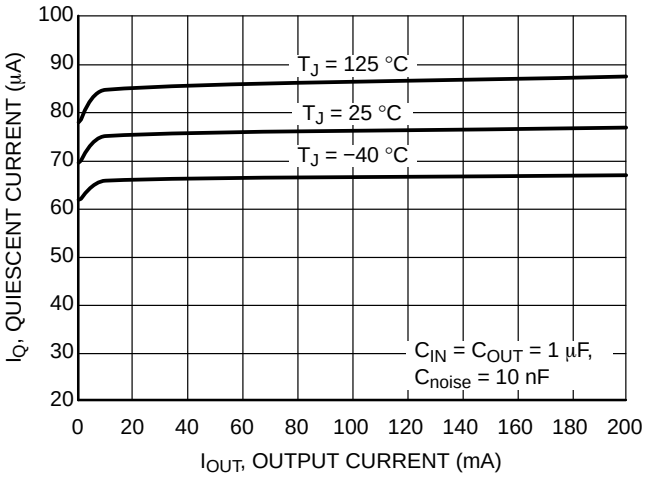


Figure 53. Quiescent Current vs. Output Current, V_{OUT} = 3.0 V

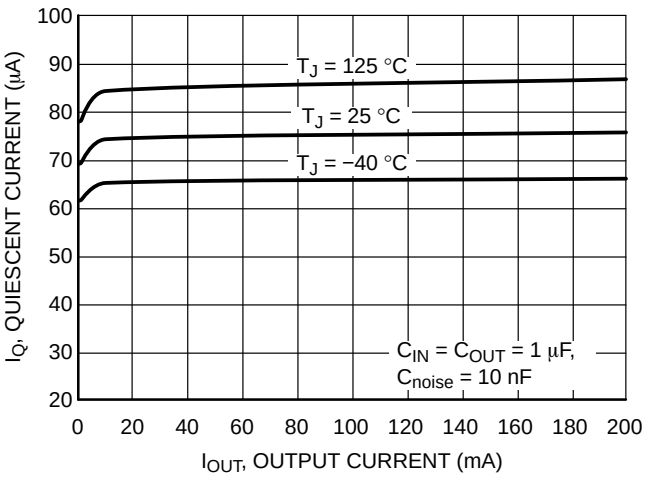


Figure 54. Quiescent Current vs. Output Current, V_{OUT} = 2.8 V

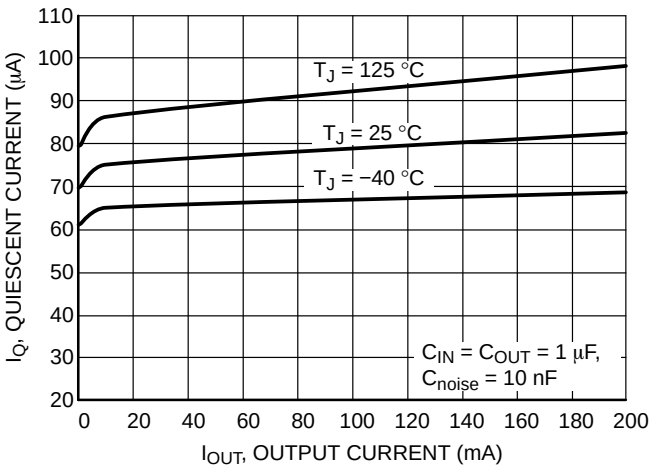


Figure 55. Quiescent Current vs. Output Current, V_{OUT} = 1.8 V

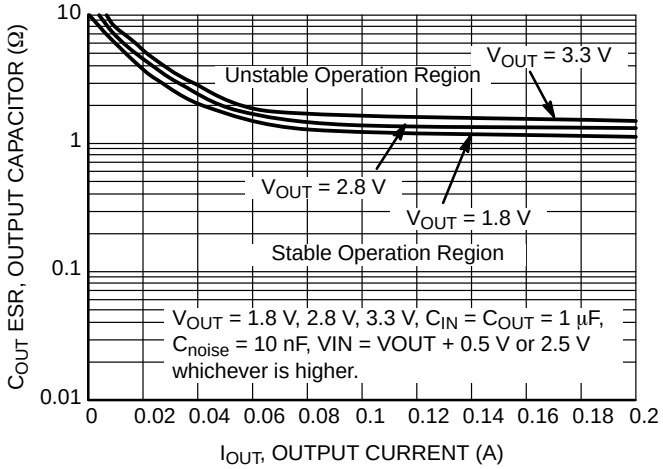


Figure 56. Output Capacitor ESR vs. Output Current

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APPLICATIONS INFORMATION

General

The NCV8570B is a high performance 200 mA low dropout linear regulator. This device delivers excellent noise and dynamic performance consuming only 75 μA (typ) quiescent current at full load, with the PSRR of (typ) 82 dB at 1 kHz. Excellent load transient performance and small package size makes the device ideal for portable applications.

Logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typically 0.1 μA.

Access to the major contributor of noise within the integrated circuit – Bandgap Reference is provided through the BYP pin. This allows bypassing the source of noise by the noise reduction capacitor and reaching noise levels below 10 μV_{RMS}.

The device is fully protected in case of output short circuit condition and overheating assuring a very robust design.

Input Capacitor Requirements (C_{IN})

It is recommended to connect a 1 μF ceramic capacitor between IN pin and GND pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise present on the input voltage. The input capacitor will also limit the influence of input trace inductances and Power Supply resistance during sudden load current changes. Higher capacitances will improve the line transient response.

Output Capacitor Requirements (C_{OUT})

The NCV8570B has been designed to work with low ESR ceramic capacitors on the output. The device will also work with other types of capacitors until the minimum value of capacitance is assured and the capacitor ESR is within the specified range. Generally it is recommended to use 1 μF or larger X5R or X7R ceramic capacitor on the output pin.

Noise Bypass Capacitor Requirements (C_{noise})

The C_{noise} capacitor is connected directly to the high impedance node. Any loading on this pin like the connection of oscilloscope probe, or the C_{noise} capacitor leakage will cause a voltage drop in regulated output voltage. The minimum recommended value of noise bypass capacitor is 10 nF. Values below 10 nF should be avoided due to possible Turn-On overshoot. Particular value should be chosen based on the output noise requirements (Figure 22). Larger values of C_{noise} will improve the output noise and PSRR but will increase the regulator Turn-On time.

Enable Operation

The enable function is controlled by the logic pin EN. The voltage threshold of this pin is set between 0.4 V and 1.2 V. Voltage lower than 0.4 V guarantees the device is off. Voltage higher than 1.2 V guarantees the device is on. The NCV8570B enters a sleep mode when in the off state drawing less than typically 0.1 μA of quiescent current. The internal 5 MΩ pull-down resistor (R_{PD}) assures that the device is turned off when EN pin is not connected.

The device can be used as a simple regulator without use of the chip enable feature by tying the EN to the IN pin.

Active Discharge

Active discharge circuitry has been implemented to insure a fast V_{OUT} turn off time. When EN goes low, the active discharge transistor turns on creating a path to discharge the output capacitor C_{OUT} through 1 kΩ (R_{DIS}) resistor.

Turn-On Time

The Turn-On time of the regulator is defined as the time needed to reach the output voltage which is 98% V_{OUT} after assertion of the EN pin. This time is determined by the noise bypass capacitance C_{noise} and nominal output voltage level V_{OUT} according the following formula:

$$t_{ON}\,[s] = C_{noise}\,[F] \cdot \frac{V_{OUT}\,[V]}{68 \cdot 10^{-6}\,[A]} \qquad \text{(eq. 1)}$$

Example:
Using C_{noise} = 100 nF, V_{OUT} = 3 V, C_{OUT} = 1 μF,

$$t_{ON} = 100 \cdot 10^{-9} \cdot \frac{3}{68 \cdot 10^{-6}} = 4.41\ ms$$

The Turn-On time is independent of the load current and output capacitor C_{OUT}. To avoid output voltage overshoot during Turn-On please select $C_{noise} \geq 10$ nF.

Current Limit

Output Current is internally limited within the IC to a typical 310 mA. The NCV8570B will source this amount of current measured with a voltage 100 mV lower than the typical operating output voltage. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 320 mA (typ). The current limit and short circuit protection will work properly up to V_{IN} = 5.5 V at T_A = 25 °C. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SDU} − 150 °C typical), Thermal Shutdown event is detected and the output (V_{OUT}) is turned off.

The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 135 °C typical). Once the IC temperature falls below the 135 °C the LDO is turned-on again.

The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Reverse Current

The PMOS pass transistor has an inherent body diode which will conduct the current in case that the $V_{OUT} > V_{IN}$.

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Such condition could exist in the case of pulling the V_{IN} voltage to ground. Then the output capacitor voltage will be partially discharged through the PMOS body diode. It have been verified that the device will not be damaged if the output capacitance is less than 22 μF. If however larger output capacitors are used or extended reverse current condition is anticipated the device may require additional external protection against the excessive reverse current.

Output Noise

If we neglect the noise coming from the (IN) input pin of the LDO, the main contributor of noise present on the output pin (OUT) is the internal bandgap reference. This is because any noise which is generated at this node will be subsequently amplified through the error amplifier and the PMOS pass device. Access to the bandgap reference node is supplied through the BYP pin. For the 1.8 V output voltage option Noise can be reduced from a typical value of 15 μVrms by using 10 nF to less than 10 μVrms by using a 100 nF from the BYP pin to ground. For more information please refer to Figures 22 through 24.

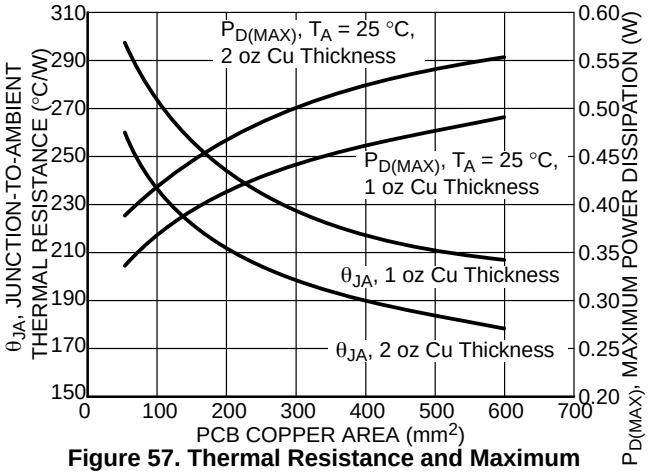


Figure 57. Thermal Resistance and Maximum Power Dissipation vs. Copper Area (TSOP-5)

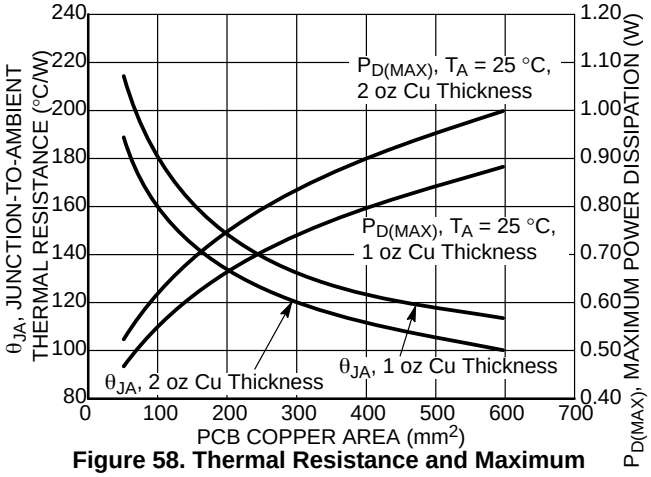


Figure 58. Thermal Resistance and Maximum Power Dissipation vs. Copper Area (DFN6)

Load Regulation

The NCV8570B features very good load regulation of 5 mV Max. in 0 mA to 200 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause 20 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The NCV8570B features very good line regulation of 0.6mV/V (typ). Furthermore the detailed Output Voltage vs. Input Voltage characteristics (Figures 47 through 49) show that up to V_{IN} = 5 V the Output Voltage deviation is typically less than 250 μV for 1.8 V output voltage option and less than 150 μV for higher output voltage options. Above the V_{IN} = 5 V the output voltage falls rapidly which leads to the typical 0.6 mV/V.

Power Supply Rejection Ratio

The NCV8570B features excellent Power Supply Rejection ratio. The PSRR can be tuned by selecting proper C_{noise} and C_{OUT} capacitors.

Minimum Load Current

NCV8570B does not require any minimum load current for stability. The minimum load current is assured by the internal circuitry.

Power Dissipation

For given ambient temperature T_A and thermal resistance $R_{\theta JA}$ the maximum device power dissipation can be calculated by:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad \text{(eq. 2)}$$

The actual power dissipation can be calculated by the formula:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN}I_{GND} \qquad \text{(eq. 3)}$$

In the frequency range from 10 Hz up to about 10 kHz the larger noise bypass capacitor C_{noise} will help to improve the PSRR. At the frequencies above 10 kHz the addition of higher C_{OUT} output capacitor will result in improved PSRR.

PCB Layout Recommendations

Connect the input (C_{IN}), output (C_{OUT}) and noise bypass capacitors (C_{noise}) as close as possible to the device pins.

The C_{noise} capacitor is connected to high impedance BYP pin and thus the length of the trace between the capacitor and the pin should be as small as possible to avoid noise pickup. In order to minimize the solution size use 0402 or 0603 capacitors. To obtain small transient variations and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. Larger copper area connected to the pins will also improve the device thermal resistance.

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ORDERING INFORMATION

Device*	Nominal Output Voltage	Marking	Package	Shipping†
NCV8570BMN180R2G	1.8 V	AK	DFN6 2 x 2.2 (Pb-Free)	3000 / Tape & Reel
NCV8570BMN250R2G	2.5 V	AP		
NCV8570BMN280R2G	2.8 V	AL		
NCV8570BMN330R2G	3.3 V	AN		
NCV8570BSN25T1G	2.5 V	ADZ	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCV8570BSN30T1G	3.0 V	ADN		

DISCONTINUED (Note 7)

NCV8570BMN300R2G	3.0 V	AM	DFN6 2 x 2.2 (Pb-Free)	3000 / Tape & Reel
NCV8570BSN18T1G	1.8 V	ADK	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCV8570BSN28T1G	2.8 V	ADM		
NCV8570BSN33T1G	3.3 V	ADP		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

7. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

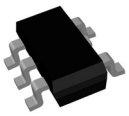
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REVISION HISTORY

Revision	Description of Changes	Date
4	Rebranded the document to **onsemi** format. NCV8570BMN300R2G, NCV8570BSN18T1G, NCV8570BSN28T1G, NCV8570BSN33T1G OPNs marked as Discontinued.	2/20/2026

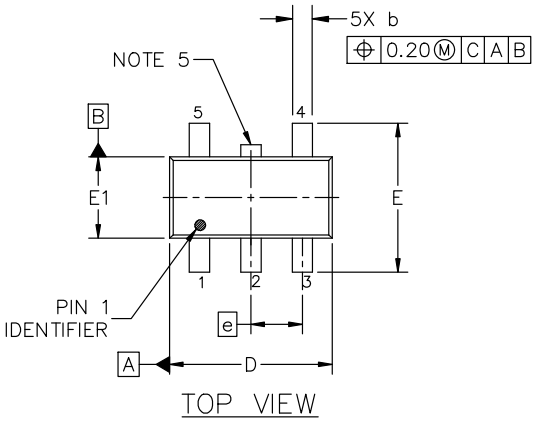
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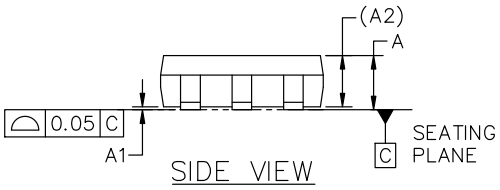


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

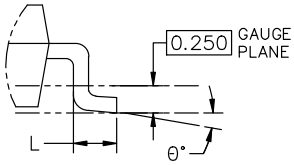
DATE 01 APR 2024



TOP VIEW



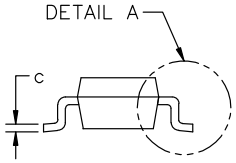
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

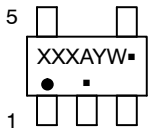
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

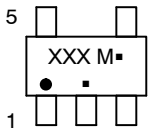
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

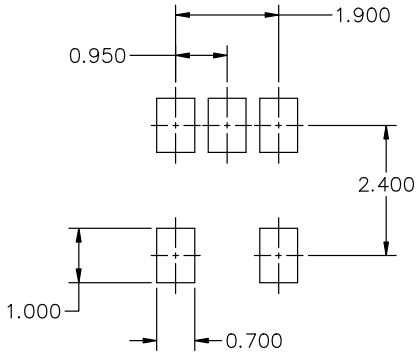
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



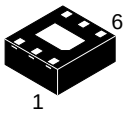
RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

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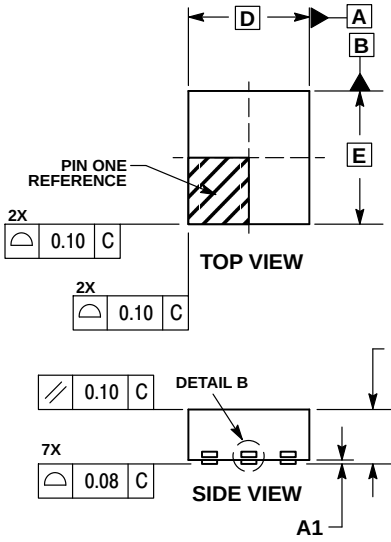
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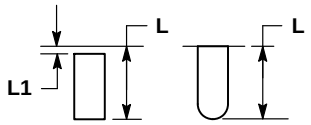


SCALE 4:1

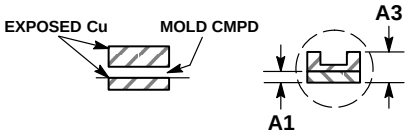
DFN6, 2x2.2, 0.65P
CASE 506BA
ISSUE A

DATE 07 JUL 2008

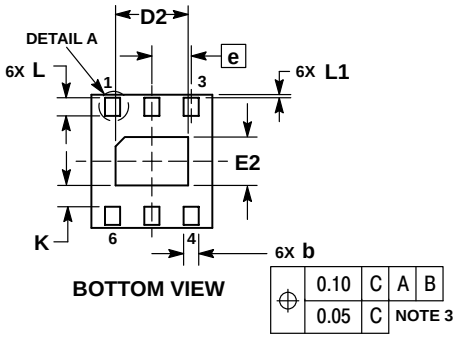




DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



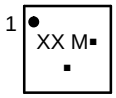
DETAIL B
ALTERNATE CONSTRUCTIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.20 BSC	
E2	0.70	0.90
e	0.65 BSC	
K	0.20	---
L	0.25	0.35
L1	0.00	0.10

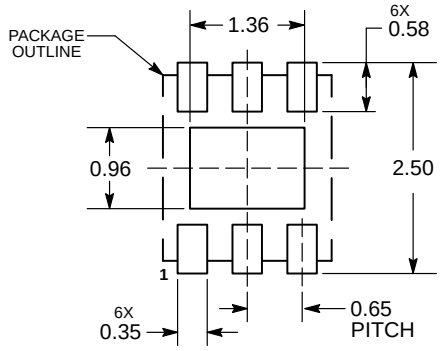
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**6 PIN DFN, 2.0X2.2, 0.65P**	**PAGE 1 OF 1**

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